

## Session 1 – Keynote Presentation

Monday Morning, September 14  
Oak Ballroom

### 8:15 AM

Welcome and Opening Remarks

Awards Presentations

Keynote Speaker Introduction

David Nairn, General Chairman

### 8:30 AM

Keynote Presentation

#### **Another Inconvenient Truth: Snails Are More Intelligent Than Us**

Dr. Thomas Williams, Synopsys Fellow, Synopsys, Inc.

For decades there has been a new CMOS technology node approximately every two years. Until recently, thanks to scaling, the key feature of every new technology node has been a 100% integration capacity and 40% performance improvement... free-of-charge. The International Technology Roadmap for Semiconductors (ITRS) has been architected in such a way that this improvement became a self-fulfilling prophecy of the roadmap itself. Everything else has been bent in the attempt to make scaling happen... forever.



For eons snails have built the cells of their shell according to the Fibonacci's numbers: 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610, 987, etc. – where each cell has a volume that is the sum of the volume of the previous two cells. Snails understand, however, that at a certain point in time growth must stop to prevent the collapse of the shell by making it too big and therefore fragile. When this point is reached, snails do stop adding larger cells, and start improving the robustness of the shell.

Back to us: technology-wise, scaling has rapidly exhausted the resources of CMOS technology, which, by now, struggles to deliver any further improvement. Economy-wise, Dr. Gordon Moore once observed:

“What we end up doing is really selling real estate. We've sold area on the silicon wafer for about a billion dollars an acre, that order of magnitude, as long as I've been in the industry.”<sup>[1]</sup>

In order to stay afloat, the semiconductor industry would need to double the number of units it sells, from one technology node to the next. Not only is this clearly impossible, but it puts the semiconductor suppliers on a collision course with their customers, who are now looking for half the silicon area from one technology node to the next. Atoms don't scale, and markets are finite.

As decimated vanguards approach the 32-nanometer node and start planning the jump to the 22-nanometer node, a number of fundamental challenges are emerging, both technical and financial, which force a thorough rethinking of how scaling has been done, and whether scaling continues to be the most appropriate solution to provide the world with the silicon content that it needs.

Like Al Gore's premise on energy consumption and global warming, there is an inconvenient truth to be acknowledged in our industry: scaling is like fossil fuels – the cheapest and easiest way to go. Unfortunately, also like fossil fuels, it is not sustainable indefinitely. And it becomes more costly and inefficient every day. New avenues, which are available today, are worth exploring and must be undertaken. That is, unless snails are more intelligent than us...

In this keynote, Dr. Williams will describe the problems with scaling and a number of possible solutions, including the latest alternative paths and their relative merits.

Dr. Thomas W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, he was with IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a B.S.E.E. from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM, is the founder or co-founder of a number of workshops and conferences dealing with testing, and was twice a Distinguished Visitor lecturer for the IEEE Computer Society. Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the Society's 2000 Treasurer. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. He is an Adjunct Professor at the University of Calgary, Calgary, Alberta, Canada; and in 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the Universitaet of

Hannover, Hannover, Germany. He was recently honored as a foreign member of the Chinese Academy of Science. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society's W. Wallace McDowell Award for outstanding contributions to the computer art in 1989. In 2007 Dr. Williams received the European Design and Automation Association Lifetime Achievement Award for "outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems."

## Session 2 - Over-Sampled Data Converters

Monday Morning, September 14

Oak Ballroom

Chair: Pavan Hanumolu, Oregon State University

Co-Chair: Alessandro Piovaccari, Silicon Laboratories

### 10:00 AM Introduction

10:05 AM **A 630 $\mu$ W Zero-Crossing-Based  $\Delta\Sigma$  ADC Using Switched-Resistor Current Sources in 45nm CMOS,**  
02-1 *Tawfiq Musah, Sunwoo Kwon\*, Hasnain Lakdawala\*, Krishnamurthy Soumyanath\* and Un-Ku Moon, Oregon State University, Corvallis, OR, \*Dongbu HiTek, Seoul, Korea \*\*Intel Corporation, Hillsboro, OR*

A delta-sigma ADC employs zero-crossing-based integrators to achieve low power operation at 50MHz. Switched resistors are used as current sources, and a new charging scheme is proposed to reduce overshoot. Test chip implemented in a 45nm CMOS achieves 54.3dB DR, 52.5dB SNR, and 47.7dB SNDR at 0.833MHz while dissipating 0.63mW.

10:30 AM **A Low-Power 1.92MHz CT  $\Delta\Sigma$  Modulator With 5-bit Successive Approximation Quantizer,**  
02-2 *Mohammad Ranjbar, Arash Mehrabi and Omid Oliaeim, University of Massachusetts, Amherst, MA*

CT Delta-Sigma modulators provide a solution for low-power analog to digital conversion with built in anti-aliasing but they are sensitive to clock jitter. One way of mitigating the jitter problem is to use a multi-bit quantizer with increased number of bits. The limiting factors are quantizer delay and exponential growth of power and complexity. This paper reports the use of a 5-bit successive approximation ADC in a wide-band CT delta-sigma. The ADC structure allows easy integration of the delay compensation mechanism with minimum hardware and power. The design is implemented in a 130nm CMOS technology and measurement results show a 62 dB dynamic range and 3.1mw power consumption from a 1.2v supply.

10:55 AM **A Self-Calibrated 2-1-1 Cascaded Continuous-Time  $\Delta\Sigma$  Modulator,** *Junpei Kamiishi, Yun-Shiang Shu\*,*  
02-3 *Koji Tomioka, Koichi Hamashita and Bang-Sup Song\*, Asahi Kasei Microsystems, Atsugi, Japan, \*University of California, San Diego, CA*

A 2-1-1 cascaded continuous-time delta-sigma modulator is self-calibrated with LMS-based adaptation. Exact noise cancellation filter is derived using a parameter-based continuous-time to discrete-time transform. A 0.18-micrometer CMOS prototype demonstrates a leakage noise spectral density below 10nV/ $\sqrt{\text{Hz}}$  after the capacitors in the Gm-C loop filters are self-trimmed with a 1.1% step.

11:20 AM **A 120dB Dynamic Range 400mW Class-D Speaker Driver with 4<sup>th</sup>-order PWM Modulator,** *Minsheng*  
02-4 *Wang, Xicheng Jiang, Jungwoo Song and Todd Brooks, Broadcom Corporation, Irvine, CA*

A 400mW class-D speaker driver is implemented in 65nm CMOS technology, using a 4th-order digital PWM modulator to eliminate the DAC and minimize the effects of analog imperfection. It achieves 120dB dynamic range with up to 88% power efficiency while driving an 8ohm speaker load.

## Session 3 – Biomedical Electronics

Monday Morning, September 14

Fir Ballroom

Chair: Ed Lee, Alfred Mann Institute, Case Western University

### 10:00 AM Introduction

10:05 AM **Ultra-low-power Electronics for Medicine**, Rahul Sarpeshkar, Massachusetts Institute of Technology  
03-1

10:40 AM **Intracortical Microstimulation to Create Vision**, Mohamad Sawan, University of Montreal  
03-2

11:15 AM **Title to be determined**, Bernard Boser, University of California, Berkeley  
03-3

## Session 4 - Nanoscale Power and Performance Optimizations

Monday Morning, September 14  
Pine Ballroom

Chair: Osamu Takahashi, IBM  
Co-Chair: Michael Seningen, Intrinsicity

10:00 AM **Introduction**

10:05 AM **Design Optimizations for Reduced Power and Higher Operating Frequency in a Custom x86-64 Processor Core**, William Keshlear, Spence Oliver, Robert Colyer, Jeremy Schreiber, Ted Antoniadis, Tom Mickelson, Tim Puzey and Michael Bates, Advanced Micro Devices, Inc., Austin, TX  
04-1

This paper describes the methodology and tools used to drive static and dynamic power savings while significantly improving the operating frequency of a 45 nm custom x86-64 processor core used in several multi-core devices. The power improvements were essential for future six-, eight-, and twelve-core server processors, but notable improvements have already been observed in the four-core, 2.7-GHz server product and the four-core, 3.0-GHz client product.

10:30 AM **A Minimum Decap Allocation Technique Based on Simultaneous Switching for Nanoscale SoC**, Kenji Shimazaki and Takaaki Okumura, Semiconductor Technology Academic Research Center  
04-2

In this paper, we propose a novel decoupling capacitance (decap) optimization technique based on simultaneous cell switching activity at the pre-layout stage. White space in the form of cell padding for the required quantity of decap is added to cells which simultaneously switch during the peak noise period, which is quickly estimated using initial timing information and the current waveforms for each cell instance, without the need to reference the power grid. The method is applied to an actual 45nm LSI and results show a 35% decap area reduction or 21.9% peak noise reduction compared with conventional decap insertion flows. The technique can improve the reliability of SoC with a runtime overhead of only 4.69% at the P&R stage in existing nanoscale SoC EDA design flows.

10:55 AM **Charge-Borrowing Decap: A Novel Circuit for Removal of Local Supply Noise Violations**, Xiongfei Meng, Resve Saleh and Steve Wilton, University of British Columbia, Vancouver, Canada  
04-3

We propose a novel circuit called charge-borrowing decap as a drop-in replacement for passive decaps to reduce supply noise for removal of "hot-spot" IR-drop problems found late in the design process. Measurement results on a 90nm test chip show that a noise reduction improvement between 42%-55% at 100MHz-1.5GHz over its passive counterpart.

11:20 AM **Circuit Techniques for Enhancing the Clock Data Compensation Effect under Resonant Supply Noise**, Dong Jiao, Jie Gu and Chris Kim, University of Minnesota, Minneapolis, MN  
04-4

Recent publications have shown that clock jitter can improve timing margin through the compensation effect between the clock cycle and the datapath delay under the influence of resonant supply noise. In this paper, novel phase-shifted clock buffer designs are proposed to enhance this "beneficial jitter effect". Compared with existing designs, our design saves 85% of the clock buffer area while achieving a similar 10% increase in maximum operating frequency for typical pipeline circuits. Measurement results are presented from a test chip implemented in a 1.2V, 65nm process.

11:45 AM **Switched Resonant Clocking (SRC) Scheme Enabling Dynamic Frequency Scaling and Low-Speed Test**, Katsuyuki Ikeuchi, Kosuke Sakaida, Koichi Ishida, Takayasu Sakurai and Makoto Takamiya, The University of Tokyo, Tokyo, Japan  
04-5

A novel Switched Resonant Clocking (SRC) scheme is proposed to solve two basic problems of the conventional resonant clocking, that is, power increase and clock waveform inability at the lower clock frequency region. The power increase prohibits widely-used dynamic frequency scaling (DFS) and the waveform instability hinders low-speed function tests. A test chip in 0.18 $\mu$ m CMOS is manufactured and measured to show that the SRC suppresses power increase at low clock frequency and enables the low-speed tests, while reducing the clock power by 8% at 1.5-GHz clock with an area penalty of 4.8%.

## Session 5 - Frequency Synthesizers

Monday Afternoon, September 14  
Oak Ballroom

Chair: Cicero Vaucher, NXP

Co-Chair: Rick Booth, Panasonic

1:30 PM **Introduction**

1:35 PM **Insights into Wideband Fractional All-Digital PLLs for RF Applications (INVITED)**, *Enrico Temporiti, Colin Weltin-Wu\*, Daniele Baldi, Riccardo Tonietto\*\* and Francesco Svelto\*, STMicroelectronics, Pavia, Italy, \*Università di Pavia, Pavia, Italy, \*\*STMicroelectronics, Grenoble, France*

Technology scaling and large-scale integration make the operating environment increasingly hostile for traditional analog design. In the area of frequency synthesis, All-Digital PLLs (ADPLLs) provide an attractive alternative to conventional PLLs. However, wideband fractional ADPLLs come with a different set of problems, principally in-band spurious tones. Techniques to suppress spurious tones would eliminate a major obstacle for ADPLLs' widespread proliferation into wireless RF applications. In this paper we first describe the evolution from the analog PLL to the divider-less ADPLL, of major interest for RF to date, then develop a model to predict location and level of spurs. Validation is performed through experiments on an ADPLL fabricated in 65nm digital CMOS.

2:25 PM **Time to Digital Converter Based on a 2-dimensions Vernier Architecture**, *Antonio Liscidini, Luca Vercesi and Rinaldo Castello, University of Pavia, Pavia, Italy*

A novel 2-dimension Vernier Time to digital converter (TDC) is presented. The proposed architecture reduces drastically the number of delay stage required by linear TDCs minimizing the power consumption and the area of the design. A 7bits TDC prototype realized in 65nm CMOS technology is presented. The chip has a resolution of 4.8ps with a power consumption of 1.7mW at a conversion rate of 50Mps.

2:50 PM **A Fractional-N PLL Modulator with Flexible Direct Digital Phase Modulation**, *Mark Ferriss, Davin Lin and Michael Flynn, University of Michigan, Ann Arbor, MI*

A 2.6GHz fractional-N synthesizer with a flexible digital modulation scheme is presented. The PLL output is modulated by adding a digital signal directly to the output of the phase detector. A pre-emphasis filter is used to allow switching rates faster than the loop bandwidth. The transmitter supports GMSK, OQPSK, BSK or any constant envelope modulation scheme. Measurements are presented at 300kBit/sec. The 0.7mm<sup>2</sup> prototype in 0.13 $\mu$ m CMOS consumes 20mA from a 1.5V supply.

3:15 PM **BREAK**

3:30 PM **A Sub-0.75°<sub>RMS</sub>-Phase-Error Differentially-Tuned Fractional-N Synthesizer with On-Chip LDO Regulator and Analog-Enhanced AFC Technique**, *Lei Lu, Lingbu Meng, Liang Zou, Hao Min and Zhangwen Tang, Fudan University, Shanghai, China*

This paper presents a low-phase-error wideband fractional-N frequency synthesizer. Differential tuning is described and a level shift circuit is proposed to obtain symmetrical tuning range. On-chip LDO regulator is designed to improve the power supply rejection for VCO. A voltage monitor is used to enhance the digital AFC technique to overcome the temperature variation. The synthesizer was implemented in a 0.18- $\mu$ m CMOS process with a 16-mA supply current and a 1.47-mm<sup>2</sup> die area. The measured in-band phase noise is less than -97 dBc/Hz at a 10-kHz frequency offset and the integrated phase error is less than 0.75°<sub>RMS</sub>. The measured reference spur is less than -71 dBc and the locking time is smaller than 20  $\mu$ s.

3:55 PM **A Sub-2.5ns Frequency-Hopped Quadrature Frequency Synthesizer in 0.13- $\mu$ m Technology,**  
05-5 *Narasimha Lanka, Satwik Patnaik and Ramesh Harjani, University of Minnesota, Minneapolis, MN*

This paper presents a fast-hopping frequency synthesizer architecture with quadrature outputs, based on sub-harmonic injection locking, that is compliant with Wireless-USB/WiMedia specifications. The overall architecture is a CMOS-only implementation and has been fabricated in 0.13- $\mu$ m SiGe BiCMOS process. Measurement results indicate lock-times of less than 2.5 ns, a locked phase noise of -114 dBc/Hz at 1 MHz offset and a quadrature accuracy of better than 0.5 degrees. The frequency synthesizer (excluding output buffers) occupies an area of 0.27 sq.mm. and consumes 14.5 mW of power. The best and worst cases spur suppression achieved are 47 and 31 dB, respectively. This is the lowest power fast-hopping quadrature frequency synthesizer that has been reported to date.

4:20 PM **A 5.2mW Ku-Band CMOS Injection-Locked Frequency Doubler with Differential Input / Output,**  
05-6 *Enrico Monaco, Mattia Borgarino, Francesco Svelto\* and Andrea Mazzanti, Università degli Studi di Modena e Reggio E, Modena, Italy, \*Università degli Studi di Pavia, Pavia, Italy*

A novel circuit topology, consisting of an LC oscillator injection locked by a push-push transistors pair, is proposed to realize a low power frequency multiplier by two. Prototypes, in 0.13 $\mu$ m CMOS, show 30% locking range around 13GHz with 3dBm input power. Core power dissipation is 5.2mW only.

## Session 6 - MEMs, Biomedical, and Sensors

Monday Afternoon, September 14

Fir Ballroom

Chair: Hasnain Lakdawala, Intel Corporation

Co-Chair: Kenneth Szajda, LSI Logic

1:30 PM **Introduction**

1:35 PM **MEMS for Integrated Timing and Spectral Processing (INVITED),** *Farrokh Ayazi, Georgia Institute of*  
06-1 *Technology, Atlanta, GA*

This paper presents a review of micro-electromechanical devices for frequency references and RF spectral processing. The application of high-Q pure silicon and AlN-on-silicon bulk acoustic wave resonators in low phase-noise reference oscillators is discussed and compensation challenges are described. Low-loss piezo-acoustic filters and high-Q tunable and switchable silver passives are presented for applications in multi-mode front-end modules and spectral processors.

2:00 PM **Fully-Monolithic, 600°C Differential Amplifiers in 6H-SiC JFET IC Technology,** *Amita Patil, Xiao-an*  
06-2 *Fu, Mehran Mehregany and Steven Garverick, Case Western University, Cleveland, OH*

A family of fully-integrated differential amplifiers were designed and fabricated in 6H-SiC, n-channel JFET integrated-circuit technology. A single-stage amplifier with resistor loads has gain-bandwidth of ~2.8 MHz, and differential-mode gain that varies by less than 1 dB from 25-600C. A two-stage amplifier with current-source loads and common-mode feedback in 1st-stage, and resistor loads in 2nd-stage has gain-bandwidth of 1.4 MHz, and differential-mode gain of 69 dB at 576C, with just 3.6 dB gain-variation from 25-576C.

2:25 PM **A 32x32 50ps Resolution 10 bit Time to Digital Converter Array in 130nm CMOS for Time**  
06-3 **Correlated Imaging.,** *Justin Richardson, Richard Walker, Lindsay Grant\*, David Stoppa\*\*, Fausto Borghetti\*\*, Edoardo Charbon^, Marek Gersbach^ and Robert Henderson, The University of Edinburgh, Edinburgh, UK, \*STMicroelectronics, Edingburgh, UK, \*\*Fondazione Bruno Kessler, Trento, Italy, ^EPFL, Lausanne, Switzerland*

We report the design and characterisation of a 32x32 time to digital (TDC) converter plus single photon avalanche diode (SPAD) pixel array implemented in a 130nm imaging process. Based on a gated ring oscillator approach, the 10 bit, 50um pitch TDC array exhibits a minimum time resolution of 50ps, with accuracy of  $\pm 0.5$  LSB DNL and 2.4 LSB INL. Process, voltage and temperature compensation (PVT) is achieved by locking the array to a stable external clock. The resulting time correlated pixel array is a viable candidate for single photon counting (TCSPC) applications such as fluorescent lifetime imaging microscopy (FLIM), nuclear or 3D imaging and permits scaling to larger array formats.

2:50 PM **RF-CMOS-MEMS Based Frequency-Reconfigurable Amplifiers (INVITED)**, *Tamal Mukherjee and Gary*  
06-4 *Fedder, Carnegie Mellon University, Pittsburgh, PA*

Chips from a foundry RF process are post-processed to release MEMS passivedevices and enable single-chip reconfigurable circuits. A MEMS variablecapacitor, capable of 7:1 tuning ratio, reconfigures a narrow-band low-noiseamplifier and a power amplifier over a 1 GHz frequency range. A suspended MEMSinductor, with > 50% improvement in Q, lowers amplifier power consumption.

**3:15 PM BREAK**

3:30 PM **Ultra-Low-Power Electronics for Non-Invasive Medical Monitoring (INVITED)**, *Lorenzo Turicchia,*  
06-5 *Soumyajit Mandal, Maziar Tavakoli\*, Leon Fay\*\*, Vinith Misra^, Jose Bohorquez, William Sanchez and*  
*Rahul Sarpeshkar, Massachusetts Institute of Technology, Cambridge, MA, \*Linear Technology*  
*Corporation, North Chelmsford, MA, \*\*SRI International, Menlo Park, CA, ^Stanford University, Stanford,*  
*CA*

Electronics for non-invasive medical monitoring promise low-cost, maintenance-free, and lightweight devices. We present results from six novelchips for reducing power consumption while retaining precision: We describe anelectrocardiograph, a pulse oximeter, a phonocardiograph, a model of the heart, an RF-antenna-powered CMOS rectifier, and a battery-free platform for medicalmonitoring.

4:20 PM **High-Voltage Tolerant Stimulation Monitoring Circuit in Conventional CMOS Process**, *Edward Lee,*  
06-6 *Alfred Mann Foundation, Santa Clarita, CA*

A 6V 8-input stimulation monitoring circuit with high-voltage analog switchesand rail-to-rail constant gm opamp was implemented in a conventional 0.18 $\mu$ mCMOS process. The on-resistance for the switches was < 3.15k $\square$  and thevariations on the opamp input gm values were <2.9% with a current consumptionof 20 $\mu$ A at 6V.

4:45 PM **Circuits Techniques and Microsystems Assembly for Intracortical Multichannel ENG Recording**  
06-7 **(INVITED)**, *Benoit Gosselin and Mohamad Sawan, École Polytechnique de Montreal, Montreal, Canada*

We present dedicated circuit techniques and strategies to design and assemble dense multi-channel microsystems intended for ENG recording. Efficient neuralinterfacing circuits are proposed and high-fidelity data reduction strategiesare demonstrated. Also, an on-chip power management scheme based on automaticbiopotential detection is suggested. The presented strategy is expected toimprove power consumption in multi-channel ENG sensors by an order of magnitude. Low-power design techniques, ultra-low-power neural signalprocessing circuits, and dedicated implementation strategies to achieve highintegration density in multi-channel microsystems are also covered mechanism of information transmission in extracellular neural.

## Session 7 - Gigabit Transceivers and Building Blocks

Monday Afternoon, September 14  
Pine Ballroom

Chair: Jin Liu, University of Texas at Dallas

Co-Chair: Jim Buckwalter, University of California, San Diego

1:30 PM **Introduction**

1:35 PM **Emerging Standards at ~10 Gbps for Wireline Communications and Associated Integrated Circuit**  
07-1 **Design and Validation (INVITED)**, *Mike Li and Sergey Shumarayev, Altera Corporation, San Jose, CA*

We first review the signaling and jitter requirements for emerging high-speedwireline communication standards at ~10 Gbps, including CEI 11G, XLAUI/CAUI, XFI, and SFP+. We then present an FPGA transceiver architecture and subsystem/circuit blocks for clocking and timing generation, transmitterbuffer, and receiver CDR and DFE, all designed and manufactured with 40-nmprocess node. Lastly, we present the signal/jitter transmitter output and receiver-tolerance measurement results at 10.3125 Gbps, with an ultra-lowrandom jitter at ~550 fs.

2:25 PM 07-2 **A 18mW 10Gbps Continuous-Time FIR Equalizer for Wired Line Data Communications in 0.12 $\mu$ m CMOS**, Hao Liu, Jin Liu, Robert Payne\*, Cy Cantrell and Mark Morgan\*, University of Texas at Dallas, Dallas, TX, \*Texas Instruments Incorporated, Dallas, TX

This paper presents a 10Gbps continuous-time FIR receiver equalizer design with a  $\frac{1}{4}$  symbol-period differential self-biased active inductor delay line in 0.12 $\mu$ m CMOS for wired line data communications. The proposed delay line, together with a proposed active inductor Cherry-Hooper transimpedance load at the FIR filter summing node, increases the equalizer speed, while reducing the equalizer power consumption to only 18mW. The prototype occupies 0.03mm<sup>2</sup> die area and measurement results show that the equalizer can compensate for 15dB channel loss at 5GHz for 10Gbps data transmission.

2:50 PM 07-3 **A 1-mW 12-Gb/s Continuous-Time Adaptive Passive Equalizer in 90-nm CMOS**, Dong Hun Shin, Ji Eun Jang, Frank O'Mahony\* and C. Patrick Yue, University of California, Santa Barbara, CA, \*Intel Corporation, Hillsboro, OR

This paper presents a frequency-domain adaptive passive equalizer for high-speed receivers. A local control loop, without feedback from the final receiver output, is used to automatically adjust the gain compensation for different channel characteristics. As a result, the equalizer does not rely on the recovered clock signal. Implemented in a 90-nm digital CMOS process, the equalizer can provide up to 13 dB of gain compensation with 6 dB of tuning range while consuming 1 mW from a 1-V supply. The equalizer is able to open the data eye of a 12-Gb/s PRBS signal after a 72-inch RG-50 coaxial cable and an 8-inch FR-4 trace, whose attenuations at 6 GHz are 10.8 and 13 dB, respectively.

**3:15 PM BREAK**

3:30 PM 07-4 **A 3x3.8Gb/s Four-Wire High Speed I/O Link Based On CDMA-Like Crosstalk Cancellation**, Tzu-Chien Hsueh, Pin-En Su and Sudhakar Pamarti, University of California, Los Angeles, CA

A signaling technique realizing three differential links over four wires is proposed. The technique uses Code Division Multiple Access (CDMA) principles to cancel the crosstalk between the links. A 3x3.8 Gb/s, 10-12 BER prototype IC built in 90nm CMOS is described and measurement results are presented.

3:55 PM 07-5 **A 5Gbps 0.13 $\mu$ m CMOS Pilot-Based Clock and Data Recovery Scheme for High-Speed Links**, Mahmoud Reza Ahmadi, Amir Amirkhany\* and Ramesh Harjani, University of Minnesota, Minneapolis, MN, \*Rambus Inc., Los Altos, CA

A 5Gbps differential link fabricated in a 0.13 $\mu$ m IBM CMOS using a pilot-based clock and data recovery where a low-amplitude bit rate clock is added to the transmit signal. The designed CDR area is 0.171mm<sup>2</sup> and consumes 17.6mW. The recovered clock rms jitter is 1.6ps for a 5% transmitter overhead.

4:20 PM 07-6 **A 10-Gbps CMOS Single Chip Optical Receiver with 2-D Meshed Spatially-Modulated Light Detector**, Shih-Hao Huang and Wei-Zen Chen, National Chiao-Tung University, Hsinchu, Taiwan

This paper presents a 10-Gbps optical receiver with monolithically integrated CMOS photo detector. A transimpedance amplifier with nested feedback and shunt-peaking is proposed for broad-band and high-gain operations. Incorporating a 2-D meshed spatially-modulated light detector, the optical receiver is capable of delivering 25-kohm transimpedance gain when driving 50-ohm output loads. The operating speed is improved by 3X over the prior art with the same technology. Implemented in a generic 180-nm CMOS technology, the chip size is 0.95 mm by 0.8 mm. This receiver core drains 118 mW from 1.8 V supply.

## Session 8 - CMOS Scaling and Beyond

Monday Afternoon, September 14  
Cedar Ballroom

Chair: Takamaro Kikkawa, Hiroshima University  
Co-Chair: Jordan Lai, TSMC

1:30 PM **Introduction**

1:35 PM **Progress and Outlook of Lithography for Semiconductor IC (INVITED)**, Burn Lin and R.G. Liu, TSMC,

08-1 *Hsinchu, Taiwan*

Progress of lithography from the lensless type to lens-based systems using different kinds of photon and electron beams is reported here. The stages of lithography development with their physical principles are linked to the corresponding impacts to IC designers to help them understand the reasons they are more and more restricted. From this vantage point, we look at the prospects of the lithography systems that will handle patterning for 32-nm half pitch and beyond in feasibility and cost.

2:25 PM **Copper Interconnect Technology for the 32 nm Node and Beyond (INVITED)**, *Jeff Gambino, Fen Chen and John He, IBM Microelectronics, Essex Junction, VT*

Copper interconnects have gained wide acceptance in the microelectronics industry due to improved resistivity and reliability compared to Al interconnects. However, there are many challenges with implementation of Cu interconnects at the 32 nm node and beyond, including increased resistivity, integration with porous low-k materials, and reliability. In addition, for RF and mixed signal technology, integration of passive devices is required. In this paper, each of these topics is addressed.

3:15 PM **BREAK**

3:30 PM **Advanced SOI CMOS Transistor Technologies for High-Performance Microprocessor Applications (INVITED)**, *Manfred Horstmann, Andy Wei, Jan Hoentschel, Thomas Feudel, Thilo Scheiper, Rolf Stephan, Martin Gerhardt, Stephan Krügel and Michael Raab, GLOBALFOUNDRIES, Dresden, Germany*

In this paper we present an overview of partial depleted Silicon on Insulator (PD SOI) CMOS transistor technologies for high performance applications. To achieve a "high performance per watt" figure of merit, transistor technology elements like PD SOI, strained Si, aggressive junction scaling or asymmetric devices need hand-in-hand development with multiple core- and power efficient designs. These techniques have been developed, applied and optimized for 45nm SOI volume manufacturing at GLOBALFOUNDRIES in Dresden. To enable further transistor scaling to 32nm design rules, High K Metal Gate (HKMG) technology is key. Different HKMG integrations as well as future strained Si technologies like strained silicon directly bonded on SOI and embedded Si:C are discussed.

4:20 PM **High Mobility Channel CMOS Technologies for Realizing High Performance LSI's (INVITED)**, *Shinichi Takagi, The University of Tokyo, Tokyo, Japan*

Channel engineering including the high mobility channel has been recognized as mandatory for high performance CMOS. We report our approaches to further improvement of MOSFETs by using strained-Si, Ge, and III-V semiconductor channels on the Si CMOS platform with an emphasis on the combination of ultra-thin body and multi-gate structures.

## Poster Session

Monday Evening, September 14  
Donner/Siskiyou/Cascade Ballrooms  
5:00 pm – 7:00 pm

M-01 **Trimless Second Order Curvature Compensated Bandgap Reference using Diffusion Resistor**, *Ajay Kumar, Texas Instruments*

A trim-less second order curvature compensated bandgap reference current using diffusion resistor is presented. An order of magnitude higher sheet-resistance ( $\times 50$ ) and tighter process control of diffusion resistor than the poly has enabled this work to achieve the same current in one-third area. The process spread of diffusion resistor and V<sub>PNP</sub> transistor tracks each other, thereby resulting in higher accuracy without using any trim techniques. The proposed circuit is fabricated in a 0.5 $\mu$ m CMOS process. The measured reference current has a variation of 46ppm/ $^{\circ}$ C over a temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C.

M-02 **A 10mW 9.7ENOB 80MSPS Pipeline ADC in 65nm CMOS Process without any Special Mask Requirement and with Single 1.3V Supply**, *Abhijit Kumar Das, Hemant Bhasin, Sundara Siva Rao Giduturi, Texas Instruments, India*

This paper describes a power and area efficient pipeline ADC design. This ADC was designed in 65nm process without any special mask requirement and can work with supply voltage of 1.3V consuming



10mW providing 9.7 ENOB at 80MSPS while occupying less than 0.2 square millimeters.

- M-03 **A 1.5mW 16b ADC with Improved Segmentation and Centroiding Algorithms and Litho-Friendly Physical Design (LFD) Used in Space Telescope Imaging Applications**, *L. Lewyn, M. Loose\* SnowBush-Gennum, \*Teledyne Imaging Sensors*

This paper describes the 16b ADC ASIC replacing the survey camera image processor in the 2009 Hubble rescue mission. The ADC uses a combination of improved MSB-LSB segmentation, 3 centroiding algorithms and litho-friendly physical design (LFD) to achieve <0.4b DNL and <2.3b INL without requiring initial or background calibration.

- M-04 **An 11mW 100MHz 16X-OSR 64dB-SNDR Hybrid CT/DT  $\Delta\Sigma$  ADC with Relaxed DEM Timing**, *S. Kwon\*, P. Hanumolu, S. Kim\*\*, S. Lee\*\*, S. You\*\*, H. Park\*\*, J. Kim\*\*, and U. Moon, Oregon State University, \*Now with Dongbu HiTek, \*\*Samsung Electronics*

A multi-bit 3rd-order hybrid Delta-Sigma ADC is presented. The ADC obviates the need for a dynamic element matching technique (DEM) in the critical feedback path. Eliminating the DEM allows to minimize feedback latency, thus helping to increase clock frequency. The first two continuous-time integrators decrease power consumption and the last discrete-time integrator mitigates the excess loop delay and the quantizer sampling timing problem. Moreover, switched-R-MOSFET-C technique offers benefit of absorbing the finite opamp delay as well as frequency scalability. The proposed ADC is also capable of converting up to +2 dBFS without pole optimization technique. A prototype IC implemented in a 65 nm digital CMOS achieves 68 dB DR, 65 dB SNR, 64 dB SNDR, and 84 dB SFDR while consuming 11 mW and clocking at 100 MHz.

- M-05 **A 14.6th-order 3.456GHz Transmit Baseband filter in 110nm CMOS for Millimeter-Wave Communication Systems**, *M. Tokumaru, H. Ikoma, Y. Yamada, K. Okamoto, A. Yamamoto, Y. Shirakawa, Panasonic Corporation*

This paper presents a 1.728Gbps transmit baseband filter for transmitters of millimeter-wave communication systems. In order to avoid the inter symbol interference, wide band and high order filter is demanded. The proposed filter consists of a 3.456GHz digital filter and an 8-bit 3.456Gbps digital to analog converter (DAC) with a clock divider, which occupies 0.265mm<sup>2</sup> in 110nm CMOS. The filter consumes 142mW and achieves the transmit spectrum very close to the mask regulated by IEEE802.15.3c.

- M-06 **64-bit Prefix Adders: Power-Efficient Topologies and Design Solutions**, *Ching Zhou, Bruce M. Fleischer, Michael Gschwind, Ruchir Puri, IBM T.J. Watson Research Center*

64-bit adders of various prefix algorithms are designed using a novel dataflow synthesis methodology. The power-performance tradeoffs are analyzed for a portfolio of popular adder topologies and design styles. The intrinsically sparser designs in hierarchical prefix scheme are demonstrated to be preferable choices for both high-performance and low-power adder applications.

- M-07 **Energy-Performance Tunable Logic**, *Bitu Nezamfar, Mark Horowitz, Stanford University*

An externally static, internally dynamic topology creates a new logic family that enables the user to tune effective transistor thresholds post-fabrication by adjusting a few power supplies. These gates can therefore be programmed for higher speed or for lower power based on the system requirements. An application of this logic to programmable interconnect circuits is shown in this paper. In a 90-nm test chip, the circuit achieves the same performance as conventional static circuits at 65% energy and has a 2X wider energy-performance tuning range. This property enables building in-field energy-performance tunable FPGAs.

- M-08 **A 6-bit Arbitrary Digital Noise Emulator in 65nm CMOS Technology**, *Tetsuro Matsuno\*, Daisuke Fujimoto\*, Daisuke Kosaka\*\*, Naoyuki Hamanishi\*\*\*, Ken Tanabe\*\*\*, Masazumi Shiochi\*\*\*, Makoto Nagata\* \*\*, \*Kobe University, \*\*A-R-Tec Corporation, \*\*\*Toshiba Corporation*

An arbitrary noise generator (ANG) is based on time-series charging of divided parasitic capacitance (TSDPC) and emulates power supply noise generation in a CMOS digital circuit. A prototype ANG incorporates an array of 32 × 32 6-bit TSDPC cells along with a 128-word vector memory and occupies 2 × 2 mm<sup>2</sup> in a 65 nm 1.2 V CMOS technology. Digital noise emulation of functional logic cores such as

register arrays and processing elements is demonstrated with chip-level waveform monitoring at power supply, ground, as well as substrate nodes.

- M-09 **A 0.92mm<sup>2</sup> 23.4mW Fully-Compliant CTC Decoder for WiMAX 802.16e Application**, *Shao-Wei Yen, Ming-Chih Hu, Chih-Lung Chen, Hsie-Chia Chang, Shyh-Jye Jou, Chen-Yi Lee, National Chiao Tung University*

An area-efficient and fully-compliant decoder for convolutional turbo code (CTC) of WiMAX 802.16e is presented. The proposed decoder can support all 17 modes specified in IEEE 802.16e system. By scaling the extrinsic information, the Max-Log MAP algorithm is used to reduce the hardware complexity with the minimized performance loss. A two-phase extrinsic memory and reversed sliding window technique are demonstrated for less memory requirement and decoding latency. Moreover, a division-free reconfigurable interleaver architecture is proposed to use simple addition and subtraction instead of division. Fabricated with the 90nm CMOS process, the proposed CTC decoder chip which occupies core area of 0.92mm<sup>2</sup> can achieve 30Mb/s with 23.4mW power consumption.

- M-10 **Embedded High-Speed BCH Decoder for New-Generation NOR Flash Memories**, *Xueqiang Wang, Dong Wu, Chaohong Hu\*, Liyang Pan, Runde Zhou, Tsinghua University, \*Intel Technology Development Co. Ltd*

A high-speed double-error-correcting (DEC) BCH decoder for new-generation NOR flash memory is presented to improve reliability. To speed up the decoding process, a multiplication-free linear transform is developed to eliminate iterations and divisions in Galois fields. Furthermore, the reverse data-flow analysis (RDFA) and smoothest descent approach are proposed to reduce latency in the parallel Chien search. Based on peripheral 180nm CMOS process, the whole BCH decoder is designed and the latency is significantly reduced to less than 5ns.

- M-11 **A 56M $\Omega$  CMOS TIA for MEMS Applications**, *J. Salvia, P. Lajevardi, M. Hekmat, B. Murmann, Stanford University*

We present a high-gain, low-noise differential transimpedance amplifier designed to interface with electrostatic micromechanical resonators. The capacitive feedback topology achieves a 56M $\Omega$  gain, 1.8MHz bandwidth, phase response near 0 degrees, and 65 fA/rootHz input-referred noise. It was fabricated in 0.18 $\mu$ m CMOS technology and dissipates 436 $\mu$ W from a 1.8V supply.

- M-12 **A 366kS/s 400 $\mu$ W 0.0013mm<sup>2</sup> Frequency-to-Digital Converter Based CMOS Temperature Sensor Utilizing Multiphase Clock**, *Kisoo Kim, Hokyu Lee, Sangdon Jung, Chulwoo Kim, Korea University, Seoul, Korea*

The proposed temperature sensor is based on CMOS ring oscillators and a frequency-to-digital converter capable of simple and efficient temperature conversion to digital value. The proposed temperature sensor consumes 400 $\mu$ W at a conversion rate of 366kS/s and performs the fastest temperature-to-digital conversion among those introduced in previous work. The whole block occupies 0.0066 mm<sup>2</sup> (0.0013 mm<sup>2</sup> for temperature sensor). Four multiphase clocks were utilized to enhance the resolution of the sensor 8 times better. After one point calibration, the chip-to-chip measurement spread was +2.748 $^{\circ}$ C ~ -2.899 $^{\circ}$ C over the temperature range of -40 $^{\circ}$ C to 110 $^{\circ}$ C.

- M-13 **Design-for-Manufacturing Features in Nanometer Logic Processes – A Reverse Engineering Perspective**, *Dick James, Chipworks Inc.*

Recently we have seen the introduction of production disciplines known collectively as Design for Manufacturability (DFM), which are techniques used to co-optimize design, layout, and processing to reduce variability and improve manufacturing parameters. This paper illustrates some different layout features used for DFM in some recent 65-, and 45-nm products.

- M-14 **Quadratic Differential and Integration Technique in V<sup>2</sup> Control Buck Converter with Small ESR Capacitor**, *Shih-Jung Wang, Yu-Huei Lee, Yung-Chih Lai, Ke-Horng Chen, National Chiao Tung University, Hsinchu, Taiwan*

This paper proposes a quadratic differential and integration (QDI) technique for the design of buck converters with small equivalent series resistance (ESR) of the output capacitor. The QDI circuit not only further removes the dependence of ESR in the V<sup>2</sup> control but also achieves a fast transient response with

small load transient voltage variation. The experimental results show the output voltage can have voltage ripple about 30 mV and recovery time of 20  $\mu$ s in case of 300 mA load current variation.

M-15 **Adaptive Performance Compensation with In-Situ Timing Error Prediction for Subthreshold Circuits**, *H. Fuketa, M. Hashimoto, Y. Mitsuyama, T. Onoye, Osaka University*

This paper presents an adaptive technique for compensating manufacturing and environmental variability in subthreshold circuits using "canary Flip-Flop" that can predict timing errors. A 32-bit Kogge-Stone adder whose performance was controlled by body-biasing was fabricated in a 65 nm CMOS process. Measurement results show that the adaptive control can compensate PVT variations and improve energy-efficiency of subthreshold circuits significantly compared to worst-case design and operation with guardbanding.

M-16 **A Full Chip Integrated Power and Substrate Noise Analysis Framework for Mixed-Signal SoC Design**, *D. Kosaka\*,\*\*\*\*, Y. Bando\*, G. Yokomizo\*\*, K. Tsuboi\*\*, Y. S. Li\*\*\*, S. Lin\*\*\*, M. Nagata\*,\*\*\*\*, \*Kobe University, \*\*STARC, \*\*\*Apache Design Solutions, Inc., \*\*\*\*A-R-Tec Corp.*

A fully integrated framework of full-chip power and substrate noise analysis is discussed, featuring description of transistor-level custom circuits as dynamic noise sources, a high capacity solver for chip-level substrate coupling, and noise back annotation flow to transistors of sensitive circuits. Recursive evaluation of power current and operation timing under the presence of dynamic IR drop greatly improves the accuracy of analysis. A 90-nm CMOS chip was examined both by on-chip noise measurements and full-chip noise analysis.

M-17 **An Accurate and Fast Behavioral Model for PLL Frequency Synthesizer Phase Noise/Spurs Prediction**, *Xiaozhou Yan, Xiaofei Kuang, Nanjian Wu, Chinese Academy of Sciences*

This paper presents a behavior model for PLL Frequency Synthesizer. All the noise sources are modeled with noise voltages or currents in time-domain. An accurate VCO noise model is introduced, including both thermal noise and 1/f noise. The behavioral model can be co-simulated with transistor level circuits with fast speed and provides more accurate phase noise and spurs prediction. Comparison shows that simulation results match very well with measurement results.

M-18 **Pathfinding for 22nm CMOS Designs using Predictive Technology Models**, *Xia Li, Wei Zhao, Yu Cao\*, Zhi Zhu, Jooyoung Song, David Bang, Chi-Chao Wang\*, Seung H. Kang, Joseph Wang, Matt Nowak, Nick Yu, Qualcomm Incorporated, \*Arizona State University*

Traditional IC scaling is difficult at the 22nm node. Dealing with these challenges increase product development cycle time. For continued CMOS scaling, it requires having Predictive Technology Models to start design explorations in new process nodes as early as possible. In this paper we propose a strategy that enables simultaneous investigation of advanced process and design concepts. We capture the heuristic device behavior during the scaling, make tradeoffs of circuit design for next technology node.

M-19 **An SRAM Reliability Test Macro for Fully-Automated Statistical Measurements of  $V_{\min}$  Degradation**, *Tae-Hyoung Kim, Wei Zhang, Chris H. Kim, University of Minnesota*

An SRAM reliability test macro is designed in a 1.2V, 65nm CMOS process for statistical measurements of  $V_{\min}$  degradation. An automated test program efficiently collects statistical  $V_{\min}$  data and reduces test time. The proposed test structure enables  $V_{\min}$  degradation measurements for different SRAM failure modes such as the SNM-limited case and the access-time-limited case. The impact of voltage stress on the time to cell data flip was measured.

M-20 **A 60 GHz CMOS Balanced Downconversion Mixer with a Layout Efficient 90° Hybrid Coupler**, *R. E. Amaya, Cornelius J. Verver, Communications Research Centre, Ottawa, Canada.*

This paper presents the design and implementation of a downconversion mixer implemented in a standard 130nm commercial CMOS process and aimed at applications in the 60 GHz ISM band. A balanced mixer configuration was implemented by using a layout efficient 90o hybrid coupler which serves as a diplexer to inject the LO signal while also providing two outputs with 3dB of attenuation and 90o phase shift. The mixer achieves a conversion gain of +0.3 dB and OIP3 of +2.3 dBm. The mixer also consumes 200uA of DC current and 8mA of peak current while driven from a single 2V supply. The layout area including test pads is 1.4mm x 1.0mm.

- M-21 **A 0.46ps RJrms 5GHz Wideband LC PLL for Multi-Protocol 10Gb/s SerDes**, C. Rao, A. Wang, S. Desai, Prism Circuits Inc.
- A 2.3 to 5GHz LC PLL is implemented in 65nm CMOS for 0.6 to 10Gb/s SerDes. The LC VCO has 67% coarse tuning range, 9.6% worst-case hold range. RJrms at TX output with a clock pattern is 460fs at 5GHz, 548fs at 3.125GHz. Total power dissipated is 29mW at 5GHz.
- M-22 **A 10MHz to 315MHz Cascaded Hybrid PLL with Piecewise Linear Calibrated TDC**, Minyoung Song, Young-Ho Kwak, Sunghoon Ahn, Wooseok Kim\*, ByeongHa Park\* and Chulwoo Kim, Korea University, \*Samsung Electronics
- An ADPLL with a piecewise linear calibrated hierarchical TDC is proposed to achieve a wide range of operation and a CPPLL is cascaded to filter out 1/f noise. A phase selectable divider is also proposed to divide the clock frequency while keeping the relative phase difference of output same as that of input. The cascaded hybrid PLL fabricated in 65nm CMOS process burns 17mW and occupies 0.4mm<sup>2</sup>. The measured jitters are 1.1nspp and 223.6psrms, respectively with a multiplication factor of 1,024.
- M-23 **A 430MHz-2.15GHz Fractional-N Frequency Synthesizer for DVB and ABS-S Applications**, P. Yu, Z. Gong, M. Gu, Y. Shi, F. Dai\*, Suzhou-CAS Semiconductors Integrated Technology Research Center, \*Auburn University
- The frequency synthesizer covers a very wide frequency range of 430MHz-2.15GHz while integrates only one on-chip inductor. The AFC helps to correct VCO sub-band selection when PVT varies. The LDO helps to suppress in-band and out-of-band noise generated by 3rd-order  $\Sigma\Delta$  modulator. The fast setting time and low phase noise make the PLL suitable of numerous multi-band, multi-standard applications such as DVB and ABS-S
- M-24 **SiGe Digital Frequency Dividers with Reduced Residual Phase Noise**, S. Horst, S. Phillips, H.M. Lavasani, F. Ayazi, J.D. Cressler, Georgia Institute of Technology
- A new design methodology for achieving very low residual phase noise in SiGe HBT digital frequency dividers is presented. A modified CML D latch design is proposed that enables the latch to draw more current, thereby reducing the residual phase noise. The latch modification yields a 10 dB phase noise improvement over a standard D latch topology, with measurements at 10 GHz resulting in a phase noise floor of -160 dBc/Hz. The circuit dissipates 350 mW of DC power, but a standard phase noise figure-of-merit that accounts for phase noise, DC power dissipation, and operating frequency, reveals that this new design is among the best in its class.
- M-25 **A 54-862 MHz CMOS Direct Conversion Transceiver for IEEE 802.22 Cognitive Radio Applications**, Jongsik Kim, Seung Jun Lee, Seungsoo Kim, Jong Ok Ha, Junki Min\*, Yun Seong Eo, Hyunchol Shin, Kwangwoon University, \*Samsung Electro-Mechanics Co.
- A CMOS single-chip transceiver IC is developed for IEEE 802.22 cognitive radio applications. Over the 54 to 862 MHz ultra wideband, the in-band harmonic distortions of the transmitter and the unwanted harmonic mixing of the receiver are effectively suppressed by exploiting the dual-path direct-conversion architecture. A seamless coverage of the full band is achieved by employing a fractional-N PLL with a single LC VCO and a multi-modulus LO generator. Implemented in 0.18  $\mu$ m CMOS, the receiver achieves 110 dB gain dynamic range, < 8.5 dB noise figure, and > -11 dBm IIP3 at the LNA bypass mode. The transmitter delivers -3 dBm output power with OP1dB and OIP3 greater than +6.4 dBm and +15.9 dBm, respectively. On-chip calibration circuits suppress the image and carrier leakage components below -41 dBc across the total band.
- M-26 **A 1.8V, Sub-mW, Over 100% Locking Range, Divide-by-3 and 7 Complementary-Injection-Locked 4 GHz Frequency Divider**, Y.-C. Lo, H.-P. Chen, J. Silva-Martinez, S. Hoyos, Texas A&M University
- A low-power wideband divide-by-odd-ratio ring-oscillator-based complementary-injection-locked frequency divider that widens its locking range over 100% is proposed. The differential architecture's frequency locking range spans from 1.4-to-4.4 GHz with an input incident power of -4dBm. The power consumption of the 0.18 $\mu$ m CMOS topology is 0.9mW while locked at 4.7GHz.

## Session 9 - Nyquist Rate ADC's

Tuesday Morning, September 15  
Oak Ballroom

Chair: Eric Naviasky, Cadence

Co-Chair: Ronald Kapusta, Analog Devices

### 9:00 AM Introduction

#### 9:05 AM 09-1 **A 10b 50MS/s Opamp-Sharing Pipeline A/D With Current-Reuse OTAs**, *Kailash Chandrashekar and Bertan Bakkaloglu, Arizona State University, Tempe, AZ*

A 10b opamp-sharing pipeline A/D using current-reuse OTAs is presented. The current-reuse OTA, with two NMOS differential inputs, facilitates opamp-sharing between consecutive stages and constant transistor biasing to minimize power consumption. The A/D is fabricated in 0.18 $\mu$ m CMOS process and achieves SNDR > 57.5dB with 9.2mW analog power consumption at 50MS/s.

#### 9:30 AM 09-2 **A 12-b 56MS/s Pipelined ADC in 65nm CMOS**, *Adrian Leuciuc, William Evans, Honghao Ji, Eric Naviasky and Xinhua He, Cadence Design Systems, Columbia, MD*

This paper describes a 1.2V, 12-b pipelined ADC implemented in a 65nm CMOS process. The circuit design techniques used to obtain high gain operational amplifiers in a deep-submicron process are described. A novel top-level simulation methodology is used to quantify the transient errors in each subrange stage, allowing their optimal design. The circuit employs various techniques for power reduction: class A-B op-amps, improved reference design, and frequency-to-current biasing.

#### 9:55 AM 09-3 **A 9.43-ENOB 160MS/s 1.2V 65nm CMOS ADC Based on Multi-Stage Amplifiers**, *Young-Ju Kim, Hee-Cheol Choi, Kyung-Hoon Lee, Gil-Cho Ahn, Seung-Hoon Lee, Ju-Hwa Kim\*, Kyoung-Jun Moon\*, Michael Choi\*, Kyoung-Ho Moon\*, Ho-Jin Park\* and Byeong-Ha Park\*, Sogang University, Seoul, Korea, \*Samsung Electronics Co., Gyeonggi-Do, Korea*

A 12-bit 160MS/s pipeline ADC is presented. The proposed multipath frequency-compensation technique enables the conventional RNMC-based three-stage amplifier to achieve a stable operation. The measured differential and integral nonlinearities are less than 0.69LSB and 1.00LSB respectively. The ADC shows a FoM of 0.75pJ/conv-step at 160MS/s and 1.2V.

#### 10:20 AM 09-4 **A Continuous-Time Input Pipeline ADC with Inherent Anti-Alias Filtering**, *David Gubbins\*, Sunwoo Kwon, Bumha Lee\*\*, Pavan Kumar Hanumolu and Un-Ku Moon, \*Linear Technology, Colorado Springs, CO, Oregon State University, Corvallis, OR, \*\*National Semiconductor, Santa Clara, CA*

The first continuous-time input pipeline Nyquist-rate ADC architecture with inherent anti-alias filtering is introduced. Such an approach overcomes many of the challenges associated with a pure switched-capacitor architecture. Inherent anti-alias filtering is implemented in the first stage MDAC using first order Sinc filtering and a simple RC filter, allowing the possibility of eliminating costly anti-alias filters. The effect of switched capacitor sampling distortion is reduced. This architecture also eases the jitter requirements of the ADC clock when compared to switched capacitor pipeline ADCs. 9.85 ENOB is achieved with 21.4mW analog power from a 1.8V supply at 26MSPS in a 0.18 $\mu$ m CMOS process.

### 10:45 AM BREAK

#### 11:05 AM 09-5 **Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC**, *Yanfei Chen, Xiaolei Zhu, Hirota Tamura\*, Masaya Kibune\*, Yasumoto Tomita\*, Takayuki Hamada\*, Masato Yoshioka\*, Kiyoshi Ishikawa\*, Takeshi Takayama\*, Junji Ogawa\*, Sanroku Tsukamoto\* and Tadahiro Kuroda, Keio University, Yokohama, Japan, \*Fujitsu Laboratories Ltd., Kawasaki, Japan*

A split capacitor DAC calibration method is proposed that a bridge capacitor larger than conventional design allows a tunable capacitor to compensate for mismatch. To guarantee proper calibration, a comparator with digital timing control offset cancellation is proposed. An 8-bit successive approximation ADC with 4b+4b split capacitor DAC calibration has been implemented in 65nm CMOS, achieving 0.3LSB DNL and INL with 180fF input capacitance.

#### 11:30 AM **A 6b 3GS/s Flash ADC with Background Calibration**, *Masashi Kijima, Kenji Ito, Kuniyoshi Kamei and*

09-6 *Sanroku Tsukamoto\**, *Fujitsu VLSI Ltd., Kasugai, Japan*, *\*Fujitsu Laboratories Ltd., Kawasaki, Japan*

A 6b 3GS/s flash ADC is implemented in a 90nm CMOS process. The proposed ADC is based on an interpolating flash architecture without a T/H. To overcome the offset mismatch among comparators, an interleaved offset calibration system is applied. The ADC achieves the ENOB of 5.8bit at 3GS/s and the ERBW of 500MHz, while consuming 90mW from a 1.2V supply. The ADC occupies a 0.28mm<sup>2</sup> area.

11:55 AM **A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS**, *Jing Yang, Thura Lin Naing and Bob Brodersen, University of California, Berkeley, CA*  
09-7

An asynchronous 6bit 1GS/s ADC is achieved by time inter-leaving two ADCs based on binary successive approximation algorithm (SA) using a capacitive ladder. The semi-close loop asynchronous technique eliminates the high internal clocks and significantly speeds up the SA algorithm. One bit redundancy is implemented to compensate the process variation of parasitic and the MOM capacitance. Fabricated in 65nm CMOS with an active area of 0.11mm<sup>2</sup>, it achieves a peak SNDR of 31.5dB at 1 GS/s sampling rate and has a power consumption of 6.7mW for the analog and digital processing.

## Session 10 - Power Management

Tuesday Morning, September 15

Fir Ballroom

Chair: Raj Amirtharajah, University of California, Davis

Co-Chair: Cory Arnold, Maxim Integrated Products

9:00 AM **Introduction**

9:05 AM **Integrating Magnetics for On-Chip Power: Challenges and Opportunities (INVITED)**, *Charles R. Sullivan, Thayer School of Engineering at Dartmouth, Hanover, NH*  
10-1

Integration of efficient power converters requires a technology for efficient, high-power on-chip inductors. The state of the art is reviewed, and possible future developments are discussed for both air-core and magnetic-core inductors. Performance limits and scaling are analyzed. General design possibilities are outlined and different approaches are compared. Magnetic materials are reviewed, and nano-granular composite materials are highlighted as an attractive option.

9:55 AM **A Wide-Load-Range Single-Inductor-Dual-Output Boost Regulator with Minimized Cross-Regulation by Constant-Charge-Auto-Hopping (CCAH) Control**, *Xiaocheng Jing, Philip Mok and Ming Chak Lee, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*  
10-2

A novel single-inductor-dual-output (SIDO) boost regulator with constant-charge-auto-hopping (CCAH) control to minimize the cross interference between channels is presented. In order to have a predictable system switching noise spectrum, the switching frequency of the converter is automatically hopped between 1.25MHz and 1.25MHz/N where N = 2 to 5 according to the loads and during transient. Load transient measurements show that the cross-regulation is less than 0.1mV/mA with a 200mA change of load current.

10:20 AM **A Single-Inductor Dual-Output Switching Converter with Low Ripples and Improved Cross Regulation**, *Weiwei Xu, Ye Li, Xiaohan Gong, Zhiliang Hong and Dirk Killat\*, Fudan University, Shanghai, China, \*Brandenburg University of Technology, Cottbus, Germany*  
10-3

This paper proposes a novel fly capacitor method for single-inductor dual-output (SIDO) switching converters to reduce the output ripples and spikes. An adaptive common-mode control is presented to suppress the cross-regulation problem. The converter can automatically switch between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) control to improve the efficiency. The SIDO converter is specified for one channel 1.2 V/400 mA and the other 1.8 V/200 mA with input voltage ranging from 2.7 V to 5 V. The chip has been fabricated on a 0.25µm CMOS mixed signal process. The conversion efficiency is 82% at a total output power of 840 mW while the output ripples are about 20 mV and spikes less than 40 mV.

10:45 AM **BREAK**

11:05 AM **An Area- and Power-efficient Monolithic Buck Converter with Fast Transient Response**, *Ying Wu, Sam Tsui and Philip Mok, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*

A voltage-mode Buck converter with a novel Pseudo-Type III compensation is presented. It maintains the fast load transient response, as confirmed by the measured loop gain, and 7 $\mu$ s settling time for 500mA load current step. It also transforms the Type III compensator into a summation of an area- and power-efficient error amplifier plus a low-power band-pass filter. Consequently, the area and power consumption of proposed compensator is reduced by 80% and 85%.

11:30 AM **An Efficiency-Enhanced Auto-Reconfigurable 2x/3x SC Charge Pump for Transcutaneous Power Transmission**, *Xiwen Zhang and Hoi Lee, The University of Texas at Dallas, Richardson, TX*

An auto-reconfigurable 2x/3x switched-capacitor charge pump (SC-CP) for transcutaneous power transmission is presented in this paper. The proposed SC-CP can automatically configure its own voltage conversion ratio by adaptive control circuitry for maintaining high efficiencies of the DC/DC regulator under coupling variations. An adaptive deadtime control is developed to improve the efficiency of the proposed SC-CP by minimizing the shoot-through current. Implemented in a standard 0.35- $\mu$ m n-well CMOS process, the proposed SC-CP achieves peak power efficiencies of 95% (2x) and 92% (3x). The efficiency of the DC/DC regulator with the proposed SC-CP is improved by >25%, compared to that using the conventional 3x SC-CP, when the input voltage varies from 1.6V to 2.4V.

11:55 AM **A Novel On-Chip Voltage Generator for Low Voltage DRAMs and PRAMs**, *Tatsuya Matano, Koji Sato, Kiyoshi Nakai and Isamu Asano, Elpida Memory, Inc., Kanagawa, Japan*

A novel on-chip voltage generator suitable for 1V range DRAMs and PRAMs has been developed using a cross charge pump circuit with a shift charge method, an incidental pumping scheme, and a dual regulator scheme. These effectiveness has been confirmed by the experimental 128Mb PRAM device using 0.072 $\mu$ m CMOS process.

## Session 11 - Digital Wireline and PLL Techniques

Tuesday Morning, September 15

Pine Ballroom

Chair: Gu-Yeon Wei, Harvard University

Co-Chair: Afshin Montaz, Broadcom

9:00 AM **Introduction**

9:05 AM **Fast Lock Scheme for Phase-Locked Loops**, *Amir Bashir, Jing Li, Kiran Ivatury, Naveed Khan, Nirav Gala, Noam Familia\* and Zulfiqar Mohammed, Intel Corporation, Folsom, CA, \*Intel Corporation, Jerusalem, Israel*

A fast lock scheme for PLLs is presented, which can enable significant power savings in SOC designs. Multiple Self-Bias PLLs were designed to operate at VCO frequencies from 1.6GHz to 5GHz, and fabricated using 65nm CMOS process. Silicon measurements indicate up to 75% reduction in worst-case PLL lock times.

9:30 AM **ADC-Based Serial I/O Receivers (INVITED)**, *Chih-Kong Yang and E-Hung Chen, University of California, Los Angeles, CA*

Fully digital receiver frontends have garnered interest for serial I/O receivers. While the speed and resolution are achievable in CMOS technologies, the challenge is to achieve low power dissipation so that the I/O links can be integrated in large ASICs. This paper describes different design techniques and shows that power can be reduced by constraining the specifications and by making architectural trade-offs.

10:20 AM **A 2.4-GHz Low-Power All-Digital Phase-Locked Loop**, *Liangge Xu, Saska Lindfors, Kari Stadius and Jussi Ryyänen, Helsinki University of Technology, TKK, Finland*

This paper presents a 2.4-GHz all-digital phase locked loop (ADPLL) frequency synthesizer for wireless applications. The ADPLL is built around a digitally controlled LC oscillator, and it covers the target

frequency range with fine frequency resolution. In the feedback path, a high-speed topology is employed for the variable phase accumulator to count full cycles of the RF output. A simple technique based on a short delay line in the reference signal path effectively lowers power consumption of the time-to-digital converter (TDC) and reduces in-band spurs of the output spectrum. Fabricated in a 65-nm CMOS, the ADPLL has an active area of 0.24 mm<sup>2</sup>. Measured output frequency range is from 2.29 to 2.92 GHz. The worst case phase noise at 1-MHz offset over the whole frequency range is -120 dBc/Hz when the PLL consumes 12 mW from a 1.2-V supply, and -112 dBc when power is lowered to 8 mW. The in-band spurs are below -61 dBc, and far-off spurs below -57 dBc.

**10:45 AM BREAK**

11:05 AM **A Nonlinear Phase Detector for Digital Phase Locked Loops**, *Ping-Hsuan Hsieh, Jay Maxey\* and Chih-Kong Ken Yang, University of California, Los Angeles, CA, \*Texas Instruments, Dallas, TX*

This paper examines several transfer curves of the phase detector in a digital phase-locked loop and illustrates the benefits of applying non-linearity to the phase transfer characteristics. Taking advantage of the programmability of the digital implementation, the proposed technique shows a better trade-off between the acquisition speed and the steady-state dithering jitter performance.

11:30 AM **Nonlinear Behavior Study in Digital Bang-Bang PLL**, *Albert Vareljian, Mohsen Moussavi, William Bereza, Walter Fergusson, Charles Berndt and Rakesh H. Patel, Altera Corp., San Jose, CA*

A simple high-performance nonlinear digital PLL is fabricated in 90 nm CMOS with operating range of 0.5 to 3.25 GHz and 1.24 ps jitter. New insights into the PLL behavior are discussed. The classical "20Log" in-band phase noise tracking does not hold for the type of nonlinear digital loops.

11:55 AM **Analysis of Digital Bang-Bang Clock and Data Recovery for Multi-Gigabit/s Serial Transceivers**, *Yehui Sun and Hui Wang, Integrated Device Technology, Shanghai, China*

A Harmonic Balance method for analyzing digital bang-bang clock and data recovery (CDR) is proposed in this paper. The jitter tolerance performance of the CDR is predicted by a function with variables that can be easily correlated to design parameters. A 6.25 Gb/s serial transceiver was fabricated in 90 nm CMOS technology. Measurements show that the jitter tolerance performance can be accurately predicted by the proposed method.

## Session 12 - Process Integration and Manufacturing Issues

Tuesday Morning, September 15  
Cedar Ballroom

Chair: Philippe Jansen, IMEC

Co-Chair: David Sunderland, Boeing Space and Intelligence Systems

9:00 AM **Introduction**

9:05 AM **Pushing the Speed Limits of SiGe:C HBTs up to 0.5 Terahertz (INVITED)**, *Stefaan Decoutere, Stefaan Van Huylenbroeck, Bernd Heinemann\*, Alexander Fox\*, Pascal Chevalier\*\*, Alain Chantre\*\*, Thomas Meister<sup>^</sup>, Klaus Aufinger<sup>^</sup> and Michael Schröter<sup>#</sup>, IMEC, Leuven, Belgium, \*IHP, Frankfurt, Germany, \*\*STMicroelectronics, Crolles, France, <sup>^</sup>Infineon Technologies, Munich, Germany, <sup>#</sup>TUD, Dresden, Germany*

The European project DOTFIVE is a 3-year project targeting a 0.5 THz SiGe Heterojunction Bipolar Transistor for the future development of communication, imaging and radar applications. The project explores further evolutionary scaling of self-aligned selective epitaxial base HBTs, and advanced process modules and disruptive novel device architectures.

9:55 AM **The Challenge of Lead-Free Electronics for Aerospace Electronic Systems (INVITED)**, *Lloyd Condra, Stephan Meschter\*, Dave Pinsky\*\* and Anthony Rafanelli\*\*, Boeing, \*BAE Systems, \*\*Raytheon*

Abstract-Most commercial electronics manufacturers are delivering lead-free electronic components, assemblies, and equipment to aerospace users, with significant impact on the design, production, and support of aerospace electronic systems. Unique aerospace requirements force the aerospace industry to



develop unique responses to the challenges posed by lead-free electronics.

**10:45 AM BREAK**

11:05 AM **High Voltage Devices in Advanced CMOS Technologies (INVITED)**, *Raúl Andrés Bianchi, Christine Raynaud, Floria Blanchet, Frederic Monsieur and Olivier Noblanc, STMicroelectronics, Crolles Cedex, France*  
12-3

CMOS technologies for mobile systems require integrated high voltage devices, on bulk and thin SOI substrates, for analog baseband and RF power applications. Main challenges for their integration in advanced CMOS are explained. Gateoxide thickness influence on the relevant figures of merit and considerations on performance-reliability tradeoff are provided

11:55 AM **Angle Sensitive Pixels in CMOS for Lensless 3D Imaging**, *Albert Wang, Patrick Gill and Alyosha Molnar, Cornell University, Ithaca, NY*  
12-4

We present a pixel-scale CMOS sensor built in an unmodified 130nm CMOS process, for near-field, lensless imaging. This angle-sensitive pixel uses local diffraction gratings to discriminate the incident angle of incoming light. Arrays of these pixels can reconstruct the 3-dimensional structure of light sources.

## Session 13 - RF Transceivers and Building Blocks

Tuesday Afternoon, September 15

Oak Ballroom

Chair: John Rogers, Carleton University

2:00 PM **Introduction**

2:05 PM **A 5.5mA 2.4-GHz Two-Point Modulation Zigbee Transmitter with Modulation Gain Calibration**, *Rui Yu, Theng-Tee Yeo, Kwang-Hung Tan, Shouxian Mou, Yike Cui, Haifeng Wang, Hwa-Seng Yap, Eugene Ting and Masaaki Itoh, WIPRO Techno Center, Singapore*  
13-1

A 2.4-GHz two-point modulation IEEE 802.15.4 (Zigbee) compliant transmitter is presented. This sigma-delta fractional-N PLL based transmitter is optimized for both low-power and low-cost purposes. A novel closed-loop calibration scheme is proposed to minimize the gain mismatch between two modulation points, which is the main source of error in two-point modulation. Fabricated in a 0.15- $\mu\text{m}$  CMOS process, the proposed transmitter achieves EVM less than 8% for 2-Mchips/s MSK modulated signal and consumes 5.5mA under a 1.55-V regulated power supply. The core area is 0.8 $\times$ 1.1mm<sup>2</sup>.

2:30 PM **A SAW-less CMOS CDMA Receiver With Active Tx Filtering**, *Himanshu Khatri, Prasad S. Gudem\* and Lawrence E. Larson, University of California, San Diego, La Jolla, CA, \*Qualcomm Inc., San Diego, CA*  
13-2

A CDMA-2000 receiver that eliminates the interstage SAW filter is presented. An active technique is proposed for filtering the transmitter leakage after downconversion. This technique improves the triple-beat (TB) and IIP2 performances by 6.5 dB each, at the expense of a small increase in DC current and noise.

2:55 PM **A High Dynamic Range ASK Demodulator for Passive UHF RFID with Automatic Over-Voltage Protection and Detection Threshold Adjustment**, *Ganesh Balachandran and Raymond Barnett, Texas Instruments, Inc., Dallas, TX*  
13-3

This paper presents a passive UHF RFID ASK demodulator that operates over a +24dBm to -14dBm RF input power range. The demodulator automatically adjusts between high sensitivity mode for weak RF signals and over-voltage protection mode for high RF power. The input over-voltage protection circuit is designed to protect the IC from high input power while not impacting the sensitivity at weak input power. The demodulator is comprised of a RF rectifier, a variable gain attenuator with automatic threshold adjustment and a nano-power data slicer. The demodulator handles demodulating signals with a minimum to maximum envelope ratio of 0.8 over the entire input power range, and the data slicer consumes only 160nA from a 0.9 to 1.25V rectified supply. The RFID chip is fabricated in a 0.13 $\mu\text{m}$  analog-CMOS technology and the entire chip occupies an area of 0.55 mm<sup>2</sup>.

3:20 PM **A 1 Watt 1-5 GHz Class B Push-Pull Si/SiGe HBT Power Amplifier**, *Tyson Wooten and Lawrence Larson, University of California at San Diego, La Jolla, CA*  
13-4

A 1-5 GHz, Class B push-pull power amplifier is reported. The amplifier utilized low loss, broadband baluns, coupled spiral inductor transformers, and a differential  $\pi$ -doubler. Output powers of greater than 30 dBm and efficiencies greater than 30% from 1 GHz to 4 GHz have been achieved.

**3:45 PM BREAK**

4:00 PM **Challenges in the Design of Cognitive Radios (INVITED)**, *Behzad Razavi, University of California, Los Angeles, CA*  
13-5

Cognitive radios are expected to perform spectrum sensing and communication in the frequency range of tens of megahertz to about 10 GHz. As such, they pose tough architecture and circuit design problems. This paper deals with issues such as broadband, low-noise amplification, multi-decade carrier frequency synthesis, and spectrum sensing. The paper also describes the effect of nonlinearity and local oscillator harmonics, demonstrating that cognitive radios entail more difficult challenges than do software-defined radios. Multi-decade synthesis techniques and RF-assisted sensing methods are also presented.

4:50 PM **A 29 dBm CMOS Class-E Power Amplifier with 63% PAE Using Negative Capacitance**, *Yonghoon Song, Sungho Lee, Jaejun Lee and Sangwook Nam, Seoul National University, Seoul, Korea*  
13-6

This paper proposes class-E power amplifier including negative capacitance to optimize shunt drain capacitance. The negative capacitance improves efficiency, compensates for surplus shunt drain capacitance resulting from parasitic capacitance, and is implemented without an external circuit. A cascode single-ended class-E RF power amplifier including driver stage is fabricated using a 0.13- $\mu$ m standard CMOS technology delivering 29 dBm with 66% drain efficiency and 63% power-added efficiency at 1.8 GHz.

5:15 PM **CMOS RF Transmitter with Integrated Power Amplifier Utilizing Digital Equalization**, *Dae Hyun Kwon, Hao Li, Yuchun Chang, Richard Tseng and Yun Chiu, University of Illinois at Urbana-Champaign, Urbana, IL*  
13-7

A digitally equalized 3.5-GHz CMOS RF transmitter (TX) with integrated 23-dBm power amplifier (PA) in 0.13- $\mu$ m CMOS is presented. I/Q mismatch and memoryless nonlinearities of the whole transmit path, including the severe amplitude and phase distortions of the on-chip Class-B PA, are compensated by a digital, two-dimensional look-up table (2-D LUT) adapted by an LMS algorithm. The equalization results in an efficient TX with minimum analog and RF complexity. When a 20-MHz, 64-QAM OFDM signal with 9.6-dB peak-to-average power ratio (PAPR) was transmitted, the measured average drain efficiency of the PA was 12.5% with a -29.6-dB EVM after equalization. An 8.7-dB EVM improvement was achieved with a regular baseband sample rate of 80 MS/s in a typical 802.11a transmitter. A peak drain efficiency of 55% and a 25-dBm saturated output power were also measured for the same PA in a stand-alone package.

## Session 14 - Micro-Robotics and Energy Harvesting

Tuesday Afternoon, September 15  
Fir Ballroom

Chairman: Gu-Yeon Wu, Harvard University

2:00 PM **Introduction**

2:05 PM **Power And Actuation Challenges For Flying Robotic Insects**, *Robert Woods, Harvard SEAS, Cambridge, MA*  
14-1

2:40 PM **Hardware Specialization And Acceleration For Ultra Low Power Computing In Microbotic Bees**, *David Brooks, Harvard SEAS, Cambridge, MA*  
14-2

3:15 PM **CMOS-Based Power Conversion Circuitry (Including Energy Harvesting Applications)**, *Seth Sanders, University of California, Berkeley, Berkeley, CA*  
14-3

**3:50 PM BREAK**

## **Session 15 - Modeling of Passive Elements and Reliability**

Tuesday Afternoon, September 15  
Pine Ballroom

Chair: Gennady Gildenblat, Arizona State University  
Co-Chair: Hidetoshi Onodera, Kyoto University

**2:00 PM Introduction**

**2:05 PM RF CMOS is More than CMOS: Modeling of RF Passive Components (INVITED),** *Zhiping Yu, Colin McAndrew\**, Tsinghua University, China, \*Freescale Semiconductor, Tempe, Az  
15-1

This paper details recent progress in modeling of inductors, transformers, and resistors. One- and two-segment inductor models are analyzed, including techniques for modeling distributed effects and coupling through a lossy substrate. Details of accurate physical modeling of polysilicon resistors, including nonlinearities, parasitics, and self-heating, are provided.

**2:55 PM Measurement and Analysis of Contact Plug Resistance Variability (INVITED),** *Karthik Balakrishnan and Duane Boning, Massachusetts Institute of Technology, Cambridge, MA*  
15-2

The importance of contacts increases with technology scaling due to higher resistance and variability. Techniques for measurement, analysis, and modeling of variation in contacts are presented. A test-chip enables contact plug resistance measurement in 35,000 DUTs. Statistical analysis shows significant layout effects on mean resistance; spatial analysis shows systematic components as well as random, normally distributed variation. Spatial separation-distance correlation is negligible. Future compact models are needed to incorporate such variability information.

**3:45 PM BREAK**

**4:00 PM Sensitivity Computation Using Domain-Decomposition for Boundary Element Method Based Capacitance Extractors,** *Yu Bi, Kees-Jan van der Kolk and Nick van der Meijs, Delft University of Technology, Delft, The Netherlands*  
15-3

We present an algorithm that enables an extension of BEM based 3-D capacitance extractors to generate both the nominal capacitances and their sensitivities w.r.t. all geometric parameters with only one extraction. The algorithm is based on the domain-decomposition technique and has been implemented in a layout-to-circuit extractor. It is shown by experiments that the additional cost for the sensitivity computation is less than 20% of the time consumption for standard capacitance extraction.

**4:25 PM Circuit Aging Prediction for Low-Power Operation,** *Rui Zheng, Jyothi Velamala, Vijay Reddy\*, Varsha Balakrishnan, Evelyn Mintarno\*\*, Subhasish Mitra\*\*, Srikanth Krishnan\* and Yu Cao, Arizona State University, Tempe, AZ, \*Texas Instruments, Dallas, TX, \*\*Stanford University, Stanford, CA*  
15-4

Low-power circuit operations pose a unique challenge to aging prediction. Traditional models ignore the impact of the sleep period and thus, overestimate the degradation rate. This work examines critical model assumptions that are responsible for the NBTI effect. It then proposes a new aging model that effectively analyzes the degradation. The new model well predicts the aging behavior of 45nm and 65nm data with different operation patterns, especially sleep mode operation and dynamic voltage scaling.

**4:50 PM Impact of Transistor Level Degradation on Product Reliability (INVITED),** *Tanya Nigam, GLOBALFOUNDRIES, Sunnyvale, CA*  
15-5

Product level lifetime margins, determined by HCI and BTI, are shrinking with scaling. Accurate device-level HCI degradation models, together with known BTI models, are needed to predict frequency degradation of a ring oscillator. Both NBTI and HCI exhibit relief during AC operation and the respective contribution to RO frequency degradation is a function of applied bias.

## Session 16 - 3D ICs and 3D Systems

Tuesday Afternoon, September 15

Cedar Ballroom

Chair: Alvin Loke, Advanced Micro Devices

Co-Chair: Ann Rincon, SMSC

### 2:00 PM Introduction

2:05 PM **Trend from ICs to 3D ICs to 3D Systems (INVITED)**, Rao Tummala, Venky Sundaram, Ritwik Chatterjee, P. Markodeya Raj, Nitesh Kumbhat, Vijay Sukumaran, Vikay Sridharan, Abhishek Choudury, Qiao Chen and Tapobrata Bandyopadhyay, Georgia Institute of Technology, Atlanta, GA

Moore's Law drove the IC industry to a billion transistor chip but major barriers are foreseen beyond 32nm. One alternative may be stacked 3D ICs, a small system part, but miniaturization may require entire system miniaturization. 3D miniaturization described herein includes Si or wafer level interposers with Through-Package-Vias (TPV), nano-scale passives, thermal materials and interfaces and fine pitch system interconnections.

2:55 PM **The Prospect of 3D-IC (INVITED)**, Simon Wong and Abbas El Gamal, Stanford University, Stanford, CA  
16-2

This paper illustrates the performance advantages of 3D integrated circuits with two specific examples, namely 3D-FPGA and 3D-SRAM. Through strategic modification of the architectures to take advantage of 3D, significant improvement in speed and reduction in power consumption can be achieved.

3:20 PM **47% Power Reduction and 91% Area Reduction in Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking**, Mitsuko Saito, Yasufumi Sugimori, Yoshinori Kohama, Yoichi Yoshida, Noriyuki Miura, Hiroki Ishikuro and Tadahiro Kuroda, Keio University, Japan  
16-3

An inductive-coupling programmable bus is developed for NAND-flash-memory stacking. 3-coil channel arrangement scheme enables random access for memory read/write. Transmission power is reduced by 47% compared to [1]. A coil-layout style, XY coil, allows coils covered by logic interconnections, reducing area by 91%. Relayed-data transmission at 1.6Gb/s, BER < 10<sup>-12</sup> is achieved.

### 3:45 PM BREAK

4:00 PM **60GHz CMOS/PCB Co-Design and Phased Array Technology (INVITED)**, Joy Laskar, Stephane Pinel, Saikat Sarkar, Padmanavan Sen, Bevin Perumana, Matthew Leung, Debasis Dawn, David Yeh, Francesco Barale, Kevin Chuang, Gopal Iyer, Jong-Hoon Lee and Patrick Melet, Georgia Institute of Technology, Atlanta, GA  
16-4

In this paper, we present a highly integrated 60 GHz CMOS/PCB single-chip digital phased array solution, embedded in QFN package. This represents a unique opportunity to develop low power 60GHz multi-gigabit radio at a similar cost structure as a Bluetooth radio, addressing the needs of a multitude of bandwidth hungry wireless multimedia applications such as high definition streaming and massive side-loading. The convergence of 60GHz CMOS digital radio, phased array technology, low power multi-gigabit mixed-signal processing, low cost filter, phased array antenna embedded in standard package is discussed. In addition, uncompressed HDMI video streaming is demonstrated for the first time, using a standard battery (AAA) operated compact 60GHz CMOS/PCB QFN based module. These solutions offer the lowest energy per bit transmitted wirelessly at multi-gigabit rate, reported till date, to meet the very stringent low-power specifications for battery operated consumer electronic portable devices.

4:50 PM **The Highly Integrated Mobile WiMAX Module Using Embedded PCB & SIP Technology**, Jeong-Hoon Cho, Hwan-Hee Lee\* and Jeong-Sik Moon, LG Innotek, Ansan-si, Korea, \*Daeduck Electronics, Ansan-si, Korea  
16-5

The highly integrated mobile WiMAX module is presented by employing embedded PCB and system in package technology. It is one chip solution that is composed of WiMAX Chipset, memory, EEPROM, TCXO, PMIC and RF Front End. Furthermore, RF components such as LPF, BPF and Balun are embedded in the multilayered organic substrate. The total size of module targeted is 15mm x 15mm x 1.34mm. The measured results of the mobile WiMAX module show the Rx sensitivity of typical -98dBm and error vector modulation of -28dB in the Tx band with 3.3 V supply. The proposed module is compatible

with IEEE802.16e standard. In this paper, the high performance RCT (Radio Conformance Test) results of WiMAX module can be achieved by using embedded BPF, LPF with low insertion loss of the 2.07dB and 0.65dB, respectively.

5:15 PM 16-6 **System on Chip with 1.12mW-32Gb/s AC-Coupled 3D Memory Interface**, *Roberto Canegallo, Luca Perugini, Alberto Pasini\*, Massimiliano Innocenti, Mauro Scandiuazzo, Roberto Guerrieri\* and PierLuigi Rolandi, STMicroelectronics, Agrate, Italy, \*University of Bologna, Bologna, Italy*

An AC-coupled 3D memory interface for chip-to-chip communication is implemented in 90nm CMOS technology. It transfers 128 bit words between stacked SRAMs in an ARM-based System on Chip (SoC) platform at 250MHz. This interface requires 0.05mm<sup>2</sup> of occupation area and achieves a 32Gbit/sec of throughput and an average energy consumption of 35uW/Gbit/sec.

## Session 17 – Panel Discussion: Design of High Performance Radios in Bulk-CMOS, SOI, SiGe or GaAs?

Tuesday Afternoon, September 15  
Fir Ballroom

Panel Organizers: Aurangzeb Khan, Everspin Technologies  
Alireza Shirvani, Marvell Semiconductor

Panelists:

Dr. Shayan Farahvash  
Senior Engineer, Manager, RF Micro Devices

Peter Rabbeni  
Technology manager, Business Development, Wireless IBM

Jim McMahon  
Senior Staff Design Engineer, RF  
Cadence

Dr. Jacob Rael  
Senior Manager  
Broadcom

Horatio Mendez  
SOI Consortium

Thomas Zirkie  
Freescale

## Poster Session

Tuesday Evening, September 15  
Donner/Siskiyou/Cascade Ballrooms  
5:00 pm – 7:00 pm

T-01 **A 3 – 14V Rail-to-Rail Constant  $g_m$  Opamp in Conventional 0.18 $\mu$ m CMOS Process**, *E. Lee, Alfred Mann Foundation*

A 3 – 14V rail-to-rail constant  $g_m$  opamp was fabricated in a conventional 0.18 $\mu$ m CMOS process using 3.3V I/O devices. Different high-voltage opamp sub-circuits were proposed. For a 14V supply, variations on the input stage  $g_m$  were <10.2%. The opamp has a ft of 1.3MHz for a current consumption of 40.7 $\mu$ A.

T-02 **An Integrated CMOS Receiver Chip for NMR-Applications**, *J. Anders, P. SanGiorgio, G. Boero, Ecole Polytechnique Federal de Lausanne (EPFL)*

We present the first CMOS-only receiver chip for NMR-applications at 300 MHz. The system consists of an on-chip reception coil, a tuning-capacitor, a downconversion-mixer and a low-frequency gain-stage as well as biasing and offset-compensation circuitry. It has an input referred voltage noise density of 0.7 nV/sqrt(Hz) and a gain of 75 dB. The power consumption is 18 mA from a single 3.3 V supply. The chip is realized in 0.35  $\mu$ m technology and occupies an area of 1200 x 850  $\mu$ m<sup>2</sup>.

T-03 **A 1.2-V 2.7-mW 160MHz Continuous-Time Delta-Sigma Modulator with Input-Feedforward Structure**, *J. Zhang, L. Yao, Y. Lian, National University of Singapore, Singapore*

A power and area efficient continuous-time input-feedforward delta-sigma modulator (DSM) structure is proposed. The coefficients are optimized to increase the input range and reduce the power. The feedforward paths and the summer are embedded into the quantizer, hence the circuit is simplified, and the power consumption and area are reduced. The prototype chip, fabricated in a 0.13- $\mu\text{m}$  CMOS technology, achieves a 68-dB DR (Dynamic Range) and 66.1-dB SNDR (signal-to-noise-and-distortion ratio) over a 1.25-MHz signal bandwidth with a 160-MHz clock. The power consumption of the modulator is 2.7 mW under a 1.2-V supply, and the chip core area is 0.082mm<sup>2</sup>.

T-04 **Dual-Loop Direct VCO Modulation for Spread Spectrum Clock Generation**, *Christopher D. LeBlanc, Benjamin T. Voegeli, Tian Xia\**, IBM, \*University of Vermont

This paper presents a new spread spectrum clock generator (SSCG) circuit for EMI reduction. The proposed design adopts a standard integer-N phased locked loop (PLL) with two dual-voltage-controlled oscillators (VCOs). A frequency modulation loop is implemented with a digital frequency limit detector to direct the spectrum-spreading profile. An integrator is applied to generate the triangular modulation signal. Comparing with some recent designs [1,2,3,4] in the literature, the spread spectrum clock generator in this paper is simple and area efficient.

T-05 **Phase Noise in a Synchronized Concurrent Dual-Frequency Oscillator**, *A. Goel, H. Hashemi*, University of Southern California

The phase noise in synchronized concurrent dual-frequency oscillators is analyzed. The phase noise of an injection locked concurrent dual-frequency oscillator for either of the frequencies follows the phase noise of external injection near that frequency for offsets within the locking bandwidth of the injection. In the system of two coupled concurrent dual-frequency oscillators with bilateral coupling, the phase noise at either frequency is 3dB smaller than that at the free running case for offsets smaller than the locking bandwidth. Measurement results show a good match with the theory.

T-06 **A Unified Parallel Radix-4 Turbo Decoder for Mobile WiMAX and 3GPP-LTE**, *Ji-Hoon Kim, In-Cheol Park*, KAIST

This paper describes the energy-efficient implementation of a high performance turbo decoder, which is designed to support both Mobile WiMAX and 3GPP-LTE. We propose a new hardware architecture that can share hardware resources for the two standards. It consists of eight retimed radix-4 SISO decoders to achieve high throughput and a dual-mode hardware interleaver. A prototype chip exhibits a decoding rate of more than 100Mb/s with eight iterations while achieving an energy efficiency of 0.31nJ/bit/iter.

T-07 **Tera-Scale Performance Machine Learning SoC with Dual Stream Processor Architecture for Multimedia Content Analysis**, *T.-W. Chen, C.-S. Tang, S.-F. Tsai, C.-H. Tsai, S.-Y. Chien, L.-G. Chen*, National Taiwan University

A new SoC architecture for multimedia content analysis is implemented in 90nm CMOS technology. It focuses on the co-acceleration of computer vision and machine learning algorithms, and two stream processors with massively parallel processing elements are integrated to achieve tera-scale performance. In the dual processor architecture, the data are transferred between processors and the high bandwidth dual memory through the local media bus, which reduces the power consumption in the AHB data access.

T-08 **A Fully Integrated CMOS UHF RFID Reader Transceiver for Handheld Applications**, *J. Wang, C. Zhang, B. Chi, Z. Wang, Z.H. Wang*, Tsinghua University of China

This paper presents a fully integrated single-chip UHF radio frequency identification (RFID) reader transceiver for short distance handheld applications. The transceiver integrates an OOK modulator and a power amplifier in transmitter chain, an IQ direct-down converter, two operational amplifiers, and two comparators in the receiver chain. A PLL frequency synthesizer is also integrated on the same chip to provide the local oscillating signals for the transceiver. The measured output P1dB power of the transmitter is 16.4dBm and the measured receiver sensitivity is -60dBm. The on-chip integer-N synthesizer achieves a frequency resolution of 200kHz with a phase noise of -92.78 dBc/Hz at 100kHz frequency offset and -124.4 dBc/Hz at 1MHz frequency offset. The reader consumes a total power of 231.2mW when the output power is 16.4dBm. The proposed reader can communicate with commercial tags in a distance of more than 50cm without any off-chip power amplifier. The chip has a die area of 4.5mm\*1.3mm including pads.

- T-09 **A 1.5GS/s 4096-Point Digital Spectrum Analyzer for Space-Borne Applications**, *Brian Richards, Nicola Nicolici\*, Henry Chen, Kevin Chao, Robert Abiad\*\*, Dan Werthimer, and Borivoje Nikolić, University of California, Berkeley, \*McMaster University, \*\*Space Sciences Laboratory*
- A high-performance digital spectrometer backend ASIC has been designed for use with an off-the-shelf ADC frontend. The design is based on an architecture described in Simulink that has been field-tested on FPGA platforms for radio astronomy applications. The architecture maximizes the utilization of operators to nearly 100%. A test structure has been added to the design to support the detection of soft errors, since several space-borne applications may expose the circuit to high-energy particles. An in-house automated design flow was used to map the same Simulink description to a 90nm CMOS ASIC, preserving cycle-accurate and bit-accurate behavior. The chip operates with clock rates up to 390MHz, delivering a throughput of up to 1.56GS/s with 710 mW of power.
- T-10 **Read/Access-Preferred (REAP) SRAM – Architecture-Aware Bit Cell Design for Improved Yield and Lower  $V_{MIN}$** , *A. Goel, P. Ndai, J.P. Kulkarni, K. Roy, Purdue University*
- We present an architecture-aware SRAM design that decouples the conflicting requirements between read stability and writeability. Read and hold failures are reduced by preferentially sizing the cell to have better read stability at the expense of write failures (at iso-area). The increased write failures are handled by stretching the write cycle. Measurement results on a 90nm 2kb test chip show 80mV higher weak-write test voltage, 61%, 25% and 500X reduction in hold, read and write failures, respectively, without any increase in access failures. This results in improved yield relative to an iso-area nominal 6T cell, with only 3% loss in performance (based on architecture level simulation) on average.
- T-11 **A 1-V 60- $\mu$ W 16-Channel Interface Chip for Implantable Neural Recording**, *W. Liew, X. Zou, L. Yao, Y. Lian, National University of Singapore*
- A 1-V 60- $\mu$ W 16-channel interface chip dedicated for implantable neural signal recording is presented. To comply with the implantation safety issue, the overall system is optimized for low power dissipation. A power efficient front-end OTA topology and a novel dual-capacitive-array SAR ADC are adopted to achieve better power efficiency. A prototype fabricated in 0.35- $\mu$ m CMOS technology achieves NEF of 2.16 and THD of 0.53% at full output swing while providing 16-kSample/s per channel output.
- T-12 **CMOS-Based Flexible Multi-Site Retinal Stimulator Toward Retinal Prosthesis Technology**, *T. Tokuda, Y. Takeuchi, T. Noda, K. Sasagawa, and J. Ohta, Nara Institute of Science and Technology*
- We developed a CMOS LSI stimulator chip for retinal prosthesis technology with features of (1) multi-site stimulation using an on-chip stimulator, (2) light-controlled (image-based) stimulation. The retinal stimulator was configured as an array of small-sized intelligent CMOS stimulators called a "unit chip." We can set different conditions for each unit chip connected to a single set of 5-channel bus wiring and perform multi-site, constant-current biphasic retinal stimulation. We implemented simple binary light-sensing circuitry on the unit chip to realize image-based patterned stimulation on the retina. We verified that all the implemented functionalities correctly work and characterized the performance of the circuitry. A demonstration for image-based patterned current injection using radially aligned unit chips was also performed.
- T-13 **Chemical Microsystem Based on Integration of Microresonant Sensor and CMOS ASIC**, *K. S. Demirci, S. Truax, L. A. Beardslee, O. Brand, Georgia Institute of Technology*
- A silicon-based microsystem consisting of a mass-sensitive resonant sensor and a CMOS ASIC containing feedback circuitry is demonstrated for portable sensing applications. The feedback circuitry sustains oscillation of the resonant sensor at its mechanical resonance frequency ranging between 200 and 800 kHz. The microsystem has been used for detection of volatile organic compounds in the gas-phase, and a limit of detection of 13 ppm for toluene is obtained with a frequency stability of 16 mHz.
- T-14 **Fixed- and Variable-Length Ring Oscillators for Variability Characterization in 45nm CMOS**, *Ji-Hoon Park, Liang-Teck Pang\*, Kenneth Duong\*\*, Borivoje Nikolic, University of California Berkeley, \*IBM T.J. Watson Research Center, \*\*Sun Microsystems*
- Fixed- and variable-length ring oscillators (RO's) are designed for characterization of circuit-topology induced variations and spatial correlations. A 930 $\mu$ m  $\times$  775 $\mu$ m test array is implemented in a low-power 45nm CMOS process. Measurements from the fixed-length RO's quantify an increase in variability with

transistor stack height in logic gates and added variability associated to the top transistor in the stack. In addition, Variable-length RO's (VRO's) are designed to measure spatial correlation with a single-gate resolution.

- T-15 **An Energy-Recycling (ER) Technique for Field Color Sequential LCD Backlight Driving**, *Ming-Hsin Huang, Yueh-Chang Tsai, Chun-Yu Hsieh, and Ke-Horng Chen, National Chiao Tung University, Hsinchu, Taiwan*

An energy-recycling (ER) technique has been proposed to implement high power conversion efficiency and low cost solution of field color sequential (FCS) LEDs backlight driving. One recycling capacitor CR and one power-transistor MR are added to synchronous boost converter to compose the ER function. When the output voltage of FCS-LEDs backlight driver switches from 40V to 26V for driving RGB LEDs during related time interval, ER technique stops to boost input voltage and switches to recycle energy from output terminal to the recycling capacitor CR. Thus, the output voltage can be rapidly switched between two different voltage levels with minimum power losses. The proposed ER technique has been fabricated by TSMC 40V BCD process. The experimental results demonstrate fast and efficient output voltage tracking performance is achieved by the proposed ER technique.

- T-16 **A Monolithic Buck Converter Using Differentially Enhanced Duty Ripple Control**, *J. Fan, X. Li\*, J. Park, A. Huang, North Carolina State University, \*Texas Instruments Corporation*

This paper reports a monolithic DC-DC buck converter using the differentially enhanced duty ripple control (DE-DRC). Without any compensation circuit, this converter is stable over a wide input and output range with constant switching frequency. The large duty ripple voltage with a big noise margin gives the DE-DRC buck converter good noise immunity. The positive and negative differential difference amplifier gains can adjust the high and low frequency portion of the loop transfer function to achieve fast load transient response and pure resistive output impedance, which is used to achieve the adaptive voltage position (AVP) function. We demonstrated a 1.85MHz single phase converter with wide conversion range of 10%-86.6%. This circuit was implemented in 0.5 $\mu$ m BCD process of TI.

- T-17 **Nonvolatile SRAM (NV-SRAM) Using Functional MOSFET Merged with Resistive Switching Devices**, *S. Yamamoto\*,\*\*, Y. Shuto\*\*,\*\*\*, S. Sugahara\*\*,\*\*\*, \*Dept. Information Processing, Tokyo Institute of Technology, \*\*CREST, JST, \*\*\*ISEL, Tokyo Institute of Technology*

The paper presents functional MOSFET (F-MOSFET) architecture using nonpolar-type resistive switching devices (RSDs) for nonvolatile SRAM (NV-SRAM) application. The architecture can be achieved by connecting a RSD to the source terminal of an ordinary MOSFET. The current drive capability of the F-MOSFET can be modified by the resistance state of the connected RSD, which is a very useful function for recently emerging nonvolatile logic and reconfigurable logic applications. NV-SRAM can be easily configured with a standard SRAM cell and F-MOSFETs. Using our developed SPICE macromodel for nonpolar-type RSDs, the circuit operation of the proposed NV-SRAM cell was computationally simulated.

- T-18 **A Simplified Method for Phase Noise Calculation**, *Massoud Tohidian, Ali Fotowat Ahmady\*, Mahmoud Kamarei, University of Tehran, \*Sharif University of Technology, Tehran, Iran*

A new phase noise calculation method is proposed in which noise sources are modeled with single tone sources. It uses a nonlinear frequency-domain analysis to calculate total gain from noise sources to the output phase noise. This single tone (ST) simulation directly calculates noise frequency contributions and is much faster than Hajimiri's impulse sensitivity function (ISF) method. A quadrature VCO has been implemented in TSMC 0.18- $\mu$ m CMOS and the predicted phase noise matches measurement.

- T-19 **Design of 2xVDD-Tolerant I/O Buffer with 1xVDD CMOS Devices**, *Ming-Dou Ker, Yan-Liang Lin\*, Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan, \*Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.*

A new 2xVDD-tolerant I/O buffer realized with only 1xVDD devices has been proposed and successfully verified in silicon. With the dynamic source output technique and the gate-controlled circuit, the proposed I/O buffer can transmit and receive the signals of 2xVDD without suffering gate-oxide reliability issue to meet the mixed-voltage interface applications in microelectronic systems.

- T-20 **A 3-Level PWM ADSL2+ CO Line Driver**, *S. Gierkink, K. Lakshmikumar, V. Mukundagiri, D. Lim, A. Murali, F. Larsen, Conexant Systems Inc.*



A PWM ADSL2+ line driver with 2.2MHz signal bandwidth is realized in a 3 metal, 2 poly 0.35 $\mu$ m CMOS process. A low 8.832MHz switching frequency is used with filtering in the feedback path to suppress aliasing. Signal processing and triangular wave generation are combined in the forward integrators. The driver delivers 100mW to a 100 $\Omega$  line with an MTPR less than -52 dB. Active area is 3mm<sup>2</sup>.

T-21 **A 65nm CMOS, Ring-Oscillator Based, High Accuracy Digital Phase Lock Loop for USB2.0**, *Anant S Kamath, Biman Chattopadhyay, Gopalkrishna Nayak, Texas Instruments Inc.*

A high accuracy, ring-oscillator based Digital PLL is presented here. Sigma-Delta dithering is used for improved frequency accuracy. To reduce noise due to Sigma Delta dithering and to allow for passive filtering of this noise, the Sigma Delta section of the DCO is limited to a small range. This range, however, is not sufficient to account for frequency drifts due to temperature: a novel temperature compensation scheme is used for this purpose. The DPLL is built in 65nm technology, and provides a 480MHz output, with a phase noise of -103.5dBc/Hz at 1 MHz offset, and a frequency accuracy of +/-100ppm. It supports various input frequencies and does not require an external component.

T-22 **A Phase Detector for 12.5Gbps Clock and Data Recovery with Optimal Detection**, *J. Jang, T. Choi, B. Jung, Purdue University*

We propose a phase detector using a matched filter that maximizes the performance for a given input noise condition. The phase detector is designed for a 12.5Gbps CDR circuit. The performance of the proposed phase detector is compared with a typical one through simulation. A DLL-based clock recovery circuit is also implemented with the proposed phase detector and measured showing noise rejection characteristic.

T-23 **Design-Space Exploration of Backplane Receivers with High-Speed ADCs and Digital Equalization**, *H. Chung, G.-Y. Wei, Harvard University*

This paper presents a backplane receiver model consisting of a simple, accurate, experimentally-verified, and parameterized high-speed flash ADC and a configurable digital equalizer for design-space exploration. Simulations demonstrate tradeoffs between ADC and equalizer bit resolution while maintaining constant receiver performance.

T-24 **A CMOS 3.3-8.4 GHz Wide Tuning Range, Low Phase Noise LC VCO**, *Bodhisatwa Sadhu, Jaehyup Kim, Ramesh Harjani, University of Minnesota*

A novel inductor switching technique is used to implement a wide-band LC VCO in 130nm CMOS. It achieves a tuning range of 87.2% with phase noise between -122 and -117.2 dBc/Hz at 1MHz offset. The resulting PFTN-FOM lies between 6.6 and 10.2 dB which is the best reported to date.

T-25 **Near-Field Communication using Phase-Locking and Pulse Signaling for Millimeter-Scale Systems**, *Yu-Shiang Lin\*, Dennis Sylvester, David Blaauw, University of Michigan, \*Now with IBM TJ Watson Research Center*

An inductive coupling based proximity communication system is proposed for data readout of remote powered sensor systems with ultra small form factor in ~mm<sup>3</sup> range for implantable applications. The passive transponder is powered with a 1 $\times$ 1mm on-chip inductor, which also enables readout signaling using pulse signaling. The required resonance frequency for pulse signaling is obtained using a transponder PLL that locks to the incoming frequency transmitted by the reader system. The system is demonstrated with 0.13 $\mu$ m CMOS technology.

## Session 18 - Analog Techniques

Wednesday Morning, September 16

Oak Ballroom

Chair: Sang-Soo Lee, Hynix Semiconductor America

Co-Chair: Julian Tham, Arda Technologies

9:00 AM **Introduction**

9:05 AM **Noise in Short Channel MOSFETs (INVITED)**, *John McNeill, Worcester Polytechnic Institute, Worcester, MA*  
18-1

For short channel MOSFETs, observed noise can be much higher than predicted from thermal noise analysis of long channel MOSFETs. The increase can be viewed as resulting from the current noise approaching a shot noise limit as carrier transit time becomes so small that thermal equilibration does not have time to occur.

9:55 AM **Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier**, *Yoshinori Kusuda, Analog Devices, Wilmington, MA*  
18-2

It proposes a local feedback, named Auto Correction Feedback (ACFB), used in a chopper amplifier to suppress its offset related ripple. It nulls out amplifier's offset in DC domain which would otherwise become modulated ripple at the chopper amplifier's output, instead of filtering the ripple by a postfilter.

10:20 AM **A 0.5V 3.6ppm/°C 2.2pW 2-Transistor Voltage Reference**, *Mingoo Seok, Gyouho Kim, Dennis Sylvester and David Blaauw, University of Michigan, Ann Arbor, MI*  
18-3

A voltage reference using a depletion-mode device was designed in a 0.13µm CMOS process for achieving ultra-low power consumption and sub-1V operation without sacrificing temperature and supply voltage insensitivity. Measurements show a temperature coefficient of 3.6ppm/oC, line sensitivity of 0.033%/V, power supply rejection ratio of -67dB, and power consumption of 2.2pW. It requires only two devices and functions down at V<sub>dd</sub>=0.5V with an area of 1350µm<sup>2</sup>. A variant for higher V<sub>out</sub> is also demonstrated.

**10:45 AM BREAK**

11:05 AM **Moving Signals On and Off Chip (INVITED)**, *Elyse Rosenbaum, Hyeon-Min Bae, Karan Bhatia\* and Adam Faust, University of Illinois at Urbana-Champaign, Urbana, IL, \*Finisar Corp., Champaign, IL*  
18-4

Today, signals being transmitted on and off chip have frequency spectra extending to 10 GHz and beyond. The parasitic impedance associated with the package and ESD protection circuit can distort a signal and must be carefully managed. An overview of methods for parasitic impedance mitigation and co-design is provided.

11:55 AM **A Widely-Tunable and Ultra-Low-Power MOSFET-C Filter Operating in Subthreshold**, *Armin Tajalli and Yusuf Leblebici, Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*  
18-5

A wide-tuning range MOSFET-C low-pass filter is presented. The wide-tuning range in this filter has been achieved without using any switchable component. The filter cutoff frequency is tunable over 20Hz to 184kHz with a constant power consumption per cutoff frequency. Realized in 0.18µm CMOS technology, the filter occupies 0.09mm<sup>2</sup>.

## **Session 19 - Test Methods and ICs for High-Speed Serdes**

Wednesday Morning, September 16

Fir Ballroom

Chair: Mike Li, Altera

Co-Chair: Gordon Roberts, McGill University

9:00 AM **Introduction**

9:05 AM **Test Strategies for Adaptive Equalizers (INVITED)**, *Kwang-Ting (Tim) Cheng and Hsiu-Ming (Sherman) Chang, University of California, Santa Barbara, CA*  
19-1

This paper provides an overview of the test strategies for both continuous-time and digitally-assisted adaptive equalizers. Conventionally, an equalizer is characterized by the explicit measurement of the eye diagram at its output, which requires a lengthy testing time and is too costly for production testing. Design for testability and special test stimuli have been developed to facilitate circuit performance characterization and go/no-go production testing. In addition, for digitally-assisted adaptive equalizers, digital signatures extracted from the tap coefficients in the digital adaptation unit can be used for performance prediction and

fault detection.

9:55 AM **Loopback Architecture for Wafer-Level At-Speed Testing of Embedded HyperTransport™ Processor Links**, Alvin Loke, Bruce Doyle, Michael Oshima\*, Wade Williams\*\*, Robert Lewis\*\*, Charles Wang\*, Audie Hanpachern\*, Karen Tucker, Prashanth Gurunath\*, Gladney Asada\*, Chad Lackey, Tin Tin Wee and Emerson Fang\*, Advanced Micro Devices, Inc., Fort Collins, CO, \*Sunnyvale, CA, \*\*Austin, TX

We present transceiver serial loopback that enables cost-effective wafer-level at-speed testing of HyperTransport™ I/O for processor die-to-die communication. Besides facilitating known-good-die testing, this feature provides observability of multi-chip module die-to-die links that are completely embedded without external pin visibility. We demonstrate production screening of 45-nm SOI-CMOS wafers at 6.4 Gb/s.

10:20 AM **An On-Chip All-Digital Measurement Circuit to Characterize Phase-Locked Loop Response in 45-nm SOI**, Dennis Fischette, Richard DeSantis and John Lee, Advanced Micro Devices, Inc., Sunnyvale, CA

An all-digital measurement circuit, built in 45-nm SOI-CMOS, enables on-chip characterization of phase-locked loop (PLL) response to a self-induced phase step. This technique allows estimation of PLL closed-loop bandwidth and jitter peak-ing. The circuit can be used to plot step-response vs. time, measure static phase error, and observe phase-lock status.

**10:45 AM BREAK**

## **Session 20 - Circuit Simulation and Design Methodology**

Wednesday Morning, September 16  
Pine Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting

Co-Chair: Colin McAndrew, Freescale

9:00 AM **Introduction**

9:05 AM **Leveraging Designer's Intent: A Path Toward Simpler Analog CAD Tools (INVITED)**, Jaeha Kim, Metha Jeeradit, Byongchan Lim and Mark Horowitz, Stanford University, Stanford, CA

Leveraging the Boolean intent of digital circuits has enabled a wide set of CAD tools that helped increase the productivity of digital designers. Increasing analog designers' productivity requires a similar encapsulation of designer's intent for analog circuits. We argue that linear system models serve this role for almost all analog circuits, while the variables of these models may be in some transformed domains, rather than being the direct voltage/current waveforms of the circuits. We show how using these models enable new ways to design, optimize, and validate mixed-signal circuits. Even systems that reach steady states only in a stochastic sense can be analyzed as linear systems. Then a remaining issue is to ensure that the non-linear circuit reaches the intended "linear" operating point during start-up, which can be addressed by global convergence analysis.

9:55 AM **System Power Distribution Network Theory and Performance with Various Noise Current Stimuli Including Impacts on Chip Level Timing (INVITED)**, Larry Smith, Shishuang Sun, Peter Boyle and Bozidar Krsnik, Altera Corp.

Power Quality has become a determining factor in product performance and reliability. The reactive portions of the power distribution network (PDN) have a greater effect on power quality than DC IR drop. Resonance in the parallel inductance and capacitance network creates an impedance peak in the frequency domain and undesirable voltage noise in the time domain. The on-chip voltage noise is usually much higher than PCB PDN noise. A method of determining and simulating circuit parameters and comparing results to a target impedance is presented. A test vehicle has been built and measured to provide laboratory measured results for PDN voltage noise. Switching current patterns are defined which generate typical and pathological voltage waveforms. PRBS patterns are used as a characterization technique to provide reasonable worst case resonance stimulation. The voltage noise is responsible for measured timing and jitter degradation in logic circuits.

**10:45 AM BREAK**

**11:05 AM GPU-Accelerated Time-Domain Circuit Simulation, Rick Poore, Agilent Technologies**  
20-3

Time-domain circuit simulation is dominated by transistor model evaluation. A modern graphics processing unit (GPU) is a parallel, high performance computer suitable for non-graphics tasks. Simulation is sped up by 3-6x by moving transistor evaluation to a GPU. Implications for writing transistor models for good GPU performance are discussed.

**11:30 AM Adjoint Sensitivity Analysis of Nonlinear Distortion in RF Circuits, Dani Tannir and Roni Khazaka, McGill University, Quebec, Canada**  
20-4

Recently, an efficient moments based method for computing the third order intercept point of RF circuits was proposed. The moments based approach did not however provide sensitivity information. In this paper we propose a new method based on moments of the adjoint network. This new approach provides both the third order intercept point as well as its sensitivity in a very computationally efficient manner. As is generally the case in adjoint based methods, the sensitivity is provided with respect to all circuit parameters simultaneously.

**11:55 AM Discrete-Time, Cyclostationary Phase-Locked Loop Model for Jitter Analysis, Socrates Vamvakos, Vladimir Stojanovic\* and Borivoje Nikolic\*\*, Richardson, TX, \*Massachusetts Institute of Technology, Cambridge, MA, \*\*University of California, Berkeley, CA**  
20-5

The paper presents a discrete-time, linear, cyclostationary PLL model for jitter analysis, which accounts for the cyclostationarity of noise injected into the PLL loop and predicts the effects of aliasing on jitter. Expressions are derived for the output jitter spectrum, which agree with event-driven simulations of a 3rd-order PLL.

## **Session 21 - SoC Architectures for Signal Processing**

Wednesday Morning, September 16  
Fir Ballroom

Chair: Henry Chang, Designer's Guide Consulting  
Co-Chair: Steve Wilton, University of British Columbia

**10:15 AM Introduction**

**10:20 AM A Heterogeneous Digital Signal Processor Implementation for Dynamically Reconfigurable Computing, Davide Rossi, Fabio Campi, Antonello Deledda, Simone Spolzino and Stefano Pucillo, University of Bologna, Italy**  
21-1

This paper describes a SoC implementation of a heterogeneous multi-core digital signal processor, including an embedded field-programmable gate array (eFPGA), a mid-grain reconfigurable datapath (DREAM), and a coarse-grain reconfigurable array (PACT-XPP) integrated on independent clock islands. An ARM processor manages communication, configuration and synchronization. The device joins the flexibility of the heterogeneous configurable engines with the dynamic frequency scaling techniques, enabling performance/power tuning. The SoC was implemented in 90nm CMOS technology and is 110mm<sup>2</sup>.

**10:45 AM BREAK**

**11:05 AM A 64-PE Folded-Torus Intra-chip Communication Fabric for Guaranteed Throughput in Network-on-Chip Based Applications, Phi-Hung Pham, Phuong Mau and Chulwoo Kim, Korea University, Seoul, Korea**  
21-2

A 64-PE folded-torus intra-chip communication fabric is proposed to provide guaranteed throughput in terms of dead- and live-lock free and in order data delivery. The intra-chip network consuming 9.4% chip area and 18% of total chip power can provide max 44.6Gb/s bisection bandwidth with an Ebit of 0.14pJ/bit/hop.

**11:30 AM A 54GOPS 51.8mW Analog-Digital Mixed Mode Neural Perception Engine for Fast Object Detection,**

21-3 *Minsu Kim, Joo-Young Kim, Seunghin Lee, Jinwook and hoi-Jun Yoo, Korea Advanced Institute of Science and Technology, Daejeon, Korea*

A mixed mode Neural Perception Engine (NPE) is proposed as the pre-processing accelerator of multi-object recognition processor to reduce the computational complexity and increase its efficiency. It consists of Motion Estimator (ME), Visual Attention Engine (VAE) and Object Detection Engine (ODE). The fabricated chip achieves 54 GOPS 51.8mW NPE. By implementing a fast and robust neuro-fuzzy algorithm in analog-digital mixed circuits, the area and power of the ODE is reduced by 59% and 44%, respectively, compared to those of all digital implementation. The NPE can increase the frame rate by 2.09x and reduce power consumption by 38% of the multi-object recognition processor.

11:55 AM **A 1.4 MHz 0.21 mW MPEG-2/4 AAC Single Chip Decoder**, *Tsung-Han Tsai, Chun-Nan Liu, Hsueh-Yi Lin, Hsing-Chuang Liu and Chia-Ying Wu, National Central University, Taiwan*  
21-4

A low power and full ASIC MPEG-2/4 AAC single chip decoder is presented. Through algorithm, architecture, RTL and circuit level lower power techniques, the proposed AAC decoder is operated at 1.4 MHz for the 44.1 KHz sampling frequency and consumes only 0.21 mW using TSMC 0.13  $\mu$ m library.

## Session 22 - Millimeter-Wave IC's

Wednesday Afternoon, September 16  
Oak Ballroom

Chair: Ramesh Harjani, University of Minnesota  
Co-Chair: Alireza Shirvani, Marvell

1:30 PM **Introduction**

1:35 PM **Paths to Terahertz CMOS Integrated Circuits (INVITED)**, *Dongha Shim, Chuying Mao, Ruonan Han, Swaminathan Sankaran\*, Eunyoung Seok\*, Changhua Cao\*\*, Wojciech Knap^ and Kenneth O, University of Florida, Gainesville, FL, \*Texas Instruments Inc., Dallas, TX, \*\*ST-Ericsson, ^GES CNSR-U, Montpellier, France*  
22-1

A 140-GHz fundamental mode VCO in 90-nm CMOS and a 410-GHz push-push VCO in 45-nm CMOS, and a 125-GHz Schottky diode frequency doubler, a 50-GHz phase-locked loop with a frequency doubled output at 100 GHz, a 180-GHz Schottky diode detector and a 700-GHz plasma wave detector in 130-nm CMOS have been demonstrated. Based on these, paths to terahertz CMOS circuits are suggested.

2:25 PM **A 60 GHz CMOS Combined mm-wave VCO/Divider with 10-GHz Tuning Range**, *Burak Çatli and Mona Mostafa Hella, Rensselaer Polytechnic Institute, Troy, NY*  
22-2

This paper proposes the use of N-push operation for combining the functions of the VCO and dividers in the mm-wave frequency range. If employed in a PLL, the combined VCO/divider (C-VCO/D) would potentially provide wider tuning range than traditional mm-wave PLLs employing injection locked frequency dividers, thus exploiting the full range available in the 60GHz ISM band (57GHz-64GHz). The C-VCO/D is fabricated in 130nm IBM CMOS technology and achieves a tuning range from 55GHz-65GHz using a  $V_{DD}=1.5V$ ,  $I_{core}=20mA$ , and  $I_{buffer}=15mA$ . The C-VCO/D has a phase noise of 97.1 dBc/Hz at 1MHz Offset.

2:50 PM **A Sliding IF Receiver For mm-wave WLANs In 65nm CMOS**, *Stefano Bozzola, Davide Guermandi\*, Federico Vecchi, Matteo Repossi\*, Massimo Pozzoni\*, Andrea Mazzanti\*\* and Francesco Svelto, Università degli Studi di Pavia, Pavia, Italy, \*STMicroelectronics, Pavia, Italy, \*\*Università di Modena e Reggio Emilia, Modena, Italy*  
22-3

This paper presents an integrated receiver with on-chip LO for HDMI at mm-waves. Measured prototypes show a remarkable -115dBc/Hz phase noise at 10MHz from 64GHz while frequency tuning range is 12.5%. Other performances are: 28dB gain, 9dB NF, 5GHz RF bandwidth, -26dBm 1-dB C.P., >60dB IRR with 80mW consumption.

3:15 PM **BREAK**

3:30 PM **A 24-GHz CMOS Sub-harmonic Mixer based Zero-IF Receiver with an Improved Active Balun**, *Rahul*

22-4 *Kodkani and Lawrence Larson, University of California at San Diego, La Jolla, CA*

The design and implementation of a 24 GHz sub-harmonic mixer-based quadrature direct-conversion receiver is presented. The receiver includes an improved active balun and a LO octet phase generator with on-chip quadrature VCO. Fabricated in a 0.13  $\mu\text{m}$  CMOS process, the RF and IF sections consume 48 mA and the LO section consumes 40 mA, using a 1.6V supply. The measured conversion gain of the receiver was 12.5 dB and Noise Figure of 7.4 dB.

3:55 PM **A mm-Wave Power Harvesting RFID Tag in 90nm CMOS**, *Stefano Pellerano, Javier Alvarado Jr.\* and*  
22-5 *Yorgos Palaskas, Intel Corporation, Hillsboro, OR, \*Raytheon Company, El Segundo, CA*

A mm-wave power-harvesting RFID tag is implemented in 90nm CMOS. Operation at mm-wave reduces antenna size and could allow antenna integration on-chip. This, together with power harvesting that can be used in lieu of a battery, can result in a CMOS-only tag with no off-chip components whatsoever. The tag harvests energy from the incoming mm-wave CW signal by the reader and then uses a 60GHz free-running oscillator to transmit back pulse-width modulated bursts. With 2dBm mm-wave input power, the tag transmits 5kb/s. The tag size is 1.3x0.95mm<sup>2</sup> including pads.

## Session 23 - ESD Design Challenges

Wednesday Afternoon, September 16  
Fir Ballroom

Chair: Manoj Sachdev, University of Waterloo  
Co-Chair: Hong-Ha Vuong, LSI

1:30 PM **Introduction**

1:35 PM **ESD Design Challenges and Strategies in Deeply-scaled Integrated Circuits (INVITED)**, *Shuqing*  
23-1 *Cao, Tze Wee Chen, Stephen G. Beebe\* and Robert W. Dutton, Stanford University, Stanford, CA,*  
*\*GlobalFoundries Inc., Sunnyvale, CA*

Challenges of design-window shrinkage in deeply-scaled silicon technologies are addressed by improving design, characterization, and modeling of I/O and ESD devices, and by developing ESD-performance co-design methodologies. Advanced ESD metrology methods are reviewed and their applications in reliability modeling are investigated. Package and wafer level CDM correlation issues are examined.

2:25 PM **Circuit Solutions on ESD Protection Design for Mixed-Voltage I/O Buffers in Nanoscale CMOS**  
23-2 **(INVITED)**, *Ming-Dou Ker and Chang-Tzu Wang, National Chiao-Tung University, Hsinchu, Taiwan*

This invited paper presents the ESD circuit solutions to protect the mixed-voltage I/O buffers in nanoscale CMOS processes against ESD stresses. The ESD protection scheme and the specific ESD clamp circuits with low standby leakage current have been successfully verified in nanoscale CMOS processes. Effective on-chip ESD protection scheme should be early started in the beginning phase of chip design in order to achieve good enough ESD robustness for IC products.

3:15 PM **BREAK**

3:30 PM **ESD Protection Circuit for 8.5Gbps I/Os in 90nm CMOS Technology**, *Hossein Sarbishaei and Manoj*  
23-3 *Sachdev, University of Waterloo, Waterloo, Canada*

In this paper we designed an ESD protected CML driver for 8.5Gbps data rate. ESD protection for this circuit is provided with DSCR. A detailed analysis is done on the impact of ESD protection on performance of the driver. It is shown that DSCR offers up to 2.7kV HBM protection with very small impact on performance of the driver

## Session 24 - Memory Trends

Wednesday Afternoon, September 16  
Pine Ballroom

Chair: Vikas Chandra, ARM

Co-Chair: Tom Andre, EverSpin Technologies

1:30 PM **Introduction**

1:35 PM **A 40-nm Low-Power SRAM with Multi-Stage Replica-Bitline Technique for Reducing Timing Variation**, Shigenobu Komatsu, Masanao Yamaoka, Masao Morimoto\*, Noriaki Maeda\*, Yasuhisa Shimazaki\* and Kenichi Osada, Hitachi Ltd., Tokyo, Japan, \*Renesas Technology Corp., Tokyo, Japan  
24-1

A multi-stage replica bitline technique for reducing access time by suppressing enable timing variation of a sense amplifier was developed. Applied to a 288-kbit SRAM of the 40-nm process node, this technique achieves 6.1% access time reduction by reducing the sense-amplifier timing variation by 43%.

2:00 PM **Low-Overhead, Digital Offset Compensated, SRAM Sense Amplifiers**, Mudit Bhargava, Mark McCartney, Alexander Hoefler\* and Ken Mai, Carnegie Mellon University, \*Freescale Semiconductor  
24-2

Device variability in modern processes has become a major concern in SRAM design. In SRAMs that use low-swing bitlines, device variability can lead to high sense amplifier offsets, which limits the design scalability. A promising method for decreasing the offset is post-silicon tuning using low-overhead, digital offset compensation in the sense amplifiers. Measured results from a 4mm<sup>2</sup> testchip in 45nm bulk CMOS show that we can reduce sense amplifier offset sigma by over 5x.

2:25 PM **Asymmetric Sizing in a 45nm 5T SRAM to Improve Read Stability over 6T**, Satyanand Nalam and Benton Calhoun, University of Virginia, Charlottesville, VA  
24-3

This paper describes a 5-transistor (5T) SRAM bitcell that uses a novel asymmetric sizing approach to achieve increased read stability. Measurements of a 32 kb 5T SRAM in a 45nm bulk CMOS technology validate the design, showing read functionality below 0.5V. The 5T bitcell has lower write margin than the 6T, but measurements of the 45nm 5T array confirm that a write assist method restores comparable writability with a 6T down to 0.7 V.

2:50 PM **An Ultra Low Power Non-Volatile Memory in Standard CMOS Process For Passive RFID Tags**, Peng Feng, Yunlong Li and Nanjian Wu, Chinese Academy of Sciences, Beijing, China  
24-4

An ultra low power, 192bit, non-volatile memory is designed in a 0.18μm standard CMOS process for passive RFID tags. The memory includes a high efficiency charge pump and a register array, and can operate under a wide supply voltage and clock frequency range. The measured results indicate that, for the supply voltage of 1.2 volts, the current consumption is 1.8μA (3.6μA) at the read (write) rate of 1.3Mb/s (0.8Kb/s).

**3:15 PM BREAK**

3:30 PM **Small-Area High-Accuracy ODT/OCD by Calibration of Global On-Chip for 512M GDDR5 Application**, Jabeom Koo, Gil-su Kim, Junyoung Song, Kwan-Weon Kim\*, Young Jung Choi\* and Chulwoo Kim, Korea University, Seoul, Korea, \*Hynix Semiconductor, Icheon, Korea  
24-5

The proposed on-die termination (ODT) calibration method is implemented by using a 0.18um CMOS technology. The proposed ODT can detect the impedance variations of each ODT/OCD independently with the help of the proposed local PVT variation sensor and can decrease the impedance mismatch error lower than 1% by calibration of global on-chip variation with small area overhead. The measured eye diagram area at 2Gbps is widened by 26% when the ODT is on. The random data rate used for testing the eye diagram is 2Gbps. The global impedance mismatch error is within 1% under the supply voltage variation from 1.7V to 1.9V. The ODT and its calibration circuit occupy 0.003mm<sup>2</sup> and 0.015mm<sup>2</sup>, respectively. The power consumption of the calibration circuit is 10mW at 2Gbps.