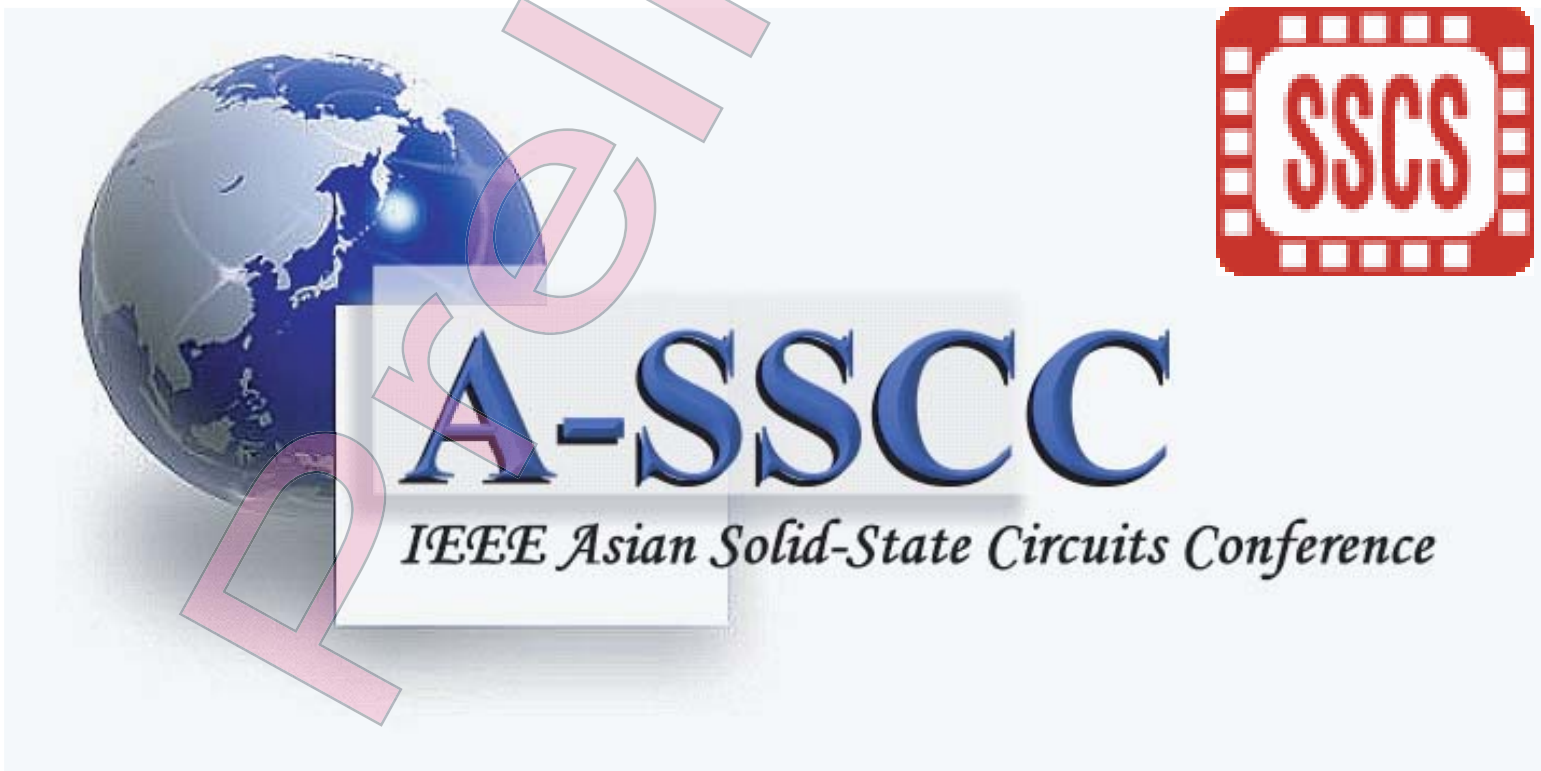
A-SSCC 2006

The 2nd
IEEE Asian Solid-State Circuits Conference

13 - 15 November 2006 - Hangzhou, China

Advance Program



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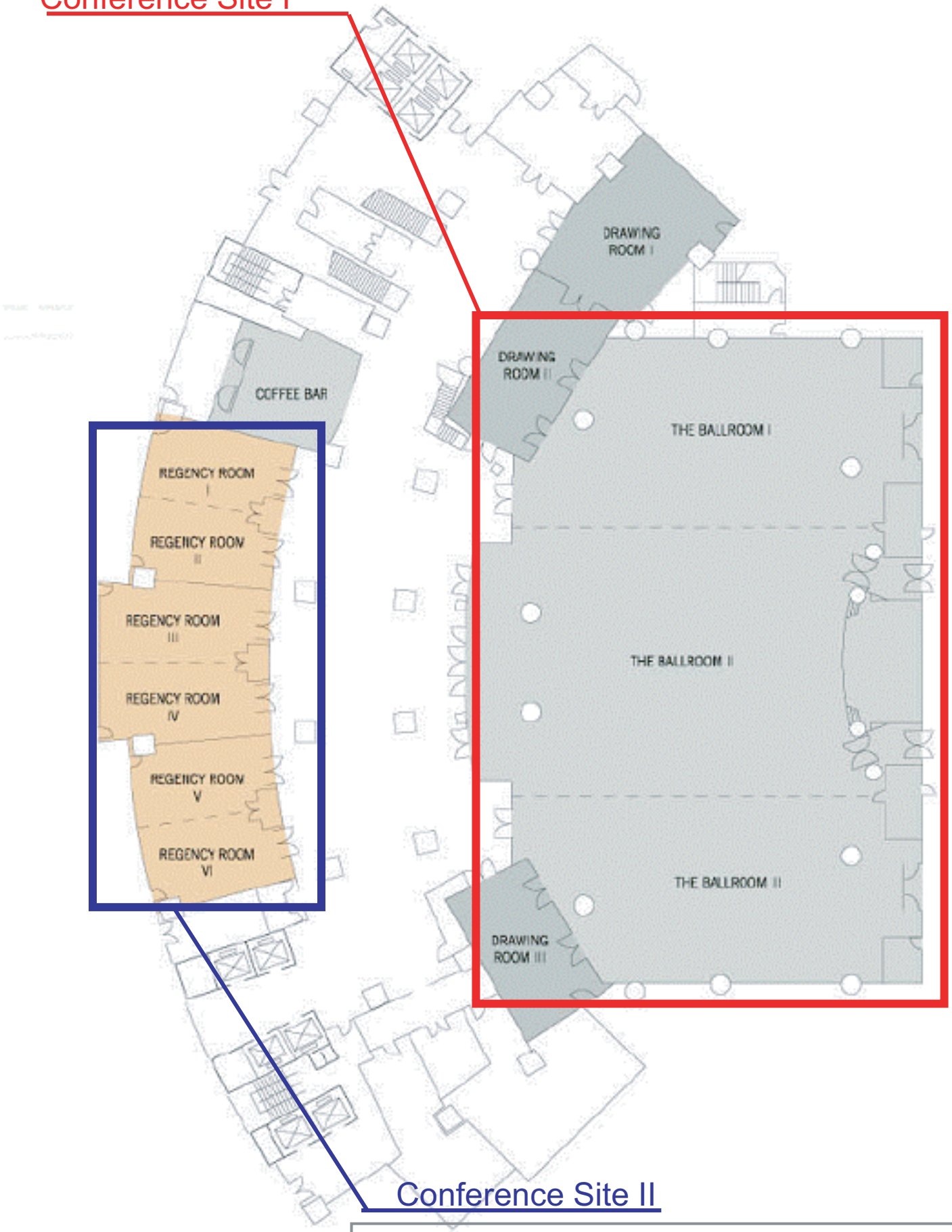
Level B2
BALLROOM I, II, III

Conference Site I



Conference Site II

Level B2
REGENCY ROOM I, II, III, IV, V, VI

A-SSCC 2006 Conference Program: November 13th, 2006

Nov. 13	9:00-10:15	**Tutorial I**	**Tutorial II**
		Advanced Embedded SRAM Design Hiroyuki Yamauchi(Fukuoka Inst. Of Tech.)	**Advanced PLL Design** Haward C. Luong(Hong Kong Univ. of Sci. and Tech.)
	10:15-10:45	Break	
	10:45-12:00	**Tutorial I**	**Tutorial II**
		Advanced Embedded SRAM Design Hiroyuki Yamauchi(Fukuoka Inst. Of Tech.)	**Advanced PLL Design** Haward C. Luong(Hong Kong Univ. of Sci. and Tech.)
	12:00-13:00	Lunch	
	13:00-14:15	**Tutorial III**	**Tutorial IV**
		Advanced Pipeline ADC Design Yun Chiu(University of Illinois)	**Advanced Sigma-delta ADC Design** Kathleen Philips(Philips Research Laboratories)
	14:15-14:45	Break	
	14:45-16:00	**Tutorial III**	**Tutorial IV**
		Advanced Pipeline ADC Design Yun Chiu(University of Illinois)	**Advanced Sigma-delta ADC Design** Kathleen Philips(Philips Research Laboratories)
	16:00-18:00	Student Design Contest Exhibition	
	18:00-20:00	Reception	

A-SSCC 2006 Conference Program: November 14th, 2006

Nov. 14	9:00-9:15	**Opening**			
	9:15-10:00	**Plenary Talk I**			
		Chinese IC Process Technology Development in the First 20 Years of the 21st Century Richard Ru-Gin Chang(SMIC)			
	10:00-10:45	**Plenary Talk II**			
		Component Technologies needed by the Ubiquitous IT Society Soo-Young Oh(ETRI)			
	10:45-11:00	Break			Student Design Contest Exhibition
	11:00-12:40	**Industry Session I: Digital** Session Co-chairs: Stefan Rusu(Intel), Chein-Wei Jen(STC/ITRI)		**Industry Session II: Analog/Memory** Session Co-chairs: Jun-ichi Okamura(Thine), Bill Zhang(ASTRI)	
	12:40-13:40	Lunch			
	13:40-15:45	**Session 1: Low Power ADC Technologies** Session Co-chairs: Kunihiko Iizuka(Sharp), Yun Chiu(U. Illinois)	**Session 2: Wireless Communications** Session Co-chairs: Jri Lee(Natl. Taiwan Univ.), Koichiro Mashiko(STARC)	**Session 3: Multimedia IC Designs** Session Co-chairs: David Chih-Wei Chang(STC/ITRI), Fumio Arakawa(Hitachi)	**Session 4: Emerging Applications in CMOS** Session Co-chairs: Ali Keshavarzi(Intel), Masahiro Nomura(NEC)
	15:45-16:05	Break/SDC Exhibition			
	16:05-17:35	**Panel Discussion I:**		**Panel Discussion II:**	Student Design Contest Exhibitio
		Future Digital Link Moderator: C.K. Ken Yang(UCLA)		**Software Defined Radio; How to realize soft and flexible RF and baseband circuits?** Moderator: Akira Matsuzawa(Tokyo Inst. Tech.)	
	17:35-17:45	Break			
	17:45-18:25	**Talk "How to write a GOOD ISSCC Paper"** Jan Van der Spiegel			
	19:00-21:00	Banquet			

A-SSCC 2006 Conference Program: November 15th, 2006

Nov. 15	9:00-9:45	**Plenary Talk III** **Deep Sub-100 nm Design Challenges** Tohru Furuyama(Toshiba)				
	9:45-10:30	**Plenary Talk IV** **From PC Multimedia Chipsets to Wireless and Digital Consumer SoC: Evolution and Challenges** Ming-Kai Tsai(MediaTek)				
	10:30-10:45	Break				Exhibition
	10:45-12:50	**Session 5: Analog Technologies I** Session Co-chairs: Yun Chiu(UICU), Hidetoshi Onodera(Kyoto Univ.)	**Session 6: Milimeter Wave** Session Co-chairs: Minoru Fujishima(Univ. of Tokyo), Hyun-Kyu-Yu(ETRI)	**Session 7: IP Design for Communication and Security** Session Co-chairs: Xiaoyang Zeng(Fudan Univ.), Kazutami Arimoto(Renesas)		
	12:50-13:50	Lunch				
	13:50-15:55	**Session 8: Analog Technologies II** Session Co-chairs: Makoto Nagata(Kobe Univ.), Junyan Ren(Fudan Univ.)	**Session 9: RF Amplifiers** Session Co-chairs: Hyungcheol Shin(Seoul Natl. Univ.), Howard Luong(Hong Kong Univ. of Sci & Tech)	**Session 10:** Digital Circuits Techniques on Timing and Noise Tolerance Session Co-chairs: Hideyuki Kabuo(Matsushita), Au-Yeu Wu(Natl. Taiwan Univ.)	**Session 11: Direction of Memory Technology** Session Co-chairs: Changhyun Kim(Samsung), Hideto Hidaka(Renesas)	
	15:55-16:10	Break				
	16:10-18:15	**Session 12: High Speed ADCs and DAC** Session Co-chairs: Masanori Otsuka(Renesas), Junyan Ren(Fudan Univ.)	**Session 13: RF Building Blocks** Session Co-chairs: Shiro Dosho(Matsushita), Mototsugy Hamada(Toshiba)	**Session 14: Wireline Communication** Session Co-chairs: Seong Hwan Cho(KAIST), Donhee Ham(Harvard Univ.)	**Session 15:** Emerging Technologies and Bio/Sensor Applications Session Co-chairs: Michael S-C Lu(Natl. Tsing Hua Univ.), Koji Kotani(Tohoku Univ.)	

Session P-I Plenary Talk I

Nov. 14 (2nd day) 9:15-10:00

P – 1 Nov. 14 (2nd day) 9:15-10:00

Chinese IC Process Technology Development in the First 20 Years of the 21st Century

Richard Ru-Gin Chang(SMIC)

Abstract:

Session P-II Plenary Talk II

Nov. 14 (2nd day) 10:00-10:45

P – 2 Nov. 14 (2nd day) 10:00-10:45

Componet Technologies Needed by the Ubiquitours IT Society

Soo-Young Oh, ETRI

Abstract: Korea has developed the world best IT infra structures and is leading the internet and mobile phone industry. Last two years, it has set up the IT development strategy, IT839 and leading the world IT industry by the simultaneous development of the IT services, IT infra structures, and IT systems. As a result, Korea has developed and commercialized Terrestrial DMB technology for the mobile TV services. It has also developed the Wibro technology which can provide the 2 ~ 10 Mbps mobile internet service at the speed of 60 ~ 120 Km/h and the cost of $20 ~ 30 per month. Both technologies have been selected as IEEE standard and ETSI standard respectively. This year, Korea is trying to commercialize the developed technologies and develop the components and softwares needed by these IT services and systems in order to lead the future ubiquitous IT society. This presentation covers the Korea IT development strategy, its results, and the components technologies needed by the future ubiquitous IT society.

Session P-III Plenary Talk III

Nov. 15 (3rd day) 9:00-9:45

P – 3 Nov. 15 (3rd day) 9:00-9:45

Deep Sub-100 nm Design Challenges

Toru Furuyama, Toshiba

Abstract: This paper will describe the problems in the design and development of deep sub-100 nm system LSI's and/or SoC's. One of the most difficult problems is the large power consumption, in both active and stand-by modes. Another problem is how to improve the development efficiency of large scale chips and related softwares. Lithography, that has been getting harder and harder, directly impacts the chip yield. Several approaches to these problems will be discussed; various low power technologies from circuit to architecture levels, highlevel language based design flow, IP reuse platform and DFM (Design for Manufacturing) related technologies.

Session P-IV Plenary Talk IV

Nov. 15 (3rd day) 9:45-10:30

P – 4 Nov. 15 (3rd day) 9:45-10:30

From PC Multimedia Chipsets to Wireless and Digital Consumer SoC: Evolution and Challenges

Ming-Kai Tsai, Media Tek Inc

Abstract: This presentation starts with evolution of the optical-storage chipsets for PC multimedia towards full-blown, next-generation SoC for wireless and digital consumer applications. Design challenges are reviewed and explored from submicron to nanometer eras in multiple levels of technology developments such as market-driven software/applications, advanced system architecture and engineering to address computation and connectivity requirements, performance-demanding but power-efficient circuit and functional blocks and the growing complexity being faced by increasingly large-scale chip integration. SoC companies will need to effectively cope with all incurred engineering issues to successfully achieve their competitive and leading positions.

Session I-I Industry Session: Digital

Nov. 14 (2nd day) 12:15-12:40

Session Co-Chairs: *Stefan Rusu(Intel), Chein-Wei Jen(STC/ITRI)*

I-I – 1 Nov. 14 (2nd day) 11:00-11:25

The UltraSPARC T1: A Power-Efficient High-Throughput 32-Thread SPARC Processor

Simon Tam, Stefan Rusu, Jonathan Chang, Sujal Vora, Brian Cherkauer and David Ayers(Intel Corporation)

Abstract: This paper describes a 95W dual-core 64-bit Xeon® MP processor implemented in a 65nm 8 metal layer process. Each processor core has a unified 1MB L2 cache and supports the Intel® Extended Memory 64 Technology and the Hyper-Threading Technology. The shared L3 cache has extensive RAS features including the Intel® Cache Safe Technology and Error Correction Codes (ECC). The processor is designed and optimized to operate at a 95W thermal design power envelope at the target product frequency. The front-side bus operates at 667MT/s or 800MT/s in a 3 load topology that is compatible with existing platforms.

I-I – 2 Nov. 14 (2nd day) 11:25-11:50

PAC DSP CORE AND ITS APPLICATIONS

David Chih-Wei Chang, I-Tao Liao, Shau-Yin Tseng and Chein-Wen Jen(STC/ITRI)

Abstract: The PAC DSP is a 32-bit programmable DSP solution which is ideal for next-generation media-rich and multi-function portable devices, such as Portable Media Player (PMP), Personal Digital Assistant (PDA), and smart phones. It provides high computation power from its parallel processing of multiple signal processing instructions and achieves efficient energy consumption form its unique architecture/micro-architecture design. Also, it maintains high application flexibility with general programmability.

I-I – 3 Nov. 14 (2nd day) 11:50-12:15

Standby Current Reduction of Compilable SRAM Using Sleep Transistor and Source Line Self Bias

Ding-Ming Kwai(Intellectual Property Library Company)

Abstract: This paper presents a compilable SRAM augmented with a sleep mode to achieve low standby power. Sleep transistor and source line self bias are added to the array, and their layouts fit the repetitive cell placement. The area overhead is minimized in such a way that the footprint remains the same. A 0.18um 512Kb test chip manufactured by two different foundries is used to demonstrate its effectiveness. The standby current measurements show substantial savings of 69% and 77%, respectively, at 1.8V. The savings can be greater if the supply voltage is lowered. This encourages sleeping at low voltage. Design choices to vary the virtual ground voltage to attain further reduction are investigated. The tradeoff is with the data retention voltage which is measured at least 0.1V higher. The fact that the cell stability is undermined in the sleep mode is the main concern to operate the SRAM at low voltage.

I-I – 4 Nov. 14 (2nd day) 12:15-12:40

A 65nm 95W Dual-Core Multi-Threaded Xeon® Processor with L3 Cache

Ana Sonia Leon and Denis Sheahan(Sun Microsystems, Inc.)

Abstract: Throughput Computing represents a new paradigm in processor design focusing on maximizing overall throughput of commercial workloads while addressing increasing demands for improved power and cooling in today's data centers. The first generation of "Niagara" SPARC processors implements a powerefficient Chip MultiThreading (CMT) architecture, which combines eight 4-threaded 64b cores, a high bandwidth interconnect crossbar, a shared 3MB L2 Cache and four doublewidth DDR2 DRAM interfaces. Implemented in 90nm CMOS technology, the 378mm2 die consumes only 63W at 1.2GHz. The UltraSPARC T1 based systems are oriented to a wide variety of applications, including WebServers, data and application servers, Java applications, search, streaming video and Telco applications.

Session I-II Industry Session: Analog/Memory

Nov. 14 (2nd day) 11:00-11:25

Session Co-Chairs: *Jun-ichi Okamura(Thin), Bill Zhang(ASTRI)*

I-II – 1 Nov. 14 (2nd day) 11:00-11:25

A 10-bit 200MS/s Pipeline A/D Converter for High-Speed Video Signal Digitizer

Tomohiro NEZUKA, Katsuhiko MISAWA and Jun-ichi OKAMURA(THine Electronics, Inc.)

Abstract: A 10-bit 200MS/s A/D converter(ADC) for high-speed video signal digitizer is presented. The ADC has a 14-bit pipeline ADC core for digital programmable gain control and reference voltage buffers optimized for high-speed A/D conversion. The ADC is fabricated in a 0.18-um multiple Vth CMOS process. The area of ADC core is 1.15mm x 0.69mm, and power consumption is 128mW@200MS/s. The measured INL and DNL are 1.05LSB and 0.55LSB respectively. The measured SNR and SFDR are 54.8dB and 63.2dB respectively.

I-II – 2 Nov. 14 (2nd day) 11:25-11:50

Future Prospective of Programmable Logic Non-Volatile Device

Charles Ching-Hsiang Hsu(eMemory Technology Inc.)

Abstract: eMemory has propose programmable non-volatile device Neobit which can be build on any process platform without adding complication.

I-II – 3 Nov. 14 (2nd day) 11:50-12:15

A 1.5-V 3.2Gb/s/pin Graphic DDR4 SDRAM with Dual-Clock System, 4 Phase Input Strobing and Low Jitter Fully Analog DLL

Joo-Hwan Cho, Ki-Won Lee, Byoung-Jin Choi, Geun-Il Lee, Kwang-Jin Na, Ho-Don Jung, Woo-Young Lee, Ki-Chon Park, Yong-Suk Joo, Jae-Hoon Cha, Se-Jun Kim, Young-Jung Choi, Patrik B. Moran, Jin-Hong Ahn, Joong-Sik Ki(Hynix Semiconductor Inc)

Abstract: A 1.5V, 512Mbit GDDR4 SDRAM using a 90-nm DRAM process has been developed. The data rate is 3.2Gbps/pin, which corresponds to 12.8GBps in x32 GDDR4 based I/O. A multi-divided architecture consisting of 4 independent 128Mb core arrays is designed to reduce power and output noise. Also, a dual-clock system, 4 phase data input strobe scheme and 4 phase fully analog DLL are used to increase internal timing margins.

I-II – 4 Nov. 14 (2nd day) 12:15-12:40

Scalability of Carbon Nanotube FET-based Circuits

Vincent Yeh, Chris Huang, Chia-Huang Fu, Chieh-Hung Chen, Tsorng-Lin Lee, Hsiang-Hui Chang, Tsung-Yao Lin and Yung-Chun Lei(MediaTek Inc.)

Abstract: Modern FM radio receiver on portable devices requires low power consumption, small size and good audio performance. This paper reports a highly integrated FM radio single-chip receiver optimized for low power consumption and minimum external components. The operating frequency is 76 MHz ~ 108 MHz which covers EURO/US/Japan FM bands. The chip integrates all essential RF front-end circuits including LNA and mixer with automatic gain control (AGC), and mixed-signal functional blocks such as channel filter, limiting amplifier, integrated FM demodulator, stereo decoder, and integrated frequency locked loop (FLL). The total current consumption is only 10 mA off 2.8 V while maintaining sensitivity as low as 1.1 μV. The audio signal-to-noise ratio (SNR) is 58 dB. Total harmonic distortion (THD) is less than 0.4 % and the stereo audio separation (SEP) is more than 30 dB. This chip is fabricated in 0.35 μm BiCMOS process and packaged in 28-pin 4x4 mm2 LGA.

Session 1 Low Power ADC Technologies

Nov. 14 (2nd day) 13:40-15:45

Session Co-Chairs: *Kunihiko Iizuka(Sharp), Yun Chiu(Univ. of Illinois)*

1 – 1 Nov. 14 (2nd day) 13:40-14:05

A 1.5MS/s,6-bit ADC with 0.5V supply

Simone Gambini and Jan Rabaey(University of California at Berkeley)

Abstract: A moderate resolution analog-to-digital converter targeting wireless sensor networks applications is presented. Employing a successive approximation architecture, the device achieves 6 bits of resolution at 1.5 MS/s output rate, while drawing 28 uA from a low 0.5 V supply, corresponding to a Figure of Merit (FOM) of .25pJ/conversion step. Low-density metal5-metal6 capacitors guarantee feedback DAC linearity while minimizing input capacitance, while the use of a passive sample and hold, combined with a class-AB comparator reduce analog power dissipation to 4 uW (30% of the total). The analog core is operational for supply values as low as .3V, even though sampling rate is reduced to

175kS/s.

1 – 2 Nov. 14 (2nd day) 14:05-14:30

A Dual Low Power 1/2 LSB INL 16b/1Msample/s SAR A/D Converter with on-chip Micorcontroller

Ka Y. Leung, Kafai Leung and Douglas R. Holberg(Silicon Laboratories Inc.)

Abstract: A 0.35um double-poly CMOS 16b SAR A/D converter uses self-calibration techniques to obtain 1/2 LSB INL. The differential and single-ended THD at 1Msample/s are 101dB and 96dB, respectively. Each ADC consumes 20mW at 3V and occupies 2.9mm2 active area, resulting in a 0.9pJ/b FOM. The chip includes 3 ADCs, 2 DACs, 8051-microcontroller, CAN controller, DMA controller, 64K flash memory and 4K RAM occupying 26mm2.

1 – 3 Nov. 14 (2nd day) 14:30-14:55

A Multibit Complex Bandpass Delta-Sigma AD Modulator with I, Q Dynamic Matching and DWA Algorithm

H. San, Y. Jingu, H. Wada, H. Hagiwara, A. Hayakawa(Gunma University), J. Kudoh, K. Yahagi, T. Matsuura, H. Nakane(Renesas Technology Corp.), H. Kobayashi(Gunma University), M. Hotta(Musashi Institute of Technology), T. Tsukada(Renesas Technology Corp.), K.Mashiko(Semiconductor Technology Academic Research Center), A.Wada(Sanyo Electric Co., Ltd.)

Abstract: A second-order multi-bit switched-capacitor complex bandpass Delta-Sigma modulator has been designed and fabricated for application to low-IF receivers in wireless communication systems such as Bluetooth and WLAN. We propose a new structure of a complex bandpass filter in forward path with I, Q dynamic matching which is equivalent to the conventional one but it can be completely divided into two separate parts. As a result, the Delta-Sigma modulator which constituted with our proposed complex filter can be completely divided into two separate parts too, and there are not any signal line crossing between the upper and lower paths by a complex filter and feedback from DACs. Therefore, the layout design of the modulator can be greatly simplified. Nine-level two quantizers and four DACs are used in the modulator for lower power implementation and higher SNDR, but the nonlinearities of DACs are not noise-shaped and the SNDR of the Delta-Sigma ADC degrades. We have employed a new complex bandpass Data-Weighted Averaging (DWA) algorithm to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy; it can be ralized just by adding simple digital circuitry. Implemented in a 0.18-um CMOS process and at 2.8V supply, the modulator achieves a measured peak signalto-noise-and-distortion (SNDR) of 64.5dB at 20MS/s with a signal bandwidth of 78kHz while dissipating 28.4mW and occupies a chip area of 1.82mm2.

1 – 4 Nov. 14 (2nd day) 14:55-15:20

A 2.5-V 14-bit 180-mW Cascaded Sigma-Delta ADC for ADSL2+ Applications

Teng-Hung Chang, Lan-Rong Dung(National Chaio Tung University), Jwin-Yen Guo and Kai-Jiun Yang(Trendchip Technologies Corporation)

Abstract: This paper presents a sigma-delta (SD) analog-todigital converter (ADC) for the extended bandwidth asymmetric digital subscriber line application(ADSL2+). The core of the ADC is a cascaded 2-1-1 SD modulator that employs a resonatorbased topology in the first stage, three tri-level quantizers, and two different pairs of reference voltages. As shown in the experimental result, for a 2.2 MHz signal

bandwidth, the ADC achieves a dynamic range of 86 dB and a peak signal-to-noise and distortion ratio (SNDR) of 78 dB with an oversampling ratio of 16. It is implemented in a 0.25-um CMOS technology, in a 2.4-mm2 active area including decimation filter and reference voltage buffers, and dissipates 180 mW from a 2.5-V power supply.

1 – 5 Nov. 14 (2nd day) 15:20-15:45

An Inverter Based 20-MHz 42-uW sigma delta ADC with 20-KHz Bandwidth and 66dB Dynamic Range

Chauchin Su, Po-Chen Lin and HungWen Lu(National Chiao Tung University)

Abstract: This paper presented an inverter based 3rd order sigma-delta ADC. Cascode structure and auto-zeroing mechanism are proposed for the gain enhancement and offset cancellation. The ADC has been implemented in TSMC 2P6M 0.18um CMOS technology with a core area of 0.54mm2. The measurement results show that for the 1-V supply, 20-KHz bandwidth, and 2-MHz sampling rate, the power consumption is 42uW and the dynamic range of 66.02dB.

Session 2 Wireless Communication

Nov. 14 (2nd day) 13:40-15:45

Session Co-Chairs: *Jri Lee(Natl. Taiwan Univ.), Koichiro Mashiko(STARC)*

2 – 1 Nov. 14 (2nd day) 13:40-14:05

A Flexible Signal Processing Platform Chip for Software Defined Radio with 103 GOPS Dynamic Reconfigurable Logic Cores

Hisanori Fujisawa, Miyoshi Saito, Seiichi Nishijima, Naoki Odate, Yuki Sakai, Katsuhiro Yoda(Fujitsu Laboratories Ltd.), Nobuo Ujiie(Fujitsu LSI Technology), Iwao Sugiyama, Teruo Ishihara, Yoshio Hirose, Hideki Yoshizawa(Fujitsu Laboratories Ltd.)

Abstract: Software defined radio (SDR) is expected as a progressive technology for wireless communication methods under multi communication systems. In addition to high performance and low power consumption, short latency is required for hardware of SDR. We developed single-chip baseband processing LSI for software defined radio based on hybrid architecture of coarse-grain reconfigurable logic cores and flexible accelerator modules to realize the required features. The performance is 103GOPS at maximum. We implemented IEEE 802.11a and IEEE 802.11b, and evaluated its performance. As experimental results, we show effectiveness of the SDR LSI in performance and latency.

2 – 2 Nov. 14 (2nd day) 14:05-14:30

A Digitally Controlled Variable-gain Low-noise Amplifier with Strong Immunity to Interferers

Masato Koutani, Hiroshi Kawamura, Shinji Toyoyama and Kunihiko Iizuka(Sharp Corporation)

Abstract: A variable-gain low-noise amplifier with capacitive step attenuators is presented. The gain is digitally controlled by current-splitting technique of cascade transistors for linearity requirements. The fabricated LNA showed IIP3 increase of -1.1 to 3.5 dBm at gain of 25.8 to 21.2 dB, respectively, wide gain range of over 42.7 dB by capacitive attenuators, NF of 1.5 dB at 650MHz, and power consumption of 15.4 mW with 2.9V supply voltage using a 0.5-um BiCMOS process.

2 – 3 Nov. 14 (2nd day) 14:30-14:55

An I/Q based CMOS Pulsed Ultra Wideband Receiver Front End for the 3.1 to 10.6 GHz Band

Wim Vereecken and Michiel S.J. Steyaert(Katholieke Universiteit Leuven)

Abstract: A pulsed Ultra Wideband receiver front end for the 3.1 to 10.6 GHz band is implemented in a 0.18um CMOS technology. The monolithic UWB receiver incorporates a mixed-signal multiphase clock generator together with an analog demodulation and amplifier chain on a die of 1.4x1.4mm2. A dual in-phase/quadrature (I/Q) receiver approach, enabling phase modulation of the UWB impulses is experimentally demonstrated. The receiver consumes 120mW from a single 1.8V power supply and is capable to detect 107M pulses per second.

2 – 4 Nov. 14 (2nd day) 14:55-15:07

A 952MS/s Max-Log MAP Decoder Chip using Radix-4x4 ACS Architecture

Cheng-Hao Tang, Cheng-Chi Wong, Chih-Lung Chen, Chien-Ching Lin and Hsie-Chia Chang(National Chiao Tung University)

Abstract: This paper proposes a high throughput Max-Log MAP decoder for turbo decodoing algorithms. The retiming technique is utilized to reduce the critical delay by parallelly executing additions and comparisons. And the two-dimensional ACS architecture is proposed to provide area-efficient design for high radix structures. The test chip can support 952MS/s data rate after implemented in 0.13um technology.

2 – 5 Nov. 14 (2nd day) 15:07-15:19

A Low-Power Cellular/PCS/WCDMA Direct-Conversion Transmitter with Enhanced VCO Remodulation Rejection

Sungho Beck, Jeong-Cheol Lee, Seungyup Yoo, Kyoohyun Lim, Hyosun Jung, Jaekyung Han, Munkyung Ahn, Tschang-Hi Lee, Kyung-lok Kim(Future Communications IC Inc.), Myung-Woon Hwang(Future Communications IC Inc. and Korea Advanced Institute of Science and Technology) and Sangwoo Han(Future Communications IC Inc.)

Abstract: This paper presents a fully integrated low-power direct-conversion transmitter for cellular/PCS/WCDMA applications. Low-power consumption is achieved with the architecture of a simplified local-oscillator network, though the harmonics of large output signal could cause interference to the VCO. This inherent problem is effectively alleviated with a wide bandwidth fractional-N frequency synthesizer and an enhanced harmonic rejection technique. The transmitter, which consists of signal-processing blocks and a S-D fractional-N frequency synthesizer with an integrated VCO, is fabricated using a 0.35mm SiGe BiCMOS process. The total current consumption at minimum power is only 23mA for the cellular and 27mA for the PCS/WCDMA; the error vector magnitude is 3.91%, 6.98% and 8.56%, respectively.

2 – 6 Nov. 14 (2nd day) 15:19-15:31

A Single-Chip CMOS Transceiver for IEEE 802.11b Wireless LAN

Ying Wang, Kangmin Hu, Guojing Ye, Xiaofeng Yi, Jirou He, Xiaoping Gao, Jingguang Wang, Juan Li, Ye Zhou, Jiayi Liang, Yumei Huang and Zhiliang Hong(Fudan University)

Abstract: A 2.4G single-chip radio-frequency (RF) transceiver front-end for IEEE 802.11b is integrated in 0.18 um CMOS technology. The direct conversion architecture is adopted for both transmitter & receiver to minimize the on-chip and off-chip components required, which ensures low cost and low power consumption.

2 – 7 Nov. 14 (2nd day) 15:31-15:43

A 70-490 MHz 50% Duty-Cycle Correction Circuit in 0.35-um CMOS

Tsung-Hsien Lin and Chao-Ching Chi(National Taiwan University)

Abstract: A 50% duty-cycle correction (DCC) circuit is reported in this paper. The proposed DCC circuit consists of a clock generator and a delay detector. The clock generator is edge-triggered by the input and produces an output signal whose pulse width is controlled by the delay detector to half of the input signal period. Meanwhile, the input phase information is preserved owing to the edge-trigger nature. The circuit is implemented in a 0.35-um CMOS process. To evaluate the output duty-cycle accuracy, a single-sideband mixing test method is adopted. This circuit operates from 70 MHz to 490 MHz, and accommodates duty cycles ranging from 10% to 90%. The output signal is corrected to 50% +/- 2%. Operated from a 3.3-V supply, the circuit dissipates 8 mA at 490 MHz.

Session 3 Multimedia IC Designs

Nov. 14 (2nd day) 13:40-15:45

Session Co-Chairs: *David Chih-Wei Chang(STC/ITRI), Fumio Arakawa(Hitachi)*

3 – 1 Nov. 14 (2nd day) 13:40-14:05

A 210MHz, 15.3mW Unified Vector and Transcendental Function Unit for Handheld 3-D Graphics Systems

Byeong-Gyu Nam, Hyejung Kim and Hoi-Jun Yoo(Korea Advanced Institute of Science and Technology)

Abstract: A low-power, area-efficient 4-way 32-bit unified vector and transcendental function unit has been developed for programmable shaders for handheld 3-D graphics systems. It adopts the logarithmic number system (LNS) at the arithmetic core for the small-size, low-power unification and single cycle throughput with maximum 4-cycle latency of various vector and transcendental functions. A novel logarithmic conversion scheme is proposed with 0.8% of maximum conversion error. A test chip is implemented by 0.18-um CMOS technology with 93K gates. It operates at 210MHz and consumes 15.3mW at 1.8V.

3 – 2 Nov. 14 (2nd day) 14:05-14:30

An 800-uW H.264 Baseline-Profile Motion Estimation Processor Core

Takahiro Iinuma, Junichi Miyakoshi, Yuichiro Murachi, Tetsuro Matsuno, Masaki Hamamoto, Tomokazu Ishihara, Hiroshi Kawaguchi, Masahiko Yoshimoto(Kobe University) and Masayuki Miyama(Kanazawa University)

Abstract: This paper describes an 800-uW H.264 baseline-profile motion estimation processor for portable video applications. It features a VLSI-oriented block partitioning strategy, a reconfigurable SIMD/systolic-array datapath architecture and a power-efficient novel SRAM circuit with a segmentation-free and horizontal/vertical accessibility. The proposed architecture can reconfigure datapath to either an SIMD or systolic array depending on processing flow. The segmentation-free access means concurrent accessibility to arbitrary consecutive pixels. The processor supports all the seven kinds of block modes, and can handle three reference frames for a VGA (640 x 480) 30-fps to QCIF (176 x 144) 15-fps sequences with a quarter-pixel accuracy. It integrates 3.3 million transistors, and occupies 2.8 x 3.1 mm2 in a 130-nm CMOS technology. The proposed processor achieves a power of 800 uW for QCIF 15-fps with one reference picture.

3 – 3 Nov. 14 (2nd day) 14:30-14:42

A 0.3mW 1.4mm2 Motion Estimation Processor for Mobile Video Application

Seiichiro Hiratsuka(Fukuoka Industrial, Science & Technology Foundation), Satoshi Goto and Takeshi Ikenaga(Waseda Univ.)

Abstract: Motion estimation is a key processing in video encoding systems. Since it requires huge computational complexity, many algorithms and LSI architectures have been proposed to reduce it. Conventional LSIs, however, are not sufficient for mobile applications which require both flexibility and low power dissipation. This paper describes an application specific instruction processor LSI for ME processing. It has a dedicated unit for SAD operations. By applying our proposed ultra-low ME algorithm named ULCMEA, it can reduce power while keeping high flexibility. A chip capable of operating at 80 MHz was fabricated using TSMC 0.18-um CMOS technology. 15K logic gates and 32Kbit SRAM have been integrated into 1.4 mm2 chip. Typical power dissipation is 0.3-mW for QCIF 15 f/s ME processing.

3 – 4 Nov. 14 (2nd day) 14:42-14:54

Efficient Motion Estimation Accelerator for H.264/AVC

Choong Jin Hyun , Sung Dae Kim and Myung H. Sunwoo(Ajou University)

Abstract: This paper presents efficient memory reuse and sub-pixel interpolation algorithms for ME (motion estimation)/MC (motion compensation) of H.264/AVC. ME is a computationally intensive task and its number of memory accesses is quite high. Moreover, sub-pixel interpolation requires many additions and multiplications. The proposed memory reuse algorithm utilizes the position similarity of the MVp (motion vector prediction) among neighboring Sub-MBs (macro blocks). It can reduce a large number of memory accesses and can save power consumption by sharing SR (search range) of the current block. In addition, simplifying weights of sub-pixel interpolation can eliminate multiplications. Therefore, the proposed memory reuse and sub-pixel interpolation algorithms can be employed for low power video compression. In addition, the proposed ME accelerator uses the proposed algorithms. Performance comparisons show a significant improvement compared with existing ME accelerators.

3 – 5 Nov. 14 (2nd day) 14:54-15:06

A Versatile Multimedia Functional Unit Design Using the Spurious Power Suppression Technique

Kuan-Hung Chen, Yu-Min Chen, Yuan-Sun Chu(National Chung Cheng University) and Jiun-In Guo(National Chung Cheng University)

Abstract: This paper presents a Versatile Multimedia Functional Unit (VMFU) which can compute six arithmetic operations, i.e. addition, subtraction, multiplication, MAC, interpolation, and SAD with different configurations. The VMFU is constructed on the basis of a row-based modified Booth encoding multiplier which consumes the lowest power among others according to our transistor-level simulations. Besides, we apply the Spurious Power Suppression Technique (SPST) to the proposed VMFU to decrease the wasted dynamic power dissipation. From the transistor-level simulations, the proposed VMFU dissipates 0.0142 mW/MHz under a 0.18um/1.8V CMOS technology. Adopting the SPST can reduce 24% power consumption with only 15% area overhead.

3 – 6 Nov. 14 (2nd day) 15:06-15:18

A SIMD Video Signal Processor with Efficient Data Organization

Liu Kunjie, Qin Xing, Yan Xiaolang and Quan Li(Zhejiang University)

Abstract: A single instruction multiple data (SIMD) Video Signal Processor (VSP) is presented in this paper. To provide flexible and efficient data organization, a separate control/data-preparing pipeline and global switch register file with write- transposer and read-permuter is designed. Since data preparation is offloaded from computing core, this VSP promises sustained performance close to its peak computational rates of 64-bit SIMD ALU/MAC datapath. The benchmarking shows that the proposed VSP forms a highly efficient solution to emerging H.264/AVC video decoder.

3 – 7 Nov. 14 (2nd day) 15:18-15:30

A Hardware-Software Co-design for H.264/AVC Decoder

YANG Kun, ZHANG Chun, DU Guoze, XIE Jiangxiang and WANG Zhihua(Tsinghua University)

Abstract: A single chip decoder SOC for H.264 baseline profile, called OR264 (OR1K based H264 decoder), is presented in this paper. The chip has mixed hardware/software architecture to combine performance and flexibility. It is partitioned that the hardware is used to boost the performance and efficiency of key operations in H.264 decoder while the software is used to control the decoding flow and to synchronize the hardware modules. The hardware can decode a MB in 851 clock cycles under ideal condition. The chip is fabricated using UMC 0.18 6-layers metal CMOS process. It contains 1.5M transistors and 176k bits embedded SRAM. The die size is 4.8mmx4.8mm and the critical path is less than 10ns.

3 – 8 Nov. 14 (2nd day) 15:30-15:42

1000 frame/sec Stereo Matching VLSI Processor with Adaptive Window-Size Control

Masanori Hariyama, Naoto Yokoyama and Michitaka Kameyama(Tohoku University)

Abstract: This paper presents a 1000-frame/sec stereo-matching VLSI for adaptive window-size control. To reduce the computational amount, the algorithm uses images divided into non-overlapping regions.

The matching result is iteratively refined by reducing a window size. Window-parallel and pixel-parallel architecture is proposed to achieve to exploit the potential parallelism.

Session 4 Emerging Applications in CMOS

Nov. 14 (2nd day) 13:40-15:45

Session Co-Chairs: *Ali Keshavarzi(Intel), Masahiro Nomura(NEC)*

4 – 1 Nov. 14 (2nd day) 13:40-14:05

Stacked-chip Implementation of On-Chip Buck Converter for Power-Aware Distributed Power Supply Systems

Kohei Onizuka, Hiroshi Kawaguchi, Makoto Takamiya and Takayasu Sakurai(University of Tokyo)

Abstract: An on-chip buck converter which is implemented by stacking chips and which is suitable for on-chip distributed power supply systems is proposed and the operation is experimentally verified for the first time. The manufactured converter achieves the maximum power efficiency of 62% for an output current of 70mA with a switching frequency of 200MHz with a 2x2mm on-chip LC output filter. The active part and the passive LC output filter are implemented on separate chips fabricated in 0.35-um CMOS and connected with metal bumps. The optimization and improvement of the power efficiency and implementation structure are also discussed.

4 – 2 Nov. 14 (2nd day) 14:05-14:30

A 6.5-mW 5-Gbps On-Chip Differential Transmission Line Interconnect with a Low-Latency Asymmetric Tx in a 180nm CMOS Technology

Takahiro Ishii, Hiroyuki Ito, Makoto Kimura, Kenichi Okada and Kazuya Masu(Tokyo Institute of Technology)

Abstract: This paper proposes an on-chip differential-transmission-line (DTL) interconnect to reduce delay and power consumption in long global interconnects. The DTL interconnect can transmit signals at near light-of-speed with small power dissipation of Tx. The proposed DTL interconnect consists of Tx, DTL and Rx, and an asymmetric Tx is employed to reduce offset delay in Tx. In the measurement result, 5Gbps signal transmission can be achieved through 3mm-length interconnect, and delay and total power consumption are 140ps and 6.5mW, respectively.A 180nm standard CMOS process was utilized. Figure of merit (FoM) for on-chip interconnects is proposed to evaluate delay and power consumption. The proposed DTL interconnect is compared with the conventional RC, DTL and optical interconnects, and it achieves the highest FoM at more than 5mm length.

4 – 3 Nov. 14 (2nd day) 14:30-14:55

A 1/2.5 inch 5.2Mpixel, 96dB Dynamic Range CMOS Image Sensor with Fixed Pattern Noise Free, Double Exposure Time Read-Out Operation

Yoshitaka Egawa, Hidetoshi Koike, Ryuta Okamoto, Hirofumi Yamashita, Nagataka Tanaka(Toshiba Corp), Junichi Hosokawa(Toshiba Digital Media Engineering Corp), Kenichi Arakawa, Hiroaki Ishida, Hideaki Harakawa, Takayuki Sakai, and Hiroshige Goto(Toshiba Corp)

Abstract: A 1/2.5 inch, 5.2Mpeixel CMOS image sensor with wide dynamic range operation mode is developed and its effectiveness for high contrast scene pictures is verified. The adopted algorithm for this operation is inherently free from fixed pattern noise generation which often resists the realization of mass production level wide dynamic range image sensors. The attained dynamic range is 96 dB with 12bit output scheme.

4 – 4 Nov. 14 (2nd day) 14:55-15:07

A High-Speed Target Tracking CMOS Image Sensor

Qingyu Lin, Wei Miao and Nanjian Wu(Chinese Academy of Sciences)

Abstract: The paper proposes a high-speed target tracking CMOS image sensor. The target tracking CMOS image sensor consists of an image sensor array, row-parallel processors, a controller and a SRAM. It implements two novel concise algorithms that composed of efficient operations: such as collision detection, separation detection and position extraction. A 64*64 pixel array high-speed target tracking CMOS image sensor chip was implemented in using 0.35um 2P4M CMOS process. An N-well/P-sub SAB diode without salicide is used as photodiode in the image sensor. The chip size is 4.5mm*2.5mm. The measured results demonstrated that the chip can perform target tracking at the rate of 1000fps with more functionality and less area than the reported digital chips. The chip power consumption is 30mW at the main clock of 20MHz.

4 – 5 Nov. 14 (2nd day) 15:07-15:19

A Silicon Micromechanical Resonator Based CMOS Bandpass Sigma-Delta Modulator

Yong Ping Xu, Rui Yu(National University of Singapore), Wan-Thai Hsu, and Andrew R. Brown(Discera Inc.)

Abstract: This paper describes a bandpass sigma-delta modulator employing a silicon micromechanical resonator as the loop filter. The micromechanical resonator is chosen primarily for its high quality factor and low power consumption. A 2nd-order prototype bandpass sigma-delta modulator is realized in a 0.35-micron CMOS process and tested with a 19.6-MHz silicon micromechanical resonator. The measured results show a peak SNDR of 51dB and a dynamic range of 52.5dB in a 200-kHz signal bandwidth.

4 – 6 Nov. 14 (2nd day) 15:19-15:31

A Fully Digital Low Cost Time Domain Smart Temperature Sensor with Extremely Tiny Size

Poki Chen, Mon-Chau Shie, Zi-Fan Zheng, Chun-Yan Chu and Yun-Yuan Shih(National Taiwan University of Science and Technology)

Abstract: A fully digital time domain smart temperature sensor without any full-custom device is proposed for painless VLSI on-chip integrations. A cyclic delay line is used to generate the thermally sensitive pulse with a width proportional to the measured temperature. The input clock is used as the timing reference, and a counter instead of an ADC is utilized for output coding. Implemented with as few as 140 FPGA Logic Elements, the proposed smart sensor was measured to have an error of -0.7~0.9 degrees over a wide temperature range of -40~130 degrees. The effective resolution is better than 0.1 degree, and the power consumption is 8.42uW at a sample rate of 2 samples/s.

4 – 7 Nov. 14 (2nd day) 15:31-15:43

Dynamically Reconfigurable Gate Array Based on Fine-Grained Switch Elements and Its CAD Environment

Masanori Hariyama, Waidyasooriya Hasitha Muthumala and Michitaka Kameyama(Tohoku University)

Abstract: Dynamically programmable gate arrays (DPGAs) promise lower-cost implementations than conventional FPGAs since they efficiently reuse limited hardware resources in time. One important issue on DPGAs is the large amount of configuration memory, which leads to area-inefficient implementation and large static power dissipation. This paper presents novel architecture of a switch block to overcome the required capacity of configuration memory. Our main idea is to exploit redundancy between different contexts by using a fine-grained switch element. The proposed MC-FPGA is designed in a 0.18um CMOS technology. The area of the proposed MC-FPGA is reduced to 45% of a typical MC-FPGA under a constraint of 8 contexts.

Session 5 Analog Technologies I

Nov. 15 (3rd day) 10:45-12:50

Session Co-Chairs: *Yun Chiu(Univ. of Illinois), Hidetoshi Onodera(Kyoto Univ.)*

5 – 1 Nov. 15 (3rd day) 10:45-11:10

A Digitally Calibrated Current-Voltage Feedback Transconductor in 0.13-um CMOS Process

Ying-Zu Lin, Yen-Ting Liu and Soon-Jyh Chang(National Cheng-Kung University)

Abstract: A digitally calibrated transconductor for high-speed operation with its linearity enhanced by negative feedback is proposed. This voltage-to-current converter is mainly composed of two parts: an operational transconductance amplifier (OTA) and a pair of feedback resistors. The measured spurious free dynamic range (SFDR) of the transconductor is 72.6 dB when the input frequency is 100 MHz. To compensate common-mode deviation due to process variation, digital calibration circuits are added. Fabricated in TSMC 0.13-um CMOS process, the transconductor occupies 250 um x 200 um active area and consumes 5.06 mW from a 1.2-V supply.

5 – 2 Nov. 15 (3rd day) 11:10-11:35

A High Speed Pseudo-Differential OTA with Mobility Compensation Technique in 1-V Power Supply Voltage

Tien-Yu Lo and Chung-Chih Hung(National Chiao Tung University)

Abstract: This paper presents a high linearity Operational Transconductance amplifier (OTA) based on pseudo-differential structures. The linearity is improved by mobility compensation techniques as the device size is scaled down to achieve high speed operation. Transconductance tuning could be achieved by a MOS operating in the linear region. The measured third-order inter-modulation (IM3) distortion under 1-V power supply voltage remains below -52 dB up to 50 MHz for a 400 mVpp differential input. The static power consumption is 2.5 mW.

5 – 3 Nov. 15 (3rd day) 11:35-12:00

1.5-V Linear CMOS OTA with -60dB IM3 for High Frequency Applications

Tien-Yu Lo and Chung-Chih Hung(National Chiao Tung University)

Abstract: A novel configuration of linearized Operational Transconductance Amplifier (OTA) for low-voltage and high frequency applications is proposed. By using double differential pairs and the source degeneration structure under nano-scale CMOS technology, the nonlinearity caused by short channel effect from small feature size can be minimized. A robust common-mode control system is designed for input and output common-mode stability, and thus reduces distortion caused by common-mode voltage variation. The linearity of the OTA is about -60dB third-order inter-modulation (IM3) distortion for up to 0.9Vpp at 40MHz.

5 – 4 Nov. 15 (3rd day) 12:00-12:25

A 1.2-V Fully-Differential OP-Amp with Buffered Reverse Nested Miller and Feedforward Compensations

Meng-Hung Shen, Li-Han Hung and Po-Chiun Huang(National Tsing Hua University)

Abstract: This paper describes a low voltage CMOS fully differential op-amp. It is constructed of three gain stages with a parallel of buffered reverse nested Miller compensation (B-RNMC) and feedforward transconductance compensation (FFTC). In BRNMC, a transconductance stage is inserted to eliminate right half-plane (RHP) zero which may degrade the phase margin. While a feedforward transconductance helps to enhance output large signal response in FFTC. Measurement results demonstrate that, using standard 0.35-um CMOS technology, larger than 90dB gain, 12MHz gain-bandwidth product, and 54 degree phase margin is achieved when driving 100pF loads. The setting time for a 1.2Vpp step is 2.4us. All the circuits dissipate 342uW under a single 1.2V power supply.

5 – 5 Nov. 15 (3rd day) 12:25-12:37

A Calibration Technique for Bandwidth of Programmable Gain Filter

Chih-Chang Lee and Tzu-Yi Yang(STC/ITRI)

Abstract: We propose a common-mode variable voltage (CMVV) method to improve the bandwidth of low pass filter for ultra-wideband (UWB) transmitter. It is based on leap-frog structure to design a 250MHz

8th -order GM-C Chebyshev low pass filter. In the analytic results, tuning the common-mode reference voltage (VCM) of common-mode feedback circuits of transconductor, the cutoff frequency of filter can be calibrated to overcome the process variation and temperature dependencies. This approach can effectively reduce the chip size and do not need excess circuits. The filter combines a resistor network and 4x13 decoder to program the gain of filter and is implemented in a CMOS 0.18um process and power dissipation is 18mW under 1.8V power supply. Measurement results show that the filter can be reformed 50% bandwidth and the gain can be programmed from -14dB to -38dB with 2dB step. The attenuation at 285MHz and 330MHz is 16dB and 32dB, respectively, and the total harmonic distortion (THD) of programmable gain filter is -37dBc for 1Vpp differential input signal at 150MHz.

5 – 6 Nov. 15 (3rd day) 12:37-12:49

A 1/f Noise reduction architecture for an Operational Amplifier in a 0.13um Standard Digital CMOS technology

Jeongwook Koh, Jung-Eun Lee, Chun-Deok Suh and Hoon-Tae Kim(Samsung Electronics Co. Ltd.)

Abstract: We present new circuit architecture ofr the 1/f noise reduction in a CMOS miller Operational Amplifier. Compared to a reference circuit, the 1/f noise reduction of 7 dB is achieved for a CMOS miller operational amplifier in 0.13 um 1.5V standard CMOS technology.

Session 6 Millimeter Wave

Nov. 15 (3rd day) 10:45-12:50

Session Co-Chairs: *Minoru Fujishima(Univ. of Tokyo), Hyun-Kyu-Yu(ETRI)*

6 – 1 Nov. 15 (3rd day) 10:45-11:10

43uW 6GHz CMOS Divide-by-3 Frequency Divider Based on Three-Phase Harmonic Injection Locking

Mizuki MOTOYOSHI and Minoru FUJISHIMA(University of Tokyo)

Abstract: A harmonic injection-locked divider (HILD) is effective for realizing a low-power phase-locked loop (PLL) circuit because the high-frequency output of a voltage-controlled oscillator (VCO) is down-converted into a low-frequency signal instantaneously. Conventional resonator-based HILDs, however, occupy a large chip area and exhibit a narrow locking range because either an LC or short-stub resonator is required. Ring-oscillator-based HILDs, on the other hand, operate at a relatively low frequency, again with a narrow locking range. In this study, a new HILD based on three-phase harmonic injection locking is proposed, which realizes a small chip area, a low power consumption, and a wide locking range. As a result of fabrication with 0.18um CMOS, a divide-by-three HILD is realized with a power consumption of 43uW, a maximum operating frequency of 6GHz, and a locking range of 80% at a supply voltage of 0.7V. The core size is 10.8um x 10.5um.

6 – 2 Nov. 15 (3rd day) 11:10-11:35

A 60GHz wide locking range CMOS Frequency Divider using Power-Matching Technique

Shon-Hang Wen, Juin-Wei Huang, Chao-Shiun Wang and Chorng-Kuang Wang(National Taiwan University)

Abstract: A 60GHz injection-locked frequency divider with power-matching technique is designed in 0.13-um CMOS technology for wide locking range. Compared with shunt-peaking version, the power-matching technique utilized in injection-locked frequency divider improves locking range by 15% based on simulation results. The measurement results show the divider free-running frequency is 30.4 GHz and the total locking range is 6 GHz (10%) at the input power of 3 dBm while consuming 8.8mW from a 1.2 V power supply.

6 – 3 Nov. 15 (3rd day) 11:35-12:00

77 and 94-GHz Downconversion Mixers in SiGe BiCMOS

Scott K. Reynolds(IBM) and Johnna D. Powell(Massachusetts Institute of Technology)

Abstract: Double-conversion superheterodyne downconverter blocks operating around 77 GHz and 94 GHz have been realized in 0.13-um SiGe BiCMOS technology. Both use a single-balanced RF mixer to downconvert the signal to an 8.8 GHz IF, which is amplified and downconverted a second time to baseband. The 77-GHz circuit achieves an upper SSB NF of 12.8 dB at 77 GHz and <12 dB at 72 GHz, with 20 dB of conversion gain and an input-referred 1-dB compression point of -14.7 dBm. The 94-GHz circuit achieves an upper SSB NF of 18.7 dB at 94 GHz, with 15 dB of conversion gain and an input-referred 1-dB compression point of -10.7 dBm. Both circuits use a bias current of 3.2 mA in the RF mixer core, with total testsite power consumption of 120 mA from a 3-V supply.

6 – 4 Nov. 15 (3rd day) 12:00-12:25

60-GHz CMOS Down-Conversion Mixer with Slow-Wave Matching Transmission Lines

Ivan C. H. Lai, Yuki Kambayashi and Minoru Fujishima(University of Tokyo)

Abstract: A cascode CMOS mixer is fabricated to exploit the unlicensed band around 60 GHz. This topology avoids the need for area-consuming power combining and uses simple matching with slow-wave transmission lines (SWTL). SWTL has a higher quality factor and allows area reduction. The circuit is fabricated in standard digital 90-nm CMOS and has a radio frequency (RF) return-loss more than 10 dB between 46 GHz and 64 GHz. At RF of 60 GHz, intermediate frequency (IF) of 4 GHz and local oscillator (LO) power of 1.5 dBm, the conversion loss is 1.2 dB and an input-referred 1-dB compression point of 0.5 dBm was measured. The length reduction of the transmission lines achieved is 47% and the resulting chip occupies an area of 0.61 mm by 0.80 mm with comparable performance to other works.

6 – 5 Nov. 15 (3rd day) 12:25-12:50

A 60GHz Class-E Power Amplifier in SiGe

Alberto Valdes-Garcia, Scott Reynolds and Ullrich R. Pfeiffer(IBM)

Abstract: A MILLIMETER-WAVE CLASS-E TUNED POWER AMPLIFIER IS REALIZED IN 0.13UM SIGE BICMOS TECHNOLOGY. TO ACCOMPLISH SWITCHING-MODE OPERATION AT 60GHZ, THE TRANSMISSION LINE INPUT IMPEDANCE TRANSFORMATION NETWORK PROVIDES A

LOW REAL SOURCE IMPEDANCE RATHER THAN OPTIMUM POWER MATCH. THE PROTOTYPE IC IS A SINGLE-ENDED SINGLE STAGE DESIGN THAT OPERATES FROM A 1.2V SUPPLY AND EMPLOYS AN AREA OF 0.98MM2. MEASUREMENT RESULTS SHOW A SATURATED OUTPUT POWER >11.1DBM WITH PEAK PAE>15% FROM 55-60GHZ. AT 58GHZ IT ACHIEVES A PEAK PAE OF 20.9%, PEAK POWER GAIN OF 4.2DB AND SATURATED OUTPUT POWER OF 11.7DBM.

Session 7 IP Design for Communication and Security

Nov. 15 (3rd day) 10:45-12:50

Session Co-Chairs: *Xiaoyang Zeng(Fudan Univ), Kazutami Arimoto(Reneas)*

7 – 1 Nov. 15 (3rd day) 10:45-11:10

A Block Scaling FFT/IFFT Processor for WiMAX Applications

Yuan Chen(National Chiao Tung University), Yu-Wei Lin(MediaTek Inc.) and Chen-Yi Lee(National Chiao Tung University)

Abstract: This paper presents a low-power design of a two-stream MIMO FFT/IFFT processor for WiMAX applications. A novel block scaling method and a new ping-pong cache-memory architecture are proposed to reduce the power consumption and hardware cost. With these schemes, half the memory accesses and 64-Kbit memory can be saved. Furthermore, by proper scheduling of the two data streams, the proposed design achieves better hardware utilization and can process two 2048-point FFTs/IFFTs consecutively within 2052 cycles. A test chip of the proposed FFT/IFFT processor has been designed using UMC 0.13 um 1P8M process with a core area of 1332x1590 um2. The SQNR performance of the 2048-point FFT/IFFT is over 48 dB for QPSK and 16/64-QAM modulations. Power dissipation of two 2048-point FFT computations is about 17.26 mW at 22.86 MHz which meets the maximum throughput rate of WiMAX applications.

7 – 2 Nov. 15 (3rd day) 11:10-11:35

The Low Power 16-bit RISC with Lossless Compression Accelerator for Body Sensor Network System

Hyejung Kim, Sungdae Choi and Hoi-Jun Yoo(KAIST)

Abstract: The low power 16-bit RISC is proposed for body sensor network system. The proposed IPEEP scheme provides zero overhead for the wakeup operation. The lossless compression accelerator is embedded in the RISC to support the low energy data compression. The accelerator consists of 16x16-bit storage array which has vertical and horizontal access path. By using the accelerator the energy consumption of the lossless compression operation is reduced by 93.8%. The RISC is implemented by 1-poly 6-metal 0.18um CMOS technology with 16k gates. It operates at 4MHz and consumes 24.2uW at 0.6V supply voltage.

7 – 3 Nov. 15 (3rd day) 11:35-12:00

Design of a Reconfigurable NoC Router with Network Interface for AMBA-based IPs

Shih-Hsun Hsu, Yu-Xuan Lin and Jer-Min Jou(National Cheng Kung University)

Abstract: Networks-on-a-chip (NoC) is a new architectural template, which helps to meet many of challenges of designing a complex system-on-a-chip (SoC). In the paper, we introduce the on-chip

network of and propose the router for NoC which provides both guaranteed and best-effort communication services. We adopt the reconfigurable recording table for circuit switching to support the guaranteed service, and in order to sufficiently utilize the bandwidth of the network we add the wormhole switching which contains several virtual channels. Additionally, our router integrates the standard interface with AMBA AHB for easier integration of the intellectual properties (IPs) of NoC. The benchmark router with 5 32-bit ports can operate at 100MHz and the bandwidth of router can be up to 16Gbps. The performance of the router is enough for providing an HDTV application on NoC.

7 – 4 Nov. 15 (3rd day) 12:00-12:12

A Scaleable DSP System for ASIP Design

Yanjun Zhang, Hu He, Zhixiong Zhou, Xu Yang and Yihe Sun(Tsinghua University)

Abstract: this paper describes a scaleable DSP architecture for ASIP design and a retargetable compiler based on ORC. By configuring this architecture, designers can easily get the ASIP for one set of applications. A DSP named THUASDSP2004 is developed manually based on this architecture and the compiler can give a satisfied result.

7 – 5 Nov. 15 (3rd day) 12:12-12:24

An Embedded Programmable Logic Matrix (ePLX) for flexible functions on SoC

Hirofumi Nakano, Takenobu Iwao(Renesas Technology Corp.), Tomoo Hishida, Hiroshi Shimomura, Tomonori Izumi, Takeshi Fujino(Ritsumeikan University), Yoshihiro Okuno and Kazutami Arimoto(Renesas Technology Corp.)

Abstract: In this paper, we propose embedded programmable logic matrix (ePLX) which is suitable for flexible System on Chip (SoC). The ePLX architecture is based on the dense two input Look-Up-Table(LUT) array and the hierarchical wiring resources, which are global/local wiring resources and with simple mapping tools. The compile flow of ePLX is also the simple one with the standard design environments, basically. We have verified the advantage of this architecture by programming the function module and mapping the circuits with high usage efficiency and doubling operation speed. The physical architecture of ePLX uses the divided power supply LUT and wiring resources that consists of SRAM with CMOS transfer gate switch elements. These techniques enable to handle the 0.6V level FV controllable programmable devices for the power management SoC. The ePLX can provide the unique additional merits for many applications under the platform design environments.

7 – 6 Nov. 15 (3rd day) 12:24-12:36

Very Low-cost VLSI Implementation of AES Algorithm

Jia Zhao, Xiaoyang Zeng, Jun Han and Jun Chen(Fudan University)

Abstract: This paper proposes a very low-cost VLSI implementation of AES algorithm. This design splits the 128bit computation in every round into four 32bit calculations and exploits 2-level pipeline to finish the process. Moreover, such improvements as module reuse and calculation order optimization, especially low-cost key expansion structure, are used to achieve high performance with very low hardware cost. Using the HHNEC 0.25um CMOS process, the scale of the design is about 12K equivalent gates and its system frequency is up to 100MHz. The throughputs of the 128bit dada encryption and decryption are as high as 256Mbit/s.

7 – 7 Nov. 15 (3rd day) 12:36-12:48

A low power side-channel attack resistant data-flow Rijndael encryption ASIC

Li Xiangyu and Sun Yihe(Tsinghua University)

Abstract: THDFAES04 is a data flow random execution Rijndael encryption ASIC, which can resist against side-channel attacks with low power. It is based on dynamic data-flow architecture and performs token matching and random service jointly by the token Hold-Match-Fetch components. In experiments, it could resist 15000 less samples correlation power analysis attack. The fabricated chip's average per-encryption energy of 128bits key AES standard is 0.053 micro joule. The die size is 2.21mm2. Its throughput distributes between 59 and 63 Mbps.

Session 8 Analog Technologies Ⅱ

Nov. 15 (3rd day) 13:50-15:55

Session Co-Chairs: *Makoto Nagata(Kobe Univ.), Junyan Ren(Fudan Univ.)*

8 – 1 Nov. 15 (3rd day) 13:50-14:15

A 19.7 MHz, 5th Order Active-RC Chebyshev LPF for IEEE802.11n with Automatic Quality Factor Tuning Scheme

Shouhei Kousai, Mototsugu Hamada, Rui Ito and Tetsuro Itakura(Toshiba Corp.)

Abstract: A fifth order LPF with a quality factor(Q) tuning circuit has been implemented for IEEE802.11n in a 0.13 um CMOS technology. The proposed Q tuning technique enables a 19.7 MHz, Active-RC Chebyshev LPF. The filter has 2 dB gain, 30 nV/Hz1/2 input referred noise, 113 dBuV input P1dB, draws 7.5 mA current from 1.5 V supply and occupies an area of 0.2 mm2

8 – 2 Nov. 15 (3rd day) 14:15-14:40

A 36/44 MHz Switched-capacitor Bandpass Filter for Cable-TV Tuner Application

Hui Zheng and Howard C. Luong(Hong Kong University of Science and Technology)

Abstract: A 36/44-MHz wide-band switched-capacitor (SC) band-pass filter is proposed for cable-TV tuner systems. The 14th-order SC biquadratic filter employs 2-path technique to achieve high attenuation and wide bandwidth at high frequency. Implemented in a 0.18-um CMOS process, the filter measures center frequencies of 36 MHz and 44 MHz with a bandwidth of 5.0 MHz and 6.2 MHz, respectively. Adjacent-channel attenuation of -58 dBc and pass-band ripple of less than 0.6 dB are achieved.

8 – 3 Nov. 15 (3rd day) 14:40-15:05

Optimization of Active Substrate Noise Canceling Technique using Power Line di/dt Detector

Taisuke Kazama(University of Tokyo), Toru Nakura(NEC), Makoto Ikeda and Kunihiro Asada(University of Tokyo)

Abstract: This paper demonstrates optimization of a feedforward active substrate noise canceling technique using a power supply di/dt detector. Our past study realized substrate noise canceling technique using di/dt detector, however the effect of di/dt canceller has not been discussed yet. For further substrate noise reduction, this study analyses the parameters which constitute di/dt canceller and develops more effective di/dt noise canceling scheme. As a result, we realized 62% substrate noise reduction by proposed multiple di/dt canceller. Compared with effect of guard ring, our multiple di/dt canceller suppressed about five times as much substrate noise as that of guard ring.

8 – 4 Nov. 15 (3rd day) 15:05-15:30

Delta-Sigma Based CMOS Stress Sensor with RF Output

Yonggang Chen, Richard C. Jaeger and Jeffrey C. Suhling(Auburn University)

Abstract: A CMOS stress sensor is merged with a delta-sigma modulator to produce a sensor with a low frequency RF output. A PMOS current mirror with two orthogonal transistors is used as the stress sensor. The delta-sigma modulator generates an output signal that can be processed digitally or monitored by a communications receiver. The frequency shift of the DSBSC output of the modulator is directly proportional to the stress induced mismatch in the sensor cell. A test chip demonstrating the sensor has been fabricated using the 1.5 MOSIS CMOS process

8 – 5 Nov. 15 (3rd day) 15:30-15:55

A Full-Digital Multi-Channel CMOS Capacitive Sensor

B.-J. Moon, D.-Y. Jung, J.-W. Chung, C.-Y. Joung, J.-S. Hong, S.-J. Lee, Y.-H. Shin(ATLab Inc.) and Changsik Yoo(Hanyang University)

Abstract: A full-digital 12-channel, 100-step capacitive sensor is described. The capacitance to be sensed forms an RC-delay line whose delay is compared with that of a reference RC-delay line. The difference of the RC delays is sensed by a simple full-digital time-to-digital converter (TDC). By compensating the parasitic capacitance at power up, the capacitive sensor implemented in a 0.35um standard digital CMOS technology shows 30fF sensing resolution. The capacitive sensor consumes 5uA per channel under 3.3V supply voltage.

Session 9 RF Amplifiers

Nov. 15 (3rd day) 13:50-15:55

Session Co-Chairs: *Hyungcheol Shin(Seoul Natl. Univ.), Howard Luong(Hong Kong Univ. of Sci & Tech)*

9 – 1 Nov. 15 (3rd day) 13:50-14:15

A Linear Mode CMOS Power Amplifier with Self-Linearizing Bias

Rimal Deep Singh and Kyung-Wan Yu(Skyworks Solutions, Inc.)

Abstract: A biasing scheme that improves the linearity of linear mode power amplifiers (PA) is presented. This technique employs adding feedback to a current mirror bias to enhance the linearity of the amplifier by compensating the nonlinear input capacitance of the core transistor. The technique is verified with simulations and implemented in a prototype 2.4 GHz PA for WLAN application. The PA is fabricated in a 0.35-um CMOS and achieves a small-signal gain of 25.4 dB, output P1dB of 25.1 dBm, and a poweradded efficiency (PAE) of 40%.

9 – 2 Nov. 15 (3rd day) 14:15-14:40

A 2.4-GHz CMOS Driver Amplifier Based on Multiple-Gated Transistor and Resistive Source Degeneration for Mobile WiMAX

Jongsik Kim(Kwangwoon University), Tae Wook Kim, Minsu Jeong, Boeun Kim(Integrant technologies Inc.) and Hyunchol Shin(Kwangwoon University)

Abstract: A CMOS driver amplifier employs two design techniques to improve its linearity in wide output power level. First, multiple-gated transistor (MGTR) technique with two auxiliary transistors extends the linear region further compared with MGTR with single auxiliary transistor. Second, resistive source degeneration significantly suppresses the unwanted 2nd-harmonic feedback effect caused by an inductive source degeneration. A 2.4-GHz differential driver amplifier has been implemented in 0.18um CMOS for Mobile WiMAX and Korean WiBro applications. It shows that the linear region with OIP3 of >= +20dBm is extended up to an output power of -5dBm, while achieving a maximum OIP3 of +28dBm, OP1dB of +7.8dBm, and a power gain of 9.2dB with dc power consumption of 1.8V and 18.7mA.

9 – 3 Nov. 15 (3rd day) 14:40-15:05

A Wide-band CMOS Low-Noise Amplifier for TV Tuner Applications

Youchun Liao, Zhangwen Tang and Hao Min(Fudan University)

Abstract: In this paper, a wide-band CMOS low-noise amplifier (LNA) is presented, in which the thermal noise of the input MOSFET is canceled exploiting a noise-canceling technique. The LNA is designed under input/output impedance matching. And its noise figure (NF) and linearity analysis are investigated particularly. The LNA chip is implemented in a 0.25-um 1P5M RF CMOS process. Measured results show that in 50-860 MHz, the voltage gain is about 13.4 dB, the NF is from 2.4 dB to 3.5 dB, and the input-referred third-order intercept point (IIP3) is 3.3 dBm. The chip consumes 30 mW at 2.5-V power supply and the core size is only 0.15mm*0.18mm.

9 – 4 Nov. 15 (3rd day) 15:05-15:30

A 0.5-6GHz Improved Linearity, Resistive Feedback 90nm CMOS LNA

Bevin G. Perumana(Georgia Institute of Technology and Intel), Jing-Hong C. Zhan, Stewart S. Taylor(Intel) and Joy Laskar(Georgia Institute of Technology)

Abstract: This paper presents a resistive feedback broadband LNA in 90nm CMOS which occupies 50um x 270um of active area. The LNA has 7GHz 3dB bandwidth and >24dB voltage gain. Across 0.5-6GHz, its input matching is better than -10dB, noise figure below 2.5dB, and iIP3 better than -11.5 dBm. Techniques to improve linearity in resistive feedback LNAs are discussed in detail. The LNA also provides an additional low power mode operation.

9 – 5 Nov. 15 (3rd day) 15:30-15:55

An Inductorless Low-Noise Amplifier with Noise Cancellation for UWB Receiver Front-End

Qiang Li and Y. P. Zhang(Nanyang Technological University)

Abstract: An inductorless low-noise amplifier (LNA) design for ultra-wideband (UWB) receiver front-end is presented. Without on-chip inductors, the ultra-wide bandwidth is achieved by a syncretic adoption of thermal noise canceling, capacitor peaking, and current reuse. Fabricated in a 0.13-um CMOS technology, the LNA exhibits a small signal gain of 11 dB and a -3 dB bandwidth of 2-9.6 GHz. The input return loss is less than -9.5 dB, and the noise figure is 3.6-4.8 dB. The LNA consumes 19 mW from a low supply voltage of 1.5 V. The LNA circuit with pad occupies only 0.17 mm-square die area, which is among the smallest reported designs.

Session 10 Digital Circuit Techniques on Timing and Noise Tolerance

Nov. 15 (3rd day) 13:50-15:55

Session Co-Chairs: *Hideyuki Kabuo(Matsushita), Au-Yeu Wu(NTU)*

10 – 1 Nov. 15 (3rd day) 13:50-14:15

A 2.5GHz, 30mW, 0.03mm2, All-Digital Delay-Locked Loop

Rong-Jyi Yang and Shen-Iuan Liu(National Taiwan University)

Abstract: A 2.5GHz, 30mW, 0.03mm2, all-digital DLL in 0.13um CMOS technology is presented. The lattice delay unit provides both a small delay step and a fixed intrinsic delay of two NAND gates. A modified binary search controller reduces the locking time and allows the DLL to track the PVT variations. This DLL locks in 24 cycles and has the closed-loop characteristic with pk-pk jitter of 14ps.

10 – 2 Nov. 15 (3rd day) 14:15-14:40

Improving Multi-Context Execution Speed on DRFPGAs

Md. Ashfaquzzaman Khan, Naoto Miyamoto, Roel Pantonial, Koji Kotani, Shigetoshi Sugawa, Tadahiro Ohmi(Tohoku University)

Abstract: In devices where interconnect delay is far dominating than logic delay, Dynamically Reconfigurable FPGA (DRFPGA) implementation has the prospect of executing circuits faster than traditional FPGA implementation, since temporal partitioning divides a long spatial wire into several

short temporal wires, thus converting interconnect delay into logic delay. To realize such prospect, reconfiguration delay and temporal communication delay of a DRFPGA must be kept as low as possible. This paper studies these issues and reports the architecture and performance of Flexible Processor III (FP3), a newly proposed DRFPGA. FP3 employs a new shift register type temporal interconnect and Nearest Neighbor (NN) type spatial interconnect to reduce the delay mentioned above. Correct behavior of FP3 chip has been confirmed and our experimental results show that there exist cases where the best user circuit speed is achieved when two or more contexts are in use.

10 – 3 Nov. 15 (3rd day) 14:40-15:05

An Alternative Cyclic Synchronous Mirror Delay for Versatility in Highly Integrated SoC

Hiroaki Nakaya, Yasuhiko Sasaki, Naoki Kato, Fumio Arakawa(Hitachi, Ltd.) and Toru Shimizu(Renesas Technology Corp.)

Abstract: We describe an alternative cyclic synchronous mirror delay (ACSMD) for highly integrated SoCs of mobile application processors. ACSMD provides the following advantages: wide operational frequency range from 0.5 to 400 MHz, 0.08 mm2 chip area, and 6.13 mW power consumption @ 400 MHz operation. The chip area and power consumption are reduced by 95% of those of a conventional hierarchical SMD with the same operational frequency and resolution. Key circuit technologies are cyclic delay line, alternating use of three delay lines, and a new loop counter.

10 – 4 Nov. 15 (3rd day) 15:05-15:17

Arbitrary Duty Cycle Synchronous Mirror Delay Circuits Design

Kuo-Hsing Cheng, Chen-Lung Wu and Shu-Yu Jiang(National Central University)

Abstract: An arbitrary duty cycle synchronous mirror delay (SMD) circuit is proposed in this paper. The conventional SMD can be locked in 2 clock cycles, but it just can accept only the narrow pulse clock signal, which will greatly restrict the application of the circuits. The modified TSPC DFF is used in the proposed SMD circuit to detect clock edge. Therefore, the proposed SMD circuit not only can be locked in 2 clock cycle time but also can accept arbitrary duty cycle clocks. Moreover, it can detect a small dead zone and makes the new circuit has better jitter performance and lower static phase error. An experiment chip was fabricated in 0.18um CMOS process. With a 1.8 V supply voltage, the measure results show that the proposed circuits can be operated from 450MHz to 750MHz. When the input clock frequency is 750MHz, the measured power dissipation was 9mW. In addition, the peak-to-peak and rms jitters were 24ps and 2.94ps, respectively.

10 – 5 Nov. 15 (3rd day) 15:17-15:29

ESD Protection Design by Using Only 1xVDD Low-Voltage Devices for Mixed-Voltage I/O Buffers with 3xVDD Input Tolerance

Ming-Dou Ker and Chang-Tzu Wang(National Chiao-Tung University)

Abstract: A new electrostatic discharge (ESD) protection design by using only 1xVDD low-voltage devices for mixed-voltage I/O buffer with 3xVDD input tolerance is proposed. A special ESD detection circuit has been proposed to improve ESD protection efficiency of ESD clamp device by substrate-triggered technique to achieve high ESD level. This design has been successfully verified in a 0.13-um CMOS process to provide an excellent circuit solution for on-chip ESD protection in the mixed-voltage I/O

buffers with 3xVDD input tolerance.

10 – 6 Nov. 15 (3rd day) 15:29-15:41

A 0.18um Probabilistic-Based Noise-Tolerate Circuit Design and Implementation with 28.7dB Noise-Immunity Improvement

I-Chyn Wey, You-Gang Chen(National Taiwan University), Changhong Yu, Jie Chen(Univ. of Alberta) and An-Yeu Wu(National Taiwan University)

Abstract: As the size of CMOS devices is scaled down to the nanoscale level, noise interferences start to significantly affect the VLSI circuit performance. Because the injected noise is random and dynamic in nature, a probabilistic-based approach is more suitable to handle signal errors than the conventional deterministic circuit designs. In this paper, we design and implement an 8-bit Markov Random Field carry lookahead adder (MRF-CLA) probabilistic-based noise-tolerant circuit in 0.18um CMOS process technology. This is the first working silicon design to prove the design concept of the noise-tolerant MRF circuits. The measurement results show that the proposed of the MRF adder can provide 28.7dB of noise-immunity as compared with its conventional CMOS design, when both circuits are facing the same server SNR environment. The MRF adder circuit can also achieve 10-6 BER when the supply voltage is only 0.45V and SNR is only 10dB. By using low-Vth device, the operating voltage can even lower to 0.24V with the same noise-tolerant ability.

10 – 7 Nov. 15 (3rd day) 15:41-15:53

A New Noise-Tolerant Dynamic Circuit Design with Enhanced PDP Performance under Low SNR Environment

You-Gang Chen, I-Chyn Wey and An-Yeu Wu(National Taiwan University)

Abstract: As the supply voltage is scaling down, both SNR and the circuit noise immunity are reduced. In this paper, we develop a new isolated noise-tolerant technique to prevent the dynamic circuit from the noise interference. As compared with the state of the art design, the noise immunity can be enhanced by 1.5X. For enhancing the noise-tolerance, we can save 81% power delay product (PDP) in severe low SNR environment. Moreover, the proposed circuit can achieve 81% and 39% energy saving as compared with the conventional domino circuit and twin-transistor design, respectively.

Session 11 Direction of Memory Technology

Nov. 15 (3rd day) 13:50-15:55

Session Co-Chairs: *Changhyun Kim(Samsung), Hideto Hidaka(Reneas)*

11 – 1 Nov. 15 (3rd day) 13:50-14:15

A 16Mb toggle MRAM with burst modes

Tadahiko SUGIBAYASHI, Noboru SAKIMURA, Takeshi HONDA, Kiyokazu NAGAHARA, Kiyotaka TSUJI, Hideaki NUMATA, Sadahiko MIURA, Ken-ichi SHIMURA, Yuko KATO, Shinsaku SAITO, Yoshiyuki FUKUMOTO, Hiroaki HONJO, Tetsuhiro SUZUKI, Katsumi SUEMITSU, Tomonori MUKAI, Kaoru MORI, Ryusuke NEBASHI, Shunsuke FUKAMI, Hiromitsu HADA, Nobuyuki ISHIWATA, Naoki KASAI and Shuichi TAHARA(NEC Corporation)

Abstract: A 16Mb toggle MRAM has been developed. It has some 100MHz burst modes that are compatible with a pseudo SRAM even although the toggle cell requires the reading and comparing sequence in write modes. To accelerate operating clock frequency, an interleaved and pipelined memory-array-group activation scheme and a noise insulation switch scheme are newly proposed. It was fabricated with a 0.13um CMOS and 0.24um MRAM process utilizing five metal layers.

11 – 2 Nov. 15 (3rd day) 14:15-14:27

A high-density and high-speed 1T-4MTJ MRAM with Voltage Offset Self Reference Read Scheme

Hiroaki Tanizaki(Renesas Design Corporation), Takaharu Tsuji, Jun Otani, Yuichiro Yamaguchi(Renesas Technology Corporation), Yasumitsu Murai(Renesas Design Corporation), Haruo Furuta, Shuichi Ueno, Tsukasa Oishi, Masanori Hayashikoshi, and Hideto Hidaka(Renesas Technology Corporation)

Abstract: A high-density 1-Transistor 4-Magnetic Tunnel Junction (1T-4MTJ) MRAM cell realizes a x0.56 cell size of conventional 1T-1MTJ cell. A self-reference sensing scheme with a partial write for a proper 1T-4MTJ cell operation and a simple voltage offset type sense amplifier for a small-signal sensing enable 56ns access time in a 1Mb memory device using a 130nm CMOS technology.

11 – 3 Nov. 15 (3rd day) 14:27-14:39

A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network

Sungdae Choi, Kyomin Sohn, Jooyoung Kim, Jerald Yoo and Hoi-Jun Yoo(Korea Advanced Institute of Science and Technology)

Abstract: A low-power periodic events generation is essential for a node controller in the network system with centralized control and the timer interrupt generation for various devices in a CPU. The proposed TCAM-based periodic event generator manages the issuing events with the programmed value and the number of the events is equal to the number of the word line of the TCAM block. The NAND-type TCAM cell operates with as low as 0.6V supply voltage and the low-energy match line precharge reduces the search line transition which causes most of the search energy dissipation. The implemented event generator consumes 184-nJ energy to schedule events of 255 nodes for 24-hours, which is less than 10% of energy consumption of conventional hardware timer blocks.

11 – 4 Nov. 15 (3rd day) 14:39-14:51

Best-Performance Less-Cost TCAM for IP Routing Address Lookup

Chao-Ching Wang and Jinn-Shyan Wang(National Chung Cheng University)

Abstract: A best-performance less-cost TCAM macro for IPv6 routing address lookup is designed and presented. The implemented 0.18um TCAM macro uses a newly proposed folded architecture on top of the tree-style AND-type match-line and the segmented search-line techniques we proposed previously to achieve a 27% increase in area utilization efficiency and a 10% reduction in energy consumption, while maintaining the world-record search speed.

11 – 5 Nov. 15 (3rd day) 14:51-15:03

A 0.6-V, 6.8-uW Embedded SRAM for Ultra-low Power SoC

Kyomin Sohn, Sungdae Choi, Jeong-Ho Woo, Jooyoung Kim and Hoi-Jun Yoo(KAIST)

Abstract: A novel embedded SRAM is proposed with features of high reliability and low power consumption. The critical control signals are made in correspondence to clock-duty cycle for high reliability. A hybrid precharge scheme is adopted for low power consumption. Additionally, an asymmetric read-write scheme is useful in a slow-but-steady write situation such as a control SoC for BSN (body sensor network). The fabricated 128-kb embedded SRAM consumes 117-uW at the worst case and 6.8-uW at normal write operation in a 0.6-V supply voltage.

11 – 6 Nov. 15 (3rd day) 15:03-15:15

Adaptive Self Refresh Scheme for Battery Operated High-Density Mobile DRAM Applications

Jin-Hong Ahn, Bong-Hwa Jeong, Saeng-Hwan Kim, Shin-Ho Chu, Sung-Kwon Cho, Han-Jin Lee, Min-Ho Kim, Sang-Il Park, Sung-Won Shin, Jun-Ho Lee, Bong-Seok Han, Jae-Keun Hong, Patrik B. Moran and Yong-Tak Kim(Hynix Semiconductor Inc.)

Abstract: Self refresh current in modern DRAMs is becoming more difficult problem to handle because the decreasing cell transistor size has a negative effect on the uniformity of capacitor charge. In order to solve this issue, adaptive self refresh(ASR) scheme has been developed. A dual period based refresh is performed in the ASR scheme to reduce power dissipation using row register information. The row register information is adaptively modified according to the cell data retention characteristics. When DRAM enters self refresh mode, only the rows which were activated for write are tested using internal refresh test circuits. The test results are used to choose the appropriate period for the dual period base self refresh operation. This paper demonstrates 512M mobile SDRAM utilizing this adaptive self refresh(ASR) capability to minimize standby power to 150uA @85C while maintaining chip area of the conventional scheme using the same process technology.

11 – 7 Nov. 15 (3rd day) 15:15-15:27

A Low Power Digital DLL with Wide Locking Range for 3Gbps 512Mb GDDR3 SDRAM

Won-Joo Yun, Hyun-Woo Lee, Young-Ju Kim, Won-Jun Choi, Sang-Hoon Shin, Hyang-Hwa Choi, Hyeng-Ouk Lee, Shin-Deok Kang, Hyong-Uk Moon, Seung-Wook Kwack, Dong-Uk Lee, Jung-Woo Lee, Young-Kyoung Choi, Nak-Kyu Park, Ki-Chang Kwean, Kwan-Weon Kim, Young-Jung Choi, Jin-Hong Ahn, Joong-Sik Kih, Ye-Seok Yang(Hynix Semiconductor Inc.)

Abstract: A new low power, low cost and high performance register-controlled digital delay locked loop with wide locking range is presented. The DLL has dual loops with single replica block, duty cycle correction enhance controller (DCCEC), smart power down controller (SPDC) for reducing the stand-by current during power down, and locking range doubler for wide locking range. The digital DLL used for 3Gbps 512Mb GDDR3 SDRAM is fabricated using an 80nm DRAM Process. Experimental results show less than +-1% duty correction from external duty error of +-5%, less than 400 cycle locking time, 1.5GHz operation frequency at 1.9V, and a wide locking range from 50MHz to 1.5GHz.

11 – 8 Nov. 15 (3rd day) 15:27-15:39

A voltage scalable advanced DFM RAM with accelerated screening for low power SoC platform

Hiroki Shimano, Fukashi Morishita, Katsumi Dosaka and Kazutami Arimoto(Renesas Technology Corp.)

Abstract: Advanced-DFM RAM which operate in 2Cell/bit, GND bitline pre-charge sensing and SSW(sense synchronized write) and has the 1cell/bit test mode for the accelerated screening against the marginal cells provides the best solution for the voltage scalable SoC memory platform

11 – 9 Nov. 15 (3rd day) 15:39-15:51

An Efficient Self Post Package Repair Algorithm and Implementation in Memory System with on-chip-ECC

Yun-Sang Lee, Jung-Bae Lee, Chang-Hyun Kim(Samsung Electronics), Sang-Uhn Cha and Hongil Yoon(Yonsei University)

Abstract: An efficient self post package repair algorithm using on-chip-ECC is proposed and the circuit implementation details are presented. The proposed algorithm identifies and stores the addresses of hard faults detected by on-chip-ECC during post package test phase and performs subsequent repairs with change supply voltage level controlled by tester. A yield improvement by 1~1.5% is expected and the efficiency of test and repair steps is enhanced by about 58~67%. The chip size overhead for its implementation is estimated to be under 0.4% for a 80nm 1Gb memory.

Session 12 High Speed ADCs and DAC

Nov. 15 (3rd day) 16:10-18:15

Session Co-Chairs: *Masanori Otsuka(Renesas), Junyan Ren(Fudan Univ.)*

12 – 1 Nov. 15 (3rd day) 16:10-16:35

A 6-bit 1.6 GS/s Flash ADC in 0.18-um CMOS with Reversed-Reference Dummy

Chien-Kai Hung, Jian-Feng Shiu, I-Ching Chen and Hsin-Shu Chen(National Taiwan University)

Abstract: A 1.6 GS/s 6-bit CMOS flash ADC using reversed-reference dummy method is demonstrated in a standard 0.18-um CMOS process. The proposed method improves linearity error at the boundary of offset averaging networks. The prototype circuit exhibits an INL of +0.32/-0.28 LSB and a DNL of +0.28/-0.28 LSB. The SNDR and SFDR achieve 32 and 44 dB at 1.6 GS/s for Nyquist input frequency. The ADC consumes 350 mW at 1.8 V supply and occupies an active chip area of 0.56 mm2

12 – 2 Nov. 15 (3rd day) 16:35-17:00

A 4-bit 1.356 Gsps ADC for DS-CDMA UWB System

Ja-Hyun Koo(Korea Univ), Bong-hyuck Park, Sang Seong Choi(ETRI), Shin-Il Lim(Seokyeong Univ), Suki Kim(Korea Univ)

Abstract: Abstract - In this paper, a 4-bit 1.356GS/s analog to digital (A/D) converter targeted for the direct spectrum code division multiple access ultra wide band (DS-CDMA UWB) is presented. The A/D converter uses a fully differential flash architecture. To achieve low power consumption and high conversion rate, the proposed converter is designed with current mode amplifier (CMA) and each preamplifier includes a dual sense amplifier (DSA). The A/D converter can sample input frequencies above 650MHz with this current mode processing technique. The A/D converter achieves 3.7 effective number of bits (ENOBs) for a 30MHz sinusoidal input and 3.35 ENOBs for a 650MHz input at a 1.356 GHz sampling rate. At 1.356GS/s, the current consumption is 38mA including digital logic with a power supply of 1.8V. The proposed A/D converter is fabricated using a 0.18-um 6Metal 1Poly CMOS process and the active area is 0.35mm2.

12 – 3 Nov. 15 (3rd day) 17:00-17:25

An Undersampling 10-bit 30.4-MSample/s Pipelined ADC

Wenjing Yin, Jie Jiang, Jun Xu, Fan Ye and Junyan Ren(Fudan University)

Abstract: A 3.3V 10bit 30.4-MS/s pipelined analog-to-digital converter (ADC) is presented. The application of undersampling input is considered and analyzed in particular. The flip-around S/H circuit is introduced to reduce the requirement of amplifier's performance and achieve low noise. The gate-voltage bootstrapped switch is used to allow a wideband input signal with excellent linearity. The gain-boost telescopic cascode amplifier is adopted to consume lower power. The ADC achieved a signal-to-noise-and-distortion ratio (SNDR) of 56.5dB (9.1ENOB) for an input of 30MHz at full speed of 30.4MHz, consuming only 52mW. The ADC is implemented in a 0.35um CMOS technology and occupies an area of 1.47mm2.

12 – 4 Nov. 15 (3rd day) 17:25-17:50

A 14-bit 200-MHz Current-Steering DAC with Switching-Sequence Post-Adjustment Calibration

Tao Chen and Georges Gielen(K.U.Leuven)

Abstract: In this paper a novice calibration method for the high-accuracy current-steering DACs is presented. Different from the traditional calibration methods which do the calibration by adjusting the current values of the current sources, our method does the calibration by dynamically rearranging the switching sequence of the current sources. Since this resequencing is performed after implementation, even the random errors can be cancelled, by this way the total area needed for the current sources can be greatly reduced. The chip has been implemented in a standard 1P6M 0.18-um CMOS technology. The core area of the chip is around 3 mm2, among which the area of the current-source block is only 0.28 mm2. The measured SFDR is 81.5 dB at 1 MHz signal frequency and 100 MHz sampling frequency.

12 – 5 Nov. 15 (3rd day) 17:50-18:02

A 6-Bit 2-GS/s Flash Aanlog-to-Digital Converter in 0.18-um CMOS Process

Ying-Zu Lin, Yen-Ting Liu and Soon-Jyh Chang(National Cheng-Kung University)

Abstract: A 6-bit flash ADC is fabricated in TSMC CMOS 0.18-um 1P6M process and supports a sampling rate up to 2 GS/s. The proposed ADC consists of a track-and-hold amplifier, a comparator array, a four-channel ROM-based 64-to-6 encoder, a multiplexer, and a clock generation and distribution system. Instead of traditional latch-based comparators used in high-speed ADCs, continuous-time comparators are employed to minimize kick-back noises and offsets. When the sampling frequency is 2 GHz, the measured SNDR is 30.01 dB at input frequency around 200 MHz. The ADC consumes 255 mW from a 1.8-V supply and occupies 3.61 mm square of die area. In addition to chip implementation, an analysis on resistive averaging network in frequency domain is presented. Characteristics of averaged differential pairs related to input frequency are revealed.

12 – 6 Nov. 15 (3rd day) 18:02-18:14

A 10-b 100-MS/s 95mW CMOS ADC IP With Emphasis on Layout Matching

Nan Wang, Ping Zhou and Da-Lai Huang(Shanghai Hua Hong NEC Electronics Co., Ltd.)

Abstract: This paper describes the design of a 10b 100Msamples/s pipelined ADC IP fabricated in a 0.25um CMOS process with MIM capacitor option. The IP core is implemented with 1.5b/stage structure, amplifier sharing technique, and swing-improved telescopic OTA design to achieve amplitude of 2.4Vpp at power supply range from 2.7V to 3.6V, dissipating only 95mW at 3.0V. For 10.7MHz input, it achieves 58.8dB SNR, 69.0dB SFDR and 66.5dB THD. With the proposed capacitor matching layout, the ADC achieves excellent differential nonliniearity of -0.174~+0.210 LSB.

Session 13 RF Building Blocks

Nov. 15 (3rd day) 16:10-18:15

Session Co-Chairs: *Shiro Dosho(Matsushita), Mototsugy Hamada(Toshiba)*

13 – 1 Nov. 15 (3rd day) 16:10-16:35

A 0.98 to 6.6GHz Tunable Wideband VCO in a 180nm CMOS Technology for Reconfigurable Radio Transceiver

Yusaku Ito, Hirotaka Sugawara, Kenichi Okada and Kazuya Masu(Tokyo Institute of Technology)

Abstract: This paper proposes a novel wideband voltage-controlled oscillator (VCO) for multi-band transceivers. The proposed VCO has a core VCO and a tuning-range extension circuit, which consists of switches, a mixer, dividers, and variable gain combiners with a spurious rejection technique. The experimental results exhibit 0.98-to-6.6GHz continuous frequency tuning with -206dBc/Hz of FoMt which is fabricated by using a 0.18um CMOS process. The frequency tuning range (FTR) is 149%, and the chip area is 800um x 540um.

13 – 2 Nov. 15 (3rd day) 16:35-17:00

A DC-7 GHz Small-Area Distributed Amplifier Using 5-port Inductors in a 180 nm Si CMOS Technology

Takeshi Ito, Daisuke Kawazoe, Kenichi Okada and Kazuya Masu(Tokyo Institute of Technology)

Abstract: This paper proposes a novel small-area distributed amplifier (DA), which utilizes two 5-port inductors to replace eight inductors. The DA is fabricated using a standard 180 nm CMOS process with 6 metal layers. The layout area of DA is 0.33 square millimeter. It is about 50 % as large as conventional DAs, and it has power gain of 6.3 dB and noise figure of 6 dB at DC-7 GHz.

13 – 3 Nov. 15 (3rd day) 17:00-17:25

A CMOS Dual Class-AB Technique for Highly Linear Even Harmonic Mixer

Ming-Feng Huang(STC/ITRI), Chung J. Kuo(Delta Electronics Inc.) and Shuenn-Yuh Lee(National Chung-Cheng University)

Abstract: A 5.25-GHz CMOS even harmonic mixer (EHM) using a dual Class-AB circuit is presented. The dual Class-AB circuit in the RF stage can improve the linearity and conversion gain for wireless receivers. In addition, the dual Class-AB circuit adjusting the mixing power from the frequency-doubling circuit can overcome the process variation. After an implemented chip, the measurement reveals that the proposed EHM has a power consumption of 4.13 mW, conversion gain of 13.133dB, IIP3 of -1.033dBm, and IIP2 of 48.267dBm under the LO frequency of 2.623GHz. With a measured linearity upon a high power conversion gain, the proposed EHM shows improved performance compared with other published active EHMs.

13 – 4 Nov. 15 (3rd day) 17:25-17:50

Advanced Fs/2 Discrete-Time GSM Receiver in 90-nm CMOS

Loïc Joet, Franck Montaudon, Alessandro Dezzani, Franck Badets, Florent Sibille, Christian Corre, Laurent Chabert, Rayan Mina, Frédéric Bailleuil, Daniel Saias, Frédéric Paillardet and Ernesto Perea(ST Microelectronics)

Abstract: A new discrete-time receiver architecture enables to specifically circumvent CMOS integration issues, taking advantage of ZIF architectures yet escaping impact of flicker noise and second-order front-end non-linearity. This architecture, compatible with further scaling, was implemented for a GSM receiver in 90-nm CMOS. This receiver occupies 1-mm2 core area, achieves -108-dBm sensitivity, and -16-dBm IIP3. It is based on a discrete-time approach centering the baseband signal at half the sampling frequency. The receiver integrates Low-Noise Amplifier, filters and two 40-MHz sigma delta Analog to Digital Converters achieving a 12-bit resolution in 100 kHz.

13 – 5 Nov. 15 (3rd day) 17:50-18:02

A CMOS Low-Distortion Variable Gain Amplifier with Exponential Gain Control

Li Yin, Ting-Hua Yun, Jian-Hui Wu and Long-Xing Shi(Southeast University)

Abstract: In this paper, a CMOS low-distortion variable gain amplifier with exponential gain amplifier is developed by utilizing a transconductance linearization scheme. The VGA is composed of a VGA core based on current-steering structure, an exponential voltage generator based on transfer characteristics of differential pair, and a stage of fixed gain amplifier. The proposed VGA circuit was verified in 0.25um CMOS technology, the measurement results show a total gain control range of 40dB, the 3-dB bandwidth is 100MHz, and a -58.5dBc third-order inter-modulation distortion at differential output of 2Vpp are obtained, the noise figure at maximum gain is 8.6dB.

13 – 6 Nov. 15 (3rd day) 18:02-18:14

A 290MHz 50dB Programmable Gain Amplifier for Wideband Communications

Hua-chin Lee, Chien-chih Lin and Chorng-kuang Wang(National Taiwan University)

Abstract: This paper presents a CMOS programmable gain amplifier (PGA) with 3dB bandwidth greater than 290MHz. The PGA can provide 50dB gain with 20dB gain control range, and the gain step is 1dB with -0.4 to +0.4dB gain error. The minimal acceptable input signal is -52dBmand the 1dB compression point is -6dBm. It consumes 4mA in core stage from1V supply voltage. This PGA is fabricated in 90nm CMOS one-poly nine-metal digital process and the core area is 0.2x0.15mm2.

Session 14 Wireline Communication

Nov. 15 (3rd day) 16:10-18:15

Session Co-Chairs: *Seong Hwan Cho(KAIST), Donhee Ham(Harvard Univ.)*

14 – 1 Nov. 15 (3rd day) 16:10-16:35

An 1.4Gbps/ch LVDS Receiver with Jitter-Boundary-Based Digital De-skew Algorithm

Youngdon Choi, Jung-Bae Lee, Chang-Hyun Kim(Samsung Electronics), Deog-Kyoon Jeong and Wonchan Kim(Seoul National University)

Abstract: This paper introduces jitter-boundary-based (JBB) digitally controlled de-skewing algorithm for high-speed link such as flat panel display (FPD) and memory system. It tracks data sampling points by way of finding the boundaries of jitter probability density function (JPDF). This boundary-based tracking algorithm offers lower bit error rate (BER) under the asymmetric jitter distribution as well as symmetric one. In addition, it lowers the accumulated jitter through the delay adjustment of data path. Test chip was fabricated with 0.25um 5-metal CMOS technology. When 87.9ps rms jitter is applied with the data rate of 1.4Gbps as an input data, it recovers data with the BER of less than 10-11. When the transition maximized pattern is applied, the receiver dissipates 381mW.

14 – 2 Nov. 15 (3rd day) 16:35-17:00

Modified LMS Adaptation Algorithm for a Discrete-Time Edge Equalizer of Serial I/O

Koon-Lun Jackie Wong, E-Hung Chen and Chih-Kong Ken Yang(University of California, Los Angeles)

Abstract: Discrete-time edge equalizers can enhance symbol-rate equalizers by compensating for inter-symbol interference at data transitions (timing ISI). The reduced timing ISI improves the timing margin and provides the CDR with clean timing information. This paper shows that adapting tap weights with standard blind LMS algorithm results in a reduced eye and may not converge. A modified algorithm is introduced to maximize the data eye.

14 – 3 Nov. 15 (3rd day) 17:00-17:12

A 90nm 1-4.25Gb/s Multi Data Rate Receiver for High Speed Serial Links

Lidong Chen, Fulvio Spagna, Phil Marzolf and John K. Wu(Intel Corporation)

Abstract: This paper describes the design of receiver that supports the multi data rate operation from 1 to 4.25Gb/s, enabling a single macro to satisfy XAUI, CX4, KX4, Fibre Channel, SAS/SATA and 1GbE protocols. The receiver performs equalization to compensate for interconnect ISI, achieves 10mV sensitivity at 4.25Gb/s by using offset corrected amplification, and performs clock data recovery with a digital algorithm that controls a recovered clock out of a phase interpolator. The receiver has been validated in 90nm CMOS with 45mW at 1.1V supply voltage and demonstrated to achieve link over 30-meter AGW24 cable at 3.125Gb/s with BER<10e-14. Measured jitter tolerance in FC mode (4.25 and 2.125pGb/s) and XAUI mode (3.125Gb/s) exceed the template with margin of more than 0.2UIpp of sinusoidal jitter.

14 – 4 Nov. 15 (3rd day) 17:12-17:24

A 40 Gb/s Optical Receiver in 80-nm CMOS for Short-Distance High-Density Interconnects

C. Kromer, G. Sialm, D. Emi, H. Jackel(Swiss Federal Institute of Technology), T. Morf and M. Kossel(IBM Research)

Abstract: An optical receiver for short-range optical data communication up to 40 Gb/s is presented. The optimum number of limiting amplifier (LA) stages is calculated to achieve a large gain-bandwidth product. The receiver features an electrical transimpedance gain of 91.4 dBOhm and a bandwidth of 19.2 GHz. For the free-space optical measurements an InGaAs/InP photo diode (PD) and the CMOS receiver chip were placed and bonded on a test substrate. At 40 Gb/s an open eye at the output of the receiver is shown at an optical input power of -4.6 dBm. Including the transmitter non-idealities, sensitivities at 20 Gb/s and 30 Gb/s of -8.2 dBm and 7.5 dBm, respectively, at a BER = 1E-12 were measured. The complete receiver consumes 56 mW from a 1.1-V supply and occupies a chip area of 230 um x 220 um only.

14 – 5 Nov. 15 (3rd day) 17:24-17:36

A 14-Gb/s 4-PAM Adaptive Analog Equalizer for 40-inch Backplane

Tai-Cheng Lee and Qui-Ting Chen(National Taiwan University)

Abstract: Limitations of frequency response in backplane interconnections impede high-speed data transmission beyond Gbps. A 14-Gb/s 4-PAM adaptive analog equalizer is proposed to compensate the 40-inch backplane interconnections by using a sum-feedback filter (SFF), relaxing the design requirement of the conventional analog feed-forward equalizers (FFE). 4-level pulse amplitude modulation (PAM) is also adopted to increase the transmission data rate over bandwidth-limited channel. The 4-PAM adaptive equalizer has been fabricated in a 0.18-um CMOS technology, while dissipating 120 mW from a single 1.8-V power supply.

14 – 6 Nov. 15 (3rd day) 17:36-17:48

A Wide-Range Burst Mode Clock and Data Recovery Circuit

Wei-Zen Chen, Chin-Yuan Wei, and Jen-Wen Chen(National Chiao-Tung University)

Abstract: This paper describes the design of a 0.625-3.125 Gbps, burst mode clock and data recovery circuit in a 0.18 um CMOS process. A novel bang-bang PD incorporating binary-search phase acquisition and dynamic loop filter is proposed to achieve rapid phase locking. The measured locking time is less than 1 ns (@ 3.125 Gbps). Integrating with a limiting amplifier and a 1 to 4 demultiplexer on a single chip, the total power dissipation is 78 mW. The input sensitivity of the burst mode receiver is about 30 mV for BER less than 10-10.

14 – 7 Nov. 15 (3rd day) 17:48-18:00

A 800MT/s Multiprocessor Bus Interface With Strobe Centering Architecture

Harry Muljono, Stefan Rusu, Kathy Tian, Mubeen Atha, Marlene Chan and Charlie Lin(Intel Corporation)

Abstract: A 65nm 1.2V GTL bus interface achieves 800MT/s 6.4GB/s data rate in a 3-load Multi-Processor (MP) environment. To enable a 20% increase in data rate compared to previous design, it utilizes a staged driver, DLL controlled predriver, Tco compensation, data/strobe time shifter, high gain

differential amplifier as well as advanced Process, Voltage and Temperature (PVT) compensation design.

14 – 8 Nov. 15 (3rd day) 18:00-18:12

A Fast-Locking CDR Circuit with an Autonomously Reconfigurable Charge Pump and Loop Filter

Jong-Kwan Woo, Hyunjoong Lee, Woo-Yeol Shin, Heesoo Song, Deog-Kyoon Jeong and Suhwan Kim(Seoul National University)

Abstract: This paper presents the design of a phase-locked loop (PLL) based clock and data recovery (CDR) circuit that meets fast locking and low jitter. We reduce the locking time of a CDR circuit by 25% by means of a new autonomously reconfigurable charge pump and loop filter in a 1.25Gb/s CDR circuit. An experimental prototype was implemented in a 0.18 um standard CMOS technology. A receiver that incorporates our CDR circuit has an active area of 380 um X 350 um.

Session 15 Emerging Technologies and Bio/Sensor Applications

Nov. 15 (3rd day) 16:10-18:15

Session Co-Chairs: *Michael S-C Lu(Natl. Tsing Hua Univ.), Koji Kotani(Tohoku Univ.)*

15 – 1 Nov. 15 (3rd day) 16:10-16:35

Scalability of Carbon Nanotube FET-based Circuits

Keshavarzi Ali(Intel)

Abstract:

15 – 2 Nov. 15 (3rd day) 16:35-17:00

CMOS Meets Bio

Yong Liu, Hakho Lee, Robert M. Westervelt and Donhee Ham(Harvard University)

Abstract: There are burgeoning efforts to use CMOS ICs for biotechnology. This paper reviews one such effort, development of a CMOS/Microfluidic hybrid system for magnetic manipulation of biological cells originally reported by the authors in [1], [2]. Programmable magnetic field patterns produced by a CMOS microcoil array IC efficiently manipulate individual cells (tagged by magnetic beads) inside a microfluidic system fabricated on top of the IC.

15 – 3 Nov. 15 (3rd day) 17:00-17:12

A 6-b DAC and Analog DRAM for a Maskless Lithography Interface in 90nm CMOS

David Fang(Intel Corp and University of California, Berkeley), Ryan Roberts, Borivoje Nikolic(University of California, Berkeley)

Abstract: A parallel, 12um-pitch, low-power 6-b segmented digital-to-analog converter (DAC) array drives an array of 3um x 3um analog DRAM cells in a 2.5/1V 90 nm CMOS process, with an application in maskless lithography. A self-calibrating compensation technique limits the effect of charge leakage and capacitive process mismatch to less than 0.5LSB over 100ms of data hold time. A 2mm x 2mm test chip implements a mixed-signal interface with 32 DACs driving four 32 x 256 analog DRAM arrays.

15 – 4 Nov. 15 (3rd day) 17:12-17:24

CMOS Low-Power Variable-Gain CMFB-Free Current Feedback Amplifier for Ultrasound Diagnostic Applications

Hio Leong Chao, Dongsheng Ma(University of Arizona), Mike Koen and Paul Prazak(Texas Instruments)

Abstract: A CMOS current feedback amplifier (CFA) for ultrasound diagnostic applications is proposed. Unlike traditional CFAs, this design employs a new symmetrical and compact architecture, without the use of common-mode feedback (CMFB) circuitry. The design proposes an active feedback technique to drastically enhance the gain-bandwidth independence. It is also the first CFA to adopt Miller compensation for better frequency response with smaller compensation capacitor. The proposed CFA was fabricated and tested with a standard 0.35 um CMOS process with competitive performance to its Bipolar and BiCMOS counterparts. The active die area is 0.052 mm^2. Experiment results show that the CFA exhibits a minimum bandwidth of 4.5 MHz with a variable gain range of 0 to 46 dB, and a power dissipation of 2.18 mW.

15 – 5 Nov. 15 (3rd day) 17:24-17:36

A Low-Voltage and Area-Efficient Adaptive SI SDADC for Bio-Acquisition Microsystems

Chih-Jen Cheng and Shuenn-Yuh Lee(National Chung-Cheng University)

Abstract: An ultra-low voltage adaptive Sigma-Delta Analog-to-Digital Converter (SDADC) with a 10-bit dynamic range for bio-microsystem applications is presented.

15 – 6 Nov. 15 (3rd day) 17:36-17:48

The low power MICS band biotelemetry architecture and its LNA design for implantable applications

Chen-Ming Hsu, Chien-Ming Lee, Tzong-Chee Yo and Ching Hsing Luo(National Cheng Kung University)

Abstract: The exclusive biotelemetry system for implantable measurement utilizing a low-power BPSK transmitter, RF terminal chip for signal up-conversion and receiver is presented. The frequency band used in the human body is the un-licensed band at 402-405 MHz allocated to Medical Implant Communication Systems (MICS) by FCC and the ISM band at 2.4GHz is used for transmission in the air. This system has following characteristics: 40 channels with 75k bandwidth, low output power in transmitter and easily be full-integrated that are suitable for implantable applications. The low noise amplifier (LNA) with current reuse technique and cascode structure for high gain and low noise figure is implemented in this paper. The chip is designed and fabricated in TSMC 0.18um 1P6M CMOS technology.

15 – 7 Nov. 15 (3rd day) 17:48-18:00

A Bandpass Delta-Sigma Interface IC for Sacrificial Bulk Micromachined Inertial Sensors

Sang-Yoon Lee, Jaeha Kim, Bong-Joon Lee, Hwi-Cheol Kim, Hyung-Ho Ko, Dong-il Dan Cho and Deog-Kyoon Jeong(Seoul National University)

Abstract: A bandpass delta-sigma interface IC for sacrificial bulk micromachined inertial sensors is presented. To achieve high resolution without precision analog circuits, the proposed architecture replaces the analog mixer of a chopper-stabilized readout amplifier with a 1-bit, 4th-order band-pass delta-sigma modulator and a digital decimator/demodulator. Leveraging the high over-sampling ratio of 8192 and the supporting circuit techniques, the interface IC provides a 128-Hz, 20-bit digital output with 113dB peak SNR and 115dB dynamic range (DR). Fabricated in 0.18um CMOS, the IC dissipates 56.1mW.

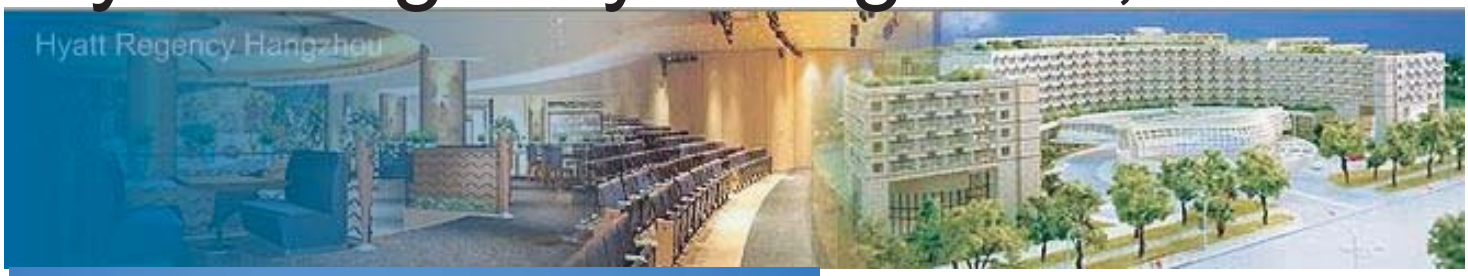
15 – 8 Nov. 15 (3rd day) 18:00-18:12

Design, Fabrication and Characterization of Novel Piezoresistive Pressure Microsensor for TPMS.pdf

Yanhong Zhang, Bingwu Liu, Litian Liu, Zhimin Tan, Zhaohua Zhang, Huiwang Lin and Tianling Ren(Tsinghua University)

Abstract: Novel piezoresistive microsensors for automotive tire pressure monitoring system (TPMS) are designed, fabricated and tested. 30um thick silicon diaphragms (from 370um*370um to 970um*970um) are adopted, thicker than that of the conventional piezoresistive pressure sensor, which extends the high stress distribution in the bulk silicon. Novel meander shape piezoresistors are designed, parts of which are fabricated on the high stress bulk silicon to obtain high linearity and sensitivity. Different diaphragm areas, piezoresistive shapes and placing methods on the microsensor performances are simulated, measured and analyzed. The whole fabrication is low-cost and compatible with standard IC process, which tolerates large process variations. Good microsensor precision (0.23%/FS) is obtained. The whole work indicates a novel solution of small size, high performance and low cost piezoresistive microsensor for TPMS and many other applications.

Hyatt Regency Hangzhou, China



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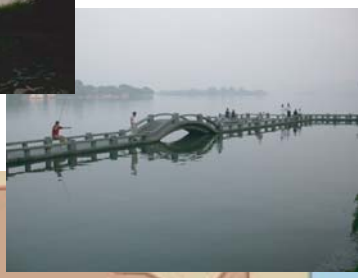

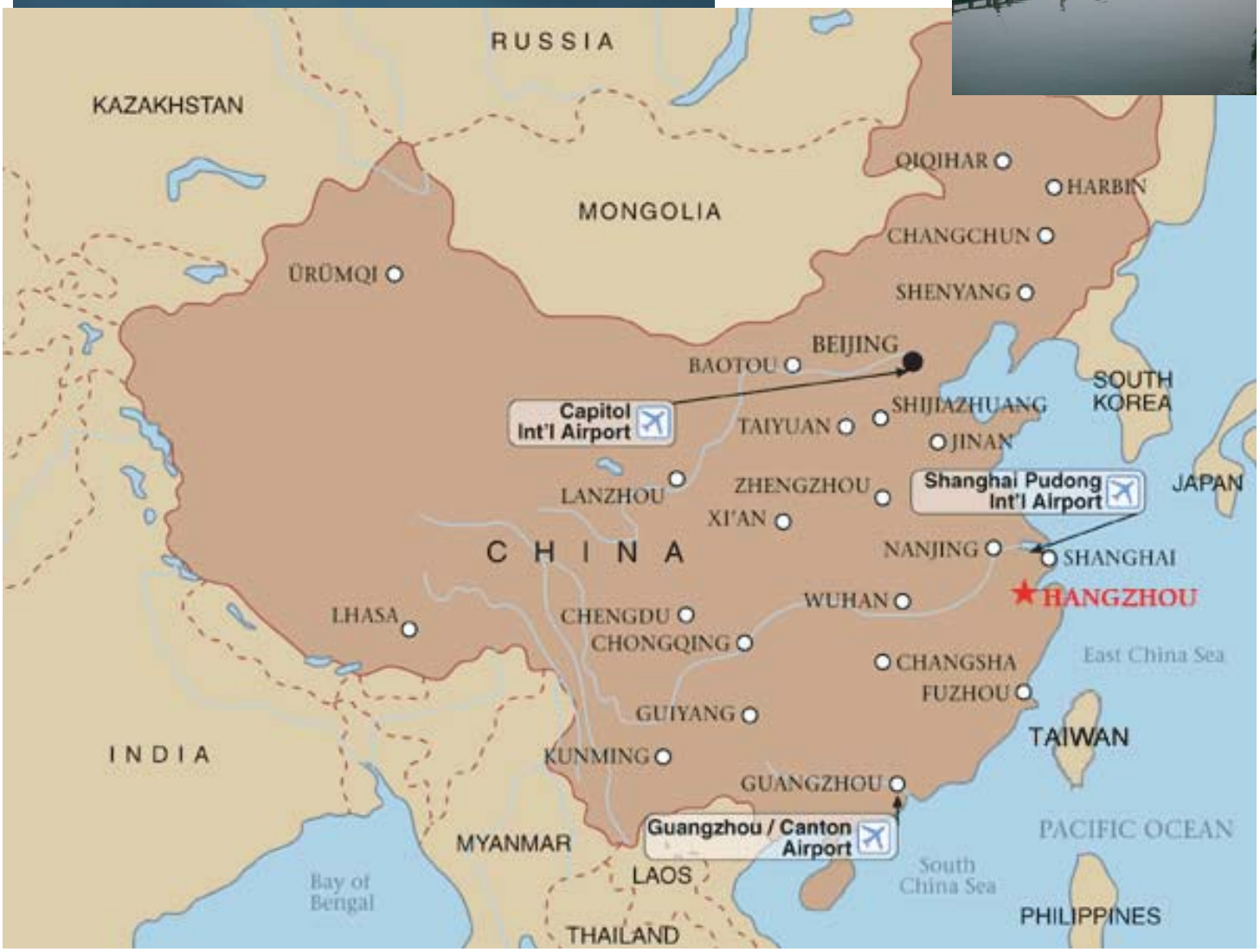

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