A-SSCC 2008

The 4th
IEEE Asian Solid-State Circuits Conference
Fukuoka, November 3-5, 2008

Advance Program

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A-SSCC2008 Program at a Glance

Nov. 3

	Navis-C	Navis-B	Navis-A	Argos-F	Argos A&B	Nire	Kusu
09:00-10:20 (80)	**Tutorial 1** **Design of Femto-joule Energy Efficient ADCs in CMOS** Geert Van der Plas (IMEC)	**Tutorial 2** **Advanced SiP design** Joungho Kim (KAIST)		Panel Exhibition by Fukuoka Industry, Science & Technology Foundation (Fukuoka IST) http://www2.lab-ist.jp/english/		Organizing Committee Office	Internet Lounge
10:20-10:40 (20)	**Break**						
10:40-12:00 (80)	**Tutorial 1** **Design of Femto-joule Energy Efficient ADCs in CMOS** Geert Van der Plas (IMEC)	**Tutorial 2** **Advanced SiP design** Joungho Kim (KAIST)					
12:00-13:00 (60)	**Lunch**						
13:00-14:20 (80)	**Tutorial 3** **Advanced Clock Distribution System** Simon Tam (Intel)	**Tutorial 4** **Economic and Design Choices for Nano-scale Electronic Systems** Siva Narendra (Tyfone)					
14:20-14:40 (20)	**Break**						
14:40-16:00 (80)	**Tutorial 3** **Advanced Clock Distribution System** Simon Tam (Intel)	**Tutorial 4** **Economic and Design Choices for Nano-scale Electronic Systems** Siva Narendra (Tyfone)					
16:00-17:30 (90)				**Student Design Contest (SDC)**			
17:30-19:00 (90)	**Welcome Reception**						

Nov. 4

	Navis-C	Navis-B	Navis-A	Argos-F	Argos A&B	Nire	Kusu
08:30-08:40 (10)	**Opening Ceremony**						
08:40-08:50 (10)	**Welcome Speech of Fukuoka Prefectural Governor**						
08:50-09:35 (45)	**Plenary Talk 1** **"Aiming for an Environmental-Oriented CE Platform"** Yoshiaki Kushiki (Panasonic)			Panel Exhibition by Fukuoka IST		Organizing Committee Office	Internet Lounge
09:40-10:25 (45)	**Plenary Talk 2** **" Foundry-Fabless Collaboration for Semiconductor SoC Industry in Korea"** Young Hwan Oh (Dongbu HiTek Semiconductor)						
10:25-10:55 (30)	**Break**			**SDC Exhibition**			
10:55-12:35 (100)	**Industry Program 1** **Processors and Multimedia Circuits** Stefan Rusu (Intel), Shaojun Wei (Phoenix Microelectronics)	**Industry Program 2** **High-Speed Signaling and Interfaces** Changhyun Kim (Samsung Electronic), Koji Kai (Panasonic)		Panel Exhibition by Fukuoka IST			
12:35-13:40 (65)	**Lunch**						
13:40-15:45 (125)	**Session 1** **Multi-stage A/D Converters** Yong Moon (Soongsil Univ.), Koichi Ono (Sony)	**Session 2** **Power and Delay Reduction Techniques for Digital Circuits** Xiaoyang Zeng (Fudan Univ.), Hideyuki Kabuo (Panasonic)	**Session 3** **Short-Range Interface Systems** Yasumoto Tomita (Fujitsu Laboratories), Hiroyuki Mizuno (Hitachi)	**Session 4** **mm-Wave CMOS Circuits** Shouhei Kousai (Toshiba), Howard Luong (HKUST)			
15:45-15:50 (5)	**Break**						
15:50-17:30 (100)	**Panel Discussion 1** **SiP2.0: What, When, and How?** Masayuki Mizuno (NEC Electronics)	**Panel Discussion 2** **Digitally Assisted Analog and RF Circuits: Potentials and Issues** Asad A. Abidi (UCLA)		Panel Exhibition by Fukuoka IST			
17:30-18:00 (30)	**Break**			**SDC Exhibition**			
18:00-18:45 (45)	**Special Lecture** **How to Write a Good JSSC Paper** Bram Nauta (Univ. of Twente)			Panel Exhibition by Fukuoka IST			
18:45-19:00 (15)	**Break**						
19:00-21:00 (120)					**Banquet**		

Nov. 5

	Navis-C	Navis-B	Navis-A	Argos-F	Argos A&B	Nire	Kusu
08:30-09:15 (45)	**Plenary Talk 3** **"4G Wireless Technology: When will it Happen? What does it Offer?"** Bill Krenik (Texas Instruments)					Organizing Committee Office	Internet Lounge
09:15-09:50 (35)	**Break**						
09:50-12:20 (150)	**Session 5** **Advanced Power Management** Yasuhiro Sugimoto (Chuo Univ.), Bill Liu (Analog Devices, Shanghai)	**Session 6** **Multimedia Signal Processing** Takeshi Ikenaga (Waseda Univ.) Oh-Kyong Kwon (Hanyang Univ.)	**Session 7** **Wireline Communication** Woo Geun Rhee (Tsinghua Univ.), Hiroyuki Okada (NEC Electronics)	**Session 8** **Memory** Hiroyuki Yamauchi (Fukuoka Inst. of Tech.), Jae-Yoon Sim (POSTECH)			
12:20-13:20 (60)	**Lunch**						
13:20-15:25 (125)	**Session 9** **Analog Circuit Techinique** Sung Min Park (Ewha Womans Univ.), Tsung-Hsien Lin (National Taiwan Univ.)	**Session 10** **Communication Signal Processing** Ramchan Woo (LG Electronics), Tai-cheng Lee (National Taiwan University)	**Session 11** **Electronics for Health** Ali Keshavarzi (TSMC), Reiji Hattori (Kyushu Univ.)	**Session 12** **RF Transceiver Circuits** Kang-Yoon Lee (Konkuk Univ.), Ryangsu Kim (Panasonic)			
15:25-15:45 (20)	**Break**						
15:45-18:15 (150)	**Session 13** **Sigma-Delta and Flash Data Converters** Hung-Sung Li (MediaTek), Sanroku Tsukamoto (Fujitsu Laboratories)	**Session 14** **Measurement & Characterization of Digital Circuits** Makoto Ikeda (Univ. of Tokyo), Vasantha Erraguntla (Intel Technology India)	**Session 15** **Clock Generation Circuits** Srikanth Gondi (K-Micro America), Koichiro Mashiko (Renesas Technology)	**Session 16** **RF Amplifiers and VCOs** Minoru Fujishima (Univ. of Tokyo), Hyunchol Shin (Kwangwoon Univ.)			

Tutorials

November 3, 2008 (Monday)

Tutorial 1

Time: 09:00-10:20, 10:40-12:00
Room: Navis C

Design of Femto-joule Energy Efficient ADCs in CMOS
Geert Van der Plas (IMEC)

Tutorial 2

Time: 09:00-10:20, 10:40-12:00
Room: Navis B

Advanced SiP Design
Joungho Kim (KAIST)

Tutorial 3

Time: 13:00-14:20, 14:40-16:00
Room: Navis C

Advanced Clock Distribution System
Simon Tam (Intel)

Tutorial 4

Time: 13:00-14:20, 14:40-16:00
Room: Navis B

Economic and Design Choices for Nano-scale Electronic Systems
Siva Narendra (Tyfone Inc.)

Student Design Contest

November 3, 2008 (Monday)

Student Design Contest

Time: 16:00-17:30
Room: Argos F

A 65 fJ/b Inductive-Coupling Inter-Chip Transceiver Using Charge Recycling Technique for Power-Aware 3D System Integration
Kiichi Niitsu (Keio University, Japan)

A 15-20GHz Delay-Locked Loop in 90nm CMOS Technology
Shen-Iuan Liu (Graduate Institute of Electronics Engineering, National Taiwan University, Taiwan)

A 4Gbps 3-bit parallel Transmitter with the Crosstalk-Induced Jitter Compensation using TX Data Timing Control
Hae-Kang Jung (POSTECH, Korea)

8Gbps CMOS ASK Modulator for 60GHz Wireless Communication
Ahmet Oncu (The University of Tokyo, Japan)

Low-power Programmable Divider for Multi-standard Frequency Synthesizers Using Reset and Modulus Signal Generator
Kyu-Young Kim (Department of Electronics and Computer Engineering, Korea University, Korea)

A Low-Power 0.7-V H.264 720p Video Decoder
Daniel Frederic Finchelstein (MIT, USA)

A Wireless Capsule Endoscopic System with a Low-Power Controlling and Processing ASIC
Xinkai Chen (Tsinghua University, China)

Digital Background Calibration of a 0.4-pJ/step 10-bit Pipelined ADC without PN Generator in 90-nm Digital CMOS
Anas A Hamouib (McGill University, Canada)

November 4, 2008 (Tuesday)

Opening Ceremony

Time: 08:30-08:40
Room: Navis B+C

Welcome Speech of Fukuoka Prefectural Governor

Time: 08:40-08:50
Room: Navis B+C

Plenary Talk 1

Time: 08:50-09:35
Room: Navis B+C

Aiming for an Environmental-Oriented CE Platform
Yoshiaki Kushiki
Matsushita Electric Industrial, Japan

Abstract: Panasonic has navigated the fiercely competitive years of the digital revolution in consumer electronics, developing many new strategies and technologies in the process. The company has vertically integrated its work in semiconductor and end-user products, developed platform strategies, and innovated new fabrication technologies. These technologies have evolved the end product business. In addition to succeeding in the new CE era, Panasonic is committed to addressing global warming and other environmental issues. Of key importance in the CE industry is the correlation between greater power savings and greater convenience for end users, particularly as device networking expands. This presentation discusses not only the improvement of energy performance in individual devices, but also the possibility of creating system-level green CE and a platform to support it.

Plenary Talk 2

Time: 09:40-10:25
Room: Navis B+C

Foundry-Fabless Collaboration for Semiconductor SoC industry in Korea
Young Hwan Oh
Dongbu Hitek Semiconductor, Korea

Abstract: The review of the trends in ecosystem and dynamics of semiconductor SoC industry in Korea is described. For the last decade, the development of SoC fabless industries has been phenomenal in that the total revenue of fabless companies became remarkably high and a number of major players of which the sales is around $200M are emerging in Korea. It was mainly on the basis of multimedia SoC integration into systems like mobile phones and digital TVs which have been pivotal IT growth engines in Korea. However, the main application of the SoCs have been limited to only a few IT areas and needs to explore the new engines to which they should be adapted, e.g., energy savings, automotives, ubiquitous sensor networks, telematics, robots and bio-industries. The new foundry-fabless collaboration areas like high voltage analog, mixed signals and RF are found considering the economic potential of the new IT system engines, excessive capital expenditure for the advanced technology nodes, longer product lifetime and focus on core competence of the foundry.

Industry Program 1 — Processors and Multimedia Circuits

Time: 10:55-12:35
Room: Navis C

Co-Chairs: Stefan Rusu (Intel Corp.)
Shaojun Wei (Phoenix Microelectronics)

Industry 1-1 — 10:55-11:20

A 125Mpixels/sec Full-HD MPEG-2/H.264/VC-1 Video Decoder for Blu-Ray Applications
Chi-Cheng Ju, Tsu-Ming Liu, Yung-Chaun Zhang, Chih-Ming Wang, Hue-Min Lin, Subrina Cheng, Chun-Chia Chen, Fred Chiu, Kung-Sheng Lin, Chung-Bin Wu, Sling Liang, Sheng-Jen Wang, Ginny Chen, TC Hsiao, Chi-Hui Wang
Mediatek Inc., Taiwan

Abstract—a fully-compliant high-definition video decoder LSI for Blu-ray Disc (BD) player is presented. It supports MPEG-2 MP@HL, H.264 HP@L4.1, and VC-1 AP@L3 video decoding in a single chip and features resource sharing and memory management unit to achieve area/throughput efficiency. A test chip is fabricated and integrates 515K logic gates with 522Kbits of embedded SRAM in 90nm single-poly seven-metal CMOS process with area of 5.06mm^2. For Blu-ray player requirements, video decoding of full 1920×1080 high-definition sequences at 60 frames per second requires 125Mpixels/sec of processing throughput which is two times higher than comparable designs [5][6] and is achieved at 200MHz clock frequency with power dissipation of 317mW at 1.0V supply voltage.

Industry 1-2 — 11:20-11:45

A Power, Performance Scalable Eight-Cores Media Processor for Mobile Multimedia Applications
Yasuyuki Ueda[1], Nobuhiro Nonogaki[1], Toshihiro Terazawa[2], Takeshi Kodaka[1], Takayuki Mori[1], Kumiko Morita[1], Hideho Arakida[1], Takashi Miura[1], Yukimasa Miyamoto[1], Yuji Okuda[1], Toshiki Kizu[1], Yoshiro Tsuboi[1]
1) Toshiba, Japan,
2) Toshiba Microelectronics, Japan

Abstract - We have developed a parallel process execution scheme, which enables reusable software to achieve high performance scalability for mobile multimedia application in according to available resources. Also, performance scalability on an eight-core media processor with low power circuits is certified by evaluating H.264 decoder. The high reusability of media processing engines and software developed on the basis of our scheme enable software solution to cover various image, media applications.

Industry 1-3 11:45-12:10

A Low Power IA Processor for Mobile Internet Devices in 45nm Hi-K Metal Gate CMOS

Gerosa, Gianfranco
Intel Corporation, USA

This paper describes a low power Intel Architecture (IA) processor specifically designed for Mobile Internet Devices (MID) with performance similar to mainstream Ultra-Mobile PCs. The design relies on high residency in a new low-power C-state in order to keep average power and idle power below a few hundred mW. The design consists of an in-order pipeline capable of issuing 2 instructions per cycle supporting 2 threads, 32KB instruction and 24KB data L1 caches, independent integer and floating point execution units, x86 front end execution unit, a 512KB L2 cache and a 533 MT/s dual-mode (GTL and CMOS) front-side-bus (FSB). The design contains 47M transistors in a die size under 25 mm2 manufactured in a 9-metal 45nm CMOS process with optimized transistors for low leakage packaged in a Halide-Free 441 ball, 14X13 mm mFCBGA. Maximum thermal design power consumption is measured at 2W using a synthetic power-virus test at a frequency of 2GHz.

Industry 1-4 12:10-12:35

Cell Broadband Engine Performance and Yield Benchmark in 65nm SOI CMOS with Spatial, Temporal and Parametric Process Variability Model

Choongyeun Cho[1], Daeik D. Kim[1], Jonghae Kim[2]
1) IBM Semiconductor R&D Center, USA
2) Qualcomm Inc., USA

Abstract—This paper introduces a process variability model to determine the performance and yield of the Cell Broadband Engine (CBE) in 65nm SOI CMOS. The model incorporates spatial (die-to-die), temporal (manufacturing process drift), and parametric dimensions, and provides microprocessor performance tracking and comprehensive view on the process variability with embedded ring oscillator measurement at the wafer level. It extracts CBE performance regularity within die for the circuit design and models, and reveals the semiconductor manufacturing signatures in wafers and lots for process technology. The model reduces performance estimation testing requirements by surpassing conventional methods' accuracy by 28%.

Industry Program 2 High-Speed Signaling and Interfaces

Time: 10:55-12:35
Room: Navis B

Co-Chairs: Changhyun Kim (Samsung Electronic)
Koji Kai (Panasonic)

Industry 2-1 10:55-11:20

A 16Gb/s/link, 64GB/s Bidirectional Asymmetric Memory Interface Cell[1]

Ken Chang, Haechang Lee, Jung-Hoon Chun, Ting Wu, TJ Chin, Kambiz Kaviani, Jie Shen, Xudong Shi
Rambus Inc, USA

Abstract- An asymmetric memory interface cell with 32 bidirectional data and four unidirectional request links operating at 16Gb/s per link is implemented in TSMC 65nm CMOS process technology. Timing adjustment and equalization circuits for both memory read and write are on the controller to reduce the memory cost. Each link operates at a maximum rate of 16Gb/s with sufficient and comparable margins in both directions at a BER of 10^{-12}. The measured energy efficiency for the controller interface cell is 13mW/Gb/s under nominal operating conditions.

Industry 2-2 11:20-11:45

Channel BER Measurement of a 5.8Gb/s/pin Unidirectional Differential I/O for a Future DRAM Application

Hoeju Chung, Youngchan Jang, Youngdon Choi, Hwanwook Park, Jaekwan Kim, Soouk Lim, Jung Sunwoo, Moonsook Park, Hyungwseuk Kim, Sang-Yun Kim, Hyun-Kyung Kim, Su-Jin Jung, Eun-Mi Lee, Youngju Kim, Yun-Sang Lee, Woo-Seop Kim, Jung-Bae Lee, Changhyun Kim
Samsung Electronics Co., LTD, Korea

Abstract - A 5.8Gb/s/pin DRAM with unidirectional differential I/Os and 1Gbit memory core was designed. TX BER measurement was performed on an electrical test board similar to a real system environment and the results show that no additional coding for the differential I/O protection, like CRC, is required up to 5.8Gb/s/pin operation. Also, an efficient timing usage method for a possible implementation of CRC computation in ODIC architecture was proposed.

Industry 2-3 11:45-12:10

1.25Gbps Optical Links for Mobile Handsets

Shin'ichiro Azuma, Ryoji Yanagimoto, Shingo Kamitani, Masakazu Edamoto, Katsumi Arata, Hirofumi Matsui, Hiroyuki Akada, Ryoichi Masuda, Kozo Hoshino, Kazuhito Nagura, Hiroaki Ogawa
Sharp Corporation, Japan

Abstract— This paper presents a 1.25Gbps optical links design for mobile handsets. The system consists of an optical connector and a SER/DES main chip. The former contains an 850nm VCSEL (vertical cavity surface emission laser), a GaAs-PIN photodiode and a transimpedance amplifier (TIA). The later includes a serializer, a deserializer, a VCSEL driver, a limiting amplifier, a PLL and a CDR. The chip and TIA were fabricated in a 0.13um CMOS process with MIM capacitors. A digital type CDR with fine timing controls allows sharing a VCO between transmitter and receiver, resulting in reduced both power consumption and silicon area. The system fully demonstrated a 1.25Gbps data and video stream transmission, consuming 108.4mW of power under 1.2V/3.3V supply voltages.

Industry 2-4 12:10-12:35

An ASIC-Ready 1.25-6.25Gb/s SerDes in 90nm CMOS with Multi-Standard Compatibility

Yoshinori Nishi, Koichi Abe, Jerome Ribo, Benoit Roederer, Anand Gopalan, Mohamed Benmansour, An Ho, Anusha Bhoi, Masahiro Konishi, Ryuichi Moriizumi, Srikanth Gondi, Vijay Pathak
Kawasaki Microelectronics America, Inc., USA

Abstract- A small area PHY transceiver that is compatible with CEI6G-LR, CEI6G-SR, SAS-6G, PCIe and XAUI standards is demonstrated. The 4-channel transceiver is realized in a 90nm CMOS process with each channel occupying a die area of 0.325mm^2. Power dissipation per channel is less than 230mW from a 1V supply for 6.25Gb/s, and scales for data rates down to 1.25 Gb/s.

Session 1 : Multi-stage A/D Converters

Time: 13:40-15:45
Room: Navis C

Co-Chairs: Yong Moon (Soongsil University)
Koichi Ono (Sony)

1-1 13:40-14:05

A 770-MHz, 70-mW, 8-bit Subranging ADC using Reference Voltage Precharging Architecture

Kenichi Ohhata, Koki Uchino, Yuichiro Shimizu, Yasuhiro Oyama, and Kiichi Yamashita
Kagoshima University, Japan

Abstract- This paper describes a high-speed low-power CMOS subranging analog-to-digital converter (ADC). A reference voltage precharging architecture and the introduction of a comparator with built-in threshold voltage in the fine ADC are proposed to reduce the settling time of the reference voltage. A T/H circuit with body-bias control circuit is employed to reduce the distortion at high sampling rate. The test chip fabricated using 90-nm CMOS technology shows a high-sampling rate of 770 MS/s and a low-power consumption of 70 mW.

1-2 14:05-14:30

A 6-b 1-GS/s 30-mW ADC in 90-nm CMOS Technology

Yuan-Ching Lien and Jri Lee
National Taiwan University, Taiwan

Abstract-A 6-b 1-GS/s subranging ADC with THA is implemented in 90-nm CMOS technology. This circuit incorporates folded input for the fine ADC as well as offset calibration and digital correction techniques, achieving greater than 5.2 ENOB and 40-dB SFDR up to the Nyquist, and 1.1-GHz ERBW with power consumption of only 30 mW.

1-3 14:30-14:55

An 8mW 10b 50MS/s Pipelined ADC Using 25dB Opamp

Min Gyu Kim[2], Volodymyr Kratyuk[1], Pavan Kumar Hanumolu[1], Gil-Cho Ahn[3], Sunwoo Kwon[1], and Un-Ku Moon[1]
1) Oregon State University, USA
2) Broadcom Corporations, USA
3) Sogang University, Korea

Abstract—A 10-bit 50MS/s pipelined ADC is presented. A 25dB open loop dc gain amplifier is employed in the MDAC operation. The low opamp dc gain in the extreme is tolerated due to the use of a reference scaling scheme in conjunction with a background offset calibration. An intermediate gain stage is inserted into the pipeline to compensate for the accumulated reduction of reference and signal swing. The prototype IC implemented in a 90nm CMOS process achieves -63.2dB THD, 48.8dB SNR, and 48.6dB SNDR, while consuming 8mW from a 1V supply.

1-4 14:55-15:07

Digital Background Calibration of a 0.4-pJ/step 10-bit Pipelined ADC without PN Generator in 90-nm Digital CMOS

Mohammad Taherzadeh-Sani and Anas A. Hamoui
McGill University, Canada

ABSTRACT- In nanometer digital CMOS, the linearity of pipelined A/D converters (ADCs) is degraded by the low dc gains of the opamps. Gain-enhancement techniques significantly increase the analog-circuit design complexity at low power and low voltage. Therefore, even in medium-resolution applications, digital background calibration is attractive for designing power-efficient ADCs. A simple, yet accurate, digital background calibration technique, which does not require a pseudo-random (PN) calibration signal, is proposed to minimize the power dissipation in the digital calibration unit. It achieves the same convergence speed and accuracy as PN-based techniques in 2-path (split) pipelined ADCs. A 10-bit 44-MS/s pipelined ADC, fabricated in a standard 1.2-V 90-nm digital CMOS process, uses the proposed calibration technique to achieve a 58.7-dB SNDR for a 21.5-MHz input, with a figure-of-merit (FOM) of 0.4 pJ/step.

1-5 15:07-15:19

A 10-b 30-MS/s 3.4-mW Pipelined ADC with 2.0-V_{pp} Full-Swing Input at a 1.0-V Supply

Kunihiko Gotoh[1], Hiroshi Ando[2], Atsushi Iwata[2]
1) Fujitsu Laboratories Ltd., Japan
2) Hiroshima University, Japan

Abstract— This paper describes a low-voltage design for a pipelined A/D converter that can operate in a 2.0-V_{pp} full-swing input range at a 1.0-V supply. To enlarge the input range of an ADC and maintain the output range of its op-amps, we propose a new front-end 2b-MDAC with S/H that can reduce the output range of all MDACs by 50 % compared with the ADC's input. We designed a 10-b pipelined ADC with the proposed 2b-MDAC. The fabricated ADC using a 90-nm CMOS process is able to operate in 2.0-V_{pp} full-swing input at a 1.0-V supply in spite of it using conventional op-amps, and has SNDR/SFDR of 57.5 dB/69.0 dB at 30 MS/s with only 3.4 mW.

1-6 15:19-15:31

A 6-bit Pipelined Analog-to-Digital Converter with Current-Switching Open-Loop Residue Amplification

Feng-Chiu Hsieh and Tai-Cheng Lee
National Taiwan University, Taiwan

Abstract—A 700-MHz 6-bit pipelined ADC with current-switching open-loop residue amplification and global-gain control is designed. Using a multiplexed-input architecture to implement T/H and MDAC circuits, transmission-gate switches are replaced by current-switching techniques. Without the need of digital calibration, a global-gain control technique is developed to eliminate the gain error. Fabricated in a 0.13- μm CMOS technology, the ADC consumes 24 mW from a 1.2-V power supply while the active area is only 0.19 mm^2.

1-7 15:31-15:43

10-bit 100MS/s CMOS Pipelined A/D Converter with 0.59pJ/Conversion-Step

Moo-Young Kim, Jinwoo Kim, Tagjong Lee and Chulwoo Kim
Korea University, Korea

Abstract—A 31mW, 10-bit 100MS/s pipelined ADC has been developed. The proposed ADC achieves low power consumption, high noise immunity, and small area by employing a new opamp sharing technique that switches the summing node in an MDAC and a current source with a PVT condition detector. The ADC shows a DNL of less than 0.48 LSB and an INL of less than 0.95 LSB. Also, a SNDR of 56.2dB is measured with a 1MHz input frequency. It has been implemented in a 0.18um CMOS process and it occupies 1.6×0.8 mm^2 of active area.

Session 2 : Power and Delay Reduction Techniques for Digital Circuits

Time: 13:40-15:45
Room: Navis B

Co-Chairs: Xiaoyang Zeng (Fudan Univ.)
Hideyuki Kabuo (Panasonic)

2-1 13:40-14:05

A ROM Based Low-Power Multiplier

Bipul C. Paul[1], Shinobu Fujita[2], and Masaki Okajima[1]
1) Toshiba America Research Inc., USA
2) Toshiba Corporation, Japan

Abstract—We present a ROM based 16x16 multiplier for low power applications. The design uses sixteen 4x4 ROM based multiplier blocks followed by carry save adders and a final carry select adder (all ROM based) to obtain the 32bit output. All ROM blocks are implemented using single transistor ROM cells and eliminating identical rows and columns for optimizing the power and performance. Measurement results in 0.18µm CMOS process show a 40% reduction in power over the conventional carry save array multiplier when operated at its maximum frequency. The ROM based design also provides 44% less delay than the array multiplier with a minimal increase (7.7%) in power. This demonstrates the low-power operation of the ROM based multiplier also at higher frequencies.

2-2 14:05-14:30

A 320-MHz 8-bit × 8-bit Pipelined Multiplier in Ultra-Low Supply Voltage

Yung-Chih Liang[1], Ching-Ji Huang[1] and Wei-Bin Yang[2]
1) Industrial Technology Research Institute, Taiwan
2) Tamkang University, Taiwan

Abstract-This paper presents a 0.5-V ultra-low voltage multiplier. In order to achieve ultra-low voltage and high speed operation, we modify the traditional pipelined architecture and adopt a PMOS forward body bias control technique, a symmetric signal path full-adder structure and a synchronous output D flip flop. Fabricated in 130nm CMOS technology, the measured operation rate of 8bit × 8bit pipelined multiplier get up to 320-MHz clock rate and the power consumption is about 1.48mW from 0.5-V power supply.

2-3 14:30-14:55

Low-Power Programmable Divider for Multi-Standard Frequency Synthesizers Using Reset and Modulus Signal Generator

Kyu-Young Kim, Woo-Kwan Lee, Hoonki Kim and Soo-Won Kim
Korea University, Korea

Abstract- This paper proposes a low-power programmable divider for multi-standard frequency synthesizers using a reset and modulus control signal (RMS) generator. The use of RMS generator enables the adaptation of only one counter. This results in less power consumption and effective area. Our design also includes modified D flip-flop design. Proposed divider was designed and fabricated in a standard 0.18-µm CMOS technology. Its divide ratio covers from 13 to 1278 at 3GHz. The average power is 3.58mW with 1.5V power supply and effective area is 0.0408mm^2.

2-4 14:55-15:20

Fast Voltage Control Scheme with Adaptive Voltage Control Steps and Temporary Reference Voltage Overshoots for Dynamic Voltage and Frequency Scaling

Yoshifumi Ikenaga[1], Masahiro Nomura[1], Yoetsu Nakazawa[2], and Yoshihiro Hayashi[1]
1) NEC Electronics Corporation, Japan
2) NEC Corporation, Japan

Abstract – We have developed a voltage control scheme to reduce control time using a delay monitor and step-by-step supply-voltage control. With this scheme, voltage control steps are adaptively controlled, and there are temporary overshoots in the reference voltage. Experimental results with a 65-nm CMOS device indicate that the adaptive voltage control steps successfully reduce the voltage control time by about 35 % over that with fixed step. Simulation results indicate that temporary reference voltage overshoots reduce control time by more than 50%. The combination of these schemes is also effective for control time reduction. (Keywords: dynamic voltage and frequency scaling (DVFS), regulator, CMOS)

2-5 15:20-15:32

Design of Energy Efficient 10ps Per Bit Adder Circuits in CMOS

Victor Navarro-Botello[1], Juan A. Montiel-Nelson[1], Saeid Nooshabadi[2]
1) University of Las Palmas de Gran Canaria, Spain
2) Gwangju Institute of Science and Technology, Korea

Abstract—This work presents the experimental results, from chip measurements, of ripple carry adder circuits using a new CMOS logic family –Feedthrough Logic (FTL). A 14–bit low power FTL adder performs faster, (2.6 times smaller propagation time delay, and 1.85 times higher maximum frequency), and provides a better energy efficiency (67.9% saving), when compared with the dynamic domino CMOS logic style. The 18–bit high speed FTL, working at its maximum frequency, outperforms the dynamic domino logic in terms of the propagation delay (19.5 times less), maximum frequency (12.1 times more), and energy efficiency per bit (96.7% better).

2-6 15:32-15:44

A 1.6mm^2 4,096 Logic Elements Multi-Context FPGA Core in 90nm CMOS

Naoto Miyamoto, Tadahiro Ohmi
Tohoku University, Japan

Abstract- In this paper, we propose a dynamically reconfigurable multi-context FPGA core named Flexible Processor IV (FP4). FP4 contains 16 x 16 physical logic elements (LE) and 16 context memory planes, thus virtually 4,096 LEs are available in total. The core size is 1.36mm x 1.15mm in 90 nm CMOS technology. A big problem for FP4 is to prevent degradation of multi-context execution speed. We have designed a temporal communication module (TCM) made up of a 16-bit shift register. We have also developed design automation software named PELOC that can divide a large circuit to some small sub-circuits while keeping critical path delay equal among all the sub-circuits. By using the TCM and PELOC, we confirmed that multi-context execution speed of FP4 is almost the same as single-context execution speed.

Session 3 : Short-Range Interface Systems

Time: 13:40-15:45
Room: Navis A

Co-Chairs: Yasumoto Tomita (Fujitsu Laboratories)
Hiroyuki Mizuno (Hitachi)

3-1 13:40-14:05

500Mbps, 670μW/pin Capacitively Coupled Receiver with Self Reset Scheme for Wireless Connectors

Katsuyuki Ikeuchi[1], Kenichi Inagaki[1], Hideki Kusamitsu[2], Toshiyasu Ito[2], Makoto Takamiya[1], and Takayasu Sakurai[1]
1) University of Tokyo, Japan
2) Yamaichi Electronics Co., Ltd, Japan

Abstract- Using capacitively coupled signaling, the feasibility of implementing an electronic connector as short as 240μm in height is demonstrated for the first time using 0.18μm CMOS technology and 125μm FR4 printed circuit boards (PCB's). Maximum data rate of 500Mbps/pin and 3.6Gbps/mm^2 are measured with 670μW/pin of power consumption even with large parasitic capacitance associated with the FR4 board. Compared to the conventional circuits, the proposed self reset circuit can send signals 2.8x faster at the same parasitic capacitance or allow 6x more parasitic capacitance at the same data rate.

3-2 14:05-14:30

A 65 fJ/b Inductive-Coupling Inter-Chip Transceiver Using Charge Recycling Technique for Power-Aware 3D System Integration

Kiichi Niitsu, Shusuke Kawai, Noriyuki Miura, Hiroki Ishikuro, and Tadahiro Kuroda
Keio University, Japan

Abstract - This paper discusses a low-power inductive-coupling link in 90 nm CMOS. The novel transmitter circuit using charge recycling technique for power-aware three-dimensional (3D) system integration is proposed and investigated. Crosstype daisy chain enables charge recycling and achieves power reduction while keeping communication performance such as high timing margin, low bit error rate and high bandwidth. There are two design issues in cross-type daisy, one is pulse amplitude reduction and another is inter-channel skew. To compensate them, inductor design and replica circuit is proposed and investigated. Test chips were designed and fabricated in 90nm CMOS to verify the proposed transmitter. Measured result showed that proposed cross-type daisy chain transmitter achieved an energy efficiency of 65 fJ/bit without degrading any of timing margin, data rate and bit error rate.

3-3 14:30-14:55

A 21.2μ*A* ΔΣ-Based Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer

Matti Paavola, Mika Kämäräinen, Erkka Laulainen, Mikko Saukoski, Lauri Koskinen, Marko Kosunen, and Kari Halonen
Helsinki University of Technology, Finland

Abstract—In this paper, a micropower interface IC for a capacitive 3-axis micro-accelerometer implemented in a 0.25 -*μ*m CMOS process is presented. The fully-integrated sensor interface consists of a ΔΣ sensor front-end that converts the acceleration signal into the digital domain, a decimator, a frequency reference, a clock generator for the front-end, a voltage and current reference, the required reference buffers, and low-dropout regulators (LDOs) needed for system-on-chip power management. The interface IC provides operating modes for 1 and 25Hz signal bandwidths. The chip with a 1.72mm^2 active area draws 21.2 *μ*A in 1Hz mode, and 97.6 *μ*A in 25Hz mode, from a 1.2−2.75V supply. In 1Hz mode with a ±2 -g capacitive 3- axis accelerometer, the measured noise floors in the x-, y-, and z-directions are 1080, 1165 and 930 $\mu g/\sqrt{\text{Hz}}$, respectively.

3-4 14:55-15:20

Differential-Drive CMOS Rectifier for UHF RFIDs with 66% PCE at -12 dBm Input

Atsushi Sasaki, Koji Kotani, and Takashi Ito
Tohoku University, Japan

Abstract-A high efficiency differential CMOS rectifier circuit for UHF RFIDs was developed. The rectifier has a cross-coupled bridge configuration and is driven by a differential RF input. Differential-drive topology enables simultaneous low ON-resistance and small reverse leakage of diode-connected MOS transistors, resulting in large power conversion efficiency (PCE), especially under small RF input power conditions. The proposed differential-drive rectifier was fabricated with 0.18 μm CMOS technology, and the measured performance was compared with those of other types of rectifiers. Dependence of the PCE on an input RF signal frequency and output loading conditions was also evaluated. 66% of PCE was achieved under conditions of 953 MHz, -12 dBm RF input and 10 KΩ DC output load. This is twice as large as that of the state-of-the-art rectifier circuit. The peak PCE increases with a decrease in operation frequency and with an increase in output load resistance.

3-5 15:20-15:32

A Passive RF Receiving and Power Switch ASIC for Remote Power Control with Zero Stand-by Power

Lingwei Zhang, Hanjun Jiang, Xuguang Sun, Chun Zhang and Zhihua Wang
Tsinghua University, China

Abstract— A passive RF signal receiving and power switch ASIC is proposed, designed and verified for remote ac power switch. This IC receives 915MHz RF signals containing power switching commands, and switches on/off the ac power relay of a household appliance accordingly. The proposed ASIC only uses energy recovered from the received RF signal, and it consumes almost zero stand-by current. The wireless identification technique is adopted to improve its anti-disturbance performance. The ASIC is designed in the 0.18μm CMOS process, and it occupies a core area of 0.9mm^2. It can work with an RF input power as low as of 40μW, and the data receiving rate is ~25kbps. The measured standby current is less than 10nA. The designed ASIC has been verified in a wireless switch demo system which can be used to switch a 220V AC bulb remotely.

3-6 15:32-15:44

A Wireless Real-Time On-Chip Bus Trace System Using Quasi-Synchronous Parallel Inductive Coupling Transceivers

Shusuke Kawai[1], Takayuki Ikari[1], Yutaka Takikawa[2], Hiroki Ishikuro[1], and Tadahiro Kuroda[1]
1) Keio University, Japan
2) Renesas Design Corp., Japan

Abstract - A 480Mb/s wireless real-time bus trace system with a pulse-based inductive coupling channel array was developed using an 0.25μm CMOS process. The size and pitch of the inductor array are determined by numerical calculation to optimize the tradeoff between the channel coupling, crosstalk, and alignment tolerance. A low-power quasi-synchronous system is proposed to obtain an enough timing margin for RX pulse detection under the presence of the clock skew. Power consumption is scalable to the data rate in this system.

Session 4 : mm-Wave CMOS Circuits

Time: 13:40-15:45
Room: Argos F

Co-Chairs: Shouhei Kousai (Toshiba)
Howard Luong (Hong Kong University of Science & Technology)

4-1 13:40-14:05

A 60GHz Variable-Gain LNA in 65nm CMOS

Arun Natarajan[1], Sean Nicolson[1,2], Ming-Da Tsai[2] and Brian Floyd[1]
1) IBM T.J Watson Research Center, USA
2) MediaTek, Taiwan

Abstract—A four-stage 60GHz low-noise amplifier is implemented in 65nm CMOS with nMOS *ft* of 210GHz. The LNA incorporates a reflection-type attenuator to provide variable gain with improved linearity in low-gain mode and a tunable notch filter for image rejection. The LNA, which consists of two common-source stages followed by two cascode stages, consumes 30.8mW and achieves 5.9dB NF and 15dB gain at 60GHz. The variable attenuator provides 10dB of gain variation with the input-referred 1dB compression point of the LNA being -15.1dBm in high gain mode and -6dBm in the low-gain mode. Each tunable notch filter stage provides an additional 8dB attenuation of 37GHz image signals, with the four-stage LNA achieving more than 35dB image-rejection[1].

4-2 14:05-14:30

A 60-GHz CMOS Power Amplifier with Marchand Balun-based Parallel Power Combiner

Y. Yoshihara, R. Fujimoto, N. Ono, T. Mitomo, H. Hoshino, and M. Hamada
Toshiba Corporation, Japan

Abstract- A novel Marchand balun-based parallel power com-biner suitable for a 60-GHz CMOS power amplifier is proposed. It improves the power efficiency by solving the issues of the phase difference of the signals to be combined and the low coupling factor of the on-chip balun in scaled CMOS technologies. The power amplifier using the proposed power combiner is fabricated in a 90nm CMOS process with 1.2 V supply. Measured power gain, output referred 1-dB compression point, and saturated out-put power are 11.2 dB, +8.3 dBm, and +11.2 dBm, respectively, at 60-GHz.

4-3 14:30-14:55

8Gbps CMOS ASK Modulator for 60GHz Wireless Communication

Ahmet Oncu, Kyoya Takano and Minoru Fujishima
The University of Tokyo, Japan

Abstract — In this paper we present a millimeter-wave CMOS amplitude-shift-keying (APh) modulator for $60GH_z$ wireless communication at greater than 1Gbps. It is designed using shunt NMOSFET switches between the signal and the ground line of a transmission line. A reduced-switch architecture is used to achieve high speed. The transmission line length between switches is adjusted to achieve high isolation with a reduced number of switches. A $60GH_z$ millimeter-wave APh modulator is successfully realized by using a 6-metal 1-poly 90nm CMOS process. The size of the chip is 0.8mm × 0.48mm including the pads. The core size is 0.61mm × 0.3mm. The isolation and maximum data rate of the modulator at $60GH_z$ are measured to be 26.6dB and $8Gbps_1$, respectively. The product of the maximum data rate and the isolation of this modulator is $170GH_z$, which is the highest value among over-Gbps APh modulators.

4-4 14:55-15:20

A 60-GHz, 14% Tuning Range, Multi-Band VCO with a Single Variable Inductor

Chi-Yao Yu, Wei-Zen Chen, and Chung-Yu Wu
National Chiao Tung University, Taiwan

Abstract—This paper presents the design of a 60-GHz, 14% tuning range VCO with a single variable inductor (VID). By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operations are achieved without sacrificing its operating frequency. Fabricated in a 90-nm CMOS process, the VCO is capable of covering frequency range from 53.1 to 61.3 GHz. The measured phase noise from a 61.3- GHz carrier is about -118.75 dBc/Hz at 10-MHz offset, and the output power is -6.6 dBm. The VCO core dissipates 8.7 mW from a 0.7-V supply. Chip size is 0.28 × 0.36 mm^2.

4-5 15:20-15:32

A 80GHz Voltage Controlled Oscillator with a Negative Varactor in 90nm CMOS Technology

Win Chaivipas, Kenichi Okada, and Akira Matsuzawa
Tokyo Institute of Technology, Japan

Abstract—A 80GHz voltage controlled oscillator is presented. A passive impedance transformation enables the transformation of a varactor capacitance into negative capacitance varactor is proposed, partially canceling the capacitance of the differential pair. This enables the transmission line resonator to be longer and have a higher impedance. Design criterion for achieving negative varactor capacitance is also presented, and design issues of millimeter wave voltage controlled oscillators are discussed. The voltage controlled oscillator is fabricated in 90nm CMOS technology and achieves a phase noise of -110dBc/Hz at 10MHz offset with 13mW power consumption from a 1.2V power supply.

4-6 15:32-15:44

A 60-GHz Direct-Conversion Transmitter on 130-nm CMOS

F. Zhang, B. Yang, B.N. Wicks, Z. Liu, C. M. Ta, Y. Mo, K. Wang, G. Felic, P. Nadagouda, T. Walsh, W. Shieh, I. Mareels, R. J. Evans and E. Skafidas
The University of Melbourne, Australia

Abstract—This paper describes the system architecture and design procedure for a 60-GHz transmitter on 130-nm CMOS process. The transmitter achieves a saturation power output of better than 4 dBm and an output-referred 1-dB compression point of 2 dBm. The LO to RF port isolation is better than 27 dB from 57 to 65 GHz. To the best of the authors' knowledge, this is the first reported 60-GHz transmitter on 130-nm CMOS that incorporates on-chip filtering.

Panel Discussion 1 : SiP2.0: What, When, and How?

Time: 15:50-17:30
Room: Navis C

SiP2.0: What, When, and How?
Organizer: Tadahiro Kuroda, Keio Univ., Japan
Moderator: Masayuki Mizuno, NEC, Japan
Panelists / Position: Ramchan Woo, LG Electronics / System Design
Nobukazu Kondo, Hitachi / System Design
Yukihiro Urakawa, Toshiba / Chip Design
Masayuki Miyamoto, Sharp / Chip Design
Koyu Asai, Renesas / Technology
Shintaro Yamamichi, NEC / Technology
Choon Heung Lee, Amkor Technology / Technology

Abstract: Up to now, SiP integration is widely used to increase chip integration density as well as flexibility of combination in heterogeneous devices. Emerging integration and stacking technologies such as 3D integration, TSV (Through Silicon Via), die-to-die proximity communications, EAD (Embedded Active Devices) are becoming greater attention. If we call the first generation SiP integration as “SiP1.0”, what is “SiP2.0” ? When and how is it practical?
Each panelists will give their anticipation of future SiP, or “SiP2.0”. This panel talk is not an "A vs. B" type of debate, but more like an evening talk where each panelist presents their visions on the next generation SiP.

Panel Discussion 2

Time: 15:50-17:30
Room: Navis B

Digitally Assisted Analog and RF Circuits: Potentials and Issues
Organizer: Akira Matsuzawa, Tokyo Tech., Japan
Moderator: Asad A. Abidi, UCLA, USA
Akira Matsuzawa, Tokyo Tech., Japan
Panelists: Asad A. Abidi, UCLA
Staszewski Bogdan, TI
Jan Craninckx, IMEC
Joel L. Dawson, MIT
Tai-Cheng Lee, NTU
Boris Murmann, Stanford Univ.
Bang Sup Song, UCSD

Abstract: Resent analog and RF circuits are increasing performance assisted by digital technology. This panel will demonstrate the potentials of this technology and discuss residual issues and potential solutions. Unlike conventional panels, this panel will not discuss explicit controversy such as A or B. The aim of this panel is to show recent new technology trend and to come out the real issues and potential solutions like tutorial session. Each panelist demonstrates the feature of digitally assisted analog and RF circuits followed by showing some residual issues in about 10 min and discuss the real issues and solutions with audiences.

Special Lecture

Time: 18:00-18:45
Room: Navis B+C

How to Write a Good JSSC Paper
Bram Nauta
University of Twente, Netherlands

November 5, 2008 (Wednesday)

Plenary Talk 3

Time: 08:30-09:15
Room: Navis B+C

4G Wireless Technology: When will it Happen? What does it Offer?

William Bill Krenik
Texas Instruments, USA

Abstract: Fourth generation (4G) technology will offer many advancements to the wireless market, including downlink data rates well over 100Mbps, low latency, very efficient spectrum use and low-cost implementations. With impressive network capabilities, 4G enhancements promise to bring the wireless experience to an entirely new level with impressive user applications, such as sophisticated graphical user interfaces, high-end gaming, high-definition video and high-performance imaging.
While these prospects are certainly exciting, questions still exist about the real meaning of "4G technology," deployment times and other pertinent details. Presented by TI's Wireless Chief Technology Officer Bill Krenik, this talk will highlight a handful of key factors that must be addressed to fully comprehend the benefits and challenges of successfully implementing 4G. Krenik will analyze 4G technology at the silicon level, touching on next-generation applications processing, modem technology, integration and cost. Efficient power management will also be investigated as a key enabler to realize 4G opportunities. Krenik also will discuss industry trends, offer predictions and shed light on how handsets will evolve with 4G deployment.

Session 5 : Advanced Power Management

Time: 09:50-12:20
Room: Navis C

Co-Chairs: Yasuhiro Sugimoto (Chuo University)
Bill Yang Liu (Analog Devices, Shanghai)

5-1 9:50-10:15

Dual-Section-Average (DSA) Analog-to-Digital Converter (ADC) in Digital Pulse Width Modulation (DPWM) DC-DC Converter for Reducing the Problem of Limiting Cycle

Yu-Chi Huang[1], Hsin-Chao Chen[1], and Ke-Horng Chen[2]
1) Industrial Technology Research Institute, Taiwan
2) National Chiao Tung University, Taiwan

Abstract—This paper proposes a dual-section average (DSA) analog-to-digital converter (ADC) to achieve a closed-loop digital pulse width modulation (DPWM) DC-DC converter with performance compatible to that by the analog PWM converter. For a 2.4V input voltage, a regulated output voltage of 1.2V can provide output current of 600mA without any offchip compensators. Besides, the output ripple can be reduced to about $8mV_{p-p}$ by theoretical result. The test chip was fabricated in 0.35μm CMOS technology. Owing to the parasitic resistance, the output ripple of the experimental result is within $30mV_{p-p}$. Furthermore, the transient recovery time is within 50μs when load current changes from 120mA to 600mA, or vice versa.

5-2 10:15-10:40

Low Power Consumption and High Power Density Integrated DC-DC Converter for Portable Equipments

S. Sugahara[1,3], K. Yamada[1], M. Edo[2], T. Sato[3], and K. Yamasawa[3]
1) Fuji Electric Device Technology Co., Ltd., Japan
2) Fuji Electric Advanced Technology Co., Ltd., Japan
3) Shinshu University, Japan

Abstract— We developed an integrated buck type DC-DC converter for portable electronic equipments. A newly developed pulse frequency modulation (PFM) control integrate circuits (ICs), which includes output power MOSFETs, achieved a low quiescent current below 14 μA and small chip size of 1.4 × 1.1 mm^2 in 0.35 μm CMOS process. The integrated converter consisted of the PFM control ICs on a planar inductor and had a maximum efficiency of 90 % and a power density above 100 W/cm^3.

5-3 10:40-11:05

A 0.35μm CMOS Sub-1V Low-Quiescent-Current Low-Dropout Regulator

Yuh-Shyan Hwang, Ming-Shian Lin, Bo-Han Hwang, Jiann-Jong Chen
National Taipei University of Technology, Taiwan

Abstract—A sub-1V CMOS low-dropout (LDO) voltage regulator with 103nA low-quiescent current is presented in this paper. The proposed LDO uses a digital error amplifier that can make the quiescent current lower than other LDOs with the traditional error amplifier. Besides, the LDO can be stable even without the output capacitor. With a 0.9V power supply, the output voltage is designed as 0.5V. The maximum output current of the LDO is 50mA at an output of 0.5V. The prototype of the LDO is fabricated with TSMC 0.35μm CMOS processes. The active area without pads is only 240μm x 400μm.

5-4 11:05-11:30

A Small-Area Voltage Regulator with High-Bandwidth Supply-Rejection Using a Regulated Replica in 45nm CMOS SOI

Thomas Toifl, Christian Menolfi, Peter Buchmann, Marcel Kossel, Thomas Morf and Martin Schmatz
IBM Zurich Research Laboratory GmbH, Switzerland

Abstract- We present a voltage regulator which uses a regulated replica in the loop in order to achieve small area, good power supply rejection over a wide frequency range, and high loop stability. The regulated replica provides accurate matching of the gm/gds ratio in the current source transistors for the replica and the load path. Power supply rejection of >22dB was measured up to 1GHz for a circuit operating at 0.8V from a 1.0V supply.

5-5 11:30-11:55

A 46-ppm/°C Temperature and Process Compensated Current Reference with On-Chip Threshold Voltage Monitoring Circuit

Ken Ueno[1], Tetsuya Hirose[2], Tetsuya Asai[1], and Yoshihito Amemiya[1]
1) Hokkaido University, Japan
2) Kobe University, Japan

Abstract—A CMOS current reference circuit has been developed in 0.35-μm CMOS process. The circuit consists of a voltage reference circuit, a noninverting amplifier, and an output MOS transistor. The circuit generates a reference current independent of temperature and process variations. Temperatureand process-compensation were achieved by making use of the zero temperature coefficient bias point of a MOSFET. Theoretical analyses and experimental results showed that the circuit generates a quite stable reference current of 18.4μA on average. The temperature coefficient, load sensitivity, and process sensitivity (σ/μ) of the circuit were 46-ppm/°C, 1.5%/V, and 4.4%, respectively. The circuit can be used as a current reference circuit for high precision analog circuit systems.

5-6 11:55-12:07

A Sub-1V Low-Dropout Regulator with an On-Chip Voltage Reference

Wei-Jen Huang and Shen-Iuan Liu
National Taiwan University, Taiwan

ABSTRACT- A sub-1V 50mA low-dropout regulator (LDR) with an on-chip voltage reference is presented. This LDR utilizes the push-pull output stage to reduce the size of the power PMOS transistor. The proposed LDR with the on-chip voltage reference has been fabricated in 0.18μm CMOS process, and its active area is 0.148mm^2. Experimental results demonstrate that the voltage reference and the LDR work for the supply voltage of 0.6V~1.2V. For the proposed LDR under a supply of 0.6V, the measured settling time, voltage dip, and quiescent current are less than 2μs, 50mV, and 16.6μA, respectively.

5-7 12:07-12:19

An Integrated Reconfigurable SC Power Converter with Hybrid Gate Control Scheme for Mobile Display Driver Applications

Feng Su and Wing-Hung Ki
The Hong Kong University of Science and Technology, Hong Kong

Abstract- An integrated switched-capacitor power converter with reconfigurable conversion ratios of 4x/5x/6x/7x/8x for mobile display driver applications is presented. This converter requires only four flying capacitors for realizing all the conversion ratios, and when achieving 4x and 5x, the original redundant flying capacitor is reconfigured to the dual-branch architecture to enhance efficiency. The advantages of both level-shifter and PN-switches control schemes are combined as a hybrid gate control scheme in eliminating reversion current. Gate switching loss of power transistors is reduced by a charge recycling mechanism. The design was fabricated in a 0.35μm 50V CMOS process. Measurement results confirm that the converter could achieve an output voltage higher than 14V for a supply voltage that ranges from 2V to 5V. The converter delivers 1mA even when the supply voltage is as low as 2V.

Session 6 : Multimedia Signal Processing

Time: 09:50-12:20
Room: Navis B

Co-Chairs: Takeshi Ikenaga (Waseda University)
Oh-Kyong Kwon (Hanyang University)

6-1 9:50-10:15

A Low-Power 0.7-V H.264 720p Video Decoder

D.F. Finchelstein, V. Sze, M.E. Sinangil, Y. Koken, A.P. Chandrakasan
Massachusetts Institute of Technology, USA

Abstract- The H.264/AVC video coding standard can deliver high compression efficiency at a cost of large complexity and power. The increasing popularity of video capture and playback on portable devices requires that the energy of the video codec be kept to a minimum. This paper proposes several architecture optimizations such as increased parallelism, multiple voltage/frequency domains, and custom voltage- scalable SRAMs that enable low voltage operation and reduce the power of a high-definition decoder. An H.264/AVC Baseline Level 3.1 decoder ASIC was fabricated in 65-nm CMOS and verified. It operates down to 0.7-V and has a measured power of 1.8mW when decoding a high definition 720p video at 30 frames per second, which is over an order of magnitude lower than previously published results.

6-2 10:15-10:40

A 66fps 38mW Nearest Neighbor Matching Processor with Hierarchical VQ Algorithm for Real-Time Object Recognition

Joo-Young Kim, Kwanho Kim, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo
KAIST, Korea

Abstract— A 66fps 38mW nearest neighbor matching processor for real-time object recognition has been fabricated in 0.13μm CMOS technology. It consists of RISC processing core, pre-fetch DMA, and two independent sets of logic merged memories. Based on hierarchical vector quantization (H-VQ) algorithm, implemented processor achieves 22.5X cycle time reduction in matching process without any accuracy loss in VQ operation. As a result, 66fps frame rate is obtained for QVGA (320x240 pixels) video images with 5632-entry database.

6-3 10:40-11:05

A 2.88mm^2 50M-Intersections/s Ray-Triangle Intersection Unit for Interactive Ray Tracing

Chen-Haur Chang, Chuan-Yiu Lee, and Shao-Yi Chien
National Taiwan University, Taiwan

Abstract—A ray-triangle intersection unit design for raytracing in embedded systems is fabricated by TSMC 0.13*μ*m technology. Bounding volume hierarchy data structure is employed to reduce the on-chip memory requirement. Multi-threading technique is used in the traversal unit to improve the hardware utilization and performance. Moreover, the cost of intersection unit is optimized with folding technique and reconfigurable datapath. Furthermore, the memory bandwidth is reduced with the proposed multi-bank cache architecture. It can provide the processing speed of 50M-intersections/s with only 2.88mm^2 in hardware cost.

6-4 11:05-11:30

A High-Speed Lossless Embedded Compression Codec for High-End LCD Applications

Yu-Hsuan Lee, Yu-Yu Lee, and Tsung-Han Tsai
National Central University, Taiwan

Abstract—Due to the great evolution of LCD panel technology, the memory bandwidth of relative display media system is significantly increased. Its impaction on system cost, EMI of transmission interface, and memory bandwidth dominates the performance of entire display media system. To eliminate this effect, a high-speed lossless embedded compression algorithm with pipelining and parallel VLSI architecture is proposed. With associated geometric-based probability model (AGPM), the compact coding flow is constructed by geometric-based binary code and contentadaptive Golomb-Rice code to achieve high-speed capability. The entire codec is implemented by TSMC 0.18-*um* 1P6M CMOS technology with Artisan cell library. The processing capability of two-level parallelism achieves Full-HD 1080p@60Hz with RGB components, and the four-level parallelism can further support 120Hz double frame rate (DFR) technique in high-end LCD applications.

6-5 11:30-11:55

A 76.8 GB/s 46 mW Low-Latency Network-on-Chip for Real-Time Object Recognition Processor

Kwanho Kim, Joo-Young Kim, Seungjin Lee, Minsu Kim, and Hoi-Jun Yoo
KAIST, Korea

Abstract—A 76.8 GB/s 46 mW low-latency network-on-chip (NoC) provides a communication platform for 125 GOPS realtime object recognition processor. The tree-based NoC with three crossbar switches is designed for low-latency and high energy efficiency by adopting dual-channel and adaptive switching. The NoC can be dynamically configured to exploit both data-level and object-level parallelism on the object recognition processor. FLIT-level clock gating and packet-based power management scheme are employed for low power consumption. The NoC is implemented in 0.13μm CMOS process and provides 76.8 GB/s aggregated bandwidth at 400MHz with 2-clock cycle latency while dissipating 46 mW at 1.2 V.

6-6 11:55-12:07

Design and Performance Evaluation of a 8-Processor 8,640 MIPS SoC with Overhead Reduction of Interrupt Handling in a Multi-Core System

Huong Thien Hoang[1], Phong The Vo[1], Y Thien Vo[1], Liem Tan Pham[1], Norimasa Otsuki[2], Masayuki Ito[2], Osamu Nishii[2]
1) Renesas Design Vietnam Co., Ltd., Vietnam
2) Renesas Technology Corp., Japan

Abstract- We have developed a platform SoC including eight SuperH processor cores for high performance applications. It achieves 8,640 MIPS at 600MHz for Dhrystone 2.1. The eight processor cores are divided into two clusters. Each cluster has a snoop controller to maintain cache coherency. The main internal system bus, packet-based split transaction, is 64 bits wide and runs at 300MHz. Eight processor cores, memory controllers, DMA, and hardware IPs are connected to this system bus. Each processor core and its on-chip user memory (URAM) can run at different frequency and operate in different power domain based on the workload of each individual core. An automatic-rotating interrupt distribution to processor cores is added to improve the system performance in handling interrupt requests. The processing time in Linux kernel is improved by 21% when SPLASH-2 is executed.

6-7 12:07-12:19

A Low-Power Processor for Portable Navigation Devices: 456 mW at 400 MHz and 24 mW in Software Standby Mode

Khoa Dac Tran[1], Phuong Van Nguyen[1], Hoa Tan Lu[1], Cuong Phuc Phan[1], Quang Hai Phan[1], Hiroyuki Kudo[2], Hiroo Masuda[2], Seiichi Negishi[2], Mitsuyoshi Yamamoto[2], Kenji Hirose[2], and Yasushi Okamoto[2]
1) Renesas Design Vietnam Co., Ltd., Vietnam
2) Renesas Technology Corp., Japan

Abstract— We have developed a processor (SH-MobileR2) optimized for both low power and high performance. SH-MobileR2 includes a 32-bit RISC type SuperH CPU with 720 MIPS performance at 400MHz operating frequency, and a Floating Point unit with 2.8 GFLOPS performance. The CPU also has a 64-KByte primary cache and a new 256-KByte secondary cache. Compared to the previous SH-MobileR processors, SH-MobileR2 has several high performance peripheral modules such as: a new DDR-SDRAM controller, an improved Video Processing unit (VPU5F), and an enhanced 2-D Graphics accelerator for higher performance applications. Low-power consumption is achieved by optimizing blends of a 90nm CMOS triple Vth cells, and using four power-down modes. The low-power consumption and the high performance of SH-MobileR2 processor is the most suitable for portable navigation devices.

Session 7 : Wireline Communication

Time: 09:50-12:20
Room: Navis A

Co-Chairs: Woo Geun Rhee (Tsinghua University)
Hiroyuki Okada (NEC Electronics)

7-1 9:50-10:15

A 4Gbps 3-bit Parallel Transmitter with the Crosstalk-Induced Jitter Compensation using TX Data Timing Control

Hae-Kang Jung[1], Kyoungho Lee[1], Jong-Sam Kim[2], Jae-Jin Lee[2], Jae-Yoon Sim[1] and Hong-June Park[1]
1) Pohang University of Science and Technology (POSTECH), Korea
2) Hynix Semiconductor Inc., Korea

Abstract - By using the data timing control at transmitter (TX) side, the crosstalk-induced jitter (CIJ) is compensated in a 4Gbps single-ended transmitter with 3-bit parallel data. CIJ is induced by the propagation velocity difference between the signal modes of parallel transmission lines. This velocity difference was compensated for by sending data early or late at TX according to the signal modes, so that the signals of different modes arrive at receiver at the same time. The proposed TX was implemented by using a 0.18μm CMOS process. The parallel transmission lines used in the measurements are 4-inch long, have the minimumallowed spacing between transmission lines to maximize CIJ. CIJ was measured to be reduced by about 50% from 53ps to 27ps at 4Gbps excluding the random jitter component of 72ps added at the TX side. The scheme used in this work can be expanded to more than three transmission lines.

7-2 10:15-10:40

Design Considerations for Low-Power High-Performance Mobile Logic and Memory Interfaces

Andy Chan, Judy Chen, Robert Palmer, John Poulton, Andrew Fuller
Rambus, Inc., USA

Abstract-- This paper highlights design considerations for low-power, high-performance mobile memory and logic interfaces, based on the results from the 14mW, 6.25Gb/s transceiver test chip demonstrated in 90nm CMOS. One of the keys to achieving 2.25mW/Gbps was the highly-sensitive, lowoffset receiver. An accurate receiver enables low-swing signaling and requires less power and area from the transmitter. The smaller transceiver design in turn lowers the clock distribution power and improves the signal quality by presenting less loading to the clock and the channel, respectively. The improved signal quality enables even lower signal swing and a “spiral of goodness” continues. This paper examines these aspects in detail and discusses their potential implications to a broad spectrum of future low-power, high-performance mobile interface designs.

7-3 10:40-11:05

Chip-to-Chip Half Duplex Data Communication at 135 Mbps Over Power-Supply Rails

Takushi Hashida, Yoji Bando, Makoto Nagata
Kobe University, Japan

Abstract—Chip-to-chip serial data communication is superposed on power supply over common Vdd/Vss connections through chip, package, and board traces. A power line transceiver demonstrates half duplex spiking communication at 135 Mbps. On-chip power line LC low pass filter attenuates pseudodifferential communication spikes by more than 30 dB, purifying power supply current for internal circuits. Chip-to-chip power line communication invokes supplementary diagnosis functionality to be embedded in SoCs at the time of power connection, with the reduced cost of pin counts.

7-4 11:05-11:30

A 15-20GHz Delay-Locked Loop in 90nm CMOS Technology

Jung-Yu Chang, Chi-Nan Chuang, Shen-Iuan Liu
National Taiwan University, Taiwan

Abstract—A 15GHz~20GHz delay-locked loop (DLL) has been fabricated in 90nm CMOS technology. It not only relaxes the speed requirement of the voltage-controlled delay line (VCDL), but also allows the VCDL not to operate at the highest frequency. When this DLL operates at 20GHz, the measured root-mean-square and peak-to-peak jitters are 0.813ps and 6.62ps, respectively. The core area is 0.25x0.4 mm^2 and the power consumption is 49mW for 0.9V supply.

7-5 11:30-11:42

A 3.2-Gb/s Transceiver with a Quarter-Rate Linear Phase Detector Reducing the Phase Offset

Kyung-Soo Ha and Lee-Sup Kim
KAIST, Korea

Abstract – In this paper, the transceiver which incorporates a PLL using a ring voltage-controlled oscillator (VCO), a phase interpolator (PI), the quarter-rate linear phase detector (PD) and an output driver with pre-emphasis is presented. The phase detector which uses a clock whose frequency is a quarter of the data rate and reduces the phase offset is proposed. The transceiver, implemented in a 0.18-*μ*m CMOS technology, operates at 3.2-Gb/s over a 10-cm PCB line with the Bit Error Rate (BER) of less than 10^{-12}. The chip area is 3.7 x 2.5 mm^2 and the core without I/O consumes 45-mA and I/O buffers consume 80-mA from a 1.8-V supply.

7-6 11:42-11:54

A 20-Gb/s Full-Rate 2^7-1 PRBS Generator Integrated with 20-GHz PLL in 0.13-μm CMOS

Jeong-Kyoum Kim[1], Jaeha Kim[2], and Deog-Kyoon Jeong[1]
1) Seoul National University, Korea
2) Rambus, Inc., USA

Abstract—This paper presents 20-Gb/s full-rate 2^7-1 PRBS generator with 20-GHz PLL. Implemented in a 0.13-μm CMOS process with f_T of only about 80 GHz, the proposed PRBS core achieves 20-Gb/s full-rate by using pulsed latches instead of flip-flops and XOR gates with inductive peaking and negative feedback. The clock buffers that drive the 20-GHz clock distribution and the pulsed-latches in the PRBS core also employ single-transformer based inductive peaking and negative feedback to achieve bandwidth of 73 GHz. The measured data jitter of the 18.8-Gb/s PRBS output is 3.55 ps_{rms} and 17.89 ps_{pp}. The measured clock jitter of the divided-by-16 clock is 1.99 ps_{rms} and 14 ps_{pp}. The fabricated PRBS generator and PLL dissipate 0.92 W and 0.19 W, respectively, from a 1.65-V supply.

7-7 11:54-12:06

A 20-Gb/s Coaxial Cable Receiver Analog Front-End in 90-nm CMOS Technology

Peter Park and Anthony Chan Carusone
University of Toronto, Canada

Abstract—A binary receiver analog front-end (AFE) targeting 20 Gb/s for use with coaxial cable channels is presented. To accommodate links of varying lengths, the AFE includes an analog peaking equalizer followed by a post-amplifier. The input preamplifier is important for achieving the required input sensitivity. A DC bias current is introduced through the feedback resistor in a conventional shunt-shunt feedback nMOS transimpedance amplifier (TIA) to level-shift the output, obviating a following level-shifting stage. The fabricated AFE occupies 0.89 mm^2 in a 90-nm CMOS process and dissipates 138 mW from a 1.3-V supply. The AFE amplifies and opens the eye pattern of a 20-Gb/s data stream transmitted over coaxial cable with 7.5-dB loss at 10 GHz.

7-8 12:06-12:18

A 10Gb/s Active-Inductor Structure with Peaking Control in 90nm CMOS

Yen-Sung Michael Lee, Samad Sheikhaei, and Shahriar Mirabbasi
University of British Columbia, Canada

Abstract—A PMOS-based active inductor circuit for high-speed I/O circuits is presented. The active inductor can operate with low voltage headroom and requires no voltage boosting. A prototype output driver circuit using the active inductor is implemented in 90nm CMOS. The peaking frequency and its corresponding magnitude of the active-inductor circuit can be adjusted to facilitate channel loss compensation. Operating at 10Gb/s over a 6-in FR4 channel, as compared to the case when the active-inductor structure is disabled, the use of active inductor circuit in the transmitter side increases the vertical eye opening at the receiver side by a factor of two and reduces the received peak-to-peak jitter by 30%. By keeping the current of the active inductor above a certain value, impedance variations are minimized and appropriate impedance matching is achieved (S_{22} less than −10 dB). The active-inductor circuit occupies 17 × 25 $μm^2$ and has a low overhead power consumption of 0.8 mW (~10% of the overall power of the prototype output driver).

Session 8 : Memory

Time: 09:50-12:20
Room: Argos F

Co-Chairs: Hiroyuki Yamauchi (Fukuoka Institute of Technology)
Jae-Yoon Sim (Pohang Univ. of Science and Tech.)

8-1 9:50-10:15

A 1.8ns Random Cycle SRAM-Interface High-Speed DRAM (SH-RAM) Compiler with Data Line Replica Architecture

Naoki Kuroda, Naoki Yamada, Toshihiro Nakamura, Yoshihiko Sumimoto, Masanobu Hirose, Kiyoto Ohta, Yasuhiro Agata, Yuji Yamasaki, Hironori Akamatsu
Matsushita Electric Industrial Co., Ltd., Japan

Abstract - The SH-RAM (SRAM-interface High-speed DRAM) is an embedded DRAM which is able to replace almost all embedded SRAMs in SoC fabricated by a 65nm LSTP embedded DRAM process. This paper describes the SH-RAM compiler which realizes a 1.8ns random cycle time and a 1.5ns random access time at 512Kbits macro without area penalty by High-Speed Bit Line Operation Technology and Data Line Replica Architecture.

8-2 10:15-10:40

A 8 GByte/s Transceiver with Current-Balanced Pseudo-Differential Signaling for Memory Interface

Seon-Kyoo Lee, Dong-Woo Jee, Yunjae Suh, Hong-June Park, and Jae-Yoon Sim
Pohang University of Science and Technology(POSTECH), Korea

Abstract - A 8 GByte/s single-ended parallel transceiver is implemented in a 0.18 μm standard CMOS with a current-balanced pseudo-differential signaling for high-speed memory interface. With a segmented group-inversion coding, 16-bit data is encoded to 20 pins for dramatic reduction of simultaneous switching noise which has been a bottleneck in high-speed parallel links. The proposed pseudo-differential signaling achieves a power-efficient current-mode parallel termination with a reduction of driving current of about 40-percent. For the termination, virtual voltage sources are self-generated by tracking the center of eye opening. The transceiver shows a BER of less than 10^{-12} at 4 Gb/s/pin.

8-3 10:40-11:05

A Low Power and High Performance Robust Digital Delay Locked Loop against Noisy Environments

Hyun-Woo Lee, Won-Joo Yun, Jong-Jin Lee, Ki-Han Kim, Nak-Kyu Park, Kwan-Weon Kim, Young-Jung Choi, Jin-Hong Ahn, Byong-Tae Chung
Hynix Semiconductor Inc., Korea

Abstract - A new low power and high performance robust digital delay locked loop is presented. The DLL has dual loops with single replica block, different-type dual DCC at input and output, replay mode function, rising edge scanner and selfcalibrated power down controller (SCPDC) for stable power management. The digital DLL used for Multi-Gbps Graphics SDRAM is fabricated using a 66nm DRAM process technology. Experimental results show duty-corrected clock from external duty error of ±10%, less than 400 cycle locking time, 1.4GHz operation frequency at 1.7V and 1.7GHz at 2.0v.

8-4 11:05-11:17

A Single-Loop DLL Using an OR-AND Duty-Cycle Correction Technique

Keun-Soo Song, Cheul-Hee Koo, Nak-Kyu Park, Kwan-Weon Kim, Young-Jung Choi, Jin-Hong Ahn, Byong-Tae Chung
Hynix Semiconductor Inc., Korea

Abstract – In this paper, we report a single-loop delay-locked loop (DLL) using a novel OR-AND duty-cycle correction (DCC) circuit. The proposed OR-AND DCC circuit employs both an analog blocks to detect duty error precisely and a digital block to correct duty-error quickly. To prove the proposed concepts, a single-loop DLL employing the proposed OR-AND DCC is demonstrated by using SPICE simulation. The DLL using 0.1- μm CMOS process provides an output clock with 16-psec peakto- peak jitter at 1-GHz operating frequency, taking 20-mA bias current from 1.8-V power supply. The proposed DCC shows an accuracy of ±1 % for ±25 % input duty error and 300 cycles duty-correction time in the range of 100MHz - 1.3 GHz operating frequencies.

8-5 11:17-11:29

A Fast GDDR5 Read CRC Calculation Circuit with Read DBI Operation

Sang-Sic Yoon, Bo-Kyeom Kim, Yong-Ki Kim, ByongTae Chung
Hynix Semiconductor Inc., Korea

Abstract — The GDDR5 provides Cyclic Redundancy Check (CRC) function to achieve high speed operation. The GDDR5 calculates the CRC with read data and transmits the results on Error Detection Code (EDC) pins. This paper presents the scheme to reduce the calculation time of CRC when the read Data Bus Inversion (DBI) is enabled. This scheme is applied to GDDR5 product manufactured with 66nm CMOS process technology and it achieved the performance more than 4.0Gbps bandwidth on the electric field test.

8-6 11:29-11:41

A Charge Recycling TCAM with Checkerboard Array Arrangement for Low Power Applications

Takahito Kusumoto, Daisuke Ogawa, Katsumi Dosaka, Masayuki Miyama, and Yoshio Matsuda
Kanazawa University, Japan

Abstract- A low power and low noise Ternary Content Addressable Memory (TCAM) architecture will be proposed. A TCAM is a powerful engine for search and sort processing, but it has serious power consumption and power line noise problems. To solve these problems, we have developed a charge recycling scheme for match lines, search lines and a Checkerboard Array arrangement. By using these technologies, TCAM power and power line noise can be reduced to 50% in comparison with conventional designs.

8-7 11:41-11:53

A 300 MHz Embedded Flash Memory with Pipeline Architecture and Offset-Free Sense Amplifiers for Dual-Core Automotive Microcontrollers

Shinya Kajiyama[1], Masamichi Fujito[2], Hideo Kasai[2], Makoto Mizuno[2], Takanori Yamaguchi[2], and Yutaka Shinagawa[2]
1) Hitachi, Ltd., Japan
2) Renesas Technology Corp., Japan

Abstract-We propose a novel 300 MHz embedded flash memory for dual-core microcontrollers targeting shared ROM architecture. One of the features is a three-stage pipeline read operation, which enables reduced access pitch and therefore reduced performance penalty due to shared ROM access conflict. The second feature is a highly sensitive sense amplifier that achieves efficient pipeline operation with two-cycle latency one-cycle pitch because of a shortened sense time of 0.63 ns. The combination of the pipeline architecture and the proposed sense amplifiers achieves significant reduction in access-conflict penalties with shared ROM and enhanced performance of 32- bit RISC dual-core microcontrollers by 30%.

8-8 11:53-12:18

A 500-MHz MRAM Macro for High-Performance SoCs

Noboru Sakimura, Ryusuke Nebashi, Hiroaki Honjo, Shinsaku Saito, Yuko Kato, and Tadahiko Sugibayashi
NEC Corporation, Japan

Abstract— A 500-MHz MRAM macro is developed using a 0.15-μm CMOS process and a newly developed MRAM process. The macro is designed using a 20.17-μm^2 5-transistor 2-magnetic tunnel junction (5T2MTJ) cell that has individual ports for writing and reading. An access time of less than 2 ns was obtained by employing a hierarchically-divided read bit line (RBL) and a high pre-charge sensing scheme. The operation speed is the highest among MRAMs that have been reported. This MRAM macro can coexist with the more area-effective 2T1MTJ-cell-based MRAM macro in SoCs.

Session 9 : Analog Circuit Techinique

Time: 13:20-15:25
Room: Navis C

Co-Chairs: Sung Min Park (Ewha Womans University)
Tsung-Hsien Lin (National Taiwan University)

9-1 13:20-13:45

A 2.0Vpp Input, 0.5V Supply Delta Amplifier with A-to-D Conversion

Yoshihiro Masui, Takeshi Yoshida, and Atsushi Iwata
Hiroshima University, Japan

Abstract—Recent progress in scaled CMOS technologies can enhance a signal bandwidth and clock frequency of analogdigital mixed VLSIs. However, inevitable supply voltage reduction causes signal voltage mismatch between a non-scaled analog chip and a scaled A-D mixed chip. To solve the problem, we present a Delta-Amplifier (DeltAMP) which can handle larger signal amplitude than the supply voltage. DeltaAMP operates by folding an analog signal within a voltage window using a virtual ground amplifier, modulation switches and comparators. The folded delta signal has to be reconstructed to the ordinal signal. A reconstruction circuit is also proposed based on Analog-Time-Digital conversion (ATD) in which pulse width analog information obtained at the comparators in DeltAMP, is converted to a digital signal by counting. A test chip of DeltAMP with ATD using a 90nm CMOS technology, achieved input voltage range of 2.0Vpp at a 0.5V supply, and SNR of 62dB at signal bandwidth of 120kHz. Measured power consumption was as low as 150μW at 0.5V supply.

9-2 13:45-14:10

A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs

Masaya Miyahara, Yusuke Asada, Daehwa Paik and Akira Matsuzawa
Tokyo Institute of Technology, Japan

Abstract - This paper presents a low offset voltage, low noise dynamic latched comparator using a self-calibrating technique. The new calibration technique does not require any amplifiers for the offset voltage cancellation and quiescent current. It achieves low offset voltage of 1.69 mV at 1 sigma in low power consumption, while 13.7 mV is measured without calibration. Furthermore the proposed comparator requires only one phase clock while conventionally two phase clocks were required leading to relaxed clock. Moreover, a low input noise of 0.6 mV at 1 sigma, three times lower than the conventional one, is obtained. Prototype comparators are realized in 90 nm 10M1P CMOS technology. Experimental and simulated results show that the comparator achieves 1.69 mV offset at 250 MHz operating, while dissipating 40 μW/GHz (20 fJ/conv.) from a 1.0 V supply.

9-3 14:10-14:35

A 65nm CMOS OpAmp for Nanoscale ULSI Library Cells

Weixun Yan and Horst Zimmermann
Vienna University of Technology, Austria

Abstract—In this paper, an OpAmp for general nanoscale ULSI library cells fabricated in 65nm digital CMOS technology is presented. The design limits of the nanoscale technologies, owing to the high noise, low intrinsic transistor gain and low supply voltage, are overcome by a suitably built topology, including a new well-compensated four-stage architecture, a fully differential structure, and a rail-to-rail input/output range with constant signal behavior. A satisfactory overall performance is attained. Measured with 1.2V supply voltage and 15pF load, the OpAmp has 90dB DC gain, 146.8MHz GBW, 71.6/94.9V/μs positive/negative slew-rate, 70dB CMRR and consumes 2.4mA current. The stability is also verified by the measurement results.

9-4 14:35-15:00

A 1-V G_m-C Low-Pass Filter for UWB Wireless Application

Tien-Yu Lo[1] and Chung-Chih Hung[2]
1) MediaTek Inc., Taiwan
2) National Chiao Tung University, Taiwan

Abstract—This paper proposes a high performance G_m-C equiripple linear phase low-pass filter for UWB wireless application. The proposed OTA is designed under low power supply voltage consideration while its gain, excess phase, and linearity are well maintained. The common-mode control system, including common-mode feedback (CMFB) and common-mode feedforward (CMFF) circuits, is added to ensure stability of the proposed filter. Measurement results show that the inter-modulation distortion (IM3) of -40dB can be achieved with 250MHz 400mV_{pp} balanced differential input signals. The filter works in 1-V supply voltage and its power consumption is 32mW.

9-5 15:00-15:12

A 12th Order Active RC Filter with Automatic Frequency Tuning for DVB Tuner Applications

Liang Zou[1], Youchun Liao[2], Hao Min[1], and Zhangwen Tang[1]*
1) Fudan University, China
2) Ratio Microelectronics Technology Co., Ltd., China

Abstract—A 12th order active RC filter for DVB Tuner applications with automatic frequency tuning (AFT) is presented in this paper. The filter is implemented in Butterworth biquad structure. The AFT circuit is introduced to compensate the frequency variation by a 7-bits switched-capacitor array. The measurement results indicate that the precision of tuning circuit can be controlled less than ±2.3%, the in-band group delay variation is 70ns, and the in-band IM3 achieves -60dB with -27dbm input power. This proposed filter circuit, fabricated in a SMIC 0.18μm CMOS process, consumes 6mA current with 1.8V power supply.

9-6 15:12-15:24

Programmable Pacing Channel With Fully On-Chip LDO Regulator for Cardiac Pacemaker

Chih-Jen Cheng, Chung-Jui Wu, and Shuenn-Yuh Lee
National Chung-Cheng University, Taiwan

Abstract—A novel dual-voltage pacing system for the implant pacemaker is presented in this paper. To reduce the ripple of the supply voltage and diminish the process variation imposed on the divided-resistor, a fully on-chip low-dropout (LDO) regulator is proposed. On the other hand, the adjustable pacing circuit together with a proposed sense feedback is adopted to deliver electrical stimuli of 16-step amplitudes to induce cardiac contraction. The pacing circuit with a LDO regulator was fabricated in TSMC 0.35- μm CMOS technology, consuming totally power of 1.29 μW including 185 nA of ground current in 1.2-V LDO and the power consumption of 30 nW in 1-V pacing step controller. Experimental results also demonstrate that the proposed LDO regulator features a power-supply rejection ratio (PSRR) of –30 dB with the output ripple of 570 μV_{pp} under the input sinusoidal wave of 19.6 mV_{pp}. Even with the load current of up to 10 μA, the LDO yields a line regulation of less than 3% deviation.

Session 10 : Communication Signal Processing

Time: 13:20-15:25
Room: Navis B

Co-Chairs: Ramchan Woo (LG Electronics)
Tai-cheng Lee (National Taiwan University)

10-1 13:20-13:45

A 10-pJ/instruction, 4-MIPS Micropower DSP for Sensor Applications

Nathan Ickes, Daniel Finchelstein, and Anantha P. Chandrakasan
Massachusetts Institute of Technology, USA

Abstract—We describe a micropower DSP intended for medium bandwidth microsensor applications (such as acoustic sensing and tracking), which achieves 4MIPS performance at 40 μW (10 pJ per instruction). Architectural optimizations for energy efficiency include a custom CPU instruction set, miniature instruction cache, hardware accelerator cores for FIR filter and FFT operations, and extensive power gating of both logic and memory.

10-2 13:45-14:10

A 0.5V 4.85Mbps Dual-Mode Baseband Transceiver with Extended Frequency Calibration for Biotelemetry Applications

Jui-Yuan Yu, Chien-Ying Yu, Shang-Bin Huang, Tsan-Wen Chen, Juinn-Ting Chen, Kuan-Ling Kuo, and Chen-Yi Lee
National Chiao Tung University, Taiwan

Abstract—This work provides a dual-mode transceiver chipset for wireless body area network (WBAN). The modulation schemes include both MT-CDMA and OFDM. A phase-frequency tunable clock generator (PFTCG) is designed with frequency and phase tuning capability on the fly. A rotator-and-synthesizer driven (RSD) frequency pre-calibration with the aid of the PFTCG enables calibration for extended 100ppm frequency error (2.5x of state-of-the-art systems). This chip is manufactured in 90nm standard CMOS process. The supply voltage to the chip core is globally applied at 0.5V with 12 power- and voltage-domain partitions for sleep-active and voltage-scaling management. The PFTCG is operated at 5MHz with RMS jitter 145ps. The transceiver chipset provides maximum 4.85Mbps data rate with 73.7% power reduction in baseband circuit processing.

10-3 14:10-14:35

A 820 Mb/s Baseband Processor LSI based on LDPC Coded OFDM for UWB Systems

Shinsuke Ushiki, Koichi Nakamura, Kazunori Shimizu, Qi Wang, Yuta Abe, Satoshi Goto and Takeshi Ikenaga
Waseda University, Japan

Abstract This paper presents a high-throughput and highlyreliable baseband processor LSI based on LDPC coding OFDM UWB. This LSI targets for wireless LAN systems inside a car which enable to translate a high-resolution video under noisy environment. A chip capable of operating at 147MHz was fabricated using UMC 0.13μm 1P8M CMOS technology. By adopting the OFDM modulation with 1024 sub-carriers, it achieves a throughput of 820Mb/s and 10^{-4} BER performance under 30dB CNR with 5/6 coding rate. Power dissipation is 189mW/391mW (TX/RX).

10-4 14:35-15:00

A 7.39mm^2 76mW (1944, 972) LDPC Decoder Chip for IEEE 802.11n Applications

Xin-Yu Shih, Cheng-Zhou Zhan, and An-Yeu (Andy) Wu
National Taiwan University, Taiwan

Abstract -- This paper presents the LDPC decoder chip for (1944,972) QC-LDPC codes in IEEE 802.11n communication system. The efficient LDPC decoder chip is designed with three design techniques, including Group Comparison (GC), Dynamic Wordlength Assignment (DWA), and Data Packet Scheme (DPS). When the target BER is 10^{-6}, the decoding performance can be improved by the coding gain of 0.48 dB and 0.63 dB with respect to (4,3) and (3,2) fixed-point NMSA, respectively. In addition, the total decoder design area can be reduced by 25% and the decoding throughput can be enhanced by 3X times with respect to conventional direct-mapping method. By using TSMC 0.13um VLSI technology, the core area and die size are only 3.88 mm^2 and 7.39 mm^2, respectively. The maximum operating frequency is measured at 111.1MHz and the power dissipation is only 76 mW.

10-5 15:00-15:12

A 50Mbps Double-Binary Turbo Decoder for WiMAX Based on Bit-level Extrinsic Information Exchange

Ji-Hoon Kim and In-Cheol Park
KAIST, Korea

Abstract-A 50Mbps, 2.24mm^2 double-binary turbo decoder is designed and implemented in 0.13μm CMOS process for the WiMAX standard. To reduce the large extrinsic memory needed in double-binary turbo decoding, the proposed decoder exchanges the bit-level extrinsic information values rather than the traditional symbol-level extrinsic information values, which is achieved by deriving two simple conversions. The proposed turbo decoder, with a low-complexity hardware interleaver generating interleaved addresses for two data flows simultaneously, provides an efficient stopping criterion for double-binary turbo decoding using bit-level extrinsic information as well as huge memory size reduction of 20.6%.

10-6 15:12-15:24

A 256-point Dataflow Scheduling 2×2 MIMO FFT/IFFT Processor for IEEE 802.16 WMAN

Fang-Li Yuan[1], Yi-Hsien Lin[1], Chih-Feng Wu[1], Muh-Tian Shiue[2] and Chorng-Kuang Wang[1]
1) National Taiwan University, Taiwan
2) National Central University, Taiwan

Abstract—In this paper, an efficient solution of MIMO FFT/IFFT processor for IEEE 802.16 WMAN is presented. By applying the proposed mixed-radix dataflow scheduling (MRDS) technique, the effective hardware utilization can be raised to 100%. Therefore, a single butterfly unit within each pipeline stage is sufficient to deal with the two data sequences and the hardware complexity is significantly reduced. The proposed FFT/IFFT processor has been emulated on the FPGA board. The SQNR is over 44dB for QPSK and 16/64-QAM signals. Furthermore, a test chip has been designed using standard 0.18μm CMOS technology with a core area of 887×842μm^2. According to the post-layout simulation results, the design consumes 46mW at 64MHz operating frequency, which meets the maximum throughput requirements of IEEE 802.16 WMAN.

Session 11 : Electronics for Health

Time: 13:20-15:25
Room: Navis A

Co-Chairs: Ali Keshavarzi (TSMC)
Reiji Hattori (Kyushu University)

11-1 13:20-13:45

A 1.12pJ/b Resonance Compensated Inductive Transceiver with a Fault-Tolerant Network Controller for Wearable Body Sensor Networks

Jerald Yoo, Seulki Lee, and Hoi-Jun Yoo
KAIST, Korea

Abstract—A low-energy inductive coupling link with a low energy fault-tolerant wearable body sensor network (BSN) controller is proposed to realize intra- and cross-layer wearable network at once. The intra-layer switch adopts the hybrid routing scheme to achieve fault-tolerance, and the cross-layer inductive transceiver employs the resonance compensator with an on-chip capacitor bank and a variable hysteresis Schmitt-Trigger to compensate dynamic and static variances of an woven inductor, achieving 10Mbps wireless transaction with the reception energy of 1.12pJ/b at 2.5V supply in 0.25μm 1P5M CMOS.

11-2 13:45-14:10

A Low Energy Sensor Node Controller for Wearable Body Sensor Network System

Hyejung Kim, Yongsang Kim, and Hoi-Jun Yoo
KAIST, Korea

Abstract— A low energy sensor node processor is proposed for wearable body sensor network system. A quadratic level bio signal compression algorithm is proposed to reduce the transmission power consumption and the memory capacity. The CR is 8.4:1, the PRD is 0.897% and the compression rate is 6.4Mbps. And the most compact AES-128 datapath is integrated for user privacy and authentication, and its normalized performance is 0.4b/cycle/k-gates. The serialized I/O interface packet, SerDes and CDR block are integrated for the efficient data transaction. The proposed processor consumes 0.56nJ/bit at 1V/2V supply voltage with 1MHz operating frequency in 0.25-μm CMOS process.

11-3 14:10-14:35

A Wireless Capsule Endoscopic System with a Low-Power Controlling and Processing ASIC

Xinkai Chen, Xiaoyu Zhang, Lingwei Zhang, Hanjun Jiang, Zhihua Wang
Tsinghua University, China

Abstract—This paper presents the design of a wireless capsule endoscopic system with a low-power controlling and processing ASIC. The ASIC aims at several design challenges including system power reduction, system miniaturization and wireless wake-up method. These challenges are met by deploying optimized system architecture, integration of an area and power efficient image compression module, a power management unit (PMU) and a novel wireless wake-up subsystem with zero standby current. The ASIC has been fabricated in 0.18-*μ*m CMOS technology. The achieved performance will be demonstrated with corresponding measurement results. The wireless capsule endoscope prototype base on the ASIC is under development and the demo system will be brought forth soon.

11-4 14:35-15:00

A Closed-Loop Power Control Function for Bio-Implantable Devices

Kouji Kiyoyama[1], Yoshito Tanaka[2], Mashahiro Onoda[3], Takafumi Fukushima[1], Tetsu Tanaka[1] and Mitsumasa Koyanagi[1]
1) Tohoku University, Japan
2) Nagasaki Institute of Applied Science, Japan
3) Terumo Corporation, Japan

Abstract— A wireless communication system with a closed-loop power control function for bio-implantable applications is described which keeps the power dissipation of implantable unit at the allowable level for human body. The function is controlled by monitoring an excessive current at the implantable unit and limiting the power transmission at the external interrogator unit. The implantable unit with the closed-loop power control function has been fabricated in a standard 0.18μm CMOS technology, achieved less than 530μW with a 1.8V and the chip core size of 0.14mm^2. The system uses inductive coupling at 13.56MHz with internal and external coils. Experimental results confirm its stable power supply to the implantable unit over a coil distance of 0.5 to 10mm.

11-5 15:00-15:12

A Two-Electrode 2.88nJ/Sample Biopotential Acquisition System for Portable Healthcare Device

Long Yan, Namjun Cho, Jerald Yoo, Binhee Kim and Hoi-Jun Yoo
KAIST, Korea

Abstract- A 2.88nJ/sample low energy biopotential acquisition system is designed for portable healthcare device. Two conductive pasteless copper electrodes with 1.2-cm diameter are used to easily interface between skin and healthcare device. Chopping technique is adopted at readout front end to obtain thermal noise floor of 1.3uVrms over 0.5~200Hz and 4-stage gain control and band selection blocks to digitally calibrate for different types of biomedical signal. An 8-bit synchronous successive approximation register (SAR) A/D is integrated to digitize biomedical signal. A test chip was implemented in 0.18um, 1.8V supply CMOS technology and successively verified by readout ECG signal with two copper contact electrodes of separating 6cm.

11-6 15:12-15:24

A CMOS Detector System for Fluorescent Bio-Sensing Application

Nan Liu, Zhiliang Hong and Ran Liu
Fudan University, China

Abstract: This system integrates CMOS compatible photodiodes, a low noise capacitive trans-impedance amplifier (CTIA) pixel circuit and a 12-bit pipelined analog-to-digital converter (ADC). The chip fabricated in a 0.18-μm standard CMOS technology occupies 1.21 mm^2 and consumes 45 mW. The photodiode (Nwell/Psub photodiode) used in the fluorescence detecting experiment has a sensitivity of 0.1 A/W at 515 nm and a dark current of 3 nA/cm^2 with reverse biased voltage of 300 mV. The maximum differential and integral nonlinearity of the designed ADC are 0.8 LSB and 3 LSB, respectively. This chip is capable of detecting fluorescence with intensity of 15 nW/cm^2 at room temperature.

Session 12 : RF Transceiver Circuits

Time: 13:20-15:25
Room: Arogs F

Co-Chairs: Kang-Yoon Lee (Konkuk University)
Ryangsu Kim (Panasonic)

12-1 13:20-13:45

A World-Band Triple-Mode 802.11a/b/g SOC in 0.13um CMOS

Chia-Hsin Wu, Yuan-Hung Chung, Anson Lin, Wei-Kai Hong, Jie-Wei Lai, Cheng-Yu Wang, Chih-Hsien Shen, Yu-Hsin Lin, Yi-Hsien Cho, Yang-Chuan Chen
MediaTek Inc., Taiwan

Abstract- A world-band triple-mode SOC compliant with 802.11a/b/g is realized in 0.13μm CMOS technology. This SOC features multiple integrated capless LDOs to be compatible with DC/DC supply for low current consumption and minimizing external BOMs. With supplying by a DC/DC converter, the measured 2.4GHz/5GHz sensitivity is -77.5dBm/-74dBm at 54Mbps, and TX 2.4GHz/5GHz 54Mbps EVM is -32dB/-30dB at an output power of -7dBm/-8dBm. This SOC consumes 71mA/83mA at RX mode and 56mA/74mA at TX mode at 2.4GHz/5GHz band respectively.

12-2 13:45-14:10

A 52 pJ/bit OOK Transmitter with Adaptable Data Rate

M.Kumarasamy Raja and Yong Ping Xu
National University of Singapore, Singapore

Abstract- A 433-MHz OOK transmitter with adaptable data rate is presented. The proposed circuit completely turns off the transmitter during the transmission of '0' and employs a speed-up scheme to obtain high data rates and low wake up time. The data rate can be adjusted and adapted to the need of applications. Realized in a 0.35-μm CMOS technology, the OOK transmitter has a measured output power of -12.7dBm with a dc power consumption of 560 μW under a 1-V power supply, and a data rate of 3 Mb/s, yielding an energy efficiency of 187 pJ/bit or 3.48 nJ/bit/mW if normalized to the transmitting power. When the proposed speed-up circuitry is enabled, data rate increases to 10 Mb/s, with a dc power consumption of 518 μW achieving an energy efficiency of 52 pJ/bit or 0.97 nJ/bit/mW when normalized.

12-3 14:10-14:35

A 1.2V Interference-Sturdiness, DC-Offset Calibrated CMOS Receiver Utilizing a Current-Mode Filter for UWB

Horng-Yuan Shih[1], Wei-Hsien Chen[2], Kai-Chenug Juang[2], Tzu-Yi Yang[2], Chien-Nan Kuo[1]
1) National Chiao-Tung University, Taiwan
2) Industrial Technology Research Institute, Taiwan

Abstract—An interference-sturdiness receiver with a currentmode filter for 3-5GHz UWB applications is implemented in a 1.2V 0.13μm CMOS process. The chip provides a maximum voltage gain of 70dB and a dynamic range of 60dB. The measured in-band OIP3 is +9.39dBm, out-of-band IIP3 -15dBm and noise figure 6.8dB in the maximum gain mode. An algorithm for the automatic digital DC offset calibration is also demonstrated.

12-4 14:35-15:00

A Programmable-Bandwidth Front-End with Clock-Interleaving Down-Conversion Filters

Ming-Feng Huang, and Lai-Fu Chen
Industrial Technology Research Institute, Taiwan

Abstract—Integration of a programmable-bandwidth frontend (PBFE) based on clock-interleaving down-conversion filter (CIDCF) is presented. After demonstration, PBFE has a programmable bandwidth from 1-MHz to 110-MHz. Under 6.14- mA power current (excluding output buffer) and 1.2-V power supply, PBFE gets +8.2-dBm IIP_3, +45-dBm IIP_2, and 2.6-dB gain. Moreover, a better than 30.59-dB alias-band rejection and 34.032-dB image rejection ratio are obtained. Using a 64- QAM signal with 54-MS/s for IEEE 802.11g standard, PBFE achieves -26.351-dB EVM on a 2.412-GHz RF frequency, 1.072-GHz LO frequency, and 1072-MS/s sampling frequency.

12-5 15:00-15:12

A 1.8-V CMOS Direct-Conversion Tuner for Mobile DTV Applications

Fei Song, Huailin Liao, Jiang Chen, Le Ye, Huaizhou Yang, Junhua Liu, Jinshu Zhao, Ru Huang
Peking University, China

Abstract -A 1.8-V 0.18μm CMOS direct-conversion Tuner for UHF band mobile digital TV applications is presented. To meet the stringent requirements of Noise Figure (NF) and IIP3, a capacitor cross-coupled (CCC) common-gate LNA and a novel high-linearity, low-flicker noise Gilbert Mixer are adopted. The LNA achieves 26dB variable gain by using digital controlled current-steering technique and a resistive attenuator. To overcome the gain roll-off at the high frequency channels, a current reuse self-biased post-LNA buffer is proposed as the interface between the VGLNA and Mixer. In addition, a fully integrated DC Offset Correction (DCOC) circuit with switchable high-pass corner frequency, is introduced to realize both low high-pass cutoff frequency and short settling time. A wideband integer-N synthesizer using an adaptive frequency calibration (AFC) of dichotomizing technique, settles less than 200μs for LO generation. The tuner achieves 3.8dB NF, 0dBm IIP3@20dB LNA gain attenuation, 92dB gain dynamic range and occupies 3.45mm× 3.4mm silicon area, while drawing 59mA from 1.8-V voltage supply.

12-6 15:12-15:24

1-Gb/s Mixed-Mode BPSK Demodulator Using a Half-Rate Linear Phase Detector for 60-GHz Wireless PAN Applications

Kwang-Chun Choi, Duho Kim, Minsu Ko and Woo-Young Choi
Yonsei University, Korea

Abstract- A mixed-mode high-speed binary phase-shift keying (BPSK) demodulator for IEEE802.15.3c mm-wave wireless personal area network (WPAN) application is realized with 0.18μm CMOS process. The demodulator core consumes 23.4 mW from 1.8 V power supply while the chip area is 165 × 110 μm^2. The power-consumption is less than that of the conventional BPSK demodulators and the chip-size is smaller. The proposed circuit is verified by 1-meter 60-GHz wireless link tests with 1-Gb/s data.

Session 13 : Sigma-Delta and Flash Data Converters

Time: 15:45-18:15
Room: Navis C

Co-Chairs: Hung S. Li (Mediatek)
Sanroku Tsukamoto (Fujitsu Laboratories)

13-1 15:45-16:10

A 2.4GHz 40mW 40dB SNDR/62dB SFDR 60MHz Bandwidth Mirrored-Image RF Bandpass ΣΔ ADC in 90nm CMOS

Julien Ryckaert[1], Jonathan Borremans[1,2], Bob Verbruggen[1,2], Joris Van Driessche[1], Liesbet Van der Perre[1], Jan Craninckx[1] and Geert Van der Plas[1]
1) IMEC, Belgium
2) Vrije Universiteit Brussel, Belgium

Abstract—A 6th order RF bandpass ΣΔ ADC operating on the 2.4GHz ISM band is presented. The bandpass loop filter is based on digitally programmable Gm-LC resonators. By using a mirrored-image sampling technique, the clock frequency is reduced to 3GS/s, thereby reducing the power consumption. Implemented in a standard 90nm CMOS process, the IC achieves 40dB and 62dB of SNDR and SFDR respectively on a 60MHz bandwidth with 40mW of power consumption.

13-2 16:10-16:35

A 350-MHz Combined TDC-DTC with 61 ps Resolution for Asynchronous ΔΣ ADC Applications

Jorg Daniels[1], Wim Dehaene[1], Michiel Steyaert[1], Andreas Wiesbauer[2]
1) Katholieke Universiteit Leuven, ESAT-MICAS, Belgium
2) Infineon Technologies AG, Austria

Abstract—A combined Time-to-Digital Digital-to-Time Converter (TDC-DTC) is presented for use in a high-precision single-bit Asynchronous ΔΣ ADC. It quantizes the 1-bit asynchronous square wave with 61 ps precision, obtaining a virtual sampling frequency of 16.4 GHz with only a 350 MHz clock. Measurements confirm that with this precision, the design of a single-bit Asynchronous ΔΣ ADC obtaining 78 dB SNDR over a 500 kHz bandwidth is feasible using only a first-order noise shaping and with a limit cycle frequency of only 8 MHz. With this technique, both the order and the bandwidth requirements of the noise shaping filter can be relaxed, which significantly reduces the analog complexity of the ΔΣ Modulator. The proposed architecture is therefore especially suited for low-voltage nanometer technologies.

13-3 16:35-17:00

A Continuous Time ΔΣ ADC with Clock Timing Calibration

Jen-Che Tsai, Jhy-Rong Chen, Kang-Wei Hsueh, and Mu-Jung Chen
MediaTek Inc., Taiwan

Abstract- A 3-order multi-bit continuous-time delta-sigma ADC with clock timing calibration circuit is presented. The clock timing calibration circuit is proposed to ensure the stability of the continuous-time delta-sigma ADC and relax the bandwidth requirement of the adder for excess loop delay compensation. The ADC has been designed and fabricated in a 0.13um CMOS process. The ADC achieves 75dB dynamic range and 69dB peak signal-to-noise ratio (SNR) at 1MHz signal bandwidth and 64MHz sampling rate while dissipating 2.2mW from 1.2V supply.

13-4 17:00-17:25

A 6b Stochastic Flash Analog-to-Digital Converter without Calibration or Reference Ladder

Skyler Weaver[1], Benjamin Hershberg[1], Daniel Knierim[2], and Un-Ku Moon[1]
1) Oregon State University, USA
2) Tektronix, Inc., USA.

Abstract—A 6-bit stochastic flash ADC is presented. By connecting many comparators in parallel, a reference ladder is avoided by allowing random offset to set individual trip points. The ADC transfer function is the cumulative density function of comparator offset. A technique is proposed to improve transfer function linearity by 8.5 dB. A test chip, fabricated in 0.18μm CMOS, achieves ENOB over 4.9b up to 18MS/s with 900mV supply and comparator offset standard deviation of 140mV. Comparators are digital cells to allow automated synthesis. Total core power consumption when f_S = 8 MHz is 631μW.

13-5 17:25-17:50

A 4-bit 10GSample/sec Flash ADC with Merged Interpolation and Reference Voltage

I-Hsin Wang, and Shen-Iuan Liu
National Taiwan University, Taiwan

Abstract—A four-bit 10GSample/sec flash analog-to-digital converter (ADC) with merged interpolation and reference voltage is presented. In this flash ADC, two clock-gated interpolation amplifiers are adopted and the number of resistor strings is reduced. An on-chip phase-locked loop is integrated to double sample the input signal and down sample the converted digital outputs, respectively. Furthermore, a digital-to-analog converter is embedded for the sake of measurements. This chip has been fabricated in 0.13um CMOS process and the ADC's power consumption is 115mW for a 1.2V supply voltage. This ADC achieves the SNDR of 25dB, INL of ±0.25LSB, and DNL of ±0.5LSB.

13-6 17:50-18:02

A 6-bit, 1.2-GS/s ADC with Wideband THA in 0.13-μm CMOS

Bo-Wei Chen, Szu-Kang Hsien, Cheng-Shiang Chiang and Kai-Cheung Juang
Industrial Technology Research Institute, Taiwan

Abstract-This paper presents a 6-bit, 1.2-GSample/s flash ADC with new proposed wideband track-and-hold amplifier (THA) fabricated in TSMC 0.13-μm CMOS process. The wideband THA employed a super source follower (SSF), which has a very low input capacitance of only 0.2-pf, to boost analog bandwidth without any passive inductor. Also the flatness of the data bandwidth of ADC will improve. Moreover, the SSF can relax the power consumption of the voltage buffer in the THA. Operating at 1.2-GS/s, the ADC achieves an effective resolution bandwidth (ERBW) of 600-MHz, and 5.12 effective bits of 500-MHz input frequency. The peak DNL and INL are measured as 0.33-LSB and 0.55-LSB, respectively. At 1.6-GS/s it achieves 5.05 effective bits for 300-MHz input frequency. This ADC consumes only 75-mW with internal references at 1.2-V supply. This corresponds to outstanding figure-of-merit (FoM) of 2.17-pJ/convstep. The test chip occupies 0.43-mm^2 active area.

13-7 18:02-18:14

A 2-GS/s 6-bit Flash ADC with Offset Calibration

Ying-Zu Lin, Cheng-Wu Lin and Soon-Jyh Chang
National Cheng-Kung University, Taiwan

Abstract-A 6-bit flash analog-to-digital converter (ADC) with a digital offset calibration scheme is fabricated in a 0.13-μm CMOS process. Adjusting the programmable loading devices of the preamplifiers enhances the linearity of the proposed ADC. To reduce power consumption, the utilized current-mode flip-flops change their operation mode depending on the sampling rate. A simple detector composed of an inverter and a diode-connected transistor senses the clock rate. This ADC consumes 170 mW from a 1.2-V supply in high-speed mode. The maximum operation speed of this ADC achieves 3.4 GS/s when the input frequency is low. When operating at 2 GS/s, its ENOB is 5.11 bit and ERBW is 650 MHz. The proposed ADC achieves an FOM of 3.79 pJ/conversion-step at 2 GS/s.

Session 14 : Measurement & Characterization of Digital Circuits

Time: 15:45-17:49
Room: Navis B

Co-Chairs: Makoto Ikeda (University of Tokyo)
Vasantha Erraguntla (Intel Technology India)

14-1 15:45-16:10

A MOS Transistor Array with Pico-Ampere Order Precision for Accurate Characterization of Leakage Current Variation

Takashi Sato, Hiroyuki Ueyama, Noriaki Nakayama, and Kazuya Masu
Tokyo Institute of Technology, Japan

Abstract—Transistor array design for accurate sub-threshold current measurement is proposed. The proposed array achieves both compact layout area and pico-ampere order precision, which is particularly useful in off-state current variation characterization. The effect of masking current caused by the transistors that share the same measurement PAD is carefully eliminated using leakage cut-off switches and potential equalizing supply. Experimental array design consisting of 1023 low threshold voltage devices demonstrated accurate measurement of subthreshold leakage current with precision of 10-pA.

14-2 16:10-16:35

An All-Digital, Highly Scalable Architecture for Measurement of Spatial Variation in Digital Circuits

Nigel Drego, Anantha Chandrakasan, and Duane Boning
Massachusetts Institute of Technology, USA

Abstract—Increased variation in CMOS processes due to scaling results in greater reliance on accurate variation models in developing circuit methods to mitigate variation. This paper investigates specific variation parameters and their measurement approach for use in such models, leading to critical considerations in aggressive voltage scaling systems. We describe a test-chip in 90nm CMOS containing all-digital measurement circuits capable of extracting accurate variation data. Specifically, we use replicated 64-bit Kogge-Stone adders, ring-oscillators (ROs) of varying gate type and stage length and an all-digital, sub-picosecond resolution delay measurement circuit to provide spatial variation data for digital circuits. Measurement data from the test-chips indicate that 1) relative variation is significantly larger in low-voltage domains, 2) within-die variation is primarily random and spatially uncorrelated and 3) die-to-die (or global) variation is strongly correlated, but degrades toward random as the power-supply voltage is lowered.

14-3 16:35-17:00

Measurement of Supply Noise Suppression by Substrate and Deep N-well in 90nm Process

Yasuhiro Ogasahara[1,3], Masanori Hashimoto[1], Toshiki Kanamoto[2], and Takao Onoye[1]
1) Osaka University, Japan
2) Renesas Technology Corp., Itami 664-0005, Japan
3) Renesas Technology Corp., Japan

Abstract—This paper measures and compares power supply and ground noises in a triple-well structure and a twin-well stricture. The measurement results of power supply and ground waveforms in a 90nm CMOS process reveal that the power noise reduction thanks to the increased junction capacitance associated with the triple-well structure overwhelms the ground noise supression due to the resistive network of p-substrate in the twinwell structure. These noise suppression effects are well correlated with the simulation that uses on-chip RC power distribution model with package inductance, chip-level p-substrate resistive mesh and distributed well junction capacitance.

14-4 17:00-17:25

On-Chip Clock Network Skew Measurement using Sub-Sampling

Pratap Kumar Das[1], Bharadwaj Amrutur[1], J. Sridhar[2], V. Visvanathan[2]
1) Indian Institute of Science, India
2) Texas Instruments, India

Abstract—We present a technique for an all-digital on-chip delay measurement system to measure the skews in a clock distribution network. It uses the principle of sub-sampling. Measurements from a prototype fabricated in a 65 nm industrial process, indicate the ability to measure delays with a resolution of 0.5ps and a DNL of 1.2 ps.

14-5 17:25-17:37

On-chip Digital I_{dn} and I_{dp} Measurement by 65 nm CMOS Speed Monitor Circuit

H. Notani[1], M. Fujii[1], H. Suzuki[1], H. Makino[2], and H. Shinohara[1]
1) Renesas Technology Corporation, Japan
2) Osaka Institute of Technology, Japan

Abstract- An on-chip digital I_{ds} measurement method is proposed in this report. In the proposed method, I_{ds} is digitally derived from the two values measured by three ring oscillators with PN balanced, N-rich, and P-rich inverters. The first value is the frequency of the PN balanced inverter ring. The second value is the frequency difference between the N-rich and the P-rich inverter rings. The post-digital processing derives NMOS I_{ds} (I_{dn}) and PMOS I_{ds} (I_{dp}) separately. The monitor circuit was designed with 65 nm CMOS technology. The mismatch error of I_{ds}, as calculated from simulated frequencies using the proposed method, is ca. 2%.

14-6 17:37-17:49

Transient-to-Digital Converter for ESD Protection Design in Microelectronic Systems

Ming-Dou Ker[1], Cheng-Cheng Yen[1], Chi-Sheng Liao[1], Tung-Yang Chen[2], and Chih-Chung Tsai[2]
1) National Chiao-Tung University, Taiwan
2) Himax Technologies, Inc., Taiwan

Abstract - An on-chip transient-to-digital converter for system-level electrostatic discharge (ESD) protection is proposed. The proposed transient-to-digital converter is designed to detect fast electrical transients during the system-level ESD events. The output digital thermometer codes can correspond to different ESD voltages under system-level ESD tests. The experimental results in a 0.18-μm CMOS integrated circuit (IC) with 3.3-V devices have confirmed the detection function and digital output codes.

Session 15 : Clock Generation Circuits

Time: 15:45-18:15
Room: Navis A

Co-Chairs: Srikanth Gondi (K-Micro America)
Koichiro Mashiko (Renesas Technology)

15-1 15:45-16:10

A 57.1-59GHz CMOS Fractional-N Frequency Synthesizer Using Quantization Noise Shifting Technique

Chao-Ching Hung, Chihun Lee, Lan-Chou Cho, and Shen-Iuan Liu
National Taiwan University, Taiwan

ABSTRACT- In this paper, a 57.1-59GHz fractional-N frequency synthesizer has been fabricated in 90nm CMOS technology. A magnetic-coupled VCO achieves the high oscillation frequency and low phase noise. A harmonic-locked PD and a multi-modulus prescaler are adopted to double the sampling frequency of a second-order delta-sigma modulator. Theoretically, the quantization noise is improved by 12dB with the same PLL bandwidth. It consumes 89mW from a 1.2V analog supply with output buffers and 16mW from a 1.2V digital supply. The chip occupies 0.86×1.28mm^2 and the measured phase noise at 58.359375GHz with the offset frequency of 1MHz is -95.1dBc/Hz.

15-2 16:10-16:35

A Hybrid Spur Compensation Technique for Finite-Modulo Fractional-*N* Phase-Locked Loops

Li Zhang[1], Xueyi Yu[1], Yuanfeng Sun[1], Woogeun Rhee[1], Zhihua Wang[1], Hongyi Chen[1], Dawn Wang[2]
1) Tsinghua University, China
2) IBM, USA

Abstract—A finite-modulo fractional-*N* PLL utilizing a 4-bit high-order ΔΣ modulator performs deterministic 16-modulo fractional-*N* operation with less spur generation and negligible quantization noise. Further spur reduction is achieved by charge compensation in the voltage domain (coarse compensation) and phase interpolation in the time domain (fine compensation). A 1.8 – 2.6GHz fractional-*N* PLL with 4-bit 4th-order deterministic ΔΣ modulation is implemented in 0.18μm CMOS. The prototype PLL consumes 35.3mW in which only 2.7mW is consumed by the digital modulator and compensation circuits.

15-3 16:35-17:00

A Wide-Range All-Digital Multiphase DLL with Supply Noise Tolerance

Hyunsoo Chae[1], Dongsuk Shin[2], Kisoo Kim[1], Kwan-Weon Kim[2], Young Jung Choi[2], Chulwoo Kim[1]
1) Korea University, Korea
2) Hynix Semiconductor, Korea

Abstract- An 80-to-832MHz all-digital 8-differential-phase DLL in a 0.18um CMOS process has been developed to achieve low-jitter and supply noise tolerance using dual window phase detector, noise tolerant delay cell and delay compensation under supply noise. The proposed DLL occupies 0.19mm^2 and dissipates 48mW at 832MHz from a 1.8V supply. The peak-to-peak jitter and rms jitter are 12ps and 1.73ps with a quiet supply at 832MHz, respectively. The peak-to-peak and rms jitter with a 100mV peak-to-peak triangular supply noise at 100MHz are 21ps and 2.99ps, respectively.

15-4 17:00-17:25

A Low-Jitter Clock Generator based on Ring Oscillator with 1/f Noise Reduction Technique for Next-Generation Mobile Wireless Terminals

Akihide Sai, Takafumi Yamaji, Tetsuro Itakura
Toshiba Corporation, Japan

Abstract- Sampling clock jitter degrades the dynamic range of an analog-to-digital converter (ADC). This paper describes a low jitter clock generator for next-generation mobile wireless terminals. The clock generator employs a novel slew rate balancing (SRB) circuit in a single-ended ring oscillator based VCO to suppress the VCO phase noise due to up-converted 1/f noise. The proposed clock generator is fabricated in a 90-nm CMOS technology. The measured results show that the SRB circuit reduces the VCO phase noise by 3-5 dB at the offset frequencies where the up-converted 1/f noise dominates. The clock generator achieves 3.0 ps rms integrated jitter. Required chip area is 0.18 mm^2 and the power consumption is 9 mW.

15-5 17:25-17:37

20Gb/s 1/4-Rate and 40Gb/s 1/8-Rate Burst-Mode CDR Circuits in 0.13μm CMOS

Hong-Lin Chu, Chang-Lin Hsieh, and Shen-Iuan Liu
National Taiwan University, Taiwan

Abstract- In this paper, 20Gb/s 1/4-rate and 40Gb/s 1/8-rate burst-mode clock and data recovery (BMCDR) circuits are presented. The proposed inductorless gated digitally-controlled oscillator using a digitally frequency calibration loop is presented. These two BMCDR circuits have been fabricated in 0.13μm CMOS technology. For a PRBS of 2^7-1, the measured peak-topeak jitter of the recovered clock for the 20Gb/s 1/4-rate and 40Gb/s 1/8-rate BMCDR circuits is 23.8ps and 51ps, respectively.

15-6 17:37-17:49

A Transistor-Based Background Self-Calibration for Reducing PVT Sensitivity with a Design Example of an Adaptive Bandwidth PLL

Seung-Jin Park, Yunjae Suh, Hyunsoo Ha, Hong-June Park, and Jae-Yoon Sim
Pohang University of Science and Technology(POSTECH), Korea

Abstract-A transistor-based background on-chip self-calibration technique is proposed to obtain PVT-independent circuit parameters. With little implementation complexity, the proposed direct I-V calibration of performance determining transistors efficiently achieves stable operation of precision circuits. As an example application to a design of a PLL, the calibration scheme adjusts critical parameters such as VCO gain and charge-pump current to achieve adaptive bandwidth characteristics. The PLL, implemented in a 0.18μm CMOS, shows a wide lock-range of 10Mhz-1Ghz with the rms jitter of 5.7ps at 1Ghz.

15-7 17:49-18:01

An 833-MHz 132-Phase Multiphase Clock Generator with Self-Calibration Circuits

Shih-Chun Lin and Tai-Cheng Lee
National Taiwan University, Taiwan

Abstract—An 833-MHz 132-phase clock generator with self-calibrated circuits is presented. Two delay-locked loops (DLLs) are used to produce phases efficiently because the number of output phase is the product of the stage numbers of the two DLLs. A DLL calibration algorithm which uses the sequential comparison method is also proposed. Only one charge pump and one phase detector are needed in calibration circuits and all output signals go through the same path. Consequently, the effect of the mismatch of the devices can be avoided and the mismatch of the path can be eliminated. This multiphase clock generator with self-calibration circuits have been fabricated in a 0.13-μm CMOS technology, while dissipating 67.2 mW from a single 1.2-V power supply.

15-8 18:01-18:13

A Multi-Band Delay-Locked Loop with Fast-Locked and Jitter-Bounded Features

Chien-Hung Kuo, Meng-Feng Lin, and Chien-Hung Chen
National Taiwan Normal University, Taiwan

Abstract-In this paper, a multi-band delay-locked loop with fastlocked and jitter-bounded features is presented. A programmable charging voltage circuit to the loop filter is developed to accelerate the locking of DLL. The shortest lock time of the proposed DLL is six clock cycles from unlock state. In the presented DLL, two phase-frequency detectors with a tunable delay cell are used to reduce the output clock jitter. A new DLLbased frequency multiplier with less active devices is also proposed to promote the operating frequency range from 200 MHz to 2 GHz. The presented DLL is implemented in a 0.18 μm 1P6M CMOS process. The core area excluding PADs is 0.34× 0.41 mm^2. The power consumption of the presented DLL is 31.5 mW at a 1.8 V of supply voltage.

Session 16 : RF Amplifiers and VCOs

Time: 15:45-18:15
Room: Argos F

Co-Chairs: Minoru Fujishima (University of Tokyo)
Hyunchol Shin (Kwangwoon University)

16-1 15:45-16:10

A 2.4-GHz CMOS Resistively Degenerated Differential Amplifier Linearized Using Source Coupled Auxiliary FET Pair

Jongsik Kim[1], Sangwon Han[1], Tae Wook Kim[2], Bo-Eun Kim[3], and Hyunchol Shin[1]
1) Kwangwoon University, Korea
2) Yonsei University, Korea
3) Integrant technologies Inc., Korea

Abstract—A resistively degenerated differential amplifier is linearized by using a source-coupled auxiliary FET pair. The structure does not lower the effective g_3 of the degenerated auxiliary FET pair while it efficiently cancels the second harmonic feedback component. Realized in 0.18-μm CMOS, the proposed differential amplifier achieves 9.8 dB of power gain, +7.7 dBm of output P_{1dB}, and +25.8 dBm of peak OIP3. The maximum output power level with OIP3 greater than +20 dBm is extended by 7 ~ 10 dB compared to the conventional structure adopting a source-decoupled auxiliary FET pair. The results prove that the proposed degeneration configuration is suitable for linearizing a resistively degenerated CMOS differential amplifier.

16-2 16:10-16:35

A Band-Reject ir-UWB LNA with 20 dB WLAN Suppression in 0.13 *μm* CMOS

Sumit Bagga[1], Zoubir Irahhauten[1], Wouter A Serdijn[1], John R Long[1], Hans Pflug[2] and John J Pekarik[3]
1) Delft University of Technology, The Netherlands
2) IMEC-NL, Holst Centre, The Netherlands
3) IBM Microelectronics, USA

Abstract—Custom designed for the IEEE802.15.4a standard, a 2-stage pseudo-differential low-noise amplifier (LNA) with a notch ≥ 20 dB in the IEEE802.11a WLAN band is presented for impulse-radio ultra-wideband (ir-UWB). This band-reject LNA is power-to-current (PI) configured employing reactive dual-loop negative feedback, which reduces the noise figure and allows for orthogonal impedance and noise matching over the prescribed bandwidth (i.e., 3.25-10.25 GHz). The LNA is fabricated in 0.13 *μm* CMOS and presents a maximum power gain of 17 dB, a -9 dBm IIP3 and a 2.5 dB noise figure at 6 GHz, when matched to 50 Ω (single-ended). Noise figure variation across the pass-band(s) is limited to ≤ 0.75 dB. Employing a current-reuse technique limits the total power consumption to ≤ 15 mW from a 1.2 V supply. The LNA occupies a die area of 1.4x1.2 mm^2.

16-3 16:35-16:47

A Noise-Suppressed Amplifier with a Signal-Nulled Feedback for Wideband Applications

Chin-Fu Li, Shih-Chieh Chou, and Po-Chiun Huang
National Tsing Hua University, Taiwan

Abstract- This paper presents a noise suppression technique that is based on the feedback topology for wideband low-noise amplifiers. By nulling the signal in the noise feedback loop, the noise suppression and the signal performance like gain, input matching and output linearity can be considered independently. The overhead on power dissipation is small since the extra loop has less linearity concern. To demonstrate its feasibility, a shuntfeedback type LNA with the proposed noise suppression loop is implemented. The voltage gain is 14.1dB, noise figure is 4.8dB and the signal bandwidth is 1.3GHz. With a 0.18μm CMOS technology, the current consumption is 1.18mA from a 1.3V supply voltage.

16-4 16:47-16:59

A Wideband CMOS Variable Gain Low Noise Amplifier Based on Single-to-Differential Stage for TV Tuner Application

Kefeng Han[1], Youchun Liao[2], Hao Min[1] and Zhangwen Tang[1]
1) Fudan University, China
2) Ratio Microelectronics Technology Co., Ltd, China

Abstract—A wideband CMOS variable gain low noise amplifier (VGLNA) used for TV tuner is presented. A single-to-differential (S2D) circuit other than an off-chip balun is applied for high gain mode and a resistive attenuator is used for input matching and five steps (6dB per step) attenuation. The performance of S2D, especially the noise factor is analyzed. The chip is implemented in a 0.18-μm 1P6M mixed-signal CMOS process. Measurements show that in 50-860MHz frequency range, the LNA achieves 15dB maximum gain, 31dB variable gain range, a minimum 3.8dB noise figure and 5.5dBm IIP3 at 15dB gain while consumes 6mA from a 1.8V supply.

16-5 16:59-17:24

2GHz CMOS Noise Cancellation VCO

Amit Bansal[1], Chun-Huat Heng[1], Yuan-Jin Zheng[2]
1) National University of Singapore, Singapore
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Abstract— A 2GHz CMOS VCO, employing noise cancellation to eliminate flicker noise up-conversion, has been fabricated in 0.35μm CMOS. An overall phase noise reduction of 10dB has been measured with the proposed technique, and phase noise of -121.6dBc/Hz@500kHz offset has been achieved. The VCO core consumes 2.8mA under 2.4V supply and occupies an area of 0.7mm×0.8mm. The proposed VCO measured FOM of -186 dBc/Hz.

16-6 17:24-17:36

SiGe HBT Quadrature VCO Utilizing Trifilar Transformers

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Abstract —A trifilar-coupling quadrature voltage-controlled oscillator (QVCO) is demonstrated by using 0.35-μm SiGe heterojunction bipolar transistor (HBT) technology. The trifilar transformer consisting of one primary coil and two secondary coils is used in this work to separate the collector and base bias for output voltage swing optimization and also to replace a conventional transistor-coupling method for quadrature output generation, simultaneously. As a result, the trifilar-coupling QVCO achieves the 191.6 dBc/Hz FOM at the supply voltage of 1.2 V. The on-chip passive single side-band (SSB) upconversion mixer is also demonstrated to fairly measure the quadrature accuracy of the QVCO. Thus, the side-band rejection ratio of 37.7 dB is achieved.

16-7 17:36-17:48

A 130M to 1GHz Digitally Tunable RF LC-Tracking Filter for CMOS RF Receivers

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Abstract- A widely tunable RF LC-tracking filter is developed for tackling the odd harmonic mixing problem in wideband CMOS RF receivers. The filter is composed of two cascaded RLC tanks, where proposed programmable transconductor stages with built-in LPF are used. IIP3 of 127.7dBμV and inputreferred noise of 20.1dBμV over signal band of 5.6MHz are confirmed by measurements. The chip, fabricated in 0.18 μm CMOS process, occupies 2.8mm^2 and draws 34-120mA from a 1.8V supply.

16-8 17:48-18:13

A Complex Band-Pass Filter for Low-IF Conversion DAB/T-DMB Tuner with I/Q Mismatch Calibration

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Abstract — This paper provides a complex band-pass filter (BPF) for low-IF conversion digital audio broadcasting (DAB) and terrestrial-digital multimedia broadcasting (T-DMB) tuner with I/Q gain and phase mismatch calibration. This calibration can be implemented in the first stage of complex BPF using feed-through resistor calibration scheme. The automatic tuning circuit with programmable clock is also presented. The measurement results show 1.536 MHz bandwidth with 2.048 MHz IF center frequency and 50 dB stop band attenuation at 0.7 MHz frequency offset. The in-band and out-band 3rd order intermodulation distortion (IMD3) are 55 and 60 dBc, respectively. After I/Q mismatch calibrating, 20 dB image rejection ratio (IRR) improvement is obtained from 38 dB to 58 dB in this work. The automatic tuning circuit guarantees less than +/- 4 % cut-off frequency variation covering the several clock requirements from demodulator ICs. The complex BPF is fabricated in 0.13 μm RF CMOS technology and consumes 9 mA with 1.2 V power supply.