A-SSCC
IEEE Asian Solid-State Circuits Conference

The 5th IEEE Asian Solid-State Circuits Conference

The Grand Hotel, Taipei, Taiwan

November 16-18, 2009

www.a-sscc.org

Preliminary

Advance Program

IEEE SSCS

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Nov. 16	10F Song Bo Room	10F Chang Chin Room	B Fl. Ji-Shang Room	V Fl. West Foyer	V Fl. V108	V Fl. V109	V Fl. West Foyer
09:00-10:20 (80)	**Tutorial 1** **Silicon Microelectronic Chips in the Human Healthcare and Life Sciences** Donhee Ham (Harvard U.)	**Tutorial 2** **Inductive-Coupling Through-Chip Interface for 3D System Integration** Tadahiro Kuroda (Keio U.)			Conference Secretariat Room	Internet Lounge	Registration
10:20-10:40 (20)	**Break**						
10:40-12:00 (80)	**Tutorial 1** **Silicon Microelectronic Chips in the Human Healthcare and Life Sciences** Donhee Ham (Harvard U.)	**Tutorial 2** **Inductive-Coupling Through-Chip Interface for 3D System Integration** Tadahiro Kuroda (Keio U.)					
12:00-13:00 (60)	**Lunch**						
13:00-14:20 (80)	**Tutorial 3** **Emerging ADC design** Un-Ku Moon (Oregon State U.)	**Tutorial 4** **Advanced RF and Analog Design in the Nano-Meter Era** Bram Nauta (Twente U.)					
14:20-14:40 (20)	**Break**						
14:40-16:00 (80)	**Tutorial 3** **Emerging ADC design** Un-Ku Moon (Oregon State U.)	**Tutorial 4** **Advanced RF and Analog Design in the Nano-Meter Era** Bram Nauta (Twente U.)					
16:00-17:30 (90)				**Student Design Contest** (SDC)			
17:30-18:00 (30)							
18:00- 19:30 (90)			**Welcome Reception**				

Nov. 17	10F Auditorium	10F Song Bo Room	10F Chang Chin Room	V Fl. V105	V Fl. V110	V Fl. West Foyer	12F The Grand Ballroom	Conference Secretariat Room V Fl. V108	Internet Lounge V Fl. V109	Registration V Fl. West Foyer
08:30-08:40 (10)	**Opening Ceremony**									
08:40-08:50 (10)	**Welcome Speech by Conference Chair** Ming-Kai Tsai (MediaTek Inc.)									
08:50-09:35 (45)	**Plenary Session 1** **"Green Future: IC Packaging Opportunities Abound"** Ho-Ming Tong (ASE Group)									
09:40-10:25 (45)	**Plenary Session 2** **"Nanoelectronics Devices: More CMOS, Fusion CMOS and Beyond CMOS"** Hisanaru Watanabe (SELET)									
10:25-10:55 (30)			Break			SDC				
10:55-12:35 (120)		**Industry Session 1** **Future Computing Technologies**	**Industry Session 2** **Advances in Wireless and Multimedia**							
12:35-13:35 (60)			Lunch							
13:40-15:45 (125)		**Session 1** **Analog Filters**	**Session 2** **RF Synthesizers**	**Session 3** **Low Power Circuit Techniques**	**Session 4** **Bio and Emerging Applications**					
15:45-16:00 (15)			Break							
16:00-17:40 (100)		**Panel Discussion 1** **Toward Low Voltage (0.5V) Design: Will Challenges Limit Operation?** Sreedhar Natarajan (TSMC)	**Panel Discussion 2** **Gigabit Transceiver: a Panacea or a Poison?** Mehmet Soyuer (IBM)							
17:40-18:10 (30)			Break			SDC				
18:10-18:55 (45)		**Speacial Session** **"All you need to know to write a winning ISSCC paper and give a smashingly good presentation"** Jan Van Der Spiegel (U. of Pennsylvania)								
19:00-21:00 (120)							**Conference Banquet**			

Nov. 18	10F Auditorium	10F Song Bo Room	10F Chang Chin Room	V Fl. V105	V Fl. V110	V Fl. V108	V Fl. V109	V Fl. West Foyer
08:30-09:15 (45)	**Plenary Session 3** **"Weak Inversion for Ultra Low-Power and Very Low-Voltage Circuits"** Eric Vittoz (EPFL)					Conference Secretariat Room	Internet Lounge	Registration
09:15-09:30 (15)	Break							
09:30-11:50 (140)		**Session 5** **Low Power Analog-to-Digital Converts**	**Session 6** **Wireline Communication Circuits**	**Session 7** **Image Signal Processing**	**Session 8** **Memory**			
11:50-12:50 (60)	Lunch							
12:50-14:55 (125)		**Session 9** **Advanced Analog Techniques**	**Session 10** **RF Building Blocks and Phased Array Receivers**	**Session 11** **Low-power System Integration Techniques and Bio-medical DSPs**	**Session 12** **Inductive Link and Clock Generation**			
14:55-15:15 (20)	Break							
15:15-17:20 (125)		**Session 13** **Power Management**	**Session 14** **RF Transcieivers and SoC**	**Session 15** **Digital Communication**				

WELCOME MESSAGE

On behalf of the Conference organizing committees, we cordially invite you to the IEEE Asian Solid-State Circuits Conference 2009 (A-SSCC 2009) in the Grand Hotel Taipei from November 16 to 18, 2009.

The first IEEE Asian Solid-State Circuits Conference took place in Taiwan in 2005, which generated plentiful scientific results and rich discussions. Since then, the conference sprouts and evolves into other Asian communities with China, Korea, and Japan all had success story as the host country with record attendances. Once again, Taiwan will have the honor to host this year's conference. As the 2009 hosting country, we raise to the challenge to ensure that all attendees will be leaving with fruitful and challenged thoughts and are eager to return for future gatherings.

The A-SSCC 2009 is a three-day program consists of plenary talks, panel discussions, and oral presentation sessions. During these sessions, attendees from the circuit community will have the opportunity to gather, discuss, and foster new ideas and observe latest scientific outcomes and future innovation of circuit field. We also formulate various tutorial sessions for attendees to gain in-depth knowledge in advanced solid-state circuit research. We hope these programs will stir intellectual challenges amongst participants and that you will have the opportunity to share insights and experience.

Aside from sharing academic knowledge, we invite you to explore the beauty of Taipei. Not only the Grand Hotel is renowned for its traditional Chineses-Palace architectural design, but also its history and story are legendary. In addition, do not miss the thousands of years' treasures that are hidden under the famed Palace Museum and once the tallest building of the world, Taipei 101. The exploration begins only when you arrive at this year's A-SSCC 2009.

With open arms and warm regards, we look forward to welcoming you to Taipei in November, 2009.

Conference Chair, Ming-Kai Tsai
Chairman of MediaTek Inc., Taiwan

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- **Ali Corporation**
- **Etron Technology, Inc.**
- **Himax Technologies, Inc.**
- **Holtek Semiconductor, Inc.**
- **Industrial Technology Research Institute**
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Wireline and Mixed-Signal Circuits

Chair: Deog-Kyoon Jeong (Seoul National University, Korea)

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Jung-Hoon Chun (SungKyunKwan University, Korea)

Emerging Technologies and Applications

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Hiroyuki Yamauchi (Fukuoka Institute of Technology, Japan)

Bor-Doou Rong (Etron Technology Inc., Taiwan)

CONFERENCE SCOPE

REGULAR SESSIONS

1. Analog Circuits & Systems

Amplifiers, comparators, switch capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; display driver circuits; non-linear analog circuits.

2. Data Converters

Nyquist-rate and oversampling A/D and D/A converters, sub-circuits for data converters including sample-and-hold circuits, calibration circuits.

3. Digital Circuits & Systems

Design, fabrication, and test of digital VLSI systems; High-speed low-power digital circuits, power-reduction and management methods for digital VLSI, leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply /substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.

4. SoC & Signal Processing Systems

System-on-chip, microprocessors, network processors, baseband communication processing system & architectures, low-power signal-processing systems; multimedia processors including video, image, audio and voice processing systems; cryptographic- and security-processing circuits and systems; bio-medical/neural signal processors.

5. RF

Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits (MMDS, 60GHz); circuits and sub-circuits for RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.

6. Wireline & Mixed-Signal Circuits

Receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token-ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers; power-line communication; Clock generation circuits, PLL, DLL, spread-spectrum clock generation.

7. Emerging Technologies and Applications

Advanced circuit technologies and techniques; ultra-low-voltage and sub-threshold logic design; molecular-, organic-, and nano-electronics; flexible substrates and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy sources and energy harvesting; biomedical and ambient-intelligence; emerging wireless applications and circuits; RFID; analog and optical processors, non-transistor-based analog and digital circuits and systems; advanced memory technologies; spintronics; and quantum storage.

8. Memory

Static, dynamic, non-volatile, and read-only memory; magnetic and ferro-electric memory designs and architectures; data storage and multi-bit-cell-based memory designs; embedded memory architectures, cache-memory systems, multi-port memory, and CAM designs, nano-crystal, phase-change, and 3D memories; yield-enhancement redundancy and ECC techniques; and memory testing and built-in self-test.

SPECIAL SESSIONS

1. Industry Program

This special category accepts only papers based on state-of-the-art products. The paper may cover specifications, applications, state-of-the-art points, chip photos, chip architecture/software, circuits (not necessarily very original, significant improvement is fine), live demo if any, characterization results, and packaging/testing results.

2. Student Design Contest

A student design contest is held among the accepted papers with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

REGISTRATION

Registration Hour

The registration desk will be located on the VIP Floor of The Grand Hotel from Monday through Wednesday during the following hours:

Monday	**November 16**	**08:30-18:00**
Tuesday	**November 17**	**08:30-18:10**
Wednesday	**November 18**	**08:30-17:20**

Invited Speakers

All invited speakers (Tutorial Sessions, Plenary Sessions, Panel Discussions, Special Session) are requested to check in at the registration desk, located on the VIP Floor West Foyer of The Grand Hotel.

Session Chair/Co-chair

Session Chair and Co-chair are requested to check-in on November 15th at the registration desk.

Registration Fee (Registration fee must be paid in New Taiwan Dollars)

Category	**Early Registration** (until Sep. 30, 2009)	**Pre-registration** (Oct. 01 - Nov. 09, 2009)	**On-site Registration** (After Nov. 10, 2009)
IEEE Member	NT$14,850 (Around US$450)	NT$18,150 (Around US$550)	NT$18,150 (Around US$550)
Non Member	NT$18,150 (Around US$550)	NT$21,450 (Around US$650)	NT$21,450 (Around US$650)
Student IEEE Member	NT$6,600 (Around US$200)	NT$8,250 (Around US$250)	NT$8,250 (Around US$250)
Student Non Member	NT$8,250 (Around US$250)	NT$9,900 (Around US$300)	NT$9,900 (Around US$300)

Regular fee includes:

- Admittance to the Conference Sessions
- Welcome Reception (November 16)
- Conference Banquet (November 17)
- Proceedings CD-ROM Version
- Coffee Breaks

Student fee includes:

- Admittance to the Conference Sessions
- Welcome Reception (November 16)
- Proceedings CD-ROM Version
- Coffee Breaks

For environmental protection purpose, the A-SSCC 2009 Technical Program Proceedings will only be available in CD-ROM this year, and for those who wish to obtain a copy of Paperback Technical Program Proceedings, please make an advance purchase.

Tutorial Registration Fee (Not Included in Full Program Registration)

Category	One Session	Two Sessions	Daily
Regular	NT$ 3,300 (Around US$100)	NT$ 6,600 (Around US$200)	US$280 (Around NT$9,200)
Student	NT$ 1,650 (Around US$50)	NT$ 3,300 (Around US$100)	US$140 (Around NT$4,620)

Tutorial registration fee includes:

- Admittance to the Tutorial Session
- Tutorial Materials
- Coffee Breaks
- Nov. 16 Lunch is provided for **Daily Tutorial Registrant** only

Additional Purchase

Proceedings of Technical Papers CD-Rom (Extra Purchase)	NT$825 (Around US$25)/copy
Proceedings of Technical Papers Paperback (Advance Purchase Only)	NT$1,155 (Around US$35)/copy
Nov. 17 Banquet Ticket (Not Included in Student and Tutorial Registration Fee)	NT$2,805 (Around US$85)/person

Registration

Participation is open to all people with interest, those who wish to attend the conference may make their registration on-line at the A-SSCC 2009 web site: http://www.a-sscc.org/index-6.html or complete the registration form (available at the A-SSCC 2009 web site) and return it to the Secretariat with payment. The deadline for the early bird registration is **September 30, 2009**, and for regular registration is **November 09, 2009**. After **November 09, 2009**, the registration will be processed at the conference site upon arrival.

Payment of Fee

Registration fees paid by credit card will be converted into New Taiwan Dollars, based on the daily exchange rate (Approx. US$1 : NT$33). Payment can be made by credit card (VISA/MATER/JCB only) or bank transfer (bank service charges should NOT be included in the registration payment).

Please make Telegraph Transfer payable to:

Beneficiary Name: Elite Professional Conference Organizer

Beneficiary Address: 4F, No.158, Jingye 1st Road,104 Taipei, Taiwan

Beneficiary Account: 145-10-022903-3

Beneficiary Bank: Hua Nan Commercial Bank, Chang-An Branch

Bank Address: No.205, Ba Der Road, 104 Taipei, Taiwan

Swift Code: HNBKTWTP 112

Upon receiving the registration form and confirming the payment, the Registration Office will send you a Confirmation e-mail, bearing your registration number. Please bring this confirmation with you and present it at the Registration Counter at the Conference Site.

Cancellation and Refunds

A written notification of cancellation must be sent to the A-SSCC 2009 Conference Secretariat. Written notification of cancellation received on or before September 30, 2007, 25% of registration fee will be deducted from the refund. No refund will be issued for cancellation notified after September 30, 2009. All refunds will be made after the conference.

CONFERENCE INFORMATION

■ **Dates**

November 16 (Monday) – 18 (Wednesday), 2009

■ **Venue**

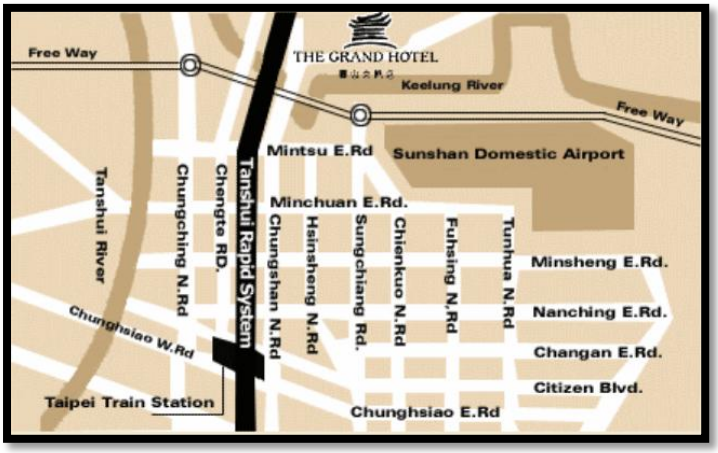
The Grand Hotel, Taipei

1, Chung Shan North Rd., Sec.4, Taipei 104, Taiwan

Tel: 886-2-2886-8888

Fax: 886-2-2885-2885

Website: www.grand-hotel.org



■ **Official Language**

English

■ **Conference Secretariat**

Elite Professional Conference Organizer

Mr. Jun Tsai

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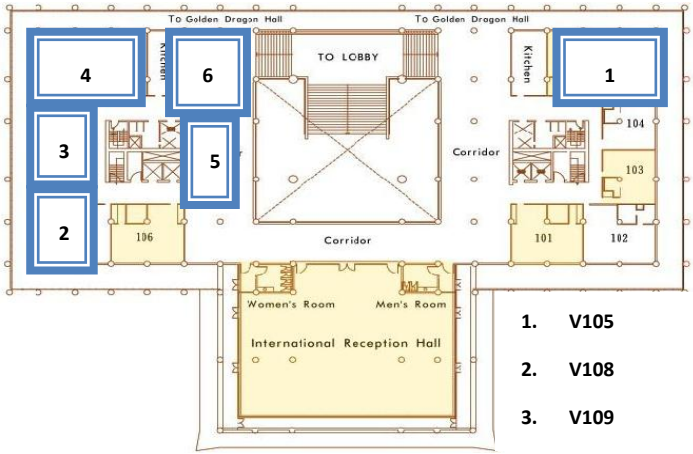
E-mail: asscc2009@elitepco.com.tw

VENUE FLOOR PLAN

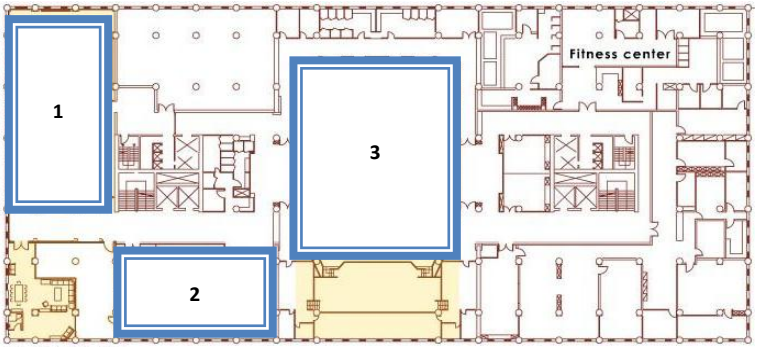
BASEMENT FLOOR

VIP FLOOR



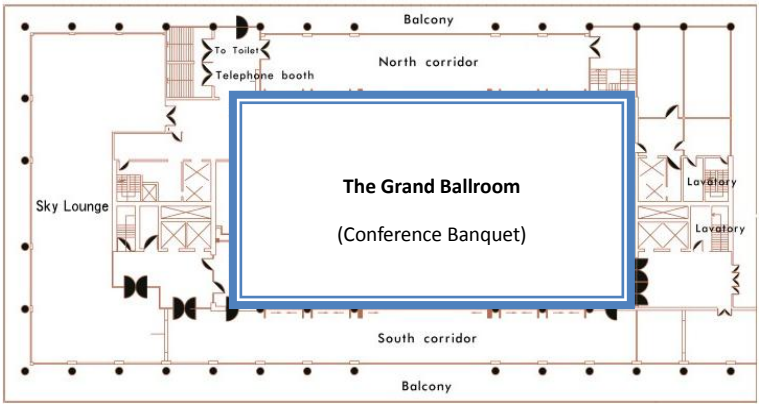
1. **V105** (Oral Sessions)
2. **V108** (Secretariat)
3. **V109** (Internet Lounge)
4. **V110** (Oral Sessions)
5. **West Foyer** (Registration)
6. **West Foyer** (Poster Sessions)

10 FLOOR



1. **Song Bo Room** (Oral Sessions)
   (Panel Discussion)
   (Tutorial Sessions)
   (Special Session)
2. **Chang Chin Room** (Oral Sessions)
   (Panel Discussion)
   (Tutorial Sessions)
3. **Auditorium** (Plenary Sessions)

12 FLOOR



INFORMATION ON TAIWAN

Visa Requirement

Visa is in general required for foreign-passport holders upon entry to Taiwan. However, if your passport and the length of your stay satisfy the following three terms, no visa is required:

- You are holding a passport issued from Australia, Austria, Belgium, Canada, Costa Rica, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Japan, Republic of Korea, Latvia, Liechtenstein, Lithuania, Luxembourg, Malaysia, Malta, Monaco, the Netherlands, New Zealand, Norway, Poland, Portugal, Singapore, Slovakia, Slovenia , Spain, Sweden, Switzerland, U.K. and U.S.A.;
- Your passport is valid for more than 6 months after entry; and
- The length of your stay is less than 30 days.

If you are nationals of the above countries eligible for visa-exempt entry but hold an emergency or temporary passport valid less than six months, you may apply for a Landing Visa at the Taiwan Taoyuan International Airport. A visa can be obtained from Taiwan's embassies, consulates or designated representative offices. Please check with your travel agent for necessary procedures.

For further visa related issues please visit Bureau of Consular Affairs, Ministry of Foreign Affairs, Republic of China (Taiwan) at http://www.boca.gov.tw/ or contact the Conference Secretariat directly.

Climate

November is the winter season in Taiwan with average temperature around 17.6-23.7 ℃.

Time Zone

Taiwan is GMT+8 and does not have seasonal time variation.

Electricity

110 Volts / 60HZ A.C.

Currency and Banks

The currency is the New Taiwan dollar (NT$). The exchange rate in recent months is around NT$32~33 for US$1. Foreign currencies can be exchanged at hotels, airports and government-designated banks. Major credit cards are widely accepted, and traveler's checks may be accepted by tourist-oriented shops and at most international hotels and banks. Banks are generally open from 09:00 to 15:30, Monday to Friday and closed on weekends and public holidays.

TUTORIALS

November 16, 2009 (Monday)

Tutorial 1

Time: 09:00-10:20, 10:40-12:00

Room: 10F Song Bo Room

Chair: Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Co-chair: Makoto Ikeda (University of Tokyo, Japan)

Silicon Microelectronic Chips in the Human Healthcare and Life Sciences

Donhee Ham

Harvard University, USA

Abstract: Silicon CMOS chips that make possible today's computers are emerging as potential new tools for rapid & sensitive electrical analysis of small biological objects (cancer markers, bacteria, virus particles, and DNA) in direct interface with them. A key potential advantage of the interface between CMOS chips and bio systems is low production cost, small size, and rapid analysis. The small, cheap, and fast CMOS bioanalytical devices can contribute to lowering healthcare cost and to facilitating fundamental biology study. In this tutorial, I will review some exciting developments in the burgeoning area of making CMOS-bio interfaces. A large amount of research is being done, and the select review topics cannot be exhaustive, but they would comprise an effective exposure to the field.

Tutorial 2

Time: 09:00-10:20, 10:40-12:00

Room: 10F Chang Chin Room

Chair: Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Co-chair: Makoto Ikeda (University of Tokyo, Japan)

Inductive-Coupling Through-Chip Interface for 3D System Integration

Tadahiro Kuroda

Keio University, Japan

Abstract: When radio communication range is shorter than 1/10 of the wave length, the electromagnetic field exhibits unique characteristics. It is called a near field. By using the near field radio vertical interface through chips can be arranged in as high density as TSV (Through Silicon Via). A wireless TSV that uses inductive coupling is attracting attention. Although it is wireless, it bares comparison with TSV in performance. Data rate per coil is over 10Gb/s. Energy dissipation is below 1pJ/b, which is 1/10 of that in the conventional high-speed serial links. Bit error rate is smaller than 10e-14. Above all, it is much inexpensive, since it is a circuit solution in standard CMOS. Research in industry has started for application study. It can be used for homogeneous and heterogeneous chip stacking for SiP. It enables staking of 64 NAND flash memory chips to realize a package-size SSD (Solid-State Drive). It raises data rate and lowers power dissipation of high-speed DRAM interface. Applications expand by extending communication ranges by enlarging coil size, such as for bus probing of a microcontroller through a package and non-contact wafer testing. Power supply can also be delivered. This lecture will cover technologies and applications of the inductive-coupling through-chip interface.

Tutorial 3

Time: 13:00-14:20, 14:40-16:00

Room: 10F Song Bo Room

Chair: Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Co-chair: Makoto Ikeda (University of Tokyo, Japan)

Emerging ADC design

Un-Ku Moon

Oregon State University, USA

Abstract: Most analog IC designers and students are fascinated by and drawn to ADCs. While some ADC realizations have had a lasting impact, examples including pipelined ADCs with digital redundancy, flash ADCs with folding and interpolation, and multi-bit delta-sigma modulators with dynamic element matching, there are many more recent and emerging ADC design techniques that are receiving much attention and also gaining momentum in some areas. Many of these ideas are showered with doubts and honest criticism. However, we may also be at a juNational Chiao Tung Universityre where a few of these developments may come to the rescue of the tough submicron scaling challenge that we analog IC designers face today. This tutorial will summarize and ponder the impact of a few selective as well as random slices of these emerging ADC designs.

Tutorial 4

Time: 13:00-14:20, 14:40-16:00

Room: 10F Chang Chin Room

Chair: Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Co-chair: Makoto Ikeda (University of Tokyo, Japan)

Advanced RF and Analog Design in the Nano-Meter Era

Bram Nauta

Twente University, Netherlands

Abstract: From a system perspective, wireless transceivers are moving towards software defined architectures. This means that wideband and flexible radio frontends are needed which can receive and transmit many different radio standards. Since there is a large amount of digital circuitry involved, the technology in which these radios have to be designed is nanometer scale CMOS. These technologies are optimized for high density digital circuits and it's quite a challenge to design the software defined architectures and the required circuits in these technologies. In this presentation several analog and RF circuit innovations will be given which take benefit from the properties of nanometer scale CMOS. Topics: Thermal noise cancelling in Balun-LNA-Mixer combination, ultra-linear filtering mixer, Polyphase distortion compensation in a software radio transmitter, A wideband harmonic rejection receiver architecture.

STUDENT DESIGN CONTEST

November 16, 2009 (Monday)

SDC

Time: 16:00-17:30

Room: VIP Floor West Foyer

SDC Chairs: Shyh-Jye Jou (National Chiao Tung University, Taiwan)

Shi-Ho Kim (Chungbuk National University, Korea)

A DVS Embedded Power Management for High Efficiency Integrated SoC in UWB System

Yu-Huei Lee (National Chiao Tung University, Taiwan)

A Micro-Network on Chip with 10-Gb/s Transmission Link

Wei-Chang Liu (National Chiao Tung University, Taiwan)

A 110GHz Inductor-less CMOS Frequency Divider

Seongwoong Lim (University of Tokyo, Japan)

An Inherently Linear Phase-Oversampling Vector Modulator in 90-nCMOS

Richard Tseng (University of Illinois at Urbana-Champaign, USA)

A 9b 100MS/s 1.46mW SAR ADC in 65nm CMOS

Yanfei Chen (Keio University , Japan)

A 45nm 0.5V 8T Column-Interleaved SRAM with on-Chip Reference Selection Loop for Sense-Amplifier

Mahmut Sinangil (Massachusetts Institute of Technology, USA)

A 10Gb/s Inductorless Quarter-Rate Clock and Data Recovery Circuit in 0.13um CMOS

Chang-Lin Hsieh (National Taiwan University, Taiwan)

A 439K Gates/10.9KB SRAM/2-328 mW Dual Mode Video Decoder Supporting Temporal/Spatial Scalable Video

Cheng-An Chien (National Chung Cheng University, Taiwan)

A new low-distortion transconductor applied in a flat band-pass filter

Ha Le-Thai (Korea Advanced Institute of Science and Technology, Korea)

An Extended XY Coil for Noise Reduction in Inductive-Coupling Link

Mitsuko Saito (Keio University, Japan)

Opening Ceremony

Time: 08:30-08:40

Room: 10F Auditorium

Welcome Speech of Conference Chairman

Time: 08:40-08:50

Room: 10F Auditorium

Ming-Kai Tsai

MediaTek Inc., Taiwan

Plenary Session 1

Time: 08:50-09:35

Room: 10F Auditorium

Chair: Tohru Furuyama (Toshiba Corporation)

Co-chair: Mototsugu Hamada (Toshiba Corporation)

Green Future: IC Packaging Opportunities Abound

Ho-Ming Tong

Advanced Semiconductor Engineering Group, Taiwan

Abstract: The “blue” planet we, mankind, and over 8 million other species reside in is quickly turning less “green” as industrialization hastens. Global warming, environmental pollution, shrinking ice caps at the poles, rising sea levels and breakage of the ozone layer are among the more visible consequences caused by accelerated consumption of energy and other natural resources by mankind as its population multiplies. The sixth big extinction seems imminent if nothing drastic and effective is done soon by mankind in a concerted manner. Today, there exists a heightened sense of realization that the world is not an infinite resource and the blue planet we live in is actually the “lonely and only” Noah’s arc that supports life the way we know it in the immense universe. To fulfill its duty as a global green citizen, the semiconductor industry has been implementing WEEE, ROHS, REACH, and more recently the environmental product declaration (EPD) to help make the society and the earth sustainable. While all this is happening, alternative and clean energies, solar and wind included, are also quickly gaining ground in addition to “green” low-power and power management products. Today, as global environmental regulations are tightened, both IC and package technologies are also becoming far more complicated. More Moore and more than Moore, which manifest themselves in system-on-chip (SoC)

and system-in-a-package (SiP), respectively, are being used more in combination to meet the ever-more-stringent cost and time-to-market requirements of consumer products with more functions built in them. In this presentation, I will review the challenges and opportunities to IC packaging subcontractors and related material suppliers as a direct outcome of the above trends to ensure SoC and SiP based IC packages meet the needs of the present generation without compromising the ability of future generations.

Plenary Session 2

Time: 09:40-10:25

Room: 10F Auditorium

Chair: Tohru Furuyama (Toshiba Corporation)

Co-chair: Mototsugu Hamada (Toshiba Corporation)

Nanoelectronics Devices: More CMOS, Fusion CMOS and Beyond CMOS

Hisatsune Watanabe

Semiconductor Leading Edge Technologies, Inc., Japan

Abstract: We are facing several difficulties with shrinking LSI chips, such as leakage currents/power consumption, variability, huge costs in R&D and production. Major semiconductor market will be absolutely dependent on further shrinking of Si CMOS transistors with improving transistor structures and lowering drive voltage, increasing wafer diameter and 3D stacking package structures. This way is More CMOS (More Moore) strategy. On the other hand, the semiconductor market will expand by integrating CMOS with new functional materials, such as RF, MEMS, Bio, or photonics. Novel algorithm implementation to CMOS such as dynamic reconfigurable circuits, multi-value circuits or brain-like circuits is also another way of the market creation. Non-CMOS circuit algorithm is intensively exploited mainly by academic sites. For acceleration of the commercialization of those R&D efforts for More CMOS, Fusion CMOS and Beyond CMOS, we need a new type of integration verification services for R&D people, particularly for university people. This might be a global need in the forthcoming nanoelectronics era.

Industry Session 1 - Future Computing Technologies

Time: 10:55-12:35

Room: 10F Song Bo Room

Chair: Stefan Rusu (Intel)

Co-chair: Shaojun Wei (Tsinghua University)

Industry Session 1-1

Time: 10:55-11:20

A 45nm 8-Core Enterprise Xeon® Processor

Stefan Rusu,

Intel Corporation, USA

Abstract: A 2.3B transistors, 8-core, 16-thread 64-bit Xeon® EX processor with a 24MB shared L3 cache was implemented in a 45nm 9-metal process. Multiple clock and voltage domains are employed to reduce power consumption. Long channel devices and cache sleep mode are used to minimize leakage. Core and cache recovery improve manufacturing yields and enable multiple product flavors using the same silicon die and package. The disabled blocks are both clock and power gated to minimize their power consumption. Idle power is reduced by shutting off the un-terminated I/O links and shedding phases in the voltage regulator to improve the power conversion efficiency.

Industry Session 1-2

Time: 11:20-11:45

A 128Mb ChainFeRAM and System Designs for HDD Application and Enhanced HDD Performance

Daisaburo Takashima, Yasushi Nagadomi, Kosuke Hatsuda, Yohji Watanabe, Shuso Fujii

Toshiba Corporation, Japan

Abstract: This paper demonstrates the hard-disk-drive (HDD) performance improvement by nonvolatile FeRAM cache. First, the 128Mb ChainFeRAM and power system designs to meet HDD application are presented. Second, the concept of nonvolatile FeRAM cache and the simulated and measured HDD performance improvement are presented. The read/write bandwidth improvements to 1.12 times, 3.3 times and 1.9 times have been obtained by bench mark tests of PC Mark 05 and FD Bench v1.01, and by PC user data for 5 days, respectively. These results have been the same level of or more effective than those of HDD rotational speed-up from 5400rpm to 7200rpm.

Industry Session 1-3

Time: 11:45-12:10

Circuits for Silicon Photonics on a "Macrochip"

Ron Ho (Sun Microsystems, USA) Jon Lexau (Sun Microsystems, USA), Frankie Liu (Sun Microsystems, USA), Dinesh Patil (Sun Microsystems, USA), Robert Hopkins (Sun Microsystems, USA), Elad Alon (University of California, Berkeley, USA), Nathaniel Pinckney (Sun Microsystems, USA), Philip Amberg (Sun Microsystems, USA), Xuezhe Zheng (Sun Microsystems, USA), John Cunningham (Sun Microsystems, USA), Ashok Krishnamoorthy (Sun Microsystems, USA)

Abstract: Recent advances in silicon photonics bring significant benefits to “macrochip” grids made of arrayed chips. Such configurations have global interconnects long enough to benefit from the high speed, low energy, and high bandwidth density of optics. In this paper we consider the constraints of large macrochip systems, and explore modulator drivers and photodetector receivers that match those constraints. We show measured results from a recent 90 nm testchip intended to mate with optical components.

Industry Session 1-4

Time: 12:10-12:35

An 8Gb/S/Link, 6.5mW/Gb/S Memory Interface with Bimodal Request Bus

Ken Chang *(Rambus Inc, USA),* Haechang Lee *(Rambus Inc, USA),* Ting Wu *(Rambus Inc, USA),* Kambiz Kaviani *(Rambus Inc, USA),* Kashinath Prabhu *(Rambus Inc, India),* Wendemagegnehu Beyene *(Rambus Inc, USA),* Norman Chan *(Rambus Inc, USA),* Catherine Chen *(Rambus Inc, USA),* Tj Chin *(Rambus Inc, USA),* Chris Madden *(Rambus Inc, USA),* Jie Shen *(Rambus Inc, USA),* Xudong Shi *(Rambus Inc, India)*

Abstract: An 8Gb/s/link power optimized controller memory interface is implemented in TSMC 40nm G CMOS process. It is composed of 32 differential data links to support 32GB/s aggregated payload. The bimodal drivers of the request bus enable support of both 12 bits of 2Gb/s/link single-ended RSL (Rambus Signaling Level) for existing XDR memory and 6 bits of 8Gb/s/link differential signaling for next generation XDR2 memory. A 1-tap pre-emphasis transmitter equalizer and a source-degenerated linear receiver equalizer with offset trim are added on this controller interface to reduce signal swing and thus minimize power in both write and read directions. The measurement results show that with 100mV swing (peak-to-peak single-ended) for the read and 150mV swing for the write, the timing margin is greater than 0.3UI at a BER of 10^12 with real memory transactions. The measured power efficiency for the PHY is 6.5mW/Gb/s.

Industry Session 2 - Advances in Wireless and Multimedia

Time: 10:55-12:35

Room: 10F Chang Chin Room

Chair: Changhyun Kim (Samsung Electronics)

Co-chair: Koji Kai (Panasonic)

Industry Session 2-1

Time: 10:55-11:20

A 90nm CMOS 13.56MHz NFC Transceiver

Steve Morris, Alastair Lefley

Innovision Research & Technology PLC, United Kingdom

Abstract: This paper presents the design of a 90nm 13.56MHz NFC Transceiver. The concept of Near Field Communication is introduced while discussing how a combination of both Initiator and Target functions are required. The Initiator circuitry used to generate the required magnetic field and demodulate the received back-scatter is explained and the passive and active Target circuitry used to receive a magnetic field whilst demodulating and load-modulating is presented. Finally there is a short description of the Evaluation Module (EVM) containing the 90nm NFC, an antenna and interface to a host processor or PC.

Industry Session 2-2

Time: 11:20-11:45

A 1.8dB NF 200mW Sip for 2.6GHz Diversity S-DMB Application

Tea-Shin Kang

FCI, Korea

Abstract: This paper presents a 1.8V 300mW System-In- Package (SiP) solution in mobile S-DMB application. This achieves a 1.8 dB noise figure at 2.6GHz, while the measured sensitivity is -101 dBm at diversity mode. The SiP is integrated RF tuner, demodulator, SDRAM and other passive components. An internal AGC is integrated for over 100dB dynamic range. The SiP is 196 pins LFBGA and the size is 10 mm x 10 mm x 1.3 mm. The SiP consumes 300mW. Index Terms - S-DMB, System-in-Package

Industry Session 2-3

Time: 11:45-12:10

A 658KGates E-Streaming Video Decoder for Digital Home Applications

Chi-Cheng Ju, Kung-Sheng Lin, Tsu-Ming Liu, Yung-Chang Chang, Chih-Ming Wang, Hue-Min Lin, Chia-Yun Cheng, Chun-Chia Chen, Fred Chiu, Ginny Chen, Tc Hsiao, Joe Chen

MediaTek Inc., Taiwan

Abstract: The first reported RealVideo-embedded video decoder is presented The embedded streaming (e-Streaming) video decoder integrates RealVideo, MPEG-2, MPEG-4, H.264, and VC-1 by 658K logic gates and 522Kbits SRAM. In particular, a RealVideo (RV) is fully-reused and is first integrated into our multi-standard video decoder [1]. It explores RV temporal reference method , RV VLD table reduction, multi-stage pipeline and memory management unit to facilitate cost and bandwidth efficiency for digital home and internet services. The test chip is fabricated and the first using 55nm CMOS process which occupies 658KGates/522Kbits SRAM on 1.56x1.56mm2 die and dissipates 195mW in full HD@30fps RV playback.

Session 1 - Analog Filters

Time: 13:40-15:45

Room: 10F Song Bo Room

Chair: Yong Ping Xu (National University of Singapore)

Co-chair: Makoto Nagata (Kobe University)

Session 1-1

Time: 13:40-14:05

A New Low-Distortion Transconductor Applied in a Flat Band-Pass Filter

Ha Le-Thai, Huy Hieu Nguyen, Hoai Nam Nguyen, Jeong Seon Lee, Sang Gug Lee

Korea Advanced Institute of Science and Technology-ICC, Korea

Abstract: A new linearity improvement technique is proposed to implement a low-distortion Gm-C band-pass filter working in high IF ranges. The purpose of the linearization technique is to eliminate " m G value of the transconductor by employing a superposition method that combines two opposite non-linear behaviors of the two parallel wings designed inside the transconductor. Instead of conventional biquad structure, a resonant-coupling structure is adopted for the band-pass filter working at center frequency of 80MHz to make the frequency response flat and stable and to allow a stable frequency tuning as well as a flexible bandwidth tuning. Fabricated in 65nm CMOS process, the implemented IF band-pass filter provides a flat band-pass whose ripple is smaller than 0.1dB, a hird-order rejection of 27dB, an IIP3 of -2dBm, and a NF of 21.5dB, while consuming 11mA from 1.2-V supply. The ilter occupies a chip size of 0.5 mm x 0.5 mm.

Session 1-2

Time: 14:05-14:30

A Discrete-Time AAF with Clock-Efficient Charge-Domain Filter for High Attenuation and Bandwidth

Ming-Feng Huang, Szu-Hsien Wu, Tzu-Yi Yang

Industrial Technology Research Institute, Taiwan

Abstract: A discrete-time (DT) anti-alias filter (AAF) with clock-efficient charge-domain filter (CECDF) for high attenuation and bandwidth was developed. This AAF possesses 88.86-dB attenuation and 13-MHz bandwidth at a 600-MS/s input-clock rate (ICR) and a 100-MS/s output-sample rate. The measured gain and IIP3 are 12.2-dB and 0-dBm, respectively, consuming only 5.56-mA from a 1.36-V power supply. The chip including clock-logical circuits occupies 0.2-mm2 in 90-nm CMOS logical process.

Session 1-3

Time: 14:30-14:55

A 250-MHz gm-C Filter with Discretized Tuning Scheme in 0.18-Um CMOS for UWB Receiver

Muthusamy Kumarasamy Raja, Muthukumara Swamy Annamalai Arasu, Zhao Bin, Henry Kok Fong Ong, Yuan Xiaojun

Institute of Microelectronics, Singapore

Abstract: A low noise, 250-MHz fifth order 0.1 dB ripple chebyshev gm-C filter, with a novel discretized tuning scheme is presented. The discrete tuning circuit switches ON/OFF small gm cells which are connected in parallel to the main gm cell, based on the PVT conditions, to correct for the shift in the cutoff frequency fc. Compared to conventional tuning schemes, proposed discrete scheme demonstrates improved performance in terms of noise and optimal voltage swing across PVT. The chip was fabricated in standard 0.18-ìm CMOS technology. Measured results show a fc of 250 MHz, equivalent input noise voltage of 85 µV, IIP3 of -2.5 dBV in pass band and 2.5 dBV in stop band, Input referred P1dB of -6.6 dBV, IIP2 of 55 dBV, consuming 19 mA from 1.8 V supply. The tuning circuit, in combination with a PTAT bias, maintains the bandwidth within ±5% of nominal fc of 250 MHz for VDD variation of 1.8±0.1V and temperature variation of -40deg C to 85deg C.

Session 1-4

Time: 14:55-15:20

On-Chip Small Capacitor Mismatches Measurement Technique Using Beta-Multiplier-Biased Ring Oscillator

Sai-Weng Sin *(University of Macau, Macau),* He-Gong Wei *(University of Macau, Macau),* U-Fat Chio *(University of Macau, Macau),* Yan Zhu, Seng-Pan U *(University of Macau, Macau),* Rui Paulo Martins *(University of Macau, Macau),* Franco Maloberti *(University of Pavia, Italy)*

Abstract: An on-chip capacitor mismatches measurement technique is proposed. The use of a beta-multiplier-biased ring oscillator improves the measurement sensitivity by over 6 times with respect to the state-of-the art. Experimental results using a 90 nm CMOS and thick-oxide transistors are presented. The method enables the measurement of capacitor with mismatches are as small as sigma=0.04% between capacitances as small as 4.3fF only. The results also demonstrated that better matching can be achieved with low-density capacitors.

Session 1-5

Time: 15:20-15:32

A 1-V 60MHz Bandpass Filter with Quality-Factor Calibration in 65nm CMOS

Tien-Yu Lo, Chuan-Cheng Hsiao, Kang-Wei Hsueh, Hung-Sung Li

MediaTek Inc., Taiwan

Abstract: A 5-th order bandpass filter is implemented in this paper. The filter can perform SAW filter function required in the tuner. In this design, leap-frog synthesis is used and the Active-RC topology is implemented. To save power consumption, the amplifier with a smaller unity gain-bandwidth is designed, and a new quality-factor calibration strategy is presented to compensate the non-ideal effect of the filter. In addition, the accurate center frequency is obtained by adopting a modified frequency tuning scheme. The filter was fabricated in 65nm CMOS process, and consumes 23.5mW under 1-V supply.

Session 1-6

Time: 15:32-15:44

A Gated Ring Oscillator Based Parallel-TDC System with Digital Resolution Enhancement

Kameswaran Vengattaramane, Jonathan Borremans, Michiel Steyaert, Jan Craninckx

IMEC/KUL, Belgium

Abstract: A digital resolution enhancement technique for time-to-digital converters (TDC) is proposed. This involves a simultaneous multi-channel measurement of a time-interval with low-complexity TDCs of varying resolutions. The coarse outputs of each converter are then digitally post-processed to obtain a single result whose precision is much better than that of any individual converter. A prototype system with 8 channels is demonstrated in 90-nm CMOS. 45MS/s output of each channel is algorithmically combined to obtain 2-3X improvement in the resolution in 4/6/8 channel modes. The chip occupies 0.3 mm2 and draws up to a maximum of 4 mA from a 1.2 V supply

Session 2 - RF Synthesizers

Time: 13:40-15:45

Room: 10F Chang Chin Room

Chair: Howard Luong (HKUST)

Co-chair: Toru Masuda (Hitachi)

Session 2-1

Time: 13:40-14:05

A 110GHz Inductor-Less CMOS Frequency Divider

Seongwoong Lim, Wasanthamala Badalawa, Minoru Fujishima

University of Tokyo, Japan

Abstract: An inductor-less 110GHz ring-type frequency divider (RILFD) has been proposed. Body-injection technique has been adopted to achieve high speed and divide-by-three operation. Moreover, body-biasing technique has been also adopted for fine tuning of operation frequency. RILFD was fabricated by a 1P12M 65nm bulk CMOS process. The core size is 10.8*8.5mm2. The locking range is 9.1%, from 100.8 to 110.4GHz, under tuning of the body-bias voltage from -0.2V to 0.4V. The RILFD consumes 4.5mW at the supply voltage of 1V (excluding an output buffer). The output phase noise is -117.6dBc/Hz at 1MHz offset. This work has been achieved the smallest core size among frequency dividers operating over 100GHz reported to date.

Session 2-2

Time: 14:05-14:30

A 5GHz 90-nm CMOS All Digital Phase-Locked Loop

Ping Lu, Henrik Sjoland

Lund University, Sweden

Abstract: An All-Digital Phase-Locked Loop (ADPLL) has been implemented in a 90nm CMOS process. It uses a phase-frequency detector (PFD) connected to two Time-to-Digital Converters (TDC). To save power the TDCs use uneven delay time in the cells of the delay line. An automatic tuning bank controller selects active bank of the Digitally Controlled Oscillator (DCO), which features three separate tuning banks for both high resolution and wide frequency tuning range. To further increase the resolution a high-speed delta-sigma modulator is also used, modulating the DCO fine tuning word. The PLL achieves a phase noise of -125dBc/Hz at 1MHz offset from a divided-by-2 carrier frequency of 2.58GHz. The core area is 0.33mm2 and the current consumption is 30mA from a 1.2V supply.

Session 2-3

Time: 14:30-14:55

A Quantization Error Minimization Using DDS-DAC for Wideband Fractional-N Frequency Synthesizer

Yi-Da Wu, Po-Chiun Huang

National Tsing Hua University, Taiwan

Abstract: This work presents a quantization error minimization technique for a fractional-N frequency synthesizer. By using a direct digital synthesis phase accumulator as the fractional divider and a DAC as pulse conversion, the quantization error can be much smaller than the one by conventional £U-£G modulated multi-modulus divider. With small quantization error, dedicated compensation mechanism is no longer necessary for wide loop bandwidth applications. To demonstrate this concept, a prototype chip is realized with the 0.18£gm CMOS. The synthesizer consumes 31mA under a single 1.8V supply. With 1MHz closed-loop bandwidth, the in-band noise is -94dBc/Hz and the 3MHz offset noise is -118dBc/Hz for the 1.8GHz output. The output exhibits 27dB phase noise reduction. The settling time is 2£gs under a 35MHz frequency step.

Session 2-4

Time: 14:55-15:20

A Charge Pump Current Calibration Technique for Delta-Sigma Fractional-N PLLs in 0.18-µm CMOS

Wei-Hao Chiu, Tsung-Hsien Lin, Tai-Shun Chang

National Taiwan University, Taiwan

Abstract: This work presents a charge pump (CP) calibration technique for a Delta-Sigma fractional-N phase-locked loop (DS-FNPLL). The proposed calibration method introduces an auxiliary path to the CP circuit and utilizes some interval within each reference cycle to detect the mismatch and then correct for the up/down current difference. The proposed CP calibration is employed in the design of a 2.4-GHz DS-FNPLL. The experimental result has demonstrated that the in-band phase noise and fractional spurs are significantly reduced when the proposed CP calibration is activated. Fabricated in a TSMC 0.18-um CMOS process, the whole DS-FNPLL consumes 23 mW from a 1.8-V supply.

Session 2-5

Time: 15:20-15:32

A 65nm CMOS 3.6GHz Fractional-N PLL with 5th-Order Delta-Signam Modulation and Weighted FIR Filtering

Xueyi Yu (*Tsinghua University, China),* Yuanfeng Sun (*Tsinghua University, China),* Woogeun Rhee (*Tsinghua University, China),* Sangsoo Ko *(Samsung Electronics, Korea),* Wooseung Choo *(Samsung Electronics, Korea),* Byeong-Ha Park *(Samsung Electronics, Korea),* Zhihua Wang (*Tsinghua University, China)*

Abstract: A 3.6GHz fractional-N PLL utilizing high-order digital modulation and weighted 13-tap finite impulse respons (FIR) filtering for low spur and enhanced noise reduction is implemented in 65nm CMOS. The prototype PLL exhibits nearly -100dBc/Hz in-band noise contribution and -126.8dBc/Hz phase noise at a 3MHz offset from a 1.8GHz carrier. With 5th-order single-loop delta-sigma modulation, the fractional spur levels of -65.6dBc and -58.5dBc are achieved within the bandwidth and near the bandwidth, respectively.

Session 2-6

Time: 15:32-15:44

A 9.3MHz to 5.7GHz Tunable LC-Based VCO Using a Divide-by-N Injection-Locked Frequency Divider

Shoichi Hara, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: This paper proposes a novel wideband voltage-controlled oscillator (VCO) for multi-band transceivers. The proposed oscillator has a core VCO and a tuning-range extension circuit, which consists of an injection-locked frequency divider (ILFD), and flip flop dividers. The 2-stage differentail ILFD can generate quadrature outputs, and it realizes 2, 3, 4, and 6 of divide ratio with very wide output frequency range. The proposed circuit is implemented by using a 90nm CMOS process, and the chip area is 250um * 200um. The measured results achieves 9.3MHz-to-5.7GHz (199%) of continuous frequency tuning range with -210dBc/Hz of FoMT.

Session 3 - Low Power Circuit Techniques

Time: 13:40-15:45

Room: VIP Floor V105

Chair: Chi-Cheng Ju (MediaTek Inc.)

Co-chair: Makoto Ikeda (University of Tokyo)

Session 3-1

Time: 13:40-14:05

A Low-Power Wide-Range Clock Synchronizer with Predictive-Delay-Adjustment Scheme for Continuous Voltage Scaling in DVFS Control

Masafumi Onouchi *(Hitachi Ltd., Japan),* Yusuke Kanno *(Hitachi Ltd., Japan),* Makoto Saen *(Hitachi Ltd., Japan),* Shigenobu Komatsu *(Hitachi Ltd., Japan),* Yoshihiko Yasu *(Renesas Technology Corporation, Japan),* Koichiro Ishibashi *(Renesas Technology Corporation, Japan)*

Abstract: A "wide-range voltage-and-frequency clock synchronizer" (WRCS) for maintaining synchronization during voltage-scaling transition during dynamic voltage-and-frequency scaling was developed. The key feature of the WRCS is so-called predictive-delay-adjustment (PDA) scheme based on a relative skew measure. The PDA scheme reduces the area of the WRCS by 77%. The area of the fabricated WRCS in a 40-nm CMOS is only 5.65x10^-3 mm^2. It was demonstrated for the first time that measured jitter is suppressed to less than 6.8% of clock period in the case of wide-range voltage variation (0.8 - 1.55 V) and wide frequency range (100 MHz - 1 GHz).

Session 3-2

Time: 14:05-14:30

A Sub-100uW Area-Efficient Digitally-Controlled Oscillator Based on Hysteresis Delay Cell Topologies

Man-Chia Chen, Jui-Yuan Yu, Chen-Yi Lee

National Chiao-Tung University, Taiwan

Abstract: This work addresses an all digitally-controlled oscillator (DCO) design with three newly proposed hysteresis delay cells (HDC). According to circuit topologies, the three HDCs are defined as on-off, cascaded, and nested HDCs. These HDCs comprise architecture, a power-of-two delay stage DCO (P2DCO), resulting in low power and low cost features. A self-calibration method is accompanied to maintain linearity of the P2DCO under PVT variations. The P2DCO is verified in a 90nm CMOS technology. The post-layout simulations show that the dynamic power is 75.9£gW and 5.21£gW in the 239.2MHz and 3.89MHz, respectively. The area of the P2DCO is 60*20£gm2.

Session 3-3

Time: 14:30-14:55

A 65-nm on-Chip Multi-Mode Asynchronous Local Power Supply Unit for Multi-Power Domain SoCs Achieving Fine Grain DVS

Motoi Ichihashi *(CEA-Leti, MINATEC, France),* Helene Lhermet *(CEA-Leti, MINATEC, France),* Edith Beigne *(CEA-Leti, MINATEC, France),* Frederic Rothan *(CEA-Leti, MINATEC, France),* Marc Belleville *(CEA-Leti, MINATEC, France),* Amara Amara*(Institut Superieur d'Electronique de Paris, France)*

Abstract: This paper discusses a local power supply unit designed for fine grain DVS in a multi-power domain SoC. The proposed unit is fully compatible with an I/O library. It delivers the module operating voltage, from 1.2 V to 0.6 V, according to predefined operating power modes and is equipped with the module power gating. The designed circuit requires five-I/O-pad pitch area in a 65-nm technology. The first test chip demonstrates that the maximum power efficiency is over 87% and the measured current consumption in stand-by mode is only 19 nA regardless of the connected module.

Session 3-4

Time: 14:55-15:20

An On-chip Continuous Time Power Supply Noise Monitoring Technique

Yoji Bando, Satoshi Takaya, Makoto Nagata

Kobe University, Japan

Abstract: A continuous-time power supply noise monitoring technique features a coverage of voltage domains at Vdd as well as at Vss and multi-channel probing at more than a hundred locations on power planes in a circuit. Methods toward quality on-chip power supply noise measurements are derived. A calibration flow eliminates the offset as well as gain errors among probing channels. A combined evaluation of on-chip measurements and off-chip circuit simulation precisely characterizes probing performance. A 90-nm CMOS on-chip monitor prototype demonstrates PS noise measurements for +-200 mV at 1.2 and 0.0V with the effective bandwidth of 1.0 GHz.

Session 3-5

Time: 15:20-15:45

On Die Parameter Extraction from Path-Delay Measurements

Tomoyuki Takahashi *(Tokyo Institute of Technology, Japan),* Takumi Uezono *(Tokyo Institute of Technology, Japan),* Michihiro Shintani *(Semiconductor Technology Academic Research Center, Japan),* Kazuya Masu *(Tokyo Institute of Technology, Japan),* Takashi Sato *(Kyoto University, Japan)*

Abstract: A device-parameter estimation through path-delay measurement is proposed, which facilitates accurate and fast ondie performance prediction and diagnosis. With the proposed technique, delay of a set of paths consisting of different logic cells are monitored. Based on the pre-characterized delaysensitivity, the process variation of a chip is estimated as an inverse problem. Discussion of good logic cell combination for delay measurement in order to maximize estimation accuracy is presented. Measurement of ring-oscillator arrays composed of various logic cells and dedicated cells yield consistent and encouring results

Session 4 - Bio and Emerging Applications

Time: 13:40-15:45

Room: VIP Floor V110

Chair: Ali Keshavarzi (Taiwan Semiconductor Manufacturing Company Ltd.)

Co-chair: Koji Kotani (Tohoku University)

Session 4-1

Time: 13:40-14:05

A 0.5uVrms 12uW Patch Type Fabric Sensor for Wearable Body Sensor Network

Long Yan

Korea Advanced Institute of Science and Technology, Korea

Abstract: A 0.5uVrms, 12uW wirelessly powered patch type fabric sensor is presented for wearable body sensor network to continuously monitor personal bioelectric signals. Thick film electrodes are screen printed on the fabric with various metal components and their impedances are characterized. A 2-stage nested chopped analog readout front end (AFE) is optimized for the fabric electrodes with reduced electrode referred noise performance of 0.5uVrms. A 10b folded SAR ADC reduces capacitive DAC (CDAC) size and relaxes the power budget of ADC driver by 94%. The proposed fabric sensor operates with system resolution of 9b and CMRR of 106dB. The chip fabricated with 0.18um CMOS technology, the fabric sensor stacked by screen printed inductor (diameter=3cm and # turns=4) can measure the ECG and EMG signals with wirelessly transmitted power through inductive coupling

Session 4-2

Time: 14:05-14:30

A Neural Recording and Stimulation Technique Using Passivated Electrodes and Micro-Inductors

Yoonkey Nam, Seonghwan Cho

Korea Advanced Institute of Science and Technology, Korea

Abstract: In this paper, a recording and stimulation method that does not require electrodes exposed to the neurons is introduced, Unlike conventional neural stimulation ICs based on micro-electrodes, the proposed method exploits eddy current induced by time-varying magnetic field of a micro-inductor. The recording circuit employs an electrolyte-insulator-metal capacitor which removes the need for the exposed metal electrode, thereby making the post-process step easier. The proposed technique also solves the problem of recording blind-time and charge-imbalance seen in the conventional MEA-based system. The proof-of-concept IC has been fabricated in 0.18um 1-poly, 4-metal standard CMOS process.

Session 4-3

Time: 14:30-14:55

A CMOS Imager and 2-D Light Pulse Receiver Array for Spatial Optical Communication

Md. Shakowat Zaman Sarker *(RIE,Shizuoka University, Japan),* Isamu Takai *(Toyota central R&D Labs, Japan),* Michinori Andoh *(Toyota central R&D Labs, Japan),* Keita Yasutomi *(RIE,Shizuoka University, Japan),* Shinya Itoh *(RIE,Shizuoka University, Japan),* Shoji Kawahito *(RIE,Shizuoka University, Japan)*

Abstract: This paper presents a CMOS imager and 2-D Light Pulse Receiver (LPR) array for car-to-car and road-to-car spatial optical communication. Using, the prototype sensor with 640x240 image pixels and 640x240 LPR cells implemented with 0.18ìm CMOS technology. Both imaging at 60fps optical communication at the carrier frequency of 1MHz are successfully performed. The measured signal amplitude and the calculation results of photocurrent show that the spatial optical communication up to 100m is possible.

Session 4-4

Time: 14:55-15:20

A 1.04 µW Truly Random Number Generator for Gen2 RFID Tag

Wei Chen, Wenyi Che, Zhongyu Bi, Jing Wang, Na Yan, Xi Tan, Junyu Wang, Hao Min

State Key Lab of ASIC and System, Auto-ID Lab, Fudan University, China

Abstract: This paper proposes a low power, low voltage Truly Random Number Generator (TRNG) for EPC Gen2 RFID tag. According to the requirements of Gen2 tag, design considerations and tradeoffs among chip area, power consumption and randomicity are presented. The proposed TRNG is composed of an analog random seed generator which uses the oscillator sampling mechanism, and Linear Feedback Shift Registers for post digital processing. Realized in SMIC 0.18 ¦Ìm standard CMOS process,it generates 16-bit random series at a speed of 40 kb/s, and their randomicity performance is verified by the FIPS 140-2 standard for security. Power consumption of the TRNG is only 1.04 ¦ÌW with a minimum supply voltage of 0.8 V, and its total chip area is 0.05 mm2.

Session 4-5

Time: 15:20-15:32

Ring Oscillator Based Random Number Generator Utilizing Wake-Up Time Uncertainty

Toru Nakura, Makoto Ikeda, Kunihiro Asada

The University of Tokyo, Japan

Abstract: This paper presents a random number generation circuit utilizing ring oscillator's wake-up time uncertainty. A ring oscillator goes into metastability state before starting to oscillate when its control voltage is increased from zero. The metastability causes the uncertainty of the wake-up time of the ring oscillator resulting in large jitter, which can be used for random number generation. We compared simple inverter and schmitt trigger type rings, number of stages of the rings, slow and fast control voltage change for the rings. The measurement results show that the slow control voltage change in a inverter type ring oscillator is effective for random number generation.

Session 4-6

Time: 15:32-15:44

Low Profile Double Resonance Frequency Tunable Antenna Using RF MEMS Variable Capacitor for Digital Terrestrial Broadcasting Reception

Yukako Tsutsumi *(Toshiba Corporation, Japan),* Masaki Nishio *(Toshiba Corporation, Japan),* Shuichi Obayashi *(Toshiba Corporation, Japan),* Hiroki Shoki *(Toshiba Corporation, Japan),* Tamio Ikehashi *(Toshiba Corporation, Japan),* Hiroaki Yamazaki *(Toshiba Corporation, Japan),* Etsuji Ogawa *(Toshiba Corporation, Japan),* Tomohiro Saito *(Toshiba Corporation, Japan),* Tatsuya Ohguro *(Toshiba Corporation, Japan),* Tasuku Morooka *(Toshiba Research Consulting Corporation, Japan)*

Abstract: It is difficult to realize the built-in antenna for wideband systems, because a frequency bandwidth of the low profile antenna is narrow. A frequency tunable antenna is a technique for wideband characteristics. In this paper a low profile double resonance frequency tunable antenna using MEMS variable capacitors is presented. It has high efficiency over a wide frequency band. Through both resonant portions from 465 to 665 MHz, the efficiency of more than -4 dB and the VSWR of less than 3 are observed in the measurement using the variable capacitor of 0.4-0.9 pF.

Panel Discussion 1 - Toward Low Voltage (0.5V) Design: Will Challenges Limit Operation?

Time: 16:00-17:40

Room: 10F Song Bo Room

Organizer: Ali Keshavarzi, Taiwan Semiconductor Manufacturing Company Ltd., USA

Moderator: Sreedhar Natarajan, Taiwan Semiconductor Manufacturing Company Ltd., USA

Panelists/Position: Arimoto, Reneasas / Microcontroller

Allison Burnet , Toumaz Medical / Medical Applications

TBD / Power Aware Design

Bora N., UCB / Process variations to enable low power design

Ali Keshavarzi, Taiwan Semiconductor Manufacturing Company Ltd. / Process and Design Optimization

TBD / Processor requirements and challenges

Peter Rickert, TI / Baseband and consumer application challenges

Abstract: Low power requirements continue to be demanding for consumer and various different applications. All ICs and every SoC being manufactured today require a cost sensitive power aware energy efficient design that can enable better systems and provide better cooling. Developing the technology and design to support very low power operations (toward 0.5V and below) is very challenging due to increasing device variations and random fluctuations. This panel will address the limitations of ultra low voltage design for some key driver applications. Note: Moderator will base questions and link each panelist area to one another through differentiated statements

Panel Discussion 2 - Gigabit Transceiver: a Panacea or a Poison?

Time: 16:00-17:40

Room: 10F Chang Chin Room

Organizer: Jri Lee, National Taiwan University

Tadahiro Kuroda, Keio University

Moderator: Mehmet Soyuer, IBM T.J. Watson Research Center

Panelists/Position: Minoru Fujishima, University of Tokyo

Kenjiro Nishikawa, NTT Network Innovation Laboratories

Bernard Shung, SiBeam

Lawrence Loh , MediaTek

Ada Poon, Stanford University

Abstract: Recently, 60-GHz and other mm-wave transceivers have demonstrated promising potential for next-generation wireless personal area networks (WPANs) and point-to-point systems. With larger available bandwidth at such high frequencies, both video and data signals can be delivered wirelessly at speeds 10-100 times faster than any existing standards. However, such designs become so challenging that we not only rely on the improvement of technology, but have to look for novel circuit techniques. This panel covers the transceiver architectures, design challenges, applications, and future opportunities for the 60-GHz and other mm-wave systems, discussing directions, strategies, and development trends in different aspects.

Special Session

Time: 18:10-18:55

Room: 10F Song Bo Room

Chair: Tohru Furuyama (Toshiba Corporation)

Co-chair: Mototsugu Hamada (Toshiba Corporation)

All you need to know to write a winning ISSCC paper and give a smashingly good presentation

Jan Van Der Spiegel

University of Pennsylvania, USA

Plenary Session 3

Time: 08:30-09:15

Room: 10F Auditorium

Chair: Tohru Furuyama (Toshiba Corporation)

Co-chair: Mototsugu Hamada (Toshiba Corporation)

Weak Inversion for Ultra Low-Power and Very Low-Voltage Circuits

Eric Vittoz

Swiss Federal Institute of Technology, Lausanne, Switzerland

Abstract: Sub-microwatt circuits were introduced more than 40 years ago for electronic watches. CMOS was soon identified as the best technology for digital subcircuits, with the problem of lowering the threshold below 1V. At the very low bias current available for the analog subcircuits, MOS transistors had to be operated below their threshold, i.e. in weak inversion. A compact design-oriented model and special design techniques were therefore developed to exploit this unusual mode of operation. After evolving as a specialty during several decades, weak inversion design has gained importance with the broadened interest for very low power. Whatever the current level, it is the only way to operate analog circuits with a supply voltage below 0.5V. For digital circuits, it can provide the ultimate speed/power ratio in a given process. With deep submicron processes, digital transition times below 1ns and analog frequencies above 1GHz can be obtained in weak inversion. This paper will visit techniques, limitations and possible future developments of weak inversion circuits.

Session 5 - Low Power Analog-to-Digital Converts

Time: 09:30-11:50

Room: 10F Song Bo Room

Chair: Seong Hwan Cho (Korea Advanced Institute of Science and Technology)

Co-chair: Leibo Liu (Tsinghua University)

Session 5-1

Time: 09:30-09:55

A CBSC Second-Order Sigma-Delta Modulator in 3μm LTPS-TFT Technology

Wei-Ming Lin, Chan-Fei Lin, Shen-Iuan Liu

National Taiwan University, Taiwan

Abstract: A second-order sigma-delta modulator has been implemented in 3um low-temperature poly-silicon thin-film transistor (LTPS-TFT) technology. Since the LTPS-TFT operational amplifier has a low open-loop gain, a large offset voltage, and the poor linearity, the proposed comparator-based switched-capacitor integrator with correlated double sampling is adopted in the modulator. The whole modulator consumes 63.3mW from an 11.2V supply and occupies 26mm2 area. In a signal bandwidth of 1.56kHz for the touch panel application, the measured input dynamic range is 69dB and the measured peak signal-to-noise plus distortion ratio is 65.63dB with the duty-cycle control technique.

Session 5-2

Time: 09:55-10:20

A CMOS 6-mW 10-Bit 100-MS/s Two-Step ADC

Yung-Hui Chung, Jieh-Tsorng Wu

National Chiao-Tung University, Taiwan

Abstract: A 10b 100MS/s two-step ADC fabricated in 90nm digital CMOS process is presented. It effectively takes advantage of the nanoscale CMOS technology to achieve low power dissipation. Its internal coarse ADC and fine ADC are realized with latch-type comparators with automatic offset calibration. The gain error and nonlinearity of the residue amplifier is corrected in the digital domain. The ADC consumes only 6mW from a single 1V supply. Measured ENOB is 9.34b. The FOM is 100 fJ per conversion-step.

Session 5-3

Time: 10:20-10:45

A 6bit, 7mW, 250fJ, 700MS/S Subranging ADC

Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: A 6 bit, 7 mW, 700 MS /s subranging ADC fabricated in 90 nm CMOS technology with SNDR of 34 dB for Nyquist input frequency is presented. The subranging architecture using CDACs, gate-weighted interpolation scheme, and digitally offset calibrating double-tail latched comparators has demonstrated an ultra low FoM of 250 fJ/conv. steps. and attractiveness for embedded IP for low power SoCs.

Session 5-4

Time: 10:45-11:10

A 9b 100MS/S 1.46mW SAR ADC in 65nm CMOS

Yanfei Chen *(Keio University, Japan),* Sanroku Tsukamoto *(Fujitsu Laboratories Ltd., Japan),* Tadahiro Kuroda *(Keio University, Japan)*

Abstract: A 9b 100MS/s successive approximation register (SAR) ADC has been implemented in 65nm CMOS, with an active area of 0.012mm2. A tri-level based charge redistribution technique improves DAC switching energy efficiency and settling time, which is achieved by connecting bottom plates of differential capacitor arrays. The ADC achieves an SNDR of 53.1dB (8.53 ENOB) and consumes 1.46mW from a 1.2V supply, resulting in an FOM of 39fJ/conversion-step.

Session 5-5

Time: 11:10-11:22

A 10-Bit 500-Ks/S Low Power SAR ADC with Splitting Comparator for Bio-Medical Applications

Wen-Yi Pang, Chao-Shiun Wang, You-Kuang Chang, Nai-Kuan Chou, Chorng-Kuang Wang

National Taiwan University, Taiwan

Abstract: This paper presents a successive approximation register analog-to-digital converter (SAR ADC) design for bio-medical applications. Splitting comparator and energy saving capacitor array are proposed to achieve low power consumption. The average switching energy of the capacitor array can be reduced by 69% compared to a conventional switching method. The measured signal-to-noise-and-distortion ratios of the ADC is 58.4 dB at 500KS/s sampling rate with an ultra-low power consumption of 42-£gW from a 1-V supply voltage. The ADC is fabricated in a 0.18-£gm CMOS technology.

Session 5-6

Time: 11:22-11:34

A 3mW 12b 10MS/S Sub-Range SAR ADC

Hung-Wei Chen, Yu-Hsun Liu, Yu-Hsiang Lin, Hsin-Shu Chen

National Taiwan University, Taiwan

Abstract: This paper presents a successive approximation analog-to-digital converter (SAR ADC) achieving high power efficiency by adopting sub-range concept. Overlapping range greatly relieves the accuracy requirement on the first 6 bit resolving in coarse conversion. The error made in the coarse conversion could be recovered during the rest 7 bit resolving in fine conversion. Hence, it can significantly reduce the capacitor array output settling time of most-significant-bit (MSB) capacitor switching, which is the speed bottleneck for traditional SAR ADC. A 3mW 12b 10MS/s sub-range SAR ADC is realized in 0.13-um CMOS process. The prototype circuit reaches SNDR 59.7dB at Nyquist input.

Session 5-7

Time: 11:34-11:46

A 10-Bit 12-Ms/S Successive Approximation ADC with 1.2-pF Input Capacitance

Guan Ying Huang

Department of Electrical Engineering, National Cheng-Kung University, Taiwan

Abstract: This paper reports a successive-approximation analog-to-digital converter (ADC) with low input capacitance. The 10-bit prototype is fabricated in a 0.13-ƒÝm CMOS process. Compared to conventional successive approximation ADCs, the proposed ADC reduces the input capacitance to 1.2 pF for 10-bit resolution. The proposed ADC is a good selection for system integration.

Session 6 - Wireline Communication Circuits

Time: 09:30-11:50

Room: 10F Chang Chin Room

Chair: Wei-Zen Chen (National Chiao Tung University)

Co-chair: Jung-Hoon Chun (Sungkyunkwan University)

Session 6-1

Time: 09:30-09:55

A 1.35GHz All-Digital Fractional-N PLL with Adaptive Loop Gain Controller and Fractional Divider

Deok-Soo Kim, Heesoo Song, Taeho Kim, Suhwan Kim, Deog-Kyoon Jeong

Seoul National University, Korea

Abstract: A 1.35GHz all-digital phase-locked loop (ADPLL) with an adaptively controlled loop filter and a 1/3-resolution fractional divider is presented. The adaptive loop gain controller (ALGC) effectively reduces the nonlinear characteristics of the bang-bang phase-frequency detector (BBPFD). The fractional divider partially compensates for the input phase error which is caused by the fractional-N frequency synthesis operation. A prototype ADPLL using a BBPFD with a dead zone free retimer, an ALGC, and a fractional divider is fabricated in 0.13¥ìm CMOS. The core occupies 0.19mm©÷ and consumes 13.7mW from a 1.2V supply. The measured RMS jitter was 4.17ps at a 1.35GHz clock output.

Session 6-2

Time: 09:55-10:20

A 10Gb/S Inductorless Quarter-Rate Clock and Data Recovery Circuit in 0.13um CMOS

Chang-Lin Hsieh, Hong-Lin Chu, Shen-Iuan Liu

National Taiwan University, Taiwan

Abstract: A 10Gb/s inductorless quarter-rate clock and data recovery (CDR) circuit is presented. In this CDR circuit, a triggering generator is proposed to realize the quarter-rate operation. Owing to the quarter-rate operation and the absence of inductors, this CDR circuit achieves low power consumption and small area simultaneously. This 10Gb/s quarter-rate CDR circuit has been fabricated in a 0.13um CMOS process. It recovers the data and clock within 5 bits. The measured peak-to-peak jitter of the recovered data and clock is 32.22ps and 30.7ps, respectively. The chip area including a PLL and a dummy GVCO is 0.2mm2. This CDR circuit consumes 122.5mW excluding output buffers from a supply voltage of 1.5V.

Session 6-3

Time: 10:20-10:45

A 6.4GT/S Point-to-Point Unidirectional Link with Full Current Compensation

Harry Muljono, Kathy Tian, Mubeen Atha, Charlie Lin, Linda K Sun, Stefan Rusu

Intel Corporation, USA

Abstract: This 45nm 1.1V unidirectional differential point-to-point link interface achieves 6.4GT/s transfer rate. To support 17 inches, 2-connector channel topology required by Multi-Processor (MP) platform, it utilizes two novel current compensation techniques that optimize the performance/power ratio of the transmitter output swing level and receiver gain/bandwidth.

Session 6-4

Time: 10:45-11:10

An 8 Gbps Fast-Locked Automatic Gain Control for PAM Receiver

Wei-Zen Chen

National Chiao-Tung University, Taiwan

Abstract: An 8 Gbps automatic gain control (AGC) loop for PAM receiver is proposed. Incorporating digital intensive gain control scheme, the dynamic range of the variable gain amplifier is 22 dB with a resolution of 0.9 dB/step. The locking time of the AGC loop is less than 200 ns and independent of input amplitude. Fabricated in a 0.18 ìm CMOS technology, the chip size is 0.62 x 0.62 mm2. The total power dissipation is 84 mW from a 1.8 V supply.

Session 6-5

Time: 11:10-11:22

A 5Gb/S Low-Power PCI Express/USB3.0 Ready PHY in 40nm CMOS Technology with High-Jitter Immunity

Mu-Shan Lin, Chien-Chun Tsai, Chih-Hsien Chang, Yung-Chow Peng, Tsung-Hsin Yu, Jinn-Yeh Chien, W.D. Chen, Chi-Chang Lu, Wei-Chih Chen

Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

Abstract: A PCI Express 2.0/1.0 compatible SERDES system had been fabricated in TSMC 40nm CMOS technology. With the implementation of one lane transceiver, PLL, and PCS, the experimental results have shown this test chip passes PCI Express 2.0/1.0 TX compliance test and RX compliance test. It also achieves receiver jitter tolerance up to 0.33UI at BER of 10-12 with stressing all spec. specified jitter sources. A compact area of 510um*710um for one lane has been achieved while consuming only 125mW from 0.9V supply.

Session 6-6

Time: 11:22-11:34

A 250Mb/S-to-3Gb/S 5x Oversampling Receiver with an All-Digital Adapting Equalizer

Min-Chung Chou, Qui-Ting Chen, Ping Chen

MediaTek Inc., Taiwan

Abstract: In this paper, a 250Mb/s-to-3Gb/s 5x oversampling receiver with an all¡Vdigital adapting equalizer is presented. A novel oversampling based inter-symbol interference (ISI) monitor and adapting flows are proposed for the equalizer to compensate channel losses. The receiver has been implemented in 65-nm CMOS process. The analog equalizer has a power consumption of 9.6 mW and an area of 0.012 mm2 including an all-digital ISI monitor and an adapting circuit. The core area of the receiver is 0.26 mm2, including the input terminations, the shared PLL, and three data channels.

Session 6-7

Time: 11:34-11:46

A Low Latency Transceiver Macro with Robust Design Technique for Processor Interface

Zhang Feng

Institute of Computing Technology, Chinese Academy of Sciences, China

Abstract: This paper describes a 65nm 16-bit parallel transceiver IP macro, whose bandwidth is 4.8GByte/s with 5pf load including the HBM 2000v ESD protection. Equalizers and CDR modules, CRC checkers and 8b/10b encoders are not added in the design for reducing the latency and the whole latency is 7ns without cables. Since the transceiver has many robust features including a PVT independent PLL with calibrations, the low skew differential clock tree, a stable current mode driver with common mode feedback. The transceiver can tolerance 20% power supply variations between 1.0V and 1.2V and work properly at different process corners and the extreme temperatures. The transceiver can be applied for the interface of sub-100nm high performance processors which require low latency and high stability. The transceiver shows a BER less than 10-15 at 3Gb/s/pin.

Session 7 - Image Signal Processing

Time: 09:30-11:50

Room: VIP Floor V105

Chair: Hirofumi Sumi (Sony Corporation)

Co-chair: Shao-Yi Chien (National Taiwan University)

Session 7-1

Time: 09:30-09:55

Tera-Scale Performance Image Stream Processor with SoC Architecture for Multimedia Content Analysis

Tse-Wei Chen, Chi-Sun Tang, Sung-Fang Tsai, Chen-Han Tsai, Shao-Yi Chien, Liang-Gee Chen

National Taiwan University, Taiwan

Abstract: A 1.0 TOPS image stream processor, which deals with image processing tasks for multimedia content analysis, is implemented in 90nm CMOS technology. Two sub processors, linear processor and order processor, are integrated to achieve tera-scale performance. In the proposed SoC architecture, the data are transferred between processors and the high bandwidth dual memory through the local media bus, which reduces the power consumption in the AHB data access. Based on the memory architecture, the maximum input data rate of the proposed image stream processor reaches 62.5Gpixel/s, which meets the requirements for real-time HDTV image processing.

Session 7-2

Time: 09:55-10:20

Crisp-Ds: Dual-Stream Coarse-Grained Reconfigurable Image Stream Processor for HD Digital Camcorders and Digital Still Cameras

Shao-Yi Chien, Tsung-Huang Chen, Jason C. Chen, Tung-Yuan Cheng

National Taiwan University, Taiwan

Abstract: A 329mW 600M-Pixels/s dual-stream coarse-grained reconfigurable image stream processor is implemented in TSMC 0.13um CMOS technology with a core size of 4.84mm^2. The reconfigurable pipeline processing element array architecture makes a good balance between computing performance and flexibility with only 10Kb on-chip memory. Moreover, a new dual-stream architecture is proposed to improve the flexibility and hardware efficiency by processing two independent image streams with two-layer context switching, and an isolation technique is also proposed to improve the power consumption. Implementation results show that it achieves 1.52 times power efficiency than previous works and can meet the requirements of high-definition video camcorders and digital still cameras.

Session 7-3

Time: 10:20-10:45

A 439K Gates/10.9KB SRAM/2-328 mW Dual Mode Video Decoder Supporting Temporal/Spatial Scalable Video

Cheng-An Chien *(National Chung-Cheng University, Taiwan),* Yao-Chang Yang *(National Chung-Cheng University, Taiwan),* Hsiu-Cheng Chang *(National Chung-Cheng University, Taiwan),* Jiun-In Guo *(National Chung-Cheng University, Taiwan),* Jia-Wei Chen *(National Chung-Cheng University, Taiwan),* Jinn-Shan Wang *(National Chung-Cheng University, Taiwan),* Chin-Hsien Wang *(Feng-Chia University, Taiwan),* Hsiang-Hui Huang *(Feng-Chia University, Taiwan),* Ching-Hwa Cheng *(Feng-Chia University, Taiwan)*

Abstract: The first dual mode video decoder with 4-level temporal/spatial scalability and 32/64-bit adjustable memory bus width is proposed. A design automation environment of simulation and verification is established to automatically verify the correctness and completeness of the proposed design. Using a 0.13 um CMOS technology, it comprises 439Kgates/10.9KB SRAM and consumes 2~328mW in decoding CIF~HD1080 videos at 3.75~30fps when it is operated at 1~150MHz, respectively.

Session 7-4

Time: 10:45-11:10

A Rate-Controllable Near-Lossless Data Compression IP for HDTV Decoder LSI in 65nm CMOS

Masato Uchiyama *(Tosihba Semiconductor Company, Japan),* Kohei Oikawa *(Tosihba Semiconductor Company, Japan),* Naoto Date *(Toshiba Corporation, Japan),* Shinichiro Koto *(Toshiba Corporation, Japan)*

Abstract: We propose a rate-controllable near-lossless embedded compression algorithm "TLS-1". The algorithm guarantees a selected compression ratio with the smart combination of variable length coding and fixed length coding. It achieves near-lossless image quality under CR = 2. We apply the algorithm to an IP in an HDTV decoder LSI in order to reduce the required external memory capacity and its bandwidth. The LSI is fabricated in a 65nm CMOS technology.

Session 7-5

Time: 11:10-11:35

A High-Frame-Rate Dense Motion Vector Field Generation Processor with Simplified Best-Match Searching Circuitries

Yuta Okano, Tadashi Shibata

University of Tokyo, Japan

Abstract: A high-frame-rate dense motion vector field generation processor employing an efficient data manipulation scheme has been developed. By reusing the result of motion vector detection at one location for the calculation at an adjacent location, the best-match searching circuitry for motion vector detection has been greatly simplified. As a result, it has become possible to generate motion vectors from all pixel sites of 256□~256-size motion images at a frame rate of 1060 frames/sec with a clock frequency of 100MHz. A prototype chip was designed and fabricated in a 0.18-ƒÊm 5-metal CMOS technology, and the operation was experimentally demonstrated.

Session 8 - Memory

Time: 09:30-11:50

Room: VIP Floor V110

Chair: Katsuyuki Sato (Taiwan Semiconductor Manufacturing Company Ltd.)

Co-chair: Bor-Doou Rong (Etron)

Session 8-1

Time: 09:30-09:55

Low Power Embedded DRAM Using 0.6V Super Retention Mode with Word Line Data Mirroring

Takayuki Iwai *(Semiconductor Company, Toshiba Corporation, Japan),* Mariko Kaku *(Semiconductor Company, Toshiba Corporation, Japan),* Takayuki Miyazaki *(Semiconductor Company, Toshiba Corporation, Japan),* Hitoshi Iwai *(Semiconductor Company, Toshiba Corporation, Japan),* Hiroyuki Takenaka *(Toshiba Microelectronics, Japan),* Atsushi Suzuki *(Toshiba Microelectronics, Japan),* Shinji Miyano *(Toshiba Microelectronics, Japan),* Mototsugu Hamada *(Toshiba Microelectronics, Japan)*

Abstract: An 88% reduction of refresh power of the 65nm embedded DRAM is achieved using Super Retention Mode(SRM) with Word Line Data Mirroring(WLDM). The retention time in Super Retention Mode is measured in the range of 0.55V to 1.2V. The minimum refresh power is obtained at 0.6V. The retention time of Super Retention Mode at 0.6V is extended by 4.1 times from that of conventional single cell operation at 1.2V. The transition time from normal mode to Super Retention Mode of 22.6ƒÊs is achieved with only 0.4% area penalty.

Session 8-2

Time: 09:55-10:20

CMOS Low-VT Preamplifier for 0.5-V Gigabit-DRAM Arrays

Akira Kotabe, Yoshimitsu Yanagawa, Satoru Akiyama, Tomonori Sekiguchi

Central Research Laboratory, Hitachi, Ltd., Japan

Abstract: A novel CMOS low-VT preamplifier suitable for low-voltage and high-speed mid-point sensing was developed for gigabit DRAM. The sensing speed of the proposed preamplifier at data-line voltage of 0.5 V is 62% higher than that of a conventional preamplifier. By activating the low-VT NMOS and PMOS cross couples temporarily during write operation, writing time is 72% shorter compared to the case with the high-VT CMOS latch only. Data-line charging current of a memory cell array with the proposed preamplifier is reduced by 26% by decreasing data-line voltage from 0.8 to 0.5 V.

Session 8-3

Time: 10:20-10:45

A Field Programmable 40-nm Pure cmos Embedded Memory Macro Using a pmos antifuse

Daichi Kaku, Toshimasa Namekawa, Kensuke Matsufuji, Osamu Wada, Hiroshi Ito, Yoshinori Sugisawa, Sakiko Shimizu, Takeshi Yamamoto, Kenji Honda, Mototsugu Hamada, Kenji Numata,

Toshiba, Japan

Abstract: A Pure CMOS One-time Programmable memory (PCOP) macro using a PMOS antifuse is designed for field programming. In this work, a Temperature-controlled programming Voltage Generator (TVG) realizes field programming by improving programming characteristics over a wide temperature range, from -40C to 125C, and supply voltage variations of +/-10%. In addition, the memory cell dimensions are optimized and reduced by 40%, which also results in better reading characteristics. PCOP has a 16-Kbit capacity, uses 1.1-V and 3.3-V power sources, occupies 0.224 mm2 and is implemented in a 40-nm pure CMOS logic technology with thin and thick oxide film transistors.

Session 8-4

Time: 10:45-11:10

A Low Supply Voltage Operation SRAM with HCI Trimmed Sense Amplifiers

Atsushi Kawasumi, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Yuki Fujimura, Tomoaki Yabe

Toshiba, Japan

Abstract: This paper proposes a new scheme utilizing the small offset voltage (Vos) sense amplifier (SA) to improve the deterioration both of the read speed and the cell stability at the low power supply. This concept is newly introduced to realize a low supply voltage operation SRAM with the small area penalty. The transistor threshold voltage shift caused by Hot Carrier Injection is used for the Vos trimming after the chip fabrication. The SA with the offset trimming circuit is implemented in the 40nm CMOS technology and the reduction of Vos by 76mV has been confirmed with the measurement and simulation results.

Session 8-5

Time: 11:10-11:22

A 45nm 0.5V 8T Column-Interleaved SRAM with on-Chip Reference Selection Loop for Sense-Amplifier

Mahmut Sinangil, Naveen Verma, Anantha Chandrakasan

Massachusetts Institute of Technology, USA

Abstract: 8T bit-cells hold great promise for overcoming device variability in deeply scaled SRAMs and enabling aggressive voltage scaling for ultra-low-power. This paper presents an array architecture and circuits with minimal area overhead to allow column-interleaving while eliminating the half-select problem. This enables sense-amplifier sharing and soft-error immunity. A reference selection loop is designed and implemented in the column circuitry. By choosing one of the two reference voltages for each sense-amplifier in a pseudo-differential scheme, selection loop effectively reduces input offset. 8T test array fabricated in 45nm CMOS achieves functionality from 1.1V to below 0.5V. Test chip operates at 450MHz at 1.1V and 5.8MHz at 0.5V while consuming 12.9mW and 46 W respectively.

Session 8-6

Time: 11:22-11:34

An on-Chip High-Speed 4-Bit BCH Decoder in MLC Nor Flash Memories

Xueqiang Wang *(Tsinghua University, China),* Dong Wu *(Tsinghua University, China),* Chaohong Hu *(Intel Technology Development (Shanghai) Co., Ltd, China),* Liyang Pan *(Tsinghua University, China),* Runde Zhou *(Tsinghua University, China)*

Abstract: An on-chip high-speed 4-bit BCH decoder for error orrecting in a MLC NOR flash memory is presented. As process shrinking beyond 45nm, double-error-correcting (DEC) BCH code is needed for reliability requirement. A novel fast-decoding algorithm is developed by eliminating finite field divisions and combining arithmetic operations. As a result, the decoding latency is significantly reduced by 80%. Furthermore, a novel architecture of the 4-bit BCH decoder in a 2b/cell NOR flash memory is proposed to obtain a good time-area trade-off. Simulation results show that the latency of the 4-bit BCH decoder achieves only 6.4ns and satisfies fast access time of a NOR Flash memory.

Session 9 - Advanced Analog Techniques

Time: 12:50-14:55

Room: 10F Song Bo Room

Chair: Bill Yang Liu (Analog Devices)

Co-chair: Tsung-Hsien Lin (National Taiwan University)

Session 9-1

Time: 12:50-13:15

A Low-Offset Latched Comparator Using Zero-Static Power Dynamic Offset Cancellation Technique

Masaya Miyahara, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: A low-offset latched comparator using new dynamic offset cancellation technique is proposed. The new technique achieves low offset voltage without pre-amplifier and quiescent current. Furthermore the overdrive voltage of the input transistor can be optimized to reduce the offset voltage of the comparator independent of the input common mode voltage. A prototype comparator has been fabricated in 90 nm 9M1P CMOS technology. Experimental results show that the comparator achieves 3.8 mV offset at 1 sigma at 500 MHz operating, while dissipating 39 uW from a 1.2 V supply.

Session 9-2

Time: 13:15-13:40

A Pseudo-Differential OTA with Linearity Imporving by HD3 Feedforward

Chao-Liang Chien, Chung-Chih Hung

National Chiao Tung University, Taiwan

Abstract: This paper presents a fully balanced structure of a CMOS Operational Transconductance Amplifier (OTA) with high linearity at 50MHz frequency. The proposed circuit, based on the conventional pseudo-differential structure, with a new concept of linearity improving by Third Order Harmonic Distortion (HD3) Feedforward to cancel the output 3rd harmonic component is introduced in this work. The OTA was fabricated in the TSMC CMOS 0.18£gm technology and dissipates 0.47mW power with 1.2V voltage supply. The measured result shows the HD3 of -62dB at 50MHz with 0.4Vpp input signal.

Session 9-3

Time: 13:40-14:05

An Accurate Current Reference Using Temperature and Process Compensation Current Mirror

Jee-Sue Lee

Chungbuk National University, Korea

Abstract: In this paper, an accurate current reference using temperature and process compensation current mirror (TPC-CM) is proposed. The temperature independent reference current is generated by summing a proportional to absolute temperature (PTAT) current and a complementary to absolute temperature (CTAT) current. The temperature coefficient and magnitude of the reference current are influenced by the process variation. To calibrate the process variation, the proposed TPC-CM uses two binary weighted current mirrors which control the temperature coefficient and magnitude of the reference current. After the PTAT and CTAT currents are measured, the switch codes of the TPC-CM are fixed in order that the magnitude of reference current is independent to temperature. And, the codes are stored in the non-volatile memory. In the simulation, the effect of the process variation is reduced to 0.52% from 19.7% after the calibration using a TPC-CM in chip-by-chip. A current reference chip is fabricated with a 3.3V 0.35um CMOS process. The measured calibrated reference current has 0.42% variation for 20¡É~100¡É.

Session 9-4

Time: 14:05-14:30

A Robust Continuous Time Loop Filter PWM Class D Amplifier with High Linearity and Good Immunity to Process Variations

Hsin-Hong Hou, Chung-Wei Lin, Wen-Tzao Chen

Industrial Technology Research Institute, Taiwan

Abstract: This paper describes a robust PWM class D amplifier with high linearity and good immunity to process variations. By using the proposed adaptive triangular wave generator (ATG), 0.0042% THD+N and 99.2dB dynamic range is achieved in this design. The standard deviation of THD+N ratio over 22 samples can be smaller by 4 times compared to the results without the adaptive triangular wave generator. This chip integrates power MOS stages and 2 channel design. The supply voltage is from 3V to 5.5V and the die area is 2.45mm x 2.9mm.

Session 9-5

Time: 14:30-14:55

A GFSK Demodulator Based on Instant Phase Computation and Adaptive Multi-Threshold Quantization

Dong Han, Yuanjin Zheng

Institute of Microelectronics, Singapore

Abstract: An ultra-low power mixed-signal Gaussian frequency shift keying (GFSK) demodulator for wireless body area networks (WBAN) is introduced. A novel multi-threshold instant phase zero-crossing detector (MIPZCD) which is composed of a 2-stage poly-phase filter (PPF), an instant phase calculator and an adaptive multi-threshold quantizer is proposed to improve the demodulator phase accuracy and data rate. The measured results show that the demodulator achieves the data rate up to 2Mbps and the input frequency range from 1.6MHz to 2.5MHz. The measured signal-to-noise ratio (SNR) for 0.1% bit error rate (BER) with the GFSK signal of 1Mbps data rate, 2MHz center frequency, and 160kHz frequency deviation is 15.8dB. The demodulator has been implemented in 0.18-um CMOS process with only 0.23mm2 active area and 410uA drain current from a 1.8V power supply.

Session 10 - RF Building Blocks and Phased Array Receivers

Time: 12:50-14:55

Room: 10F Chang Chin Room

Chair: Shouhei Kousai (Toshiba Corporation)

Co-chair: Ryangsu Kim (Panasonic Corporation)

Session 10-1

Time: 12:50-13:15

A 0.9-3.0 GHz Fully Integraded Tunable CMOS Power Amplifier for Multi-Band Transmitters

Daisuke Imanishi, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: A tunable power amplifier (PA) from 0.9 GHz to 3.0 GHz is presented. This paper proposes an output impedance tuning method by using resistive feedback and a parallel resonance consisting of an inductor and a tunable capacitor array. The proposed multi-band PA can adjust the output impedance to 50 ohm over a wide frequency range, so external isolators following PAs can be eliminated. The PA is implemented by using a 0.18 um CMOS process, and the supply voltage is 3.3 V. Over all of the frequency range, the PA realizes output return loss S22 of smaller than -10 dB, power gain of larger than 16 dB, output 1-dB compression point of larger than 17 dBm, and power added efficiency (PAE) at 1-dB compression point of larger than 10 %.

Session 10-2

Time: 13:15-13:40

An Inherently Linear Phase-Oversampling Vector Modulator in 90-nm CMOS

Richard Tseng *(UIUC, USA),* Hao Li *(UIUC, USA),* Dae Hyun Kwon *(UIUC, USA),* Ada Poon *(Stanford, USA),* Yun Chiu *(UIUC, USA)*

Abstract: A four-antenna vector modulator (VM) beamforming receiver in 90-nm CMOS operating between 2.4 and 4.9 GHz is presented. The VM is based on a phase-oversampling technique that allows the synthesis of inherently linear, high-resolution complex gains without complex variable gain amplifiers. It achieves 360° phase shift programmability with 8-bit digital control, a measured < 4.2° phase error at a back-off of 4 dB from the maximum gain setting, and a complex gain constellation with a mean error vector magnitude of < 2%. The monolithic beamformer also demonstrates an interference cancellation of > 24 dB for interferers impinging from different directions.

Session 10-3

Time: 13:40-14:05

A 25 GHz CMOS Phased Array Receiver Front-End Based on Subsector Beam Steering Technique

Ting-Yueh Chin, Sheng-Fuh Chang, Chia-Chan Chang, Jen-Chieh Wu

National Chung Cheng University, Taiwan

Abstract: A 25-GHz 4-element phased-array receiver front-end based on a new subsector beam steering architecture is presented. The architecture divides the receive area into five subsectors with four characteristic beams and steers the receive beam in each subsector by combining two weighted signal amplitudes from the four received channels. The experimental chip consumes as low as 30 mW and takes only 1.43 mm2 in 0.13-um CMOS technology. It has 10-12 dB power gain, 9-10.5 dB NF and -15 dBm P1dB in 24.5-26 GHz.

Session 10-4

Time: 14:05-14:30

A 30GHz Integrated Time-Division Multiplexing Front-End for Phased-Array Applications in SiGe

Wei Deng *(Eindhoven University of Technology, Netherlands),* Reza Mahmoudi, Fernando Fortes *(Eindhoven University of Technology, Netherlands),* Edwin van der Heijden *(Instituto Superior de Engenharia de Lisboa, Portugal),* Arthur van Roermund *(Eindhoven University of Technology, Netherlands)*

Abstract: This paper presents a fully integrated receiver front-end for time-division multiplexing phased-array system. The 30GHz front-end includes a low-noise amplifier (LNA), a 4:1 multiplexer, a mixer, and a clock sequencer. The circuit has been implemented in a 0.25ìm, 130GHz-fT SiGe process. The front-end shows a input reflection coefficient (S11) of -20dB, a minimum measured LNA-Multiplexer noise figure (NF) of 4.1dB, and a maximum conversion gain (CG) of 18.9dB at 30GHz. Measurements show a 1dB input compression point of -32.3dBm, a third order intercept point (IIP3) of -22dBm, and a channel isolation of 23dB at 30GHz. This system reduces receiver power consumption by reducing ADC numbers

Session 10-5

Time: 14:30-14:42

Inductorless 1-10.5 GHz Wideband LNA for Multistandard Applications

Sven Karsten Hampel *(Leibniz Universitaet Hannover, Germany),* Oliver Schmitz *(Leibniz Universitaet Hannover, Germany),* Marc Tiebout *(Infineon Technologies Austria AG, Austria),* Ilona Rolfes *(Leibniz Universitaet Hannover, Germany)*

Abstract: This article presents the design of a fully integrated inductorless wideband LNA for wireless applications including WLAN,Bluetooth and UWB. The circuit was fabricated in 65nm CMOS technology and operates at a supply voltage of 1.2 V. The twostage design is comprised of a current reuse shunt feedback input stage followed by a differential pair, incorporating an active inductor load to compensate the gain roll-off. The circuit exhibits a peak gain of 16.5dB, while the 3-dB bandwidth as well as the input and output matching of better than -10 dB rangefrom 1-10.5GHz. The noise figure is kept below 5dB within this frequency range, offering a minimum noise figure of 3.9dB. The linearity in terms of P1dB,out and oIP3 offers nearly constant behavior with -5dBm and 3dBm respectively. The active area takes up only 0.021mm2.

Session 10-6

Time: 14:42-14:54

A Tunable Low-Noise Amplifire for Digital TV Applications

Yoshimitsu Takamatsu, Ryuichi Fujimoto, Takaya Yasuda, Tsuyoshi Sekine, Takuya Hirakawa, Masato Ishii, Motohiko Hayashi, Nobuyuki Itoh

Semiconductor Company, Toshiba Corporation, Japan

Abstract: This paper presents a tunable low-noise amplifier (LNA) for digital TV (ISDB-T) applications. To receive all channels from 470MHz to 770MHz and to relax distortion characteristics of following circuit blocks such as an RF variable-gain amplifier and a mixer, tunable techniques for LNAs are required. A novel output matching configuration for tunable LNAs is proposed, and an input matching technique is also described. A tunable LNA using the proposed tunable techniques is fabricated using 90nm CMOS technology. Measured results show the proposed techniques are suitable for the LNAs for digital TV (ISDB-T) applications.

Session 11 - Low-power System Integration Techniques and Bio-medical DSPs

Time: 12:50-14:55

Room: VIP Floor V105

Chair: Fumio Arakawa (Renesas Technology Corporation)

Co-chair: Tai-Cheng Lee (National Taiwan University)

Session 11-1

Time: 12:50-13:15

A Micro-Network on Chip with 10-Gb/S Transmission Link

Wei-Chang Liu *(National Chiao Tung University, Taiwan),* Chih-Hsien Lin *(National Chiao Tung University, Taiwan),* Shyh-Jye Jou *(National Chiao Tung University, Taiwan),* Hung-Wen Lu *(National Chiao Tung University, Taiwan),* Chau-Chin Su *(National Chiao Tung University, Taiwan),* Kai-Wei Hong *(National Central University),* Kuo-Hsing Cheng *(National Central University),* Shyue-Wen Yang *(National Yunlin University of Science & Technology, Taiwan),* Ming-Hwa Sheu *(National Yunlin University of Science & Technology, Taiwan)*

Abstract: In this paper, a micro-network on chip (MNoC) with 10-Gb/s transmission link is proposed. A prototype system with two 5-port packet-based on-chip micro-switches and a 10-Gb/s data transceiver with an all digital data recovery circuit and a self-calibration clock generator are designed. This chip is implemented in 0.13£gm CMOS technology. The core area of this chip is 990£gm*1600£gm and the power consumption is 158mW (60mW for micro-switches and 98mW for 10-Gb/s data transceiver) at 1.2V supply voltage with 10-Gb/s transmission data rate.

Session 11-2

Time: 13:15-13:40

Geyser-1: a Mips R3000 CPU Core with Fine Grain Runtime Power Gating

Daisuke Ikebuchi, Naomi Seki, Yu Kojima, Masahiro Kamata, Lei Zhao, Hideharu Amano

KEIO University, Japan

Abstract: Geyser-1, a prototype MIPS R3000 CPU with fine grain runtime PG for major computational components in the execution stage is available.The evaluation results on the real chip reveals that the fine grain runtime PG mechanism works without electric problems.It reduces the leakage power 7% at 25 centigrade and 24% at 80centigrade.The evaluation results using benchmark programs show that the power consumption can be reduced from 3% at 25centigrade and 30% at 80 centigrade.

Session 11-3

Time: 13:40-14:05

A Low Cost, Low Power AES ASIC with High DPA Resisting Ability

Bo Yu, Xiangyu Li, Naiwen Zhang, Yihe Sun

Tsinghua University, China

Abstract: THUAES06 that implements the standard AES algorithm is characterized by low cost, low power and high differential power analysis (DPA) resisting ability enhancement. The DPA resisting ability enhancement is achieved by using fine grained shuffling as the DPA countermeasure of the main part and implementing vulnerable function unit with dual rail asynchronous circuits. THUAES06 is implemented in SMIC 0.18¦Ìm technology. Its average energy of encrypting or decrypting one 128 bits plaintext or cipher text is 19nJ if initial key need not to be changed. Its core area is 0.43mm2. The power traces needed to disclose the secrete keys are more than 33,000.

Session 11-4

Time: 14:05-14:30

A 130-uW, 64-Channel Spike-Sorting DSP Chip

Vaibhav Karkare, Sarah Gibson, Dejan Markovic

UCLA, USA

Abstract: Spike sorting is an important processing step in various neuroscientific and clinical studies. An on-chip spike-sorting DSP must provide data rate reduction while maintaining a power density much less than 800 uW/mm2. Most existing designs either provide only spike detection for multi-channel processing, or they provide detection and feature extraction only for a single channel. We demonstrate a chip for detection, alignment, and feature extraction simultaneously for 64 channels. Spike-sorting algorithms identified from a complexity-performance analysis are implemented on ASIC using a Matlab/Simulink based architecture design framework. The chip has a modular architecture which allows it to be configured to process 16, 32, 48, or 64 channels. Inactive cores are power-gated to reduce power consumption when the chip operates for less than 64 channels. The chip is implemented in a 90-nm CMOS process and has a power dissipation of 130 uW (power density of 20 uW/mm2) when processing all 64 channels. A data rate reduction of 91.25% (11.71 Mbps to 1.02 Mbps) is achieved.

Session 11-5

Time: 14:30-14:55

A Real-Time ECG QRS Detection ASIC Based on Wavelet Multiscale Analysis

Phyu Myint Wai

IME, Singapore

Abstract: This paper presents for the first time QRS detection algorithm implemented in Application Specific Integrated Circuit (ASIC). The algorithm based on the dyadic wavelet transform (DYWT) multiscale-product scheme is designed especially for real-time applications as well as it provides accurate detection of the QRS complex. The algorithm is evaluated based on the MIT-BIH database and achieves a sensitivity of 99.63% and a positive predictivity of 99.89% of R-waves detection. The results show that the algorithm outperforms several well-known QRS complex detection algorithms. The proposed algorithm is then implemented in ASIC and fabricated with 0.18-um CMOS technology and it consumes 176 uW at an operating frequency of 1 MHz with a supply voltage of 1.8 V.

Session 12 - Inductive Link and Clock Generation

Time: 12:50-14:55

Room: VIP Floor V110

Chair: Masaki Hirata (NEC)

Co-chair: Jri Lee (National Taiwan University)

Session 12-1

Time: 12:50-13:15

A 1.3pJ/B Inductive Coupling Transceiver with Adaptive Gain Control for Cm-Range 50Mbps Data Communication

Seulki Lee, Jerald Yoo, Kiseok Song, Hoi-Jun Yoo

Korea Advanced Institute of Science and Technology, Korea

Abstract: A 1.3pJ/b inductive coupling transceiver is proposed for Cm-range multimedia data transmission in mobile device applications. Its Transmission Time Control (TTC) scheme and Adaptive Gain Control (AGC) scheme reduce the energy consumption below to 1.3pJ/b. Inductor with self-resonance frequency above 200MHz achieves the data rate over 50Mbps. The receiver sensitivity can be enhanced to increase the communication distance up to 7cm by relative magnitude comparison between two nodes of the receiver inductor. The transceiver consumes only 65uW in total with 1V supply.

Session 12-2

Time: 13:15-13:40

A Wafer Test Method of Inductive-Coupling Link

Kazutaka Kasuga, Tsutomu Takeya, Mitsuko Saito, Hiroki Ishikuro, Tadahiro Kuroda

Keio University, Japan

Abstract: This paper provides the method for Wafer test of an inductive-coupling link. The inductive-coupling link can be tested whether it operates correctly before stacking chips. We provided the method that verify the operation of an inductive-coupling link from the relation between coupling coefficient of inductors and power that transmitter consumes.

Session 12-3

Time: 13:40-13:52

An Extended XY Coil for Noise Reduction in Inductive-Coupling Link

Mitsuko Saito, Kazutaka Kasuga, Tsutomu Takeya, Noriyuki Miura, Tadahiro Kuroda

Keio University, Japan

Abstract: Inductive-coupling link between stacked chips communicates by using on-chip coils. XY-coil layout style allows logic interconnections to go through the coil, which saves interconnection resources consumed by the coil. However, logic interconnections generate capacitive-coupling noise on the coil and degrade signal in the inductive-coupling link. Extended XY coil with ground shields is presented for noise reduction. Simulation study shows noise voltage is reduced to 1/5 of the conventional XY coil. This noise reduction reduces transmit power. Test-chip measurement in 0.18m CMOS demonstrates that the transmit power at 1Gb/s with BER<10-12 is reduced by 60% compared to the conventional XY coil.

Session 12-4

Time: 13:52-14:04

Loop Latency Reduction Technique for All-Digital Clock and Data Recovery Circuits

I-Fong Chen *(Graduate Institute of Electronics Engineering & Department of Electrical Engineering, National Taiwan University, Taiwan),* Rong-Jyi Yang *(Department of Electrical Engineering, National Taiwan University of Science and Technology, Taiwan),* Shen-Iuan Liu *(Graduate Institute of Electronics Engineering & Department of Electrical Engineering, National Taiwan University, Taiwan)*

Abstract: This paper presents an all-digital implemented clock and data recovery circuit. To alleviate the instability contributed by the large latency of digital loop filter, the architecture of two integral paths is proposed in this work. The loop latency from the digital loop filter can be removing by introducing a high speed pre-accumulator cascaded by a low speed accumulator. It increases the phase margin and also improves the loop stability. A smaller proportional gain for the digital loop filter can be chosen without sacrificing the stability. Hence the jitter performance can be improved. The experimental chip occupies a chip area of 0.432mm2 in standard 0.18ƒÝm CMOS technology. It consumes 23.4mW from a 1.8V supply and achieves a peak-to-peak jitter of 0.064 unit interval while operating at the bit rate of 1.25Gb/s.

Session 12-5

Time: 14:04-14:29

A 1.3-330-MHz Direct Clock Synthesizer for Display Interface Using Fractional Multimodulus Frequency Divider

Ho Young Song, Han-Kyu Chi, Heesoo Song, Deog-Kyoon Jeong

Seoul National University, Korea

Abstract: A 1.3-MHz to 330-MHz video clock synthesizer consisting of a fine-resolution fractional frequency divider and a divider-merged delta-sigma modulator (DSM) is presented. The proposed architecture provides a wide frequency range of output clock, and good jitter performance with reduced design complexity. Moreover, the divider-merged DSM guarantees the cycle-accurate frequency synthesis. The proposed fractional divider can divide the clock frequency with 4-bit fractional resolution using the proposed phase-switching technique. Fabricated in a 0.13-ƒÝm CMOS technology, the synthesizer has maximum peak-to-peak period jitter of 120 ps.

Session 12-6

Time: 14:29-14:54

A Delay-Locked Loop with Digital Background Calibration

Wei-Ming Lin, Kuang-Fu Teng, Shen-Iuan Liu

National Taiwan University, Taiwan

Abstract: A delay-locked loop (DLL) with digital background calibration is presented. The static phase error of a DLL may exist owing to the current mismatch in the charge pump (CP). A digital background calibration using the time amplifier is presented. This DLL is fabricated in a CMOS 0.18um technology. The measured input frequency range of this DLL is from 400MHz to 525MHz. The measured static phase error without and with calibration is 113.8ps and 27.8ps, respectively, at 525MHz. The measured peak-to-peak jitter without and with calibration is 15.56ps and 15.11ps, respectively. The power consumption is 25.2mW at 500MHz and the area is 0.85mm2.

Session 13 - Power Management

Time: 15:15-17:20

Room: 10F Song Bo Room

Chair: Yasuhiro Sugimoto (Chuo University, Japan)

Co-chair: Po-Chiun Huang (National Tsing Hua University)

Session 13-1

Time: 15:15-15:40

A DVS Embedded Power Management for High Efficiency Integrated SoC in UWB System

Yu-Huei Lee *(National Chiao Tung University, Taiwan),* Shih-Jung Wang *(National Chiao Tung University, Taiwan),* Yao-Yi Yang *(National Chiao Tung University, Taiwan),* Ke-Horng Chen *(National Chiao Tung University, Taiwan),* Ying-Hsi Lin *(Realtek Semiconductor Corporation, Taiwan)*

Abstract: This 65 nm power management module with 1 V low-voltage PWM controller and dynamic self-biasing mechanism aims to integrate with ultra-wideband (UWB) system to get high efficiency and compact size. The on-chip pre-regulator with power conditioning circuit provides a constant and noiseless supply voltage. Compensation enhancement multistage amplifier increases system loop gain and stabilizes the system without off-chip compensation circuit. Moreover, the proposed self-biasing mechanism enhances the power conversion efficiency by 4 % through the handover technique. With the excellent line/load transient response, the proposed power management has the highest efficiency about 93.5% and 0.356 mm2 silicon die area.

Session 13-2

Time: 15:40-16:05

Loop Bandwidth Extension Technique for PWM Voltage Mode DC-DC Switching Converters

Chenchang Zhan, Wing-Hung Ki

HKUST, China

Abstract: A loop bandwidth extension technique for voltage mode pulsewidth modulated switching converters operating in continuous conduction mode is proposed. The conventional fixed ramp is replaced by a ramp with a variable slope adjusted by the output voltage through a low power and area-efficient transconductance cell, pushing the complex pole pair of the LC filter to a higher frequency and hence improves the system loop bandwidth. Theoretical analysis is presented. A prototype buck converter with a maximum load current of 50mA is fabricated using a 0.35ƒÝm CMOS process, occupying an active area of 0.095mm2. Experimental results show that the proposed converter has reduced transient overshoot and undershoot, and settling times are reduced by 50% compared to a conventional voltage mode buck converter. The results match well with the theoretical analysis.

Session 13-3

Time: 16:05-16:30

An Integrated Linear Regulator with Fast Output Voltage Transition for SRAM Yield Improvement

Chun-Yen Tseng *(National Tsing Hua University, Taiwan),* Po-Chiun Huang *(National Tsing Hua University, Taiwan),* Li-Wen Wang *(Taiwan Semiconductor Manufacturing Company, Taiwan)*

Abstract: This work presents a fully integrated linear regulator design that can dynamically assign the SRAM cell voltage to increase the read/write margin. To minimize the timing overhead between read/write mode switches, this design adopts two separate feedback loops for bias and load regulations. Individual optimization for each loop makes fast reference tracking and load regulation possible. To verify this concept, a prototype LDO is realized with a 1.8-V 0.18£gm CMOS. The output voltage can be freely set between 0.9 and 1.7-V. The measured transition speed is 48ns/0.3V. The maximum current efficiency is 94.7% under a 20mA current loading.

Session 13-4

Time: 16:30-16:55

An Energy-Recycling (Er) Technique for Reducing Power Consumption of Field Color Sequential (FCS) RGB LEDs Backlight Module

Ming-Hsin Huang *(National Chiao Tung University, Taiwan),* Yueh-Chang Tsai *(National Chiao Tung University, Taiwan),* Shih-Wei Wang *(National Chiao Tung University, Taiwan),* Dian-Rung Wu *(National Chiao Tung University, Taiwan),* Ke-Horng Chen *(National Chiao Tung University, Taiwan),* Chien-Yu Chen *(Industrial Technology Research Institute, Taiwan)*

Abstract: A single driving module with field color sequential (FCS) LCD technology needs to dynamically switch output voltage between 40 V for 12 series G- and B- color LEDs and 26 V for 12 series R-color LEDs at related time cluster. Thus, an energy-recycling (ER) technology is proposed to accelerate voltage settling and save compressed energy when the driving voltage is pressed from 40 V to 26 V. Only one recycling capacitor and one Schottky diode are added into the power structure of synchronous boost converter for composing the proposed ER technology. A proposed energy-recycling mode (ERM) controller is plugged into a boundary current mode (BCM) controller to control energy delivering and recycling. The proposed ER technology was fabricated by TSMC 0.25 £gm 2.5/5 V BCD process. Experimental results demonstrate fast and efficient tracking performance of driving voltage is achieved.

Session 13-5

Time: 16:55-17:07

A Method for Realizing a Fast Response Time for the Output Current Change of a MOS Current-Mode Buck DC-DC Converter Which Utilizes a Quadratic and Vi

Toru Sai, Yasuhiro Sugimoto

Chuo University, Japan

Abstract: In this study, a fast response time of less than 10 us has been realized for the sudden output current change between 220 mA and 20 mA of a MOS current-mode buck DC-DC converter which utilizes a quadratic and input-voltage-dependent compensation slope. The test chip of a MOS current-mode buck DC-DC converter using a 0.35-um CMOS process and a 5 MHz clock realized a 40.8 mV output voltage change and a 7.2 us of the response time for the sudden output current change between 220 mA and 20 mA.

Session 13-6

Time: 17:07-17:19

Digitally Controlled Low-EMI Switching Converter with Random Pulse Position Modulation

Chien-Hung Tsai

National Cheng Kung University, Taiwan

Abstract: A fully digital controlled low-EMI switching converter combining RPPM (Random Pulse Position Modulation), our improved version of Hybrid DPWM (Digital Pulse Width Modulator) and AEDPWM (Area-Efficient DPWM) schemes is proposed to achieve low-EMI (Electromagnetic Interference) with reduced area and power consumption. A FPGA-controlled prototype buck converter operating at 1 MHz switching frequency with 1.8 V input voltage and 0.6-1.2V output voltage is presented to demonstrate the technique. The resulting switching noise suppression capability is up to 18 dB in average.

Session 14 - RF Transceivers and SoC

Time: 15:15-17:20

Room: 10F Chang Chin Room

Chair: Hyunchol Shin (Kwangwoon University)

Co-chair: Chien-Nan Kuo (National Chiao Tung University)

Session 14-1

Time: 15:15-15:40

A 1.2V 57mW Mobile ISDB-T SoC in 90nm CMOS

Jeong-Cheol Lee *(FCI, Korea),* Myung-Woon Hwang *(FCI, Korea),* Seokyong Hong *(FCI, Korea),* Moon-Kyung Ahn *(FCI, Korea),* Sengheon Jeong *(FCI, Korea),* Yong-Hun Oh *(FCI, Korea),* Hyunha Cho *(FCI, Korea),* Jechel Moon *(FCI, Korea),* Jong-Ryul Lee *(FCI, Korea),* Sangwoo Han *(FCI, Korea),* Che Handa *(Megachips Corporation, Japan),* Tomohito Fujie *(Megachips Corporation, Japan)*

Abstract: This paper presents a 1.2 V 57 mW SoC using a 90 nm CMOS process in mobile ISDB-T application. This achieves -98.5 dBm sensitivity at QPSK, CR = -2/3 with 2.5 dB NF of RF tuner block and 5.6 dB C/N of OFDM block at UHF-band. To integrate RF tuner and OFDM in a small single die, a wideband single LC-VCO operating from 1.8 GHz to 3.3 GHz is proposed and OFDM is designed by hard-wired logic.

Session 14-2

Time: 15:40-16:05

A Low Power 60GHz OOK Transceiver System in 90nm CMOS with Innovative on-Chip AMC Antenna

Fujiang Lin, James Brinkhoff, Kai Kang, Duy Dong Pham, Wooi Gan Yeoh

Institute of Microelectronics, Singapore

Abstract: Building on an efficient active and passive device modeling strategy, a 60 GHz OOK transceiver system including on-chip antenna in 90nm CMOS is designed. The key features of the circuits are small power consumption and size. With the modulator connected to an innovative artificial magnetic conductor (AMC) on-chip antenna, free space transmission at 2Gb/s is demonstrated. Also, an on-chip psuedo-link demonstrates 1Gb/s transmission, using only 26 pJ/bit for the modulator and 6 pJ/bit for the demodulator. The receiver consists of on-chip antenna, LNA with 20dB gain & 5.7dB noise figure, detector and limiting amplifier. Recovery of a 1.5Gb/s NRZ signal is demonstrated.

Session 14-3

Time: 16:05-16:30

A 400-MHz/900-MHz/2.4-GHz Multi-Band FSK Transmitter in 0.18-um CMOS

Kuan-Chao Liao, Po-Sheng Huang, Wei-Hao Chiu, Tsung-Hsien Lin

Graduate Institute of Electronics Engineering and Department of Electrical Engineering, Taiwan

Abstract: In this paper, a multi-band FSK Tx is implemented to operate at the 400-MHz/900-MHz/2.4-GHz bands. The Tx adopts a mixer-based architecture and is designed to support a data rate over 1 Mbps. To reduce the chip area, several inductor-less circuits are devised. A mixer which incorporates a Cherry-Hopper amplifier as the loading stage is proposed to widen the circuit bandwidth without resorting to the inductive-peaking technique. In the oscillator design, the proposed VCO adopts the current reuse principle to strengthen the latches for a given current. It achieves a higher frequency operation at lower power consumption, resulting in a better VCO FOM among inductor-less architectures. The proposed Tx is verified in a 0.18-um CMOS process, and is suitable for low-cost wireless applications.

Session 14-4

Time: 16:30-16:55

A DTR UWB Transmitter/Receiver Pair for Wireless Endoscope

Chul Kim*(University of New South Wales, Australia),* Saeid Nooshabadi *(Gwangju Institute of Science and Technology, Korea)*

Abstract: This paper introduces an ultra-wideband (UWB) system and its integrated circuit design for biotelemetry in-vivo wireless endoscope application that enables real-time diagnosis with high resolution images. The implemented UWB transmitter (Tx)/receiver (Rx) pair is a non-coherent differential transmit-reference (DTR) architecture. All-digital pulse generator (PG) Tx, and merged radio frequency (RF) Rx frond end including the low noise amplifier (LNA), mixer and low-pass filter (LPF) have been implemented along with the analog baseband using a 0.18um digital CMOS process. The PG operates at 200Mbps at an ultra low 27pJ/bit transmit energy.

Session 14-5

Time: 16:55-17:07

A 700-µW Single-Chip IC for Wireless Continuous-Time Healthcare Monitoring in 0.18-µm CMOS

Tee Hui Teo

Institute of Microelectronics, Agency for Science Technology and Research, Singapore

Abstract: A mixed-signal RF sensor node was designed and implemented in 0.18 um CMOS process. The sensor node consists of a sensor interface circuits, an analog-to-digital converter (ADC), a digital signal processor (DSP) unit and a radio-frequency (RF) transmitter unit. The sensor node was designed for use in a wireless health monitoring system. Only minimal off-chip components are allowed in this implementation for improved user experience, which are antenna, crystal resonator and supply decoupling capacitors. Low-power low voltage design techniques such as sub-threshold design were employed intensively to minimize the power consumption of the sensor node IC and maximize the battery life. The sensor consumes only about 700 ìW at 0.7 V supply and it enables continuous- and real-time electrocardiogram (ECG) monitoring for more than 200 hours without changing the battery when a typical button-cell battery is used.

Session 14-6

Time: 17:07-17:19

3-5GHz IR-UWB Timed Array Transmitter in 0.18µm CMOS

Shengxi Diao *(Institute of Microelectronics, Singapore),* Yuanjin Zheng *(Institute of Microelectronics, Singapore),* Yuan Gao *(Institute of Microelectronics, Singapore),* Chun-Huat Heng *(National University of Singapore, Singapore),* Xiaojun Yuan *(Institute of Microelectronics, Singapore)*

Abstract: This paper presents a dual-channel timed array transmitter for impulse radio ultra wideband wireless communication systems. The transmitter can generate UWB pulses in two separate transmitter paths with tunable path delay difference of 0-250ps to achieve beamforming capability. Through injection locking with 800MHz input reference, the generated UWB pulse centers at 4GHz and covers 3-5GHz band with 10-dB sideloble rejection. Fabricated in 0.18um CMOS technology, the transmitter cosumes 37mA at 10Mbps under 1.8V supply.

Session 15 - Digital Communication

Time: 15:15-17:20

Room: VIP Floor V105

Chair: Tomohisa Wada (University of the Ryukyus)

Co-chair: Zhiyi Yu (Fudan University)

Session 15-1

Time: 15:15-15:40

A Real-Time Programmable LDPC Decoder Chip for Arbitrary QC-LDPC Parity Check Matrices

Xin-Yu Shih, Cheng-Zhou Zhan, An-Yeu Wu

National Taiwan University, Taiwan

Abstract: For the applications of next-generation channel-adaptive communication systems, a real-time programmable LDPC decoder architecture is proposed with three design techniques: divided-group comparison (DGC), adaptive wordlength assignment (AWA), and efficient early termination scheme (EETS). By utilizing programmable principle, the hardware architecture can support arbitrary Quasi-Cyclic LDPC parity check matrices, including various locations of 1¡¦s, information bits, codeword lengths, and code rates. The prototyping LDPC decoder chip using 0.13um CMOS technology, which supports up to 23 code rates with a maximum block size of 1536 bits, only occupies 4.94 mm2 die area, operates at 125 MHz, and dissipates 58 mW power.

Session 15-2

Time: 15:40-16:05

A 26.9K 314.5Mbps Soft (32400, 32208) BCH Decoder Chip for DVB-S2 System

Yi-Min Lin, Chih-Lung Chen, Hsie-Chia Chang, Chen-Yi Lee

National Chiao Tung University, Taiwan

Abstract: This paper provides a soft BCH decoder using error magnitudes to deal with least reliable bits. With soft information from the previous decoder defined in digital video broadcasting (DVB), the proposed soft BCH decoder provides much lower complexity and latency than the traditional hard BCH decoder while still maintaining performance. The proposed error locator evaluator architecture evaluates error locations without Chien search, leading to high throughput. Borck-Pereyra error magnitudes solvers (BP-EMS) is presented to improve decoding efficiency and hardware complexity. The experimental result reveals that our proposed soft (32400, 32208) BCH decoder defined in DVB-S2 system can save 50.0% gate-count and 47.4% decoding latency in standard CMOS 90nm technology.

Session 15-3

Time: 16:05-16:30

A WiMAX Turbo Decorder with Tailbiting BIP Architecture

Hiroaki Arai *(Tohoku University, Japan),* Naoto Miyamoto *(Tohoku University, Japan),* Koji Kotani *(Tohoku University, Japan),* Hisanori Fujisawa *(Fujitsu Laboratories Ltd., Japan),* Takashi Ito *(Tohoku University, Japan)*

Abstract: A new pipelining architecture named tailbiting BIP is proposed for high-throughput and energy-efficient WiMAX turbo decoders. Conventional sliding window (SW) decoders suffer from many warm-up calculations and large memory size when the number of pipeline stages is increased. Instead of the SW, we combined the tailbiting method with BIP. Consequently, more than 50% of the warm-up calculation was reduced, and necessary memory size became constant. We have implemented a tailbiting BIP WiMAX turbo decoder with 4 pipeline stages in the area of 3.8 mm2 using 0.18-mm technology. The chip achieves 45 Mbps/iter and 3.11 nJ/b/iter at 99 MHz operation.

Session 15-4

Time: 16:30-16:50

A 62.8 mW 4X4 MIMO-OFDM Modem with One-Symbol-Locked Timing Recovery, Frequency-Dependent I/Q Mismatch Estimation and Adaptive Equalization

Ming-Fu Sun, You-Hsien Lin, Wei-Chi Lai Lai, Ta-Yang Juan, Cheng-Yuan Lee, Yen-Her Chen, Chang-Ying Chuang, Ternh-Yin Hsu

National Chiao Tung University, Taiwan

Abstract: A 4¡Ñ4 multi-input multi-output (MIMO) orthogonal frequency-division multiplexing (OFDM) modem with one-symbol-locked timing recovery, anti-I/Q mismatch frequency recovery, frequency-dependent I/Q mismatch estimation and adaptive equalization is implemented in 0.13-£gm CMOS library. This chip occupies 4.6¡Ñ4.6 mm^2 and consumes 62.8 mW at 1.2 V.

Session 15-5

Time: 16:50-17:15

A 5Mgate/414mW Networked Media SoC in 0.13um CMOS with 720p Multi-Standard Video Decoding

Ning Ma, Zhibo Pang, Jun Chen, Hannu Tenhunen, Li-Rong Zheng

iPack Vinn Excellence Center, Royal Institute of Technology (KTH), Sweden

Abstract: A flexible and high performance SoC is developed for networked media applications by integrating two RISC cores, Ethernet interface and coarse-grained configurable video decoding unit. Real-time MPEG-2/MPEG-4/RealVideo decoding is achieved for on-line video streams. The SoC is fabricated in 0.13um CMOS technology with die size of 6.4mm * 6.4mm. Flexible power management strategy is implemented. The maximum power consumption is 414mW at 1.2V supply voltage with the corresponding system frequency of 216MHz, when real-time HD (1280x720@25fps) video streams are decoded. The power consumption is reduced to 95mW for real-time CIF (352x288@25fps) video stream decoding at 27MHz system frequency.