IEEE Asian Solid-State Circuits Conference 2012
November 12-14, 2012
Kobe International Conference Center, Japan

"Integrated Circuits toward Smarter Society"

Integrated circuits improved the quality of human life in evolutionary and revolutionary ways by providing smart devices with internet access and electronic equipment with huge computing power. One of the emerging trends of integrated circuits is to apply the technology toward the smarter society, which drastically improves the quality of life of people with the aid of mass-producible electronic devices equipped with high performance & low power integrated circuits. Sensors, RF and analog circuits, data converters, and digital signal processing circuits will be required to implement the smart mobile devices which enable high-quality human life. State-of-the-art R&D results will be presented in the conference.

Plenary Talks (Nov. 13-14)

9:20-10:05, Nov. 13
"Expectations for the Semiconductor Technologies in EVs and HVs"
Dr. Shoichi Sasaki
Professor, Keio Univ. Japan

10:05-10:50, Nov. 13
"Semiconductor Memory Scaling and Beyond"
Dr. Sungjoo Hong
SVP, SK hynix Inc. Korea

9:00-9:45, Nov. 14
"Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment"
Dr. Ming-Fong Chen
Superintendent, NTU Hospital, Taiwan

9:45-10:30, Nov. 14
"Technology Challenges and Opportunities for Ubiquitous Computing"
Dr. Shekhar Borkar
Intel Fellow, Intel Corp. U.S.A.

Panel Discussions (Nov. 13)

Disruptive Design for Emerging Technology after 3D Devices/FinFET and Beyond; How Can We Make It ?

Organizer: Yung-Chow Peng, TSMC, Taiwan
Co-organizer: Youngmin Shin, Samsung, Korea, South
Moderator: Toshiro Hiramoto, The University of Tokyo, Japan
Panelists:
- Vinod Kariat, Cadence, Unite States
- Seiichiro Yamaguchi, Fujitsu, Japan
- Aaron Thean, IMEC, Belgium
- Jae Cheol Son, Samsung, Korea, South
- Jong-Ho Lee, Seoul National University, Korea, South
- Philippe Magarshack, STMicroelectronics, France
- Sally Liu, TSMC, Taiwan

Challenge for Zero Stand-by Power Management - Road-map to the "Normally-Off Computing" -

Organizer: Kazutami Arimoto, Okayama Prefecture Univ., Japan
Co-organizer: Toru Shimizu, Renesas Electronics, Japan
Moderator: Hiroshi Nakamura, The University of Tokyo, Japan
Panelists:
- S. Fujita, Toshiba, Japan
- H. J. Yoo, KAIST, Korea, South
- M. Hayashikoshi, Renesas Electronics, Japan
- H. Takada, Nagoya University, Japan
- Steven Bartling, Texas Instruments, United States
- TBD, IMEC, Belgium
- Shey-shi, National Taiwan University, Taiwan

Technical Sessions (Nov. 13-14)

Analog Interfaces and Amplifiers
Advanced Memory
TX/RX Architecture and Building Blocks
Energy Efficient Circuits and Techniques
High-Speed Transceivers and Building Blocks
Nyquist-Rate ADCs
Emerging Biomedical Circuits and Systems
Low-Power Digital Communication and Multimedia SoCs
Power Management ICs
Oversampling ADCs
Millimeter-Wave Circuits and Systems
Clock Generation and Timing Circuits
SSD Memory and High Frequency Analog
Ultra Low-Power Circuits for Emerging Communication Systems
VCO and PLL
Low-Power SoCs and Circuits

Tutorials (Nov. 12)

1. **SoC Power Reduction and Management Techniques**
   Stefan Rusu, Intel
2. **Designing CMOS Wireless LAN System-on-a-Chip**
   Srenik Mehta, Qualcomm Atheros
3. **High Performance SRAM Design in Deep Nanometer Technologies**
   Jente B Kuang, IBM
4. **Smart Sensor Design in Standard CMOS**
   Kofi Makinwa, Delft Univ. of Technology

Industry Sessions (Nov. 13)

1. **Leading Edge SoCs and Memory**
2. **Energy Efficient Circuits for Emerging Applications**

Early-bird registration is due on September 16

Online registration is available at:

http://www.a-sscc2012.org/

Organized by IEEE SSCS

A-SSCC 2012 Program at-a-glance

Monday, November 12

Time	Room 401 (4F)	Room 402 (4F)	Reception Hall (3F)	Lobby (4F)
9:00 - 9:30				
9:30 - 10:50	**Tutorial Ⅰ** "SoC Power Reduction and Management Techniques" Stefan Rusu (Intel)	**Tutorial Ⅱ** "Designing CMOS Wireless LAN System-on-a-Chip" Srenik Mehta (Qualcomm Atheros)		
10:50 - 11:05	**Break**			
11:05 - 12:25	**Tutorial Ⅰ** "SoC Power Reduction and Management Techniques" Stefan Rusu (Intel)	**Tutorial Ⅱ** "Designing CMOS Wireless LAN System-on-a-Chip" Srenik Mehta (Qualcomm Atheros)		
12:25 - 13:25	**Lunch**			**On-Site Registration (9:00-17:30)**
13:25 - 14:45	**Tutorial Ⅲ** "High Performance SRAM Design in Deep Nanometer Technologies" Jente B Kuang (IBM)	**Tutorial Ⅳ** "Smart Sensor Design in Standard CMOS" Prof. Kofi Makinwa (Delft Univ. of Technology)		
14:45 - 15:00	**Break**			
15:00 - 16:20	**Tutorial Ⅲ** "High Performance SRAM Design in Deep Nanometer Technologies" Jente B Kuang (IBM)	**Tutorial Ⅳ** "Smart Sensor Design in Standard CMOS" Prof. Kofi Makinwa (Delft Univ. of Technology)		
16:20 - 17:30			**Student Design Contest (SDC) Exibition**	
17:30 - 19:30	**Welcome Reception (Reception Hall)**			
19:45 - 20:45	**TCP Meeting (International Conference Room)**			

Tuesday, November 13

Time	International Conference Room Room 301 (3F)	Room 406 (4F)	Room 401,Room 402 (4F)	Room 403 (4F)	Reception Hall (3F)		Lobby
8:30 - 9:00							
9:00 - 9:10	**Opening Ceremony**						
9:10 - 9:20	**Welcome Speech**						
9:20 - 10:05	**Plenary Talk 1** "Expectations for the Semiconductor Technologies in EVs and HVs" Dr. Shoichi Sasaki (Keio Univ., Japan)						
10:05 - 10:50	**Plenary Talk 2** "Semiconductor Memory Scaling and Beyond" Dr. Sungjoo Hong (SK hynix Inc., Korea)						
10:50 - 11:05	**Break**				**SDC Exhibition**	**Supporter's Exhibition**	**On-Site Registration (8:30-17:30)**
11:05 - 12:45	**Industry Program 1** Leading Edge SoCs and Memory		**Industry Program 2** Energy Efficient Circuits for Emerging Applications				
12:4 5- 13:45	**Lunch**						
13:45 - 15:50	**Session 1** Analog Interfaces and Amplifiers	**Session 2** Advanced Memory	**Session 3** TX RX Architecture and Building Blocks	**Session 4** Energy Efficient Circuits and Techniques			
15:50 - 16:05	**Break**				**SDC Exhibition**		
16:05 - 17:45	**Panel Discussion 1** Disruptive design for emerging technology after 3D Devices/FinFET and beyond; How can make it?		**Panel Discussion 2** Challenge for Zero Stand-by Power Management - Road-map to the "Normally-Off				
17:45 - 18:00							
18:00 - 18:30	**move to Cruiser**						
19:00-21:20	**Banquet (Cruising in Kobe bay)**						

Wednesday, November 14

	International Conference Room Room 301 (3F)	Room 401 (4F)	Room 402 (4F)	Room 403 (4F)	Reception Hall (3F)	Lobby
8:30 - 9:00						
9:00 - 9:45	**Plenary Talk 3** "Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment" Dr. Ming-Fong Chen (NTU Hospital, Taiwan)					
9:45 - 10:30	**Plenary Talk 4** "Technology Challenges and Opportunities for Ubiquitous Computing" Dr. Shekhar Borkar (Intel, U.S.A.)					**On-Site Registration (8:30-12:00)**
10:30 - 10:45	**Break**					
10:45 - 12:50	**Session 5** High speed Transceivers and Building Block	**Session 6** Nyquist-Rate ADCs	**Session 7** Emerging Biomedical Circuits and Systems	**Session 8** Low-Power Digital Communication & Multimedia SoCs	**Supporter's Exhibition**	
12:50 - 13:50	**Lunch**					
13:50 - 15:55	**Session 9** Power Management ICs	**Session 10** Oversampling ADCs	**Session 11** Millimeter-Wave Circuits and Systems	**Session 12** Clock Generation and Timing Circuits		
15:55 - 16:10	**Break**					
16:10 - 18:15	**Session 13** SSD Memory and High Frequency Analog	**Session 14** Ultra Low-Power Circuits for Emerging Communication System	**Session 15** VCO & PLL	**Session 16** Low-Power SoCs & Circuits		

A-SSCC 2012 Tutorial -Monday, November 12

Monday, November 12
9:30-12:25 Tutorial I:
SoC Power Reduction and Management Techniques

Stefan Rusu, Intel

CMOS process technology scaling has enabled higher feature integration in system-on-chip with multiple CPU and graphics cores and larger on-die caches. Reducing and managing power consumption is the most challenging task in today's highly complex systems. In this tutorial, we will review power reduction and management techniques implemented in recent microprocessor and SoC designs, covering the entire spectrum from server to handheld applications. We will review flip-flop power optimization techniques, clock loading reduction, low-voltage operation, leakage reduction techniques, dynamic voltage and frequency scaling, and fine-grain power management techniques. Special attention will be devoted to adaptive circuit techniques that reduce the voltage and frequency design guard-bands. This tutorial includes recent innovations and practical examples from both industry and academic research.

9:30-12:25 Tutorial II:
Designing CMOS Wireless LAN System-on-a-Chip

Srenik Mehta, Qualcomm Atheros

Wireless LAN SoCs are ubiquitous today in mobile, computing, and consumer electronics. The simultaneous push for low-cost and high-performance has necessitated the use of scaled CMOS technology with extensive use of digital calibration. This tutorial provides an overview of the challenges in designing CMOS wireless LAN System-on-a-Chip from the perspective of an analog/RF designer. An overview of transceiver building blocks, integration issues, and calibration techniques are described. Two system-on-a-chip examples are presented to contrast the techniques required for low-cost highly integrated 1x1 WLAN SoC versus a high-performance 3x3 WLAN SoC.

13:25-16:20 Tutorial III:
High Performance SRAM Design in Deep Nanometer Technologies

Jente B Kuang, IBM

Multi-core processors demand larger on-die memories in order to maximize system performance. Further, continued scaling of the CMOS devices is being enabled through technological advancements such as fully depleted SOI, high -K metal gate, FinFETs with double gate and even further, three-dimensional circuits are being utilized to push the frontiers of high-performance circuits. All of these technological advancements present unique set of challenges to high performance memory design. This tutorial discusses trends and challenges in high performance SRAM design in deep nanometer technologies including memory designs across high performance and energy efficiency spectrum, assist circuits, reliability and memory design in exa-scale era.

13:25-16:20 Tutorial IV:
Smart Sensor Design in Standard CMOS

Prof. Kofi Makinwa, Delft University of Technology

Smart sensors are everywhere! They can be found in our homes, our cars and in nearly all mobile phones. However, processing weak sensor signals is quite challenging, especially when it must be done in standard CMOS, whose precision is limited by $1/f$ noise, component tolerances and mismatch. In this tutorial, a system approach to the design of smart sensors will be presented. The use of dynamic techniques, such as chopping, auto-zeroing, dynamic element matching and $\Sigma\Delta$ modulation, to trade speed for precision will be discussed. Examples will be given of state-of-the-art CMOS smart sensors for the measurement of temperature, humidity, magnetic field and even wind velocity.

Tuesday, November 13

9:20 -10:50 Plenary Session 1

09:20 **Plenary Talk 1: Expectations for the Semiconductor Technologies in EVs and HVs**
Dr. Shoichi Sasaki
Professor, Keio University, Japan

10:05 **Plenary Talk 2: Semiconductor Memory Scaling and Beyond**
Dr. Sungjoo Hong
Senior VP, Head of R&D Division, SK hynix Inc., Korea, South

11:05-12:45 Industry Session 1: Leading Edge SoCs and Memory

11:05 **The First 22 nm IA System-on-Chip Using tri-Gate Transistors**
S. Siers
Intel, United States

11:30 **A 1.94mm2, 38.17mW Dual VP8/H.264 Full-HD Encoder/ Decoder LSI for Social Network Services (SNS) Over Smart-Phones**
C. Ju, T. Liu, Y. Chen, K. Lee, C. Cheng, H. Chao, C. Wang, T. Wu, T. Lin, H. Chou, Y. Lin, C. Liu
Mediatek,Taiwan

11:55 **A High Performance 64Gb MLC NAND Flash Memory in 20nm CMOS Technology**
J. Park, S. Lee, K. Baek, C. Jeon, T. Kang, M. Kim, D. Choi, J. Choi, H. Chung, J. Kim, E. Jang, C. Lee
SK hynix semiconductor, Korea, South

12:20 **The Next Generation 64b S3 Core in a SPARC T4 Processor**
J. Shin, R. Golla, H. Li, S. Dash, M. Doherty, G. Grohoski, C. McAllister
Oracle, United States

11:05-12:45 Industry Session 2: Energy Efficient Circuits for Emerging Applications

11:05 **0.5V Start-Up 0.77mm2 Dual Drive Mode on-Chip Single-Inductor Dual-Output (SIDO) DC-DC Boost Converter for Battery and Solar Cell Operation Portable Equipments**
Y. Nakase, S. Hirose, H. Onoda, Y. Ido, Y. Shimizu, T. Oishi, T. Kumamoto, T. Shimizu
Renesas Electronics, Japan

11:30 **Circuit Design Challenges and Solutions for Optical Ring Modulators**
P. Amberg, E. Chang, F. Liu, J. Lexau, X. Zheng, G. Li, I. Shubin, J. Cunningham, A. Krishnamoorthy, R. Ho
Oracle Labs, United States

11:55 **A 0.5V 10MHz-to-100MHz 0.47uW/MHz Power Scalable Ad-PLL in 40nm CMOS**
Y. Hiraku{2}, I. Hayashi{2}, H. Chung{1}, T. Kuroda{1}, H. Ishikuro{1}
{1}Keio University, Japan; {2}Semiconductor Technology Academic Research Center, Japan

12:20 **A Low-Power 6.6-Gb/s Wireline Transceiver for Low-Cost FPGAs in 28nm CMOS**
J. Savoj, K. Hsieh, F. An, M. Buckley, J. Im, X. Jiang, A. Jose, V. Kireev, K. Lai, H. Pham, D. Turker, D. Wu, K. Chang
Xilinx, Inc., United States

13:45-15:50 Session 1: Analog Interfaces and Amplifiers

13:45 **An Energy-Efficient BBPLL-Based Force-Balanced Wheatstone Bridge Sensor-to-Digital Interface in 130nm CMOS**
J. Van Rethy, H. Danneels, V. De Smedt, W. Dehaene, G. Gielen
KU Leuven, Belgium

14:10 **An Integrated 12-V Electret Earphone Driver with Symmetric Cockcroft-Walton Pumping Topology for in-Ear Hearing Aids**
J. Tsai{2}, C. Tseng{2}, W. Tseng{2}, T. Shia{1}, P. Huang{2}
{1}Industrial Technology Research Institute, Taiwan; {2}National Tsing-Hua University, Taiwan

14:35 **A Chopper Stabilized Instrumentation Amplifier with Dual DC Cancellation Servo Loops for Biomedical Applications**
D. Han, Y. Zheng
Nanyang Technological University, Singapore

15:00 **A 0.02mV/C Digital Offset Compensation Technique for Comparators and Differential Amplifiers**
K. Wong, M. Le, K. Kim
Broadcom, United States

Tuesday, November 13

13:45-15:50 Session 1: Analog Interfaces and Amplifiers (Continued)

15:25 **A 1-V Low-Power Rail-to-Rail Operational Amplifier with High Programmable Accuracy**
S. Dai{2}, X. Cao{2}, T. Yi{2}, A. Hubbard{1}, Z. Hong{2}
{1}Boston Universtiy, United States; {2}Fudan University, China

13:45-15:50 Session 2 : Advanced Memory

13:45 **Adaptive Program Verify Scheme for Improving NAND Flash Memory Performance and Lifespan**
S. Park{1}, D. Shin{2}
{1}Samsung Electronics, Korea, South; {2}Sungkyunkwan University, Korea, South

14:10 **An Efficient BCH Decoder with 124-Bit Correctability for Multi-Channel SSD Applications**
H. Tsai, C. Yang, H. Chang
National Chiao Tung University, Taiwan

14:35 **A 250-MHz 18-Mb Full Ternary Cam with Low Voltage Match Line Sense Amplifier in 65nm CMOS**
I. Hayashi, T. Amano, N. Watanabe, Y. Yano, Y. Kuroda, M. Shirata, S. Morizane, K. Dosaka, K. Nii, H. Noda, H. Kawai
Renesas Electronics, Japan

15:00 **An Embedded Energy Monitoring Circuit for a 128kbit SRAM with Body-Biased Sense-Amplifiers**
Y. Sinangil, A. Chandrakasan
Massachusetts Institute of Technology, United States

15:25 **A 0.2V 16Kb 9T SRAM with Bitline Leakage Equalization and Cam-Assisted Write Performance Boosting for Improving Energy Efficiency**
B. Wang{2}, T. Nguyen{2}, J. Zhou{1}, M. Je{1}, T. Kim{2}, A. Do{2}
{1}Institute of Microelectronics, Singapore; {2}Nanyang Technological University, Singapore

13:45-15:50 Session 3 : TX RX Architecture and Building Blocks

13:45 **A Low-power Reconfigurable Multi-Band Sliding-IF Transceiver for WBAN Hubs in 0.18um CMOS**
L. Zhang, H. Jiang, J. Wei, J. Dong, W. Li, J. Gao, J. Cui, F. Li, B. Chi, C. Zhang, Z. Wang
Tsinghua University, China

14:10 **A 65nm CMOS, 1.5-mm2 Bluetooth Transceiver with Integrated Antenna Filter for Co-Existence with a WCDMA Transmitter**
M. Ashida, H. Majima, Y. Yoshihara, M. Nozawa, S. Oda, Y. Suzuki, H. Kobayashi, J. Deguchi, S. Kousai, R. Fujimoto, S. Ishizuka, S. Kawaguchi, Y. Unekawa, M. Hamada, T. Terada
Toshiba, Japan

14:35 **A Power-Efficient All-Digital IR-UWB Transmitter with Configurable Pulse Shaping by Utilizing a Digital Amplitude Modulation Technique**
S. Geng{2}, X. Chen{2}, W. Rhee{2}, J. Kim{1}, D. Kim{1}, Z. Wang{2}
{1}Samsung Advanced Institute of Technology, Korea, South; {2}Tsinghua University, China

15;00 **A 1.55mW Mixed-Signal Integrating Mixer for Direct Spectrum Estimation in 0.13um CMOS**
K. Banovic, A. Chan Carusone
University of Toronto, Canada

15:25 **A 2.4 GHz CMOS Doherty Power Amplifier with Dynamic Biasing Scheme**
K. Onizuka, K. Ikeuchi, S. Saigusa, S. Otaka
Toshiba, Japan

15:37 **A 3.0-W Wireless Power Receiver Circuit with 75-% Overall Efficiency**
Y. Moon{1}, Y. Roh{1}, C. Yoo{1}, D. Kim{2}
{1}Hanyang University, Korea, South; {2}Samsung Electronics, Korea, South

13:45-15:50 Session 4 : Energy Efficient Circuits and Techniques

13:45 **A Built-in Self-Adjustment Scheme with Adaptive Body Bias Using P/N-Sensitive Digital Monitor Circuits**
A. Islam, K. Norihiro, I. Tohru, O. Hidetoshi
Kyoto University, Japan

14:10 **Green Semiconductor Technology with Ultra-Low Power on-Chip Charge-Recycling Power Circuit and System**
S. Okura{2}, F. Morishita{2}, K. Arimoto{1}, L. Okamura{3}, T. Yoshihara{3}
{1}Okayama Prefectural University, Japan; {2}Renesas Electronics, Japan; {3}Waseda University, Japan

Tuesday, November 13

13:45–15:50 Session 4 : Energy Efficient Circuits and Techniques (Continued)

14:35 **On-Chip Dual-Ring-Oscillator-Based Random-Fluctuation-Measurement Method for Detecting Lowest Voltage in Adaptive Voltage Scaling Systems**
G. Ono, M. Owa, M. Nakayama, Y. Kanno
Hitachi, Japan

15:00 **Monitoring Effective Supply Voltage Within Power Rails of Integrated Circuits**
T. Okumoto, K. Yoshikawa, M. Nagata
Kobe University, Japan

15:25 **A 0.3-V All Digital Crystal-Less Clock Generator for Energy Harvester Applications**
J. Liu{1}, W. Lee{1}, H. Huang{3}, K. Cheng{2}, C. Huang{1}, Y. Liang{1}, J. Peng{1}, Y. Chu{1}
{1}Industrial Technology Research Institute
{2}National Central University, Taiwan;
{3}National Taipei University, Taiwan

16:05–17:45 Panel Discussion 1: Disruptive design for emerging technology after 3D Devices/FinFET and beyond; How can we make it ?

Organizer: Yung-Chow Peng, TSMC, Taiwan
Co-organizer: Youngmin Shih, Samsung, Korea, South
Moderator: Toshiro Hiramoto, The University of Tokyo, Japan
Panelist: Vinod Kariat, Cadence, United States
Seiichiro Yamaguchi , Fujitsu, Japan
Aaron Thean, IMEC, Belgium
Jae Cheol Son, Samsung, Korea, South
Jong-Ho Lee, Seoul National University, Korea, South
Philippe Magarshack, STMicroelectronics, France
Sally Liu, TSMC, Taiwan

16:05–17:45 Panel Discussion 2: Challenge for Zero Stand-by Power Management – Road-map to the "Normally-Off Computing"

Organizer: Kazutami Arimoto, Okayama Prefecture University, Japan
Co-organizer: Toru Shimizu, Renesas Electronics, Japan
Moderator: Hiroshi Nakamura, The University of Tokyo, Japan
Panelist: S. Fujita, Toshiba, Japan:
H. J. Yoo, KAIST, Korea, South
M. Hayashikoshi, Renesas Electronics, Japan
H. Takada, Nagoya University, Japan
Steven Bartling, Texas Instruments, United States
TBD, IMEC, Belgium
Shey-shi, National Taiwan University, Taiwan

18:00–20:00 Banquet

Wednesday, November 14

9:00–10:30 Plenary Session 2

09:00 **Plenary Talk 3: Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment**
Dr. Ming-Fong Chen
Superintendent, NTU Hospital, Taiwan

09:45 **Plenary Talk 4: Technology Challenges and Opportunities for Ubiquitous Computing**
Dr. Shekhar Borkar
Intel Fellow, Intel, United States

10:45–12:50 Session 5 : High Speed Transceivers and Building Block

10:45 **A 20Gb/s Adaptive Duobinary Transceiver**
S. Liu, I. Lee, Y. Ying
National Taiwan University, Taiwan

11:10 **A 2.3-mW, 5-Gb/s Decision-Feedback Equalizing Receiver Front-End with Static-Power-Free Signal Summation and CDR-Based Precursor ISI Reduction**
S. Son, H. Kim, M. Park, K. Kim, J. Kim
Seoul National University, Korea, South

11:35 **A 24-Gb/s Source-Series Terminated Driver with Inductor Peaking in 28-nm CMOS**
K. Suzuki, Y. Tomita, H. Yamaguchi, T. Cheung, T. Yamamoto, H. Tamura
Fujitsu Laboratories, Japan

Wednesday, November 14

10:45–12:50 Session 5 : High Speed Transceivers and Building Block (Continued)

12:00 **A 5 Gb/s 1/4-Rate Clock and Data Recovery Circuit Using Dynamic Stepwise Bang-Bang Phase Detector**
Y. Lee{2}, S. Chang{2}, R. Chu{2}, Y. Lin{2}, Y. Chen{2}, J. Goh{2}, C. Huang{1}
{1}Himax Technologies, Inc., Taiwan; {2}National Cheng-Kung University, Taiwan

12:25 **A 0.1-1.5 GHz 8-Bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection**
M. Chen, A. Hafez, C. Yang
UCLA, United States

10:45–12:50 Session 6: Nyquist-Rate ADCs

10:45 **A 1-GHz, 17.5-mW, 8-Bit Subranging ADC Using Offset-Cancelling Charge-Steering Amplifier**
K. Ohhata, H. Takase, M. Tateno, M. Arita, N. Imakake, Y. Yonemitsu
Kagoshima University, Japan

11:05 **Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/s Pipelined-SAR ADC**
Z. Jianyu, Z. Yan, S. Sai Weng, U. Seng Pan, M. Rui Paulo
Univ. of Macau, China

11:25 **A 12-Bit 8.47-fJ/Conversion-Step 1-MS/s SAR ADC Using Capacitor-Swapping Technique**
M. Wu, Y. Chung, H. Li
MediaTek, Taiwan

11:45 **A 40nm CMOS Full Asynchronous Nano-Watt SAR ADC with 98% Leakage Power Reduction by Boosted Self Power Gating**
R. Sekimoto, A. Shikata, K. Yoshioka, T. Kuroda, H. Ishikuro
Keio University, Japan

12:05 **A 0.05mm^2 0.6V 500kS/s 14.3fJ/Conversion-Step 11-Bit Two-Step Switching SAR ADC for 3-Dimensional Stacking CMOS Imager**
J. Lin{2}, H. Huang{2}, C. Hsieh{2}, H. Chen{1}
{1}Industrial Technology Research Institute, Taiwan;
{2}National Tsing Hua University, Taiwan

12:25 **A 9b 1GS/s 27mW Two-Stage Pipeline ADC in 45nm SOI-CMOS**
J. Pernillo{1}, M. Flynn{2}
{1}Univeristy of Michigan, United States; {2}University of Michigan, United States

10:45 – 12:50 Session 7 : Emerging Biomedical Circuits and Systems

10:45 **Ultrasonic Imaging Front-End Design for CMUT: a 3-Level 30Vpp Pulse-Shaping Pulser with Improved Efficiency and a Noise-Optimized Receiver**
K. Chen, A. Chandrakasan, C. Sodini
MIT, United States

11:10 **A Wirelessly Powered and Interrogated Blood Flow Monitoring Microsystem Fully Integrated with a Prosthetic Vascular Graft for Early Failure Detection**
J. Cheong{1}, C. Ho{1}, S. Ng{1}, R. Xue{1}, H. Cha{2}, P. Khannur{1}, X. Liu{1}, A. Lee{1}, W. Park{2}, L. Lim{1}, C. He{1}, M. Je{1}
{1}Institute of Microelectronics, A-STAR (Agency for Science, Technology and Research), Singapore;
{2}Seoul National University of Science and Technology, Korea, South

11:35 **An Inductively Powered CMOS Multichannel Bionic Neural Link for Peripheral Nerve Function Restoration**
K. Ng{3}, X. Liu{3}, J. Zhao{3}, S. Yen{3}, Y. Xu{3}, T. Tan{2}, M. Je{1}
{1}Institute of Microelectronic, Singapore; {2}National University Hospital, Singapore; {3}National University of Singapore, Singapore

12:00 **100-Channel Wireless Neural Recording System with 54-Mb/s Data Link and 40%-Efficiency Power Link**
M. Je{1}, K. Cheng{1}, X. Zou{1}, J. Cheong{1}, R. Xue{1}, Z. Chen{1}, L. Yao{1}, H. Cha{1}, S. Cheng{1}, P. Li{1}, L. Liu{2}, L. Andia{1}
{1}Institute of Microelectronics, A-STAR (Agency for Science, Technology and Research), Singapore;
{2}Nanyang Technological University, Singapore

12:25 **A Dynamic Impedance Matched Acupuncture-Type Diagnosis System with Concurrent Feedback of Physiological Signals**
K. Song, S. Hong, T. Roh, U. Ha, H. Yoo
KAIST, Korea, South

12:37 **A Single-Chip Time-Interleaved 32-Channel Analog Beamformer for Ultrasound Medical Imaging**
J. Um, J. Kim, E. Song, Y. Kim, J. Sim, H. Park
POSTECH, Korea, South

Wednesday, November 14

10:45-12:50 Session 8 : Low-Power Digital Communication and Multimedia SoCs

10:45 **A 40 nm 535 Mb/s Multiple Code-Rate Turbo Decoder Chip Using Reciprocal Dual Trellis**
C. Lin, C. Wong, H. Chang
National Chiao Tung University, Taiwan

11:10 **First (50,2,4) Nonbinary LDPC Convolutional Code Decoder Chip Over GF(256) in 90nm CMOS**
C. Lin, C. Chen, H. Chang, C. Lee
National Chiao Tung University, Taiwan

11:35 **A Successive Cancellation Decoder ASIC for a 1024-Bit Polar Code in 180nm CMOS**
A. Mishra{3}, A. Raymond{1}, L. Amaru{3}, G. Sarkis{1}, C. Leroux{2}, P. Meinerzhagen{3}, A. Burg{3}, W. Gross{1}
{1}McGill University, Montreal, Canada;
{2}Institut Polytechnique de Bordeaux, Bordeaux, France;
{3}EPFL, Switzerland

12:00 **Crisp-II: Coarse-Grained Reconfigurable Image Stream Processor for Image-Processing and Intelligent Operations in QFHD Video Cameras**
T. Cheng, L. Chen, S. Chien
National Taiwan University, Taiwan

12:25 **A Dynamic Resource Controller with Network-on-Chip for a 10.5nJ/Pixel Object Recognition Processor**
J. Oh, I. Hong, G. Kim, J. Park, H. Yoo
KAIST, Korea, South

12:37 **An 800Mhz Cryptographic Pairing Processor in 65nm CMOS**
Y. Li, J. Han, S. Wang, D. Fang, X. Zeng
Fudan University, China

13:50-15:55 Session 9 : Power Management ICs

13:50 **A Package Bondwire Based 80% Efficiency 80MHz Fully-Integrated Buck Converter with Precise DCM Operation and Enhanced Light-Load Efficiency**
C. Huang, P. Mok
The Hong Kong University of Science and Technology, Hong Kong

14:15 **A Single-Inductor Dual-Output (SIDO) Converter with Switchable Digital-or-Analog Low-Dropout Regulator for Ripple Supression and High Efficiency Operation**
Y. Lee{1}, W. Chen{1}, C. Chiu{1}, K. Chu{1}, K. Chen{1}, Y. Lin{2}, C. Huang{2}, C. Lee{2}
{1}National Chiao Tung University, Taiwan;
{2}Realtek Semiconductor,Taiwan

14:40 **Automatic Loading Dectection (ALD) Technique for 92% High Efficiency Interleaving Power Factor Correction (PFC) Over a Wide Ouptut Power of 180W**
J. Tsai
National Chiao Tung University, Taiwan, Taiwan

15:05 **A Chip-Area-Efficient CMOS Low-Dropout Regulator Using Wide-Swing Voltage Buffer with Parabolic Adaptive Biasing for Portable Applications**
Y. Liu, C. Zhan, L. Cheng, W. Ki
HKUST, Hong Kong

15:30 **A Low-Power and Low-Cost Digitally-Controlled Boost LED Driver IC for Backlights**
T. Oh, A. Cho, S. Ki, I. Hwang
Kangwon National University, Korea, South

13:50-15:55 Session 10: Oversampling ADCs

13:50 **A 1.2V 64fJ/Conversion-Step Continuous-Time ΣΔ Modulator Using Asynchronous SAR Quantizer and Digital ΔΣ Truncator**
H. Tsai, C. Lo, C. Ho, Y. Lin
MediaTek Inc., Taiwan

14:15 **A 7.5 mW 9 MHz CT ΔΣ Modulator in 65 nm CMOS with 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations**
M. Andersson{2}, M. Anderson{1}, L. Sundström{1}, P. Andreani{2}
{1}Ericsson AB, Sweden; {2}Lund University, Sweden

Wednesday, November 14

13:50-15:55 Session 10: Oversampling ADCs (Continued)

14:40 **A 101 dB DR 1.1 mW Audio ΔΣ Modulator with Direct-Charge-Transfer Adder and Noise Shaping Enhancement**
T. Wang{1}, W. Li{1}, H. Yoshizawa{2}, M. Aslan{3}, G. Temes{1}
{1}Oregon State University, United States; {2}Saitama Institute of Technology, Japan; {3}Texas Instruments, United States

15:05 **A 0.8 V 80.3 dB SNDR Stage-Shared ΔΣ Modulator with Chopper-Embedded Switched-Opamp for Biomedical Application**
C. Hsiao, W. Chen, C. Hsieh
National Tsing Hua University, Taiwan

15:30 **A 22.4uW 80dB SNDR ΣΔ Modulator with Passive Analog Adder and SAR Quantizer for EMG Application**
Z. Chen{2}, Y. Jiang{2}, C. Cai{2}, H. Wei{2}, S. Sin{2}, S. U{2}, Z. Wang{1}, R. Martins{2}
{1}Tsinghua University, China; {2}University of Macau, Macau

13:50-15:55 Session 11: Milimeter Wave Circuits and Systems

13:50 **A 245 GHz, 2.6mW/Pixel Antenna-Less CMOS Imager with 0.7fW/Hz^0.5 Nep and 3.5m Backscattered Range**
A. Tang, H. Wu, F. Chang
UCLA, United States

14:15 **A 34.8%-PAE CMOS Transmitter Frontend for 24-GHz FMCW Radar Applications**
H. Chen, L. Lu
National Taiwan University, Taiwan

14:40 **A 0.7V-to-1.0V 10.1 dBm-to-13.2 dBm 60-GHz Power Amplifier Using Digitally-Assisted LDO Considering HCI Issue**
R. Wu, Y. Tsukui, R. Minami, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Japan

15:05 **A 60 GHz Wideband Active Balun Using Magnitude and Phase Concurrent Correction *Technique in 65nm CMOS***
S. Chou, F. Huang, C. Wang
National Taiwan University, Taiwan

15:30 **A 60GHz VCO with 25.8% Tuning Range by Switching Return-Path in 65nm CMOS**
W. Fei, H. Yu, K. Yeo, W. Lim
Nanyang Technological University, Singapore

15:42 **A 60GHz CMOS Rectifier with -27.5dBm Sensitivity for mm-Wave Power Detection**
S. Kawai, T. Mitomo, S. Saigusa
Toshiba, Japan

13:50 - 15:55 Session 12 : Clock Generation and Timing Circuits

13:50 **A Spread Spectrum Clock Generator Using Phase/Frequency Boosting with a Peak Power Reduction 14.6dB, RMS Jitter 1.45ps and Power 4.8mW/GHz for USB 3.0**
Y. Choi, S. Jeon, B. Ki, J. Sim, H. Park
POSTECH, Korea, South

14:15 **A Multi-Phase Multi-Frequency Clock Generator Using Superharmonic Injection Locked Multipath Ring Oscillators As Frequency Dividers**
A. Hafez, M. Chen, K. Yang
UCLA, United States

14:40 **A High-Resolution Wide-Range Dual-Loop Digital Delay-Locked Loop Using a Hybrid Search Algorithm**
J. Kim, S. Han
Hongik University, Korea, South

15:05 **An All-Digital Phase-Locked Loop with Dynamic Phase Control for Fast Locking**
Y. Chuang, S. Tsai, C. Liu, T. Lin
National Taiwan University, Taiwan

15:30 **A Cint-Less Type-II PLL with ΔΣ DAC Based Frequency Acquisition and Reduced Quantization Noise**
Z. Zhang, X. Chen, W. Rhee, Z. Wang
Tsinghua University, China

15:42 **Delay-Line Based Fast-Locking All-Digital Pulsewidth-Control Circuit with Programmable Duty Cycle**
J. Su, T. Liao, C. Hung
National Chiao Tung University, Taiwan

16:10 – 18:15 Session 13: SSD Memory and High Frequency Analog

16:10 **Vset/Reset and Vpgm Generator Without Boosting Dead Time for 3D-ReRAM and NAND Flash Hybrid Solid-State Drives**
T. Hatanaka{2}, K. Takeuchi{1}
{1}Chuo University, Japan;
{2}Chuo University, The University of Tokyo, Japan

16:35 **An Integrated Variable Positive/Negative Temperature Coefficient Read Reference Generator for MLC PCM/NAND Hybrid 3D SSD**
K. Miyaji{1}, K. Johguchi{1}, K. Higuchi{2}, K. Takeuchi{1}
{1}Chuo University, Japan; {2}University of Tokyo, Japan

17:00 **A 5.8GHz Digital Arbitrary Phase-Setting Type II PLL in 65nm CMOS with 2.25deg Resolution**
L. Li{2}, M. Ferriss{1}, M. Flynn{2}
{1}IBM T. J. Watson Research Center, United States;
{2}University of Michigan, United States

17:25 **A 0.5V GFSK 200uW Limiter/Demodulator with Bulk-Driven Technique for Low-IF Bluetooth**
C. Lai, M. Shen, Y. Wu, P. Huang
National Tsing Hua university, Taiwan

17:50 **Wireless Wafer Probing for on-Chip Analog Voltage Measurement**
D. Lee, D. Wentzloff, J. Hayes
University of Michigan, United States

16:10 – 18:15 Session 14: Ultra Low-Power Circuits for Emerging Communication System

16:10 **Photovoltaic-Assisted CMOS Rectifier Circuit for Synergistic Energy Harvesting from Ambient Radio Wave**
K. Kotani, T. Bando, Y. Sasaki
Tohoku University, Japan

16:35 **A 45uW Injection-Locked FSK Wake-Up Receiver for Crystal-Less Wireless Body-Area-Network**
J. Bae, H. Yoo
KAIST, Korea, South

17:00 **A 2.4/5.8 GHz 10 µW Wake-Up Receiver with -65/-50 dBm Sensitivity Using Direct Active RF Detection**
K. Cheng{2}, X. Liu{1}, M. Je{1}
{1}Institute of Microelectronics, Singapore;
{2}National Cheng Kung University, Taiwan

17:25 **An Asymmetrical QPSK/OOK Transceiver SoC and 15:1 JPEG Encoder IC for Multifunction Wireless Capsule Endoscopy**
Y. Gao{2}, S. Cheng{2}, W. Toh{2}, Y. Kwok{1}, X. Chen{1}, W. Mok{1}, H. Win{1}, B. Zhao{2}, Y. Zheng{2}, S. Sun{1}, M. Je{2}, C. Heng{3}
{1}Institute for Infocomm Research, ASTAR, Singapore;
{2}Institute of Microelectronics, ASTAR, Singapore;
{3}National University of Singapore, Singapore

17:50 **A QPSK/16-QAM OFDM-Based 29.1Mbps LINC Transmitter for Body Channel Communication**
P. Tsai{2}, J. Chang{2}, T. Chen{1}, C. Lee{2}
{1}MediaTek, Taiwan;
{2}National Chiao-Tung University, Taiwan

18:02 **Continuous-Time High-Precision IR-UWB Ranging-System in 90 nm CMOS**
S. Sudalaiyandi, H. Hjortland, T. Vu, Ø. Næss, T. Lande
University of Oslo, Norway

16:10-18:15 Session 15 : VCO and PLL

16:10 **A 0.38 mm², 10MHz-6.6 GHz Quadrature Frequency Synthesizer Using Fractional-*N*- Injection-Locked Technique**
W. Deng, A. Musa, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Japan

16:35 **A 0.5-V 5.5-GHz Class-C-VCO-Based PLL with Ultra-Low-Power ILFD in 65 nm CMOS**
S. Ikeda, T. Kamimura, S. Lee, N. Kanemaru, H. Ito, N. Ishihara, K. Masu
Tokyo Institute of Technology, Japan

17:00 **An Energy-Efficient 2.4-GHz PSK/16-QAM Transmitter**
C. Lin{1}, Y. Liu{2}, C. Fu{3}, H. Lakdawala{3}, T. Lin{1}
{1}National Taiwan University, Taiwan, Taiwan;
{2}imec ¡V Holst Centre, Eindhoven, Netherlands;
{3}Intel, United States

16:10-18:15 Session 15 : VCO and PLL (Continued)

17:25 **Heterogeneous Coupled Ring Oscillator Arrays for Reduced Phase Noise at Lower Power Consumption**
P. Dubey{2}, D. Belot{2}, S. Chatterjee{1}
{1}IIT Delhi, India; {2}STMicroelectronics, France

17:50 **A Low Voltage Sub 300uW 2.5GHz Current Reuse VCO**
M. Taghivand{1}, M. Ghahramani{2}, M. Flynn{2}
{1}Stanford University, Qualcomm Atheros, United States;
{2}University of Michigan, United States

18:02 **4 GHz Locking Range and 0.19 pJ Low-Enegy Differential Dual-Modulus 10/11 Prescaler**
T. Mitsunaka{2}, M. Yamanoue{2}, K. Iizuka{2}, M. Fujishima{1}
{1}Hiroshima University, Japan; {2}SHARP, Japan

16:10-18:15 Session 16 : Low-Power SoCs and Circuits

16:10 **Real-Time Instruction-Cycle-Based Dynamic Voltage Scaling (iDVS) Power Management for Low-Power Digital Signal Processor (DSP) with 53% Energy Savings**
S. Peng
National Chiao Tung University, Taiwan

16:35 **Ultra-Low-Energy Near-Threshold Biomedical Signal Processor for Versatile Wireless Health Monitoring**
X. Liu, J. Zhou, X. Liao, C. Wang, J. Luo, M. Madihian, M. Je
Institute of Microelectronics, Singapore

17:00 **Performance and Side-Channel Attack Analysis of a Self Synchronous Montgomery Multiplier Processing Element for RSA in 40nm CMOS**
B. Devlin{2}, H. Ueki{1}, S. Mori{1}, S. Miyauchi{1}, M. Ikeda{2}, K. Asada{2}
{1}Renesas Electronics, Japan;
{2}The University of Tokyo, Japan

17:25 **A Body Bias Generator Compatible with Cell-Based Design Flow for Within-Die Variability Compensation**
N. Kamae, A. Tsuchiya, H. Onodera
Kyoto University, Japan

17:50 **Self-Test Methodology and Structures for Pre-Bond TSV Testing in 3D-IC System**
C. Wang, J. Zhou, B. Zhao, X. Liu, M. Je
Institute of Microeletronics, Singapore

Registration Fee (Japanese Yen)

	Type	Early-Bird	Late Registration	On-site Registration
		Until Sep. 16	Sept.17 - Oct. 31	Nov. 1 and after
Regular	IEEE Member	45,000	55,000	65,000
	Non-IEEE Member	60,000	70,000	80,000
Student	IEEE Member	20,000	26,000	32,000
	Non-IEEE Member	25,000	32,000	39,000
Additional Order				
Additional Banquet			12,000	
Additional Proceedings			6,000	
Additional Tutorial Book			4,000	
Additional Proceedings (CD-R only)			2,500	
Tutorials				
Tutorial (Regular)	One Session		10,000	
	Two Sessions		16,000	
	Daily (Four Sessions)		25,000	
Tutorial (for Students)	One Session		5,000	
	Two Sessions		9,000	
	Daily (Four Sessions)		13,000	

Early-bird registration is due on September 16

Online registration is available at:

http://www.a-sscc2012.org/

For further information, contact at:
a-sscc2012@semiconportal.com

Supporters

Supporter's Exhibition (Nov. 13 -14)

Affiliation	Overview
Agilent Technologies Japan, Ltd.	Communication with Foundry is very important for circuit designer. Which process is the best for my circuit? How the simulation model is accurate in the range of L, W and temp? But there is no good tool to communicate each other, before. MQA is the golden standard communication tool between foundry and circuit designer. Over 100 company have already use MQA. And Agilent EEsof EDA has many circuit design solution in ADS, GoldenGate and SystemVue, Fast Yield Contributor, Circuit Validation with real modulated signal, EM simulation on Virtuoso.
ATRENTA K.K.	Atrenta's SpyGlass® Predictive Analysis software platform significantly improves design efficiency for the world's leading semiconductor and consumer electronics companies. More than two hundred companies and thousands of design engineers worldwide rely on SpyGlass to reduce risk and cost before traditional EDA tools are deployed. Atrenta will be showing how SpyGlass addresses issues such as lint, power, clock synchronization, constraints, testability and routing congestion in their booth.
Mentor Graphics Japan Co., Ltd.	Mentor Graphics® is a leader in electronic design automation software. Our innovative products and solutions help engineers conquer design challenges in the increasingly complex worlds of board and chip design. At A-SSCC 2012, we demonstrate our new D2S backend solutions which are Pyxis products as our analog design environment tools, Olympus-SoC as our P&R tool, Calibre products as our physical verification tools and Tessent products as our test solution tools.
MIPS Technologies	MIPS Technologies as the leading microprocessor IP vendor will introduce the trend of the latest microprocessor technologies including our new and the industry's most efficient Aptiv(TM) microprocessor cores.
NEC Corporation	CyberWorkBench and EMIStream have been developed by NEC over the course of twenty years. CyberWorkBench is a C-based LSI design platform developed around the "All-in-C" paradigm that allows high level synthesis and verification of any ANSI-C or SystemC program generating high quality RTL. EMIStream is a PCB level EMI suppression support tool that can suppress undesirable EMI generated from PCB at an early design stage with EMI Design Rule Check and Power Plane Resonance Analysis features. For more information, visit us at www.cyberworkbench.comwww.emistream.com
OneSpin Solutions Japan K.K.	As the EDA provider with the broadest range of verification products, OneSpin Solutions GmbH is uniquely equipped to handle the verification requirements of both IC and FPGA designers. The technologies employed in OneSpin's products enable the designer to completely verify their designs, not to only check for specific behaviors. OneSpin representatives will be at A-SSCC to meet with designers in search of verification solutions utilizing formal verification, equivalence checking, advanced linting, and verification coverage analysis.
Renesas Electronics Corporation	Renesas Electronics, the world's number one supplier of microcontrollers, is a premier supplier of advanced semiconductor solutions including microcontrollers and a broad range of analog and power devices. At A-SSCC2012, Renesas will present the leading-edge low power MCU technology for smart equipments and demonstrate a unique solution "Smart Analog" for sensor applications.
ROHM Co., Ltd.	TBD
Semiconductor Technology Academic Research Center (STARC)	Semiconductor Technology Academic Research Center (STARC) was founded in December 1995 with investment from leading Japanese semiconductor companies. STARC will present Company Profile with following activities with academia and industry. -Joint research with universities -Education for LSI design engineers -Prototype fabrication support -Several open program between industry-academia or industry-industry And STARC will especially present summary of Extremely Low Power Project commissioned by METI and NEDO.

Conference Venue of A-SSCC 2012: Kobe International Conference Center

WHERE IN JAPAN:

Kobe is located in Hyogo Prefecture, one of several prefectures in the mid-west of Japan that, together, are known as the 'Kansai Region'. This is Japan's premier tourism area for overseas visitors making Kobe an ideal base city for visiting world heritage sites, both to the east and to the west. The Port of Kobe and its man-made islands are located on the north shore of the Osaka Bay.

EASY ACCESS:

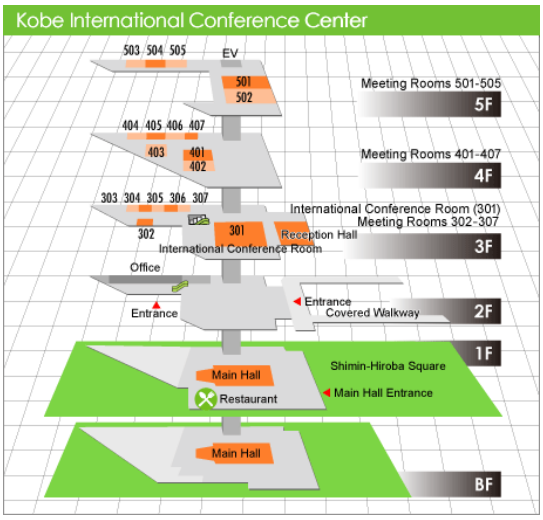
As a port city, built on a history of transportation, and with its own airport and Shinkansen station(Shin-Kobe), Kobe offers easy access for both domestic and overseas travelers.

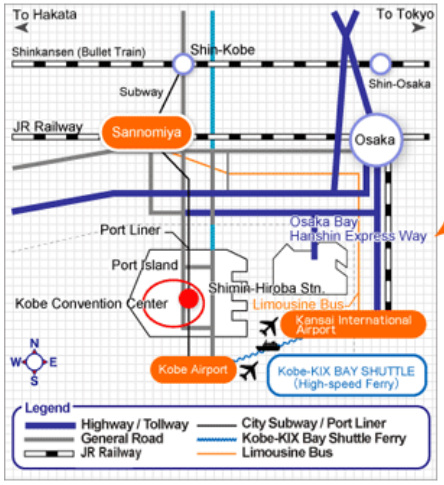
CONVENTION VENUES:

Closer to the airport than any other convention centers in Japan! Kobe Convention Center (the International Conference Center, International Exhibition Halls and other key venues) are located on Port Island, about 10 minutes from downtown Kobe (Sannomiya) and only 8 minutes from Kobe Airport.

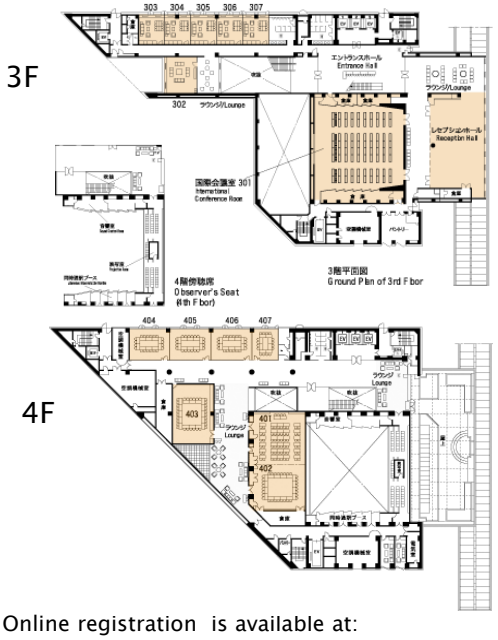
The Kobe International Conference Center has a Main Hall with seats for 692 people for plenary meetings and the International Conference Room has capacity for 360 delegates. Both provide a 6-language interpreting system for international audiences.

Kobe International Conference Center





http://kobe-cc.jp/english/access/index.html



Online registration is available at:

http://www.a-sscc2012.org/

For further information, contact at:
a-sscc2012@semiconportal.com