A-SSCC 2010

The 6th

IEEE Asian Solid-State Circuits Conference

Beijing, November 8-10, 2010

Advance Program

http://a-sscc2010.a-sscc.org

Tutorials

November 8, 2010 (Monday)

Tutorial 1

Time: 9:00-10:20, 10:40-12:00

Room: Crowne Ballroom A

An ultra low-power analog circuit and ADC design

Prof. Akira Matsuzawa, Tokyo Inst. Tech.

Tutorial 2

Time: 9:00-10:20, 10:40-12:00

Room: Conference Room 1

Embedded Memory Design in Nano-Scale CMOS Technology

Dr. Kevin Zhang, Intel

Tutorial 3

Time: 13:00-14:20, 14:40-16:00

Room: Crowne Ballroom A

Circuit-Level Power Management

Dr. Gordon Gammie, Texas Instrument

Tutorial 4

Time: 13:00-14:20, 14:40-16:00

Room: Conference Room 1

RF Integrated Circuit Design in Deep Submicron CMOS

Prof. John Long, TU Delft

Student Design Contest

November 8, 2010 (Monday)

Student Design Contest

Time: 16:00-17:30

Room: Foyer of Level 2

Minimized Transient and Steady-State Cross Regulation in 55nm CMOS Single-Inductor Dual-Output (SIDO) Step-Down DC-DC Converter

Yu-Huei Lee, National Chiao Tung University, Taiwan

A 2.1 μW Area-Efficient Capacitively-Coupled Chopper Instrumentation Amplifier for ECG Applications in 65 nm CMOS

Qinwen Fan, TU Delft, Netherlands

A 12-Bit 800-Ms/S Switched-Capacitor DAC with Open-Loop Output Driver and Digital Predistortion

Clayton Daigle, Stanford University, United States

A 1V 350μW 92dB SNDR 24 Khz ΔΣ Modulator in 0.18μm CMOS

Liyuan Liu, Tsinghua University, China

A Sub-mW All-Digital Signal Component Separator with Branch Mismacth Compensation for OFDM LINC Transmitters

Tsan-Wen Chen, National Chiao-Tung University, Taiwan

A 65nm 2.97GHz Self Synchronous FPGA with 42% Power Bounce Tolerance

Benjamin Devlin, University of Tokyo, Japan

A 92mW 76.8GOPS Vector Matching Processor with Parallel Huffman Decoder and Query Re-Ordering Buffer for Real-Time Object Recognition

Seungjin Lee, KAIST, Korea, South

A High-Speed, on-Chip Implementation of Teager Kaiser Operator for in-Band Interference Rejection

Waclaw Godycki, Cornell University, United States

A Low Data Rate FM-UWB Transmitter with Delta-Sigma Based Sub-Carrier Modulation and Quasi-Continuous Frequency-Locked Loop

Bo Zhou, Tsinghua University, China

A 31mA CMOS Wideband BD-II B2&B3 Mode Receiver with 55dB Gain Dynamic Range

Chuan Wang, Institute of Microelectronics, Peking University, China

A 58-63.6GHz Quadrature PLL Frequency Synthesizer in 65nm CMOS

Ahmed Musa, Tokyo Institute of Technology, Japan

A 0.8V 57GHz-to-72GHz Differential-Input Frequency Divider with Locking Range Optimization in 0.13μm CMOS

Sujiang Rong, The Hong Kong University of Science and Technology, Hong Kong

A Coreless Maximum Power Point Tracking Circuit of Thermoelectric Generators for Battery Charging Systems

Sungkyu Cho, Chungbuk National University, Korea

An Ultra-Low-Cost RFID Tag with 1.67 Gbps Data Rate by Inkjet Printing on Paper Substrate

Botao Shao, the Royal Institute of Technology (KTH), Sweden

November 9, 2010 (Tuesday)

Open Ceremony

Time: 8:15-8:20

Room: Crowne Ballroom A & B

Welcome Speech

Time: 8:25-8:35

Room: Crowne Ballroom A & B

Plenary Talk 1

Time: 8:35-9:20

Room: Crowne Ballroom A & B

Is 3D Integration the Way out of the Crossroads?

Dr. Cheng-Wen Wu

Vice President and General Director, ITRI-ICL, Taiwan

Abstract: In the past few years, we have witnessed the energy crisis and the financial tsunami that played an unwanted duo, changing the world in many aspects that affect most of us. While companies are working hard in getting out of the slump, many research organizations are rethinking how their R&D budget should be invested. We consider 3D integration based on the Through-Silicon-Via (TSV) technology a cost-effective way to explore new applications in the future, alleviating the fast growing development cost of system-on-chip (SOC) products. However, there are technical problems to be solved and business models to be established before the industry is ready for manufacturing TSV-based 3D integrated devices. In this talk we will first give an overview of the status of the worldwide semiconductor industry, identifying challenges and trends, which somewhat justify our focus on 3D integration. We will then discuss the design and test issues, and some solutions for 3D integrated devices. We will propose approaches from our work at ITRI and NTHU.

Plenary Talk 2

Time: 9:25-10:10

Room: Crowne Ballroom A & B

Future Television – Super Hi-Vision and Beyond

Dr. Takayuki Ito

Executive Research Engineer of NHK, Japan

Abstract: NHK is conducting research on two themes of future television; one is Super Hi-Vision and the other is integral 3DTV system. In the talk, outline of these two television systems will be introduced and impacts to the semiconductor industry will be discussed.

We consider Super Hi-Vision as the ultimate goal of two dimensional television system. It is designed to be viewed with 100 degrees of visual angle to provide viewers sensation of reality and immersive sensation as if they were at the site of video scene. This super reality television system requires sixteen times more resolution than current Hi-Vision. In the talk, the specification of Super Hi-Vision is explained and a road map toward introducing Super Hi-Vision to the home is shown.

Research on integral 3DTV will also be shown as a candidate of post Super Hi-Vision. In the talk, the ability of this system and current status of research will be introduced as well as break-throughs needed.

Industry Program 1 — Industrial Solutions to Silicon Scaling Challenges

Time: 10:40-12:10

Room: Crowne Ballroom A

Co-Chairs: Toru Shimize (Renesas)
Ting Wu (Rambus)

Industry 1-1 — 10:40-11:10

Asymmetric Cross-Coupled Sense Amplifier for Small-Sized 0.5-V Gigabit-DRAM Arrays

Akira Kotabe, Yoshimitsu Yanagawa, Riichiro Takemura, Tomonori Sekiguchi, Kiyoo Itoh

Hitachi, Ltd., Central Research Laboratory, Japan

Abstract: A new sense amplifier (SA) and relevant circuits were proposed for low-power, high-speed, and small-sized 0.5-V gigabit DRAM arrays. The SA, consisting of a low-VT NMOS preamplifier and a cross-coupled high-VT PMOS latch, achieved 46% area reduction compared to our previously proposed SA with a low-VT CMOS preamplifier. Separation of the SA and a data-line pair, and overdrive of the latch achieved a restoring time of 13.4 ns and a sensing time of 6 ns. An adaptive leakage control of the preamplifier reduced the leakage current of the SA to 2% of that without the control.

Industry 1-2 — 11:10-11:40

A 28 nm Dual-Port SRAM Macro with Screening Circuitry Against Write-Read Disturb Failure Issues

Yuichiro Ishii{2}, Hidehiro Fujiwara{2}, Shinji Tanaka{2}, Tomonori Doguchi{2}, Osamu Kuromiya{1}, Hideo Chigasaki{1}, Y. Tsukamoto{2}, Koji Nii{2}, Yuji Kihara{2}, Kazumasa Yanagisawa{2}

{1}Renesas Design Corporation, Japan; {2}Renesas Electronics Corporation, Japan

Abstract: We propose a circuit technique for an 8T dual-port (DP) SRAM in order to screen degraded minimum operating voltage (Vmin) due to the write/read disturb issue. This circuitry allows us to generate the write/read disturb condition without relying on the conventional costly asynchronous operation. We designed and fabricated a 512-kb DP-SRAM macro using 28-nm low-power CMOS technology, and confirmed assured screening of failures in the write/read disturb operations.

Industry 1-3 — 11:40-12:10

On-Chip CMOS Position Sensors Using Coherent Detection

Alex Chow, Ron Ho, David Hopkins, Darko Popovic

Oracle, United States

Abstract: The migration towards multi-chip integration in microelectronic systems has motivated the use of on-chip sensors for in situ measurement of chip alignment, both at initial assembly and during system operation. This paper presents a CMOS position sensor that measures chip alignment by measuring differences in coupling capacitance. Unlike previous implementations, the present demonstration is immune to transistor leakage current, and can thus operate at high temperatures. A coherent detection scheme further lowers the noise floor, improving accuracy when the chips are far apart.

Industry Program 2 — Processors

Time: 10:40-12:10

Room: Crowne Ballroom B

Co-Chairs: Stefan Rusu (Intel Corporation)

ShaoJun Wei (Tsinghua University)

Industry 2-1 — 10:40-11:10

A 48-Core IA-32 Processor with on-Die Message-Passing and DVFS for Performance and Power Scaling in 45nm CMOS

Jason Howard

Intel Corporation, United States

Abstract: This paper describes a microprocessor that integrates 48 IA-32 cores, 4 DDR3 memory channels, and a voltage regulator controller in a 6×4 2D-mesh network-on-chip topology. At each mesh node is a five-port packet-switched router shared between two cores. Core-to-core communication uses message passing while exploiting 384KB of on-die shared memory. Power management takes advantage of 8 voltage and 28 frequency islands to allow independent DVFS of cores and mesh. At the nominal 1.1V supply, cores operate at 1GHz and the 2D-mesh operates at 2GHz. The 567mm2 processor has 1.3 billion transistors, dissipates between 25W and 125W, and is implemented in 45nm Hi-K CMOS.

Industry 2-2 — 11:10-11:40

A 40nm 16-Core 128-Thread SPARC SoC Processor

Jinuk Luke Shin, Dawei Huang, Bruce Petrick, Changku Hwang, Ana Sonia Leon, Allan Strong

Oracle, United States

Abstract: A 16-core SPARC SoC processor enables up to 512 threads in a 4-way glueless system to maximize throughput. The 6MB L2Cache, 512GB/s Crossbar and the 312-pin SerDer IO of 2.4Tb/s support the required high bandwidth. Multiple power and clock domains as well as power management and circuit techniques, optimize performance, power, variability and yield trade-offs across the 377mm2 die.

Industry 2-3 — 11:40-12:10

Next Generation Intel® Atom™ Processor Based Ultra Low Power SoC for Handheld Applications

Rabiul Islam, Anil Sabbavarapu, Rajesh Patel, Manish Kumar, Jeff Nguyen, Binta Patel, Amrish Kontu

Intel Corporation, United States

Abstract: A new Intel ATOM processor based SoC is presented in 45nm low power CMOS technology. The design of the SoC is optimized for handheld applications to add performance features that are power efficient. Clock distribution and IO interfaces are optimized to reduce power. Power reduction techniques including extensive distributed power gating is deployed to the entire SoC to reduce both active and standby power. Measured S0i1 and S0i3 standby power numbers are 8mW and 70 micro-Watts respectively.

Session 1 — RF Transceivers and Building Blocks

Time: 13:10-15:15

Room: Crowne Ballroom A

Co-Chairs: Shouhei Kousai (Toshiba)

Julien Ryckaert (IMEC)

1-1 — 13:10-13:35

A Low Data Rate FM-UWB Transmitter with Delta-Sigma Based Sub-Carrier Modulation and Quasi-Continuous Frequency-Locked Loop

Bo Zhou, Rui He, Jian Qiao, Jinghui Liu, Woogeun Rhee, Zhihua Wang

Tsinghua University, China

Abstract: This paper describes the architecture and circuit design of a low data rate FM-UWB transmitter. A delta-sigma fractional-N PLL with a multi-phase relaxation oscillator is designed to enable sub-carrier modulation with reduced quantization noise. The triangular waveform output of the relaxation oscillator directly modulates an LC VCO to have the UWB-compliant spectrum. The center frequency of the LC VCO is quasi-continuously tuned by a delta-sigma DAC based frequency-locked loop with the power consumption of 1.1mW. The 3.43-4.03GHz FM-UWB transmitter implemented in 0.18μm CMOS consumes the total power of 9.6mW.

1-2 — 13:35-14:00

A 5.9mW 50Mbps CMOS QPSK/O-QPSK Transmitter Employing Injection Locking for Direct Modulation

Shengxi Diao{1}, Yuanjin Zheng{1}, Yuan Gao{1}, Xiaojun Yuan{1}, Minkyu Je{1}, Chun-Huat Heng{2}

{1}Agency for Science, Technology and Research / IME, Singapore; {2}National University of Singapore, Singapore

Abstract: A 900MHz QPSK/O-QPSK transmitter suitable for biomedical high quality imaging application is presented. The phase modulation is achieved by directly modifying the self-resonant frequency of a sub-harmonic injection-locked oscillator through capacitor bank switching. Due to the simplicity of the proposed architecture, implemented in 0.18μm CMOS technology, it consumes very low power of 3mW and 5.88mW with 1.2V and 1.4V supply voltages respectively, while transmitting at 50Mbps data rate. The transmitter can deliver output power of -3.3dBm at 1.4V supply with an EVM of 6.6%.

1-3 — 14:00-14:25

A 18 mW Tx, 22 mW Rx Transceiver for 2.45 GHz IEEE 802.15.4 WPAN in 0.18-μm CMOS

Kumarasamy Muthusamy Raja, Xuesong Chen, Yan Dan Lei, Zhao Bin, Ben Choi Yeung, Xiao-Jun Yuan

Agency for Science, Technology and Research / IME, Singapore

Abstract: This paper demonstrates a highly integrated transceiver for 802.15.4, consuming a dc power of 18 mW and 22.3 mW in the Tx and Rx mode respectively, which is the lowest reported so far. The gm boosted LNA shares the dc current with mixer, complex filter uses transistorized biquads, Limiting Amplifier and RSSI chain uses two local loops to save dc power. In the Tx, 2-point direct FSK modulation using normal sized varactors are used in the PLL, which not only obviates the need for auto calibration but also saves dc power due to the absence of DAC. The low IF receiver achieves a sensitivity of -94 dBm, an over load point of -20 dBm adjacent and alternate channel rejections of 40 dB and 55 dB respectively and a linear RSSI range of 89 dB. The transmitter delivers an OQPSK modulated signal of 0 dBm, with an EVM of 7% and the output spectrum meets the mask requirements of 802.15.4, FCC & ETSI. Implemented in 0.18um CMOS, loop filter and the crystal resonator for the PLL are the only external components apart from the decoupling capacitors.

1-4 14:25-14:50

A Linearity Improvement Technique for a Class-AB CMOS Power Amplifier with a Direct Feedback Path

Kun-Seok Lee, Hamhee Jeon, Youngchang Yoon, Hyungwook Kim, Jihwan Kim, Chang-Ho Lee

Georgia Institute of Technology, United States

Abstract: A new linearity improvement technique is introduced for a class-AB CMOS Power Amplifier (PA). The proposed PA has two stages and each stage has a cascode configuration. A direct feedback path from the input of the power stage to the input of the driver stage via an Accumulation-mode MOS (AMOS) varactor is adopted to improve the linearity. This additional path provides a negative feedback loop for the second-order harmonic, and the AMOS varactor controls the loop gain and the amount of the phase shift of the feedback signals. The proposed PA has been implemented in a standard 0.18μm CMOS technology. The measured results show that a gain of 21.4 dB, a maximum output power of 23.5 dBm with 43.1 % of peak Power-Added-Efficiency (PAE), and a linear output power of 21.4 dBm with 40 % PAE using a 1.85 GHz single tone. The two-tone test demonstrates 10 dBc improvement in the third-order Intermodulation Distortion (IMD3) compared to a conventional PA.

1-5 14:50-15:02

An Antenna Mismatch Immuned CMOS Power Amplifier

Youngchang Yoon{1}, Hyungwook Kim{1}, Kwanyeob Chae{1}, Jeongwon Cha{1}, Hyoungsoo Kim{2}, Chang-Ho Lee{1}

{1}Georgia Institute of Technology, United States; {2}University of North Texas, United States

Abstract: A 2.4 GHz reconfigurable CMOS power amplifier to minimize antenna mismatch effects is presented. The PA is implemented by using a 0.18μm RF CMOS process, and the supply voltage is 3.3 V. The proposed PA is compared to a conventional PA with a fixed matching network. By utilizing the proposed reconfigurable matching network, both the efficiency and the output power are improved under an antenna mismatch condition while satisfying the linearity specifications. For example, the maximum linear power and PAE are increased from 11.1-dBm to 16.1-dBm and from 8.1% to 19% at a $\Gamma = 0.3 \angle 45$ condition, respectively. To our knowledge, this is the first fully-integrated CMOS PA with a reconfigurable matching network that improves the robustness to the antenna mismatch.

1-6 15:02-15:14

A CMOS MedRadio Receiver RF Front-End with Complementary Current-Reuse LNA for Biomedical Applications

Hyouk-Kyu Cha, Kumarasamy Muthusamy Raja, Xiao-Jun Yuan, Minkyu Je

Agency for Science, Technology and Research / IME, Singapore

Abstract: An ultra-low-power 401-406 MHz Medical Device Radiocommunication Service (MedRadio) receiver RF front-end for biomedical telemetry applications is implemented using 0.18-μm CMOS technology with a 1-V supply voltage. The receiver RF front-end employs the proposed complementary current-reuse low-noise amplifier (CCRLNA) which shows enhanced noise and linearity performance in comparison to the well-known source degeneration cascode LNA at equal power consumption and design conditions. The RF front-end including the proposed CCRLNA,transconductor, I/Q folded mixer, and LO buffers achieves a conversion gain of 28.7 dB, NF of 5.5 dB, and IIP3 of -25 dBm while consuming less than 500 uW from a 1-V supply voltage and occupying 0.7mm^2 of core die area.

Session 2 — Power Management

Time: 13:10-15:15

Room: Crowne Ballroom B

Co-Chairs: Li Geng (Xi'an Jiaotong University)

Yasuhiro Sugimoto (Chuo University)

2-1 13:10-13:35

A Multi-Mode Digital Controller with Windowed ADC and Self-Calibrated DPWM for Slew-Enhanced Switching Converter

Po-Hsiang Lan, Chun-Yen Tseng, Feng-Chang Yeh, Po-Chiun Huang

National Tsing Hua Univ., Taiwan

Abstract: Windowed ADC is an attractive solution for the high efficiency digitally-controlled converters. However its limited conversion range restricts the transient speed for the dynamic voltage scaling applications. For slew rate improvement, this work designed a multi-mode PI/PID controller incorporated with the windowed ADC operation. In addition, to make output stable with no limit cycling, a current-controlled delay-line ADC and a DPWM with self calibration loops are proposed. The prototype chip is realized in a standard 0.18μm CMOS process. The switching frequency of the buck converter is up to 5MHz. The average current consumed in the digital controller, ADC and DPWM are 0.25, 0.2 and 0.7mA, respectively. The transient time from 1-V to 1.7-V step is 30us that is 2.5 times faster than the conventional linear controller design.

2-2 13:35-14:00

A 1-V Input, 0.2-V to 0.47-V Output Switched-Capacitor DC-DC Converter with Pulse Density and Width Modulation (PDWM) for 57% Ripple Reduction

Xin Zhang{2}, Yu Pu{2}, Koichi Ishida{2}, Yoshikatsu Ryu{1}, Yasuyuki Okuma{1}, Po-Hung Chen{2}, Kazunori Watanabe{1}, Takayasu Sakurai{2}, Makoto Takamiya{2}

{1}Semiconductor Technology Academic Research Center, Japan; {2}University of Tokyo, Japan

Abstract: A SC DC-DC converter with PDWM control scheme for high power efficiency, low output ripple is proposed and implemented using 65nm CMOS process. A control scheme using both PDM and PWM is introduced to enable a high efficiency with wide output current range, and suppress the output ripple with low output voltage, respectively. The proposed SC DC-DC converter has 0.2-V to 0.47-V output voltage and delivers 0.25-mA to 10-mA output current from a 1-V input supply with a peak efficiency of 87%. Compared with the conventional PDM, the proposed SC DC-DC converter with PDWM reduces the output ripple by 57% in the low output voltage region with the efficiency penalty of 2%.

2-3 14:00-14:25

Minimized Transient and Steady-State Cross Regulation in 55nm CMOS Single-Inductor Dual-Output (SIDO) Step-Down DC-DC Converter

Yu-Huei Lee{1}, Tzu-Chi Huang{1}, Yao-Yi Yang{1}, Ke-Horng Chen{1}, Ying-Hsi Lin{2}, Wen-Shen Chou{1}, Chen-Chih Huang{2}, Yi-Kuang Chen{2}

{1}National Chiao Tung University, Taiwan; {2}Realtek Semiconductor Corp., Taiwan

Abstract: A single-inductor dual-output (SIDO) step-down converter with continuous conduction mode (CCM) control is proposed for high efficiency system-on-a-chip (Soc) integration. The cross regulation in steady-state output voltage ripple, which is rarely mentioned, is effectively reduced as well as in transient response. The low-voltage energy distribution controller (LV-EDC) circuit guarantees good voltage regulation and low output voltage ripple simultaneously. In addition, within the allowable output voltage ripple, the automatic energy bypass (AEB) mechanism can reduce the number of energy delivery path to decrease the switching loss. Two outputs are operated with the load-dependent energy path for improving the power conversion efficiency. The chip fabricated in 55 nm CMOS achieves 91 % peak efficiency, low output voltage ripple, and excellent load transient

response.

2-4 14:25-14:50

A Right-Half-Plane (RHP) Zero Alleviating Skill in the Solid-Duty-Control (SDC) Boost Converter

Han-Hsiang Huang, Dian-Rung Wu, Ke-Horng Chen

National Chiao Tung University, Taiwan

Abstract: This paper proposed a solid-duty-control technique in the boost converter to keep a constant duty control to reduce dip voltage during load transient period. Besides, due to variable transient enhancement controller, fast transient response is achieved. The proposed SDC technique can provide a stable and regulated output for edge-lit LED backlight systems. Compared to conventional design without any fast transient technique, experimental results show the undershoot voltage and recovery time are improved 30 % and 80 %, respectively.

2-5 14:50-15:02

Design of High Output Current, High Switching Frequency Current Mode Buck DC-DC Regulator in WLCSP for Portable Applications

Bin Shao, Bill Liu

Analog Devices, Inc., China

Abstract: the paper introduces a high output current and high switching frequency buck DC-DC regulator with gate scaling function to improve the efficiency at light load together with reduced output voltage ripple and noise. External FET driver is also implemented as an option to move the excessive heat from inside the chip for thermal sensitive applications. A fast current sensing loop method is used to minimize the limitation of minimum on time of the conventional current mode buck converter. A guardring strategy for power MOSFET to prevent the latch up and minority carrier injection is also discussed. It is fabricated in TSMC 0.35um CMOS process with dual-poly and quad-metal. The WLCSP (Wafer Level Chip Scale Package) is used to minimize the parasitic, as well as to reduce the board size in application. The measurement result reaches nearly 85% efficiency at 2A load current when input voltage is 3.6V and output voltage is 1.1V.

2-6 15:02-15:14

A CMOS Bandgap and Sub-Bandgap Voltage Reference Circuits for Nano-Power LSIs

Tetsuya Hirose{2}, Ken Ueno{1}, Nobutaka Kuroki{2}, Masahiro Numa{2}

{1}Hokkaido University, Japan; {2}Kobe University, Japan

Abstract: This paper proposes CMOS bandgap reference (BGR) and sub-BGR circuits without resistors for nano-power LSIs. The BGR circuit consists of a nano-ampere current reference, a bipolar transistor, and a proportional to absolute temperature (PTAT) voltage generator. The PTAT voltage generator consists of source-coupled differential pairs and generates a positive temperature dependent voltage. The PTAT voltage generator cancels negative temperature dependence of a base-emitter voltage in a PNP bipolar transistor. The circuit generates a bandgap voltage of silicon. The sub-BGR circuit uses a voltage divider to generate low-voltage bandgap reference. Experimental results demonstrated that the BGR and sub-BGR circuits can generate a 1.18-V and 553-mV reference voltages, respectively. The power dissipation of the BGR and sub-BGR circuits were 108-nW and 110-nW, respectively.

Session 3 — High-speed Links

Time: 13:10-15:15

Room: Conference Room 8

Co-Chairs: Hiroyuki Okada (Renesas Electronics Corporation)

Woogeun Rhee (Tsinghua University)

3-1 — 13:10-13:35

A 30Gb/S/Link 2.2Tb/S/mm2 Inductively-Coupled Injection-Locking CDR

Yasuhiro Take, Noriyuki Miura, Tadahiro Kuroda

Keio University, Japan

Abstract: This paper presents a 30Gb/s/link 2.2Tb/s/mm2 inductive-coupling link for a high-speed DRAM interface. The data rate per layout area is the highest among DRAM interfaces reported up to now. The proposed interface employs a high-speed injection-locking CDR technique that utilizes the derivative property of inductive coupling. Compared to conventional injection-locking CDR based on an XOR edge detector, our technique doubles the operation speed and increases the data rate to 30Gb/s/link. As a result, the data rate per layout area is increased to 2.2Tb/s/mm2, which is 2X that of the state-of-the-art inductive-coupling link, and 22X that of the state-of-the-art wired link.

3-2 — 13:35-14:00

A 5-Gb/S Digitally Controlled 3-Tap DFE Receiver for Serial Communications

Jae-Duk Han{3}, Woo-Yeol Shin{1}, Woo-Seok Choi{1}, Jung-Hoon Chun{2}, Suhwan Kim{1}, Deog-Kyoon Jeong{1}

{1}Seoul National University, Korea, South; {2}Sungkyunkwan University, Korea, South; {3}Tli Inc., Korea, South

Abstract: Decision feedback equalizers (DFEs) play a critical role in high-speed communications through band-limited channels. We implemented a 3-tap DFE receiver for 5-Gb/s data bandwidth. To realize a multi-tap DFE operation, a digital-control scheme is proposed that does not use analog circuits for biasing, such as DACs. In addition to the conventional loop unrolling, several techniques including combined feedback are used to reduce the latency of the feedback path. Fabricated in a 0.13µm CMOS process, the prototype of the proposed DFE core has an area of 0.009 mm^2 and consumes 8.4 mW from a 1.2-V supply, achieving a BER of less than 10^-11 over a pair of 28-inch Nelco 4000-6 board traces.

3-3 — 14:00-14:25

A 0.8V 57GHz-to-72GHz Differential-Input Frequency Divider with Locking Range Optimization in 0.13µm CMOS

Sujiang Rong, Howard C. Luong

Hong Kong University of Science and Technology, Hong Kong

Abstract: A current-bleeding technique is presented to enhance and maximize the locking range of a differential-input Miller divider (MD) without extra inductor and extra power. The maximum locking range and the associated optimal bleeding current to achieve minimum required output amplitude are derived. Implemented in a 0.13 micron CMOS technology and with 0dBm input power, the divider prototype measures a locking range of 23.2% from 56.7GHz to 71.6GHz, which is enhanced more than 5 times compared to that of the conventional MD, while consuming the same power of 5mW at 0.8V supply.

3-4 14:25-14:50

A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO Using E-TSPC Frequency Divider with Forward Body Bias for Sub-Picosecond Jitter Clock Generation

Wei Deng, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: This paper investigates the adoption of LC-VCO to replace ring VCO for ultra-low-voltage sub-picosecond jitter clock generation in future 0.5-V LSI and power aware LSI. A 0.5-V LC-VCO using E-TSPC frequency divider with forward body bias technique is proposed and implemented. Significant performances, in terms of 0.6-ps jitter, 50MHz-to-6.4GHz frequency tuning range with 2 bands and sub-1mW Pdc, have been achieved in the measurement results.

3-5 14:50-15:02

A 10-Gb/S Optical Receiver Front-End with 5-mW Transimpedance Amplifier

Kyu-Sang Park{2}, Byoung-Joo Yoo{3}, Moon-Sang Hwang{3}, Hankyu Chi{3}, Hyun-Chang Kim{3}, Jeong-Woo Park{1}, Kyungock Kim{1}, Deog-Kyoon Jeong{3}

{1}Electronics and Telecommunication Research Institute, Korea, South; {2}GCT Semiconductor Inc., United States; {3}Seoul National University, Korea, South

Abstract: This paper describes a 10-Gb/s optical receiver front-end fabricated in a 0.13μm CMOS technology. To realize a wide bandwidth transimpedance amplifier (TIA) when the input parasitic capacitance is large, an area-efficient stacked spiral transformer is implemented. By using a capacitance multiplication technique, the baseline wander resulting from a current offset cancellation is minimized. The TIA achieves a transimpedance gain of 58.5dBΩ, an area of 0.02mm^2, and a bandwidth of 7.9GHz. The limiting amplifiers (LAs) following the TIA use negative impedance converters to enhance the bandwidth. The TIA and the LAs consume 5mW and 28.4mW, respectively with a supply voltage of 1.2V.

3-6 15:02-15:14

A 1.0Gb/S/ch Clock-Shared Differential Signaling(CSDS) Tx Using Termination Resistance Tuning and Multi-Phase Clock Spreading for EMI Reduction

Kyoung-Hoi Koo, Jaejin Park, Donguk Park, Eon-Guk Kim, Seungho Lee, Bongjae Kwon, YoungKeun Lee, Kyu-Myung Choi

Samsung Electronics, Korea, South

Abstract: A Clock-shared differential signaling(CSDS) transmitter is fabricated in 0.13 μm CMOS for 120 Hz 10-bit FullHD TVs. The proposed Tx driver takes advantages of PVT-insensitive tunable termination resistance with double feedback loops, and small reference voltage fluctuation. Moreover, a fully-digital duty cycle corrector is proposed, and compared to non-clock spreading, the relative near-field EMIlevel of multi-phase clock spreading is enhanced by 4.4 dB at the operating frequency of 500 MHz. The CSDS Tx with 34 channels consumes 300mW at a 2.5 V power supply and 1.0Gb/s/ch.

Session 4 — Emerging Circuit Technologies

Time: 13:10-15:15

Room: Conference Room 9

Co-Chairs: Reiji Hattori (Kyushu University)

Chi-Cheng Ju (MediaTek Inc.)

4-1 — 13:10-13:35

A 0.18μm CMOS Single-Photon Sensor for Coaxial Laser Rangefinders

Cristiano Niclass, Mineki Soga, Satoru Kato

Toyota Central R&D Labs, Inc., Japan

Abstract: This paper introduces a low-noise single-photon sensor in a 0.18μm CMOS technology for scanning-based coaxial optical rangefinders. At the core of the sensor, macro pixels consisting of 10x10 single-photon detectors enable time-of-flight measurements by taking advantage of temporal and spatial correlations. Unlike conventional silicon photo-multipliers, or multi-pixel photon counters, our sensor features a pulse-shaping and summing stage that accurately resolves the number of quasi-simultaneous photon detections. Sensor characterization data are reported. When mounted on a practical rangefinder setup, the sensor enables distance measurements up to 50 meters with repeatability error lower than 26cm throughout the range, using 10 laser pulses.

4-2 — 13:35-14:00

An Ultra-Low-Cost RFID Tag with 1.67 Gbps Data Rate by Inkjet Printing on Paper Substrate

Botao Shao{2}, Qiang Chen{2}, Yasar Amin{2}, David Sarmiento Mendoza{2}, Ran Liu{1}, Li-Rong Zheng{2}

{1}Fudan University, China; {2}Royal Institute of Technology, Sweden

Abstract: A fully metallic inkjet printed passive RFID tag on paper substrate is presented. The tag consists of an ultra-wide-band antenna, a microstrip transmission line with distributed shunt capacitors as information coding element which is reconfigurable by inkjet printing process. Tapered microstrip line is employed to overcome the limitation of low conductivity and thin film thickness of inkjet printed metal tracks. Measurement results show that the tag features a robust readability over 80 cm reading distance and a high data rate of 1.67 Gb/s

4-3 — 14:00-14:12

Low Noise Capacitive Sensor for Multi-Touch Mobile handset's Applications

Seunghoon Ko{1}, Hyungcheol Shin{1}, Jaemin Lee{1}, Hongjae Jang{1}, Kwyro Lee{1}, Byeong-Cheol So{2}, Ilhyun Yun{2}

{1}Korea Advanced Institute of Science and Technology, Korea, South; {2}SAIN InfoCom, Korea, South

Abstract: This paper presents a capacitive sensor design for multiple channels at the X-Y crossing of ITO patterns on the LCD panel.

4-4 14:12-14:24

Energy Efficient Current-Mode Signaling Scheme

Marshnil Dave, Mahavir Jain, Rajkumar Satkuri, Maryam Shojaei Baghini, Dinesh Sharma

Indian Institute of Technology, Bombay, India

Abstract: This paper describes a novel energy-efficient current-mode signaling scheme (CMS scheme) for long on-chip interconnects. The scheme was fabricated in 180nm process. Measurement results show that the proposed 6mm long link offers 22% improvement in delay for 81% lower energy consumption at 0.62Gbps over voltage-mode scheme. While being less sensitive to intra-die variations, the proposed scheme offers 20% improvement in power-delay-product over the CMS scheme proposed by Katoch et al. in [5].

4-5 14:24-14:49

A 65nm 2.97GHz Self Synchronous FPGA with 42% Power Bounce Tolerance

Benjamin Devlin, Makoto Ikeda, Kunihiro Asada

University of Tokyo, Japan

Abstract: We have designed and measured the performance and robustness to PVT variations of an improved Self Synchronous FPGA (SSFPGA) in 65nm CMOS which achieves 2.97GHz throughput at 1.2V. The proposed SSFPGA employs a 38x38 array of 4-input,3-stage Self Synchronous Configurable Logic Blocks (SSCLB), with the introduction of a new dual tree-divider 4 input LUT to achieve a 4.5x throughput improvement over our previous model. We have measured correct operation with 500mVp-p, 1.12GHz externally introduced power supply noise at 1.2V power supply, equivalent to 42% power supply bounce. We have measured the sensitivity against power supply noise frequency, and showed that the sensitivity has a strong correlation with the average operating frequency. Results show the SSFPGA can adapt and is inherently robust to these variations with a internal throughput measured ranging from 300MHz to 4.07GHz, while maintaining correct operation.

4-6 14:49-15:14

On-Chip Sine-Wave Noise Generator for Analog IP Noise Tolerance Measurement

Masaaki Soda{2}, Yoji Bando{1}, Satoshi Takaya{1}, Toru Ohkawa{2}, Toshiharu Takaramoto{2}, Toshio Yamada{2}, Shigetaka Kumashiro{2}, Tohru Mogami{2}, Makoto Nagata{1}

{1}Kobe University, Japan; {2}Selete, Japan

Abstract: A sine-wave noise generator with harmonic eliminated waveform is proposed for measuring noise tolerance of Analog IPs. In the waveform, the harmonics till 13th are eliminated by combining seven rectangular waves with 22.5 degree spacing phases. This waveform includes only high region frequency harmonic components which are easily suppressed by low-order filter. In the circuit, the harmonic eliminated waveform generator is combined with a current controlled oscillator and a frequency adjustment circuit. The sine-wave noise generator can generate power line noise from 20 MHz to 220 MHz with 1 MHz step. The SFDR of 45 dB is obtained at 100 MHz noise frequency.

Panel Discussion 1

Time: 15:45-17:25

Room: Crowne Ballroom A

What lies ahead for devices that realize a “symbiotic society”?

Organizer: Tadahiro Kuroda, Keio Univ., Japan

Moderator: Masayuki Mizuno, Renesas Electronics, Japan

Panelists: Rudy Lauwereins, IMEC
Tsutomu Matsumoto, Yokohama National Univ.
Someone from ADI
Baher Haroun, TI
Akira Matsuzawa, Tokyo Institute of Technology
Someone from Renesas Electronics

Abstract: Up to now, Si LSIs have been widely used, and have played a key role in achieving “ubiquitous computing”. In “ubiquitous computing”, devices gather information from ubiquitous environment and provide services through accumulated information and their analysis. These services will become more of a necessity for individuals, rather than a convenience. Thus, human beings will become more dependent on “ubiquitous computing” in such society. Such society can be called a “symbiotic society”, which will offer new opportunities to the semiconductor industry.

In this panel, each specialist will talk about technical challenges involved in realizing a “symbiotic society”. This panel talk is not an "A vs. B" type of debate, but more like an evening talk where each specialist presents one’s vision.

Panel Discussion 2

Time: 15:45-17:25

Room: Crowne Ballroom B

Dream of System and Reality of Device; How can Circuit Designers Cope with them?

Organizer: Tadahiro Kuroda, Keio Univ., Japan

Moderator: Hitoshi Wakabayashi, Sony, Japan

Panelists: Naoki Yamauchi, Renesas, Automotive
Ramchan Woo, LG, Mobile
Toshihiro Matsui, AIST, Robot
Toshiro Hiramoto, U. Tokyo
Satoshi Inaba, Toshiba
Clement Wann, TSMC
Yoshihiro Hayashi, STARC
Kohji Nii, Renesas

Abstract: System engineers are dreamers. Future robots, automotives, cellular phones, and imaging systems will require much higher performance.

On the other hand, device engineers are realistic. They address difficult technical issues that need to be challenged by collaboration between device and circuit engineers. For instance, increasing device variations may require post-fabrication calibration and modification. Non-planer device structure for improving the short-channel effect may add limitation in layout. Degradation in reliability may need error detection and correction. This panel will describe future technology in 2020 from both system and device perspectives and discuss how circuit designers can cope with the dream and the reality.

November 9, 2010 (Tuesday)

Plenary Talk 3

Time: 8:15-9:00

Room: Crowne Ballroom A & B

From Connecting Every-body to Connecting Every-thing: Why, When and How?

Dr. Rudy Lauwereins

Vice President, Director of IMEC, Belgium

Abstract: Over forty years of happy CMOS scaling brought the room-sized super-computer for the nerds into everyone's pocket, literally connecting every-body on earth. In an economy which is based on double digit growth, the obvious next step is to connect every-thing on earth. This move redirects the focus from electronics-for-infotainment to electronics helping to solve the mounting societal problems our earth faces: better and more affordable health care for everyone, safer and more efficient transportation, cleaner and more sustainable environment, etc. Realizing this requires abandoning the traditional keyboard/screen user interface to make the electronic devices autonomous, independent from a human in the loop, and to provide its services hidden in the background. In this presentation, I will zoom into the various challenges we need to tackle to make electronics truly hidden and autonomous. I will use preventive personalized health care as an application driver.

Plenary Talk 4

Time: 9:05-10:50

Room: Crowne Ballroom A & B

High Performance SOC for Mobile Applications

Dr. Nam-Sung Woo

Executive VP & GM, Samsung Electronics, Korea

Abstract: The area of mobile applications is observing a big shift in its foundation. Traditionally, mobile applications emphasized low power consumption at the cost of low performance. However, the recent spread of "smart" mobile devices (e.g., smart phone) asks for very high computing performance of underlying chips.

This presentation will show the upside trend of computing requirement for SOC chips used for mobile applications. In addition, we will describe how engineering teams are coping with the enhanced requirements; we will cover various issues including architecture design, circuit design, 3D packaging, and advanced processing technologies. Finally, we will explain the interaction between software and hardware in the SOC development.

Session 5 Wide-band and Reconfigurable Receiver Design

Time: 10:20-12:25

Room: Crowne Ballroom A

Co-Chairs: Baoyong Chi (Tsinghua University)

Chien-Nan Kuo (National Chao Tung University)

5-1 10:20-10:45

A 31mA CMOS Wideband BD-II B2&B3 Mode Receiver with 55dB Gain Dynamic Range

Chuan Wang, Congyin Shi, Le Ye, Zhongyuan Hou, Huailin Liao, Ru Huang

Institute of Microelectronics, Peking University, China

Abstract: A CMOS wideband receiver for BD-II B2&B3 mode is presented. The chip demonstrates a noise figure of 4.0dB and a 2dB CNR desensitization point of 4dBm at 800MHz GSM blocker. Due to the optimized design of an ESD-protected LNA and a 1/f-noise-reduced high-LO-RF-isolation Mixer, the spurious level is suppressed below -113dBm referred to the RF input. The fractional-N synthesizer obtains LO phase noise of -92dBc/Hz@1KHz and -117dBc/Hz@1MHz, with the reference spurs are below -60dBc. The integrated 4th-order LPF has tunable 7.5MHz/10MHz/15MHz corner frequency. The mixed-signal AGC loop, including 4-bit ADCs, variable gain amplifier and programmable amplifier, achieves 55dB gain dynamic range. The receiver consumes 31mA from a 1.8-V supply voltage while occupying a 5.5-mm2 die area including ESD pads.

5-2 10:45-11:10

A Reconfigurable Dual-Channel Tri-Mode All-Band RF Receiver for Next Generation GNSS

Dongpo Chen, Wenjie Pan, Peichen Jiang, Jing Jin, Jun Wu, Junzhang Tan, Chao Lu, Jianjun Zhou

Shanghai Jiao Tong University, China

Abstract: A dual-channel fully integrated RF receiver is designed and implemented for next generation Global Navigation Satellite Systems (GNSS) in a 0.18μm CMOS process. Its two independent channels are capable of receiving 2MHz, 4MHz or 20MHz bandwidth signals around 1.2GHz and 1.57GHz, for GPS, Galileo, and Compass systems. Gain controls along with an all-digital automatic gain control (AGC) loop are implemented in each channel to improve the noise and anti-interference performance of the receiver. While drawing 25mA current per channel from a 1.8V supply, this receiver achieves a total noise figure of 2.6dB, an image rejection of 28dB, and a maximum voltage gain of 110dB, with a die area of 2.4*3mm2 including ESD and I/O pads.

5-3 11:10-11:35

A Quadrature Bandpass Continuous-Time Delta-Sigma Modulator for Tri-Mode GSM-Edge/UMTS/DVB-T Receivers with Power Scaling Technique

Chen-Yen Ho{2}, Wei-Shan Chan{2}, Yung-Yu Lin{1}, Tsung-Hsien Lin{2}

{1}MediaTek Inc., Taiwan; {2}National Taiwan University, Taiwan

Abstract: A second-order multi-bit quadrature bandpass continuous-time delta-sigma modulator (QBP-CTDSM) employing a power scaling technique (PST) is reported in this paper for GSM-EDGE/UMTS/DVB-T receivers. This modulator employs the proposed operational amplifiers (op-amp) with PST to optimize power consumption among the tri-mode operation. The QBP-CTDSM is fabricated in a 0.18-μm CMOS process. It achieves 81/61.2/60.9 dB SNDR across 270-kHz/5-MHz/8-MHz bandwidth with a programmable center frequency spanning from 500 kHz to 12 MHz. Measured from a 1.8-V supply voltage, the power consumptions are 4.9/8.9/12.1 mW for GSM-EDGE/UMTS/DVB-T modes, respectively, which results in FOMs of 0.99/0.95/0.84 pJ/conversion.

5-4 11:35-12:00

A High-Speed, on-Chip Implementation of Teager Kaiser Operator for in-Band Interference Rejection

Waclaw Godycki, Rajeev Dokania, Xiao Wang, Alyssa Apsel

Cornell University, United States

Abstract: Recently, Teager-Kaiser (T-K) energy operator has been proposed for narrowband interference rejection in ultra wide band (UWB) impulse radio (IR) systems. However, sampling and performing the energy operation in the digital domain is impractical for high frequency signals. In this paper we present an analog implementation of the T-K operator. The fabricated circuit was measured to reject in-band interferers 17 times (~25dB) larger the amplitude than the signal. The design works up to 4.5GHz, for a signal bandwidth of 500MHz-1.3GHz. The design was also measured to work well with up to 500Mbps BFSK demodulation and AM pulse demodulation.

5-5 12:00-12:12

A CMOS Active Feedback Wideband Single-to-Differential LNA Using Inductive Shunt-Peaking for Saw-Less SDR Receivers

Donggu Im{1}, Ilku Nam{2}, Jaeyoung Choi{1}, Bumkyum Kim{1}, Kwyro Lee{1}

{1}Korea Advanced Institute of Science and Technology, Korea, South; {2}Pusan National University, Korea, South

Abstract: A wideband active feedback single-to-differential (S-to-D) LNA composed of a S-to-D converter, a voltage combiner, and a negative feedback network is proposed. By feeding the single-ended output of the voltage combiner, which is used for combining the differential output of the S-to-D converter, to the input of the LNA through the feedback network, a wideband S-to-D LNA exploiting negative feedback is implemented. By using shunt-peaking of the source follower (SF) based active inductor, the proposed S-to-D LNA can achieve wider loop gain bandwidth with balun functionality. The 3-dB gain bandwidth of the proposed S-to-D LNA is above 5 GHz and the NF is below 4 dB from 100 MHz to 5 GHz. An average voltage gain of 18 dB and an IIP3 of -5 dBm are obtained.

5-6 12:12-12:24

Wide Band LNA with BW Expansion by Capacitive Feed Forward Technique

Mousa Othman{2}, Shuhei Amakawa{1}, Noboru Ishihara{2}, Kazuya Masu{2}

{1}Hiroshima University, Japan; {2}Tokyo Institute of Technology, Japan

Abstract: This paper presents a wide band low noise amplifier (LNA) that utilizes shunt feedback topology (SF). SF based lna suffers from strict trade-off between the input matching reflection coefficient (S11) and noise figure NF. To break this trade-off a feed forward (FF) stage is added to achieve two in-phase nodes in the path of the signal where “a negative" Miller capacitance can be obtained by employing another capacitive FF resulting in a partial cancellation of the parasitic capacitance associated with the dominant pole hence expanding the BW of both gain and S11 while slightly affect the NF. The LNA was realized using 90 nm CMOS technology and achieves gain of 14 dB, S11 < -10 dB and NF less than 2.2 dB in the frequency range from 0.5-2.2 GHz and less than 2.8 dB in the entire BW of 0.1-5GHz while draws 10 mA from 1.2 V DC source and occupies 0.003 mm^2

Session 6 — Nyquist-rate Data Converters

Time: 10:20-12:25

Room: Crowne Ballroom B

Co-Chairs: Tai-Cheng Lee (National Taiwan University)

Hung S. Li (Mediatek Inc.)

6-1 — 10:20-10:45

A 12-Bit 800-Ms/S Switched-Capacitor DAC with Open-Loop Output Driver and Digital Predistortion

Clayton Daigle, Alireza Dastgheib, Boris Murmann

Stanford University, United States

Abstract: A 12-bit 800-MS/s DAC implemented in 90-nm CMOS is presented. The design uses three interleaved, pipelined, switched-capacitor cores followed by an open-loop output driver. The driver is linearized using digital predistortion. Measured SFDR is greater than 58 dB for signal frequencies below 200 MHz, and greater than 53 dB for signal frequencies below 400 MHz, all with output swings as large as 2.9 Vppd. Power dissipation is 103 mW when delivering a full scale signal current of 16 mA.

6-2 — 10:45-11:10

A 10b Linear Interpolation DAC Using Body-Transconductance Control for AMLCD Column Driver

Changbyung Park, Ki-Duk Kim, Sung-Woo Lee, Gyu-Sung Park, Seung-Tak Ryu, Gyu-Hyeong Cho

Korea Advanced Institute of Science and Technology, Korea, South

Abstract: A 10-b interpolation DAC is implemented for AMLCD column driver using 4b control of body potential via a built-in body buffer for interpolation in the buffer amplifier. Measured INL and DNL are 0.36 LSB and 0.35LSB on 10b accuracy, respectively. Each channel of driver IC has a height of 295um, a pitch of 14μm and a static current of 1μA. The fabricated chip is in 90n CMOS process.

6-3 — 11:10-11:35

A 0.8mW 5bit 250MS/S Time-Interleaved Asynchronous Digital Slope ADC

Pieter Harpe, Cui Zhou, Kathleen Philips, Harmke de Groot

Holst Centre - IMEC, Netherlands

Abstract: Slope and digital-ramp converters are normally limited to very low sampling rates, since they require a digital counter at a highly oversampled clock rate. In this work, an asynchronous digital slope architecture is introduced that only requires a non-oversampled clock, thus enabling a much higher speed of operation. The low complexity and the inherent accuracy of the slope-architecture enable very good power-efficiency without using calibration techniques. A 2-channel time-interleaved 5bit prototype was implemented in a 90nm CMOS technology. The measured prototype achieves an ENOB of 4.6bit, while operating at 250MS/s and consuming 0.8mW from a 1V supply.

6-4 — 11:35-12:00

A 10b 320MS/S Self-Calibrated Pipeline ADC

Hung-Wei Chen, Wei-Ting Shen, Wei-Chih Cheng, Hsin-Shu Chen

National Taiwan University, Taiwan

Abstract: A high-speed low-power self-calibrated pipeline ADC is presented. Gain error due to low-gain opamp used in multiplying DAC (MDAC) is corrected by the proposed foreground calibration technique. It adjusts the inter-stage gain by connecting a calibration capacitor into the MDAC positive feedback path. It only requires 168 clock cycles to complete the calibration without external precise references. The calibration circuit does not consume power during normal conversion. The prototype ADC in 90nm low-power CMOS technology achieves conversion rate of 320MS/s with SFDR and SNDR of 66.7dB and 54.2dB. The total power dissipation is 42mW and it occupies an active chip area of 0.21mm^2. Its figure-of-merit (FOM) is 313fJ/conversion-step.

6-5 12:00-12:12

A 0.5 V, 1.2 mW, 110 fJ, 600 Ms/S, 5 Bit Flash ADC

Masaya Miyahara, James Lin, Kei Yoshihara, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: An ultra-low voltage operation of 0.5 V, 5-bit Flash ADC has been developed and achieved an ENOB of 4.2-bit at a conversion rate of 600 MS/s. It consumes only 1.2 mW and attained an ultra-low FoM of 110 fJ/conv. steps. A forward body bias technique and gate-interpolated double-tail latched comparator with variable delay method to compensate the mismatch voltage are introduced.

6-6 12:12-12:24

A 3-Gs/S 5-Bit 36-mW Flash ADC in 65-nm CMOS

Tomohiko Ito, Tetsuro Itakura

Toshiba corporation, Japan

Abstract: A 3-GS/s 5-bit flash ADC is fabricated for millimeter-wave communication systems in 65nm CMOS technology. The proposed foreground calibration method reduces the input-referred DC offset, achieving the resolution of 4.7 ENOB at 200MHz input frequency and keeping more than 4.3 ENOB even at Nyquist. The ADC consumes only 36.2mW including the power of the clock buffer and the resistor ladder from 1-V supply. The ADC has the FoM of 0.6pJ/conv at Nyquist.

Session 7 High-precision PLLs and Low-power Circuits for Communication

Time: 10:20-12:25

Room: Conference Room 8

Co-Chairs: Yasushi Hayakawa (Renesas Electronics Corporation)

Ting-Ping Liu (nuvoTon Technology)

7-1 10:20-10:45

250Mbps-5Gbps Wide-Range CDR with Digital Vernier Phase Shifting and Dual Mode Control in 0.13μm CMOS

Sang-Yoon Lee{2}, Hyung-Rok Lee{3}, Young-Ho Kwak{1}, Byoung-Joo Yoo{2}, Daeyun Shim{3}, Chulwoo Kim{1}, Deog-Kyoon Jeong{2}

{1}Korea University, Korea, South; {2}Seoul National University, Korea, South; {3}Silicon Image, United States

Abstract: A multi-port serial link with a wide-range CDR using digital Vernier phase shifting and dual mode control is presented. The proposed Vernier phase shifter generates fine-resolution phase steps and provides unlimited phase rotating. With the dual mode control, the proposed CDR extends the operating range from 250Mbps to 5Gbps. The proposed CDR provides 13.34ps phase steps at 5Gbps and achieves a BER of less than 10 to the power of -12 for the range of 250Mbps to 5Gbps. Fabricated in a 0.13-μm CMOS process, the proposed CDR dissipates 19.2mW at 5Gbps from a 1.2-V supply.

7-2 10:45-11:10

A 58-63.6GHz Quadrature PLL Frequency Synthesizer in 65nm CMOS

Ahmed Musa, Rui Murakami, Takahiro Sato, Win Chiavipas, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Japan

Abstract: This paper proposes a 60GHz quadrature PLL frequency synthesizer that has a tuning range capable of covering the whole band specified by the IEEE802.15.3c with exceptional phase noise. The synthesizer is constructed using a 20GHz PLL that is coupled with a frequency tripler to generate the 60GHz signal. The 20GHz PLL generates a signal with a phase noise as low as -106dBc/Hz using tail feedback to improve the phase noise. The proposed 60GHz ILO uses a combination of parallel and tail injection to enhance the locking range by reducing the Injection Locked Oscillator (ILO) current at the moment of injection. Both the 20GHz PLL and the ILO were fabricated using a 65nm CMOS process and measurement results show a phase noise of -96dBc/Hz at 60GHz while consuming 77.5mW from a 1.2V supply. To to author's knowledge this phase noise is about 20dB better then recently reported QPLL and about 10dB compared to differential PLL operating at similar frequency.

7-3 11:10-11:35

A 40-GHz Phase-Locked Loop for 60-GHz Sliding-IF Transceivers in 65nm CMOS

Hammad Mehmood Cheema{1}, Reza Mahmoudi{1}, Paul van Zeijl{2}, Arthur van Roermund{1}

{1}Eindhoven University of Technology, Netherlands; {2}Philips Research, Netherlands

Abstract: This paper presents a 40 GHz phase-locked loop as an enabling component for sliding-IF 60 GHz transceivers. The PLL front-end includes, a 40 GHz LC voltage controlled oscillator (VCO) and a quadrature injection locked frequency divider (ILFD), which are tuned simultaneously to align their tuning and locking range, respectively. The PLL back-end consists of an optimized divider chain, PFD, CP and a second-order passive loop filter integrated on chip. The PLL can be locked from 38.2 to 43.6 GHz corresponding to a down-conversion range of 57.3 to 65.4 GHz, thus covering all IEEE 802.15.3c channels. The phase noise for a 40.2 GHz output is -89.7, -94 and -112 dBc/Hz at 1 MHz, 4 MHz and 10 MHz offsets, respectively. The settling time is lower than 2usec and reference spurs are lower than -42dB. Implemented in a 65nm bulk CMOS technology, the PLL consumes 22.8 mW, excluding buffers, from a 1.2 V supply and occupies 1.67x0.745 mm2 silicon area.

7-4 11:35-12:00

A Low-Cost, Leakage-Insensitive Semi-Digital PLL with Linear Phase Detection and FIR-Embedded Digital Frequency Acquisition

Rui He{2}, Chengwen Liu{2}, Xueyi Yu{2}, Woogeun Rhee{2}, Joon-Young Park{1}, Changhyun Kim{1}, Zhihua Wang{2}

{1}Samsung Electronics, Korea, South; {2}Tsinghua University, China

Abstract: A semi-digital PLL utilizing a hybrid DCO is presented. A mixed-mode loop control with an analog proportional path and a digital integration path provides linear phase tracking, leakage-insensitive loop filtering, and technology scalability. With the absence of the linear TDC, the semi-digital PLL with the hybrid DCO can relax design difficulties such as achieving low power or requiring an advanced CMOS technology. Also, the hybrid finite-impulse response (FIR) filtering method is employed to reduce the DCO quantization noise without causing latency. The prototype PLL implemented in 0.18μm has the active area of 0.6mm2 where only 0.01mm2 is occupied by the analog loop filter.

7-5 12:00-12:12

A New Transformer-Coupled Differential Armstrong VCO for Very Low Power Operation

Tai Nghia Nguyen, Jong-Wook Lee

Kyung Hee University, Korea, South

Abstract: We present a novel differential Armstrong VCO suitable for very low power operation. The proposed Armstrong VCO adopted a new transformer structure which effectively enhanced the output voltage swing under low supply voltage of 0.4 V. The Armstrong VCO was implemented in 0.13 μm RF CMOS process, and measurement showed the oscillation frequency range from 13 to 14.85 GHz (tuning range of 13.3%). Under 0.6 mW power consumption, the new Armstrong VCO achieved a measured phase noise performance of -98.7 dB/Hz at 1 MHz offset from 13.66 GHz carrier. The figure-of-merit (FOM) shows excellent performance and the results demonstrate a potential of Armstrong VCO for achieving a good phase noise performance under very low power consumption.

7-6 12:12-12:24

A 0.45V-to-2.7V Inductive-Coupling Level Shifter

Keita Takatsu, Kiichi Niitsu, Tsunaaki Shidei, Noriyuki Miura, Tadahiro Kuroda

Keio University, Japan

Abstract: This paper presents a 0.45V-to-2.7V level shifter utilizing inductive coupling. Since primary and secondary coils are AC-coupled, each coil can be biased at arbitrary voltage independent from the conversion level difference. This enables both the primary and the secondary circuits to operate at the optimal operating region. In addition, the inductive coupling itself can provide an additional intermediate level-shifting by exploiting a coil-turn ratio between the primary and the secondary coils. As a result, wide-range voltage level conversion can be achieved. Test chip measurement in 65nm CMOS demonstrates voltage level conversion from 0.45V to 2.7V. Compared to a conventional level shifter, the primary voltage is reduced by 0.24V. In addition, the energy-delay product is reduced to 1/8.

Session 8 Digital Clocking and Timing Circuits

Time: 10:20-12:25

Room: Conference Room 9

Co-Chairs: Ravishankar Kuppuswamy (Intel Technology India Private Ltd)

Leibo Liu (Tsinghua University)

8-1 10:20-10:45

A Sub-mW All-Digital Signal Component Separator with Branch Mismacth Compensation for OFDM LINC Transmitters

Tsan-Wen Chen, Ping-Yuan Tsai, Jui-Yuan Yu, Chen-Yi Lee

National Chiao Tung University, Taiwan

Abstract: This paper presents a sub-mW all-digital signal component separator (SCS) with a novel branch mismatch compensation scheme for OFDM LINC transmitters, including a phase calculator and a digital-control phase shifter (DCPS) pair. This chip is manufactured in 90nm standard CMOS process with active area 0.06mm2. The DCPS can generate phase-modulated signal at IF 100MHz with 8-bit resolution and RMS error 9.33ps. The phase calculation can be operated with 50MHz speed at 0.5V supply voltage, resulting in 73.88% power reduction, and the overall SCS power is only 0.95mW. The proposed SCS with mismatch compensation provides 0.02dB gain and 0.15degrees phase fine-tune resolution, and the system EVM with 64-QAM OFDM signals is -29.81dB.

8-2 10:45-11:10

2.07GHz Floating-Point Unit with Resonant-Clock Precharge Logic

Jerry Kao{2}, Wei-Hsiang Ma{2}, Suhwan Kim{1}, Marios Papaefthymiou{2}

{1}Seoul National University, Korea, South; {2}University of Michigan, United States

Abstract: This paper presents an 8-cycle 64 FO4 single-precision fused-multiply-add floating-point unit (FPU) chip with fine-grain resonant clocking and dynamic-evaluation static-latch logic to achieve dynamic-logic levels performance with significant power reduction. Fabricated in a 90nm low-power RVT technology, the resonant FPU achieves clock speeds up to 2.07GHz. At its resonant frequency of 1.81GHz, it dissipates 334mW, yielding 31.5% lower power and 32% more GFLOPS/W over a conventionally-clocked

version of the same FPU implemented on the same die.

8-3 11:10-11:35

A Circuit for on-Chip Skew Adjustment with Jitter and Setup Time Measurement

Masahiro Sasaki, Nguyen Ngoc Mai Khanh, Kunihiro Asada

University of Tokyo, Japan

Abstract: This paper reports a circuit for on-chip skew adjustment with jitter and setup time measurement. A test chip has been fabricated in a 65-nm CMOS process. It successfully measures the random jitter distribution and the relative setup time. This circuit is necessary because direct measurement cannot be performed by external equipment. Setup time of a D-FF is measured by sweeping over the range of an adjustable input delay line. Its jitter is represented by a Cumulative Distribution Function which is measured by sampling the setup time repeatedly. The skew can be adjusted based on the setup time and jitter determined by our method. Furthermore, this method can be extended for almost any number of Target/Reference Programmable Delay Lines. This system enables designers to adjust skew between the distributed clock paths as well as to measure sub-picosecond level jitter and setup time of D-FFs beyond 10-GHz.

8-4 11:35-12:00

A Process-Insensitive Current-Controlled Delay Generator with Threshold Voltage Compensation

He-Gong Wei, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Martins

University of Macau, Macau

Abstract: A process-insensitive current-controlled delay generator is presented with a large tunable range of the time delay. By adopting process variation compensation techniques in the generation of time delay, the delay generator is able to provide process-insensitive clock pulses. The circuit has been fabricated in 90nm CMOS technology, consumes 310μW from a 1.1V supply. Using, in a typical case, 20μA of reference current, it can generate a delay of 2.36 ns. The delay variation observed in 14 measured chips has shown a standard deviation of 1.24%.

8-5 12:00-12:12

A Phase-to-Digital Converter for Wide Tuning Range and PVT Tolerant ADPLL Operating Down to 0.3V

Isamu Hayashi{2}, Takeshi Matsubara{1}, Satoshi Kumaki{1}, Abul Johari{1}, Hiroki Ishikuro{1}, Tadahiro Kuroda{1}

{1}Keio University, Japan; {2}Semiconductor Technology Academic Research Center, Japan

Abstract: A Phase-to-Digital Converter (PDC), - an improved scheme of Time-to-Digital Converter (TDC) -, is presented. The resolution of PDC is completely tracking to generated clock period. This scheme effectively reduces the calibration efforts in conventional TDC. The key technologies are digitally Controlled Coupled Oscillator (DCCO) and body-bias controlled vernier TDC. This PDC should be a key component of wide tuning range and PVT variation tolerant All Digital PLL (ADPLL).

8-6 12:12-12:24

A 300- to 800-MHz De-Skew Clock Generator for Arbitrary Delay

Yu-Cheng Hung, Kevin Fong, Tai-Cheng Lee

National Taiwan University, Taiwan

Abstract: A low jitter 300- to 800-MHz de-skew clock generator for arbitrary wide range delay is proposed to minimize the instability of the clock settling while maintaining wide loop bandwidth. The clock skew problem is detrimental in the high speed applications, especially when the skew is longer than multi-cycles. The proposed generator was fabricated in a 0.18μm CMOS process. The clock generator achieves a measured RMS jitter of 5.8 ps at 800 MHz clock at less than 100-ns settling time. The total core area is 0.525*0.396 mm2 and the power consumption is 10.8mW from a 1.8V supply.

Session 9 — Emerging Medical Applications I

Time: 13:25-15:30

Room: Crowne Ballroom A

Co-Chairs: Paul Marchal (IMEC)

C. Patrick Yue (University of California, Santa Barbara)

9-1 — 13:25-13:50

A 1Mb/S, -75dBm Sensitive Fully Integrated Body Channel Transceiver for a Low Energy Compact Wearable Healthcare Sensor

Long Yan, Joonsung Bae, Hoi-Jun Yoo

Korea Advanced Institute of Science and Technology, Korea, South

Abstract: An 1Mb/s fully integrated FSK transceiver using human body as a transmission medium is presented for a low energy compact wearable healthcare sensor. 20-40MHz is utilized for body channel communication (BCC) and divided into 4 sub-channels to tolerate body induced interferences. FSK transmitter adopts 8b digitally controlled LC oscillator and replaces power consuming PLLs to achieve fast switching radio within 1us. The direct conversion receiver guarantees the operation at -75dBm unstable FSK spectrum received through body, and provides BER less than 10-6 without the help of external bulky X-tal oscillator. The transceiver of 2.1mm *3.3mm was fabricated in 0.18μm CMOS process, and dissipates 2.3mW/3.1mW in the transmitter (TX) and receiver (RX), respectively.

9-2 — 13:50-14:15

A 2.3uW Wireless Intraocular Pressure/Temperature Monitor

Yi-Chun Shih{2}, Tueng Shen{1}, Brian Otis{1}

{1}Univerisity of Washington, United States; {2}University of Washington, United States

Abstract: We present the design of an ultra-low power, wireless capacitance/temperature sensing device for continuous intraocular pressure monitoring. The device is wirelessly powered and demonstrates a power consumption of 2.3uW at 1.5V during continuous reading. The chip converts both capacitance and temperature to frequency using a time-interleaved relaxation oscillator, which modulates RF backscatter to a reader for computation of measured samples. The chip exhibits measured capacitance and temperature standard deviations of 1.4fF and 0.4°C, respectively.

9-3 — 14:15-14:40

A SoC with 3.9mW 3Mbps UHF Transmitter and 240μW MCU for Capsule Endoscope with Bidirectional Communication

Hanjun Jiang{2}, Fule Li{2}, Xinkai Chen{1}, Yanqing Ning{1}, Xu Zhang{1}, Bin Zhang{1}, Teng Ma{1}, Zhihua Wang{2}

{1}Ecore Technologies, China; {2}Tsinghua University, China

Abstract: An ULP SoC for wireless capsule endoscopes has been implemented, providing bidirectional communication between the capsule and the external data logger. The SoC is composed of a programmable UHF band transceiver with 3Mbps MSK transmitting and 64kbps OOK receiving, a 1.2V MCU with a dedicated image compressor, multiple on-chip voltage regulators, and etc.. The SoC can work with a power supply down to 2.5V. The 3Mbps transmitter working at 400MHz band consumes only 3.9mW power, and the MCU draws only 200uA current from 1.2V supply. Fabricated in 0.18μm CMOS, the SoC occupies a die area of 13.3mm2 including the I/O pads.

9-4 14:40-15:05

A Tactile Sensor ASIC for a Sensorized Guidewire in Minimally Invasive Surgical Operations

Kok Lim Chan, Kei-Tee Tiew, Andreas Astuti Lee, Jianwen Luo, Simon Sheung Yan Ng, Minkyu Je

Agency for Science, Technology and Research / IME, Singapore

Abstract: In this paper, a tactile sensor ASIC for a sensorized guidewire in minimally invasive surgical operations is presented. The chip has been fabricated in 0.18μm CMOS and occupies an area of only 500μm x 650μm. A 7-bit resolution is achieved for the sensor resistance ranging between 20KOhm and 800KOhm, with an overall power consumption of only 250uW.

9-5 15:05-15:17

A 21.6μW Inductively Powered Implantable IC for Blood Flow Measurement

Pradeep Basappa Khannur, Kok Lim Chan, Jia Hao Cheong, Kai Kang, Andreas Astuti Lee, Xin Liu, Huey Jen Lim, Kotlanka Ramakrishna, Minkyu Je

Agency for Science, Technology and Research / IME, Singapore

Abstract: This paper presents a fully integrated inductively powered implantable circuits for blood flow measurement, which are embedded within vascular prosthetic grafts for early detection of graft degradation or failure. The ASIC interfaces with micro-fabricated pressure sensors and uses a 13.56MHz carrier frequency for power transfer and command/data communication. A backscatter-modulated passive telemetry is used for transmitting sensor readout information to an external monitoring device. The chip has been fabricated in 0.18μm CMOS process, occupies a total active area of 1.5X1.78mm2 and consumes a total power of 21.6uW. The rectifier achieves an efficiency of 66%. The sub-uW 10-bit SAR ADC achieves an ENOB of 8.5 bits at 106KS/s conversion rate.

9-6 15:17-15:29

A Coreless Maximum Power Point Tracking Circuit of Thermoelectric Generators for Battery Charging Systems

Sungkyu Cho, Namjae Kim, Soonseo Park, Shiho Kim

Chungbuk National University, Korea, South

Abstract: We have proposed and fabricated MPPT circuit for TEG without digital controller unit. The experimental and simulation results from the proposed MPPT circuit employing the boost cascaded-with-buck converter dealt with rapid variation of temperature and abrupt changes of load current have shown that the proposed method allows stable operation with high power transfer efficiency. The main advantage of proposed method is analog tracking circuit by sampling half VOC level without DSP or micro controller unit for calculating peak power point by iterative methods. The proposed MPPT circuit has merit in cost and miniaturization of system compared to conventional MPPT algorithms.

Session 10 — Analog Filters and Techniques

Time: 13:25-15:30

Room: Crowne Ballroom B

Co-Chairs: Po-Chiun Hung (National Tsing Hua Univ.)

Seng-Pan (Ben) U (University of Macau)

10-1 13:25-13:50

Zero-Crossing Detector Based Reconfigurable Analog System

Payam Lajevardi, Anantha Chandrakasan, Hae-Seung Lee

Massachusetts Institute of Technology, United States

Abstract: A reconfigurable analog system is presented that implements pipelined ADCs, switched-capacitor filters, and programmable gain amplifiers. Each block employs a zero-crossing based circuit for easy reconfigurability and power efficiency. Configured as a 10-bit ADC, the chip consumes 1.92mW at 50MSPS with ENOB of 8.02b and FOM of 150fJ/conversion-step. A third order Butterworth filter is also demonstrated. The chip is implemented in 65nm technology

10-2 13:50-14:15

Parasitic Discrete-Time-Pole Cancelling Techniques for Ultra-Wideband Discrete-Time Charge-Domain Baseband Filters

Atsushi Yoshizawa, Sachio Iida

Sony Corporation, Japan

Abstract: Parasitic discrete-time-pole cancelling techniques that use a discrete-time IIR BPF are presented. Parasitic capacitors, which usually cause undesirable lowpass parasitic discrete-time poles in ultra-wideband applications, are reused to provide bandpass parasitic discrete-time poles, which improves the frequency characteristics in parallel with passband equalizer circuits. A novel charge transfer scheme that reduces the parasitic sensitivity of the output node is also implemented.

10-3 14:15-14:40

A Cascade Non-Decimation Charge-Domain Filter with Noise-Folding Reduction

Ming-Feng Huang, Szu-Hsien Wu

Industrial Technology Research Institute, Taiwan

Abstract: A cascade non-decimation charge-domain filter (CNCDF) with noise-folding reduction for high attenuation and bandwidth was proposed. The CNCDF, based on non-decimation property, could suppress the noise-folding source from a down-sampling rate and duplicate-sampled signals upon a sensible input-clock rate (ICR). By using 600-MS/s ICR, the measurement showed 91-dB attenuation of the first folding signal, 95-dB stop-band attenuation, and 10-MHz bandwidth. The chip also possessed 30-dB gain and 6-dBm IIP3, consuming 11.86-mA current from a 1.2-V power supply. The chip, including ESD and clock-logical circuits, occupies 3.6 mm2 in 90-nm CMOS process.

10-4 14:40-15:05

A 2.3mA 240-to-500MHz 6th-Order Active-RC Low-Pass Filter for Ultra-Wideband Transceiver

Le Ye, Huailin Liao, Congyin Shi, Junhua Liu, Ru Huang

Peking University, China

Abstract: This paper presents a 6th-order active-RC low-pass filter with 240 MHz to 500 MHz tunable bandwidth, which is suitable for the ultra-wideband transceivers. The filter consumes only 2.3 mA from 1.8 V supply voltage, which is mainly attributed to the proposed highly power-efficient operational amplifier (Opamp) with an adaptive-biased pole-cancellation push-pull source follower as the buffer stage to drastically extend the bandwidth. The technique of high-frequency common-mode rejection using parasitic capacitor is utilized to guarantee the Opamp stability. In addition, the filter adopts the Q-tuning technique and Opamp GBW compensation mechanism, which relax the GBW requirement of the Opamp to further reduce the power consumption. The filter achieves 1.36 pW/pole/Hz normalized power, 13.1 nV√Hz input-referred noise density, 15.9 dBm in-band IIP3, and 34 dBm out-of-band IIP3, respectively. The chip is fabricated in a standard 0.18μm CMOS process, and occupies 0.23 mm2 silicon area without pads.

10-5 15:05-15:17

A 70-280 MHz Frequency and Q Tunable 53 dB SFDR Gm-C Filter for Ultra-Wideband

Weinan Li, Yumei Huang, Zhiliang Hong

Fudan University, China

Abstract: A 70-280 MHz 5th-order Chebyshev Gm-C low-pass filter was implemented in 0.13μm CMOS process to support both WiMedia UWB and lower rate IR-UWB applications. The filter response is accurately maintained over 4x frequency range by using unit Gm cell arrays and independent Q tuning circuit. To improve linearity of Gm-C filter in low supply voltage, a modified LC ladder topology is proposed. The IIP3 performance is improved more than 10 dB compared to conventional Gm-C filter. A measured spurious free dynamic range (SFDR) of more than 50 dB is maintained when the filter cut-off frequency is programmed. It occupies an area of 0.12 mm2 and consumes 21 mW under supply of 1.5 V.

10-6 15:17-15:29

Clocked Comparator for High-Speed Applications in 65nm Technology

Mohamed Abbas{3}, Yasuo Furukawa{1}, Satoshi Komatsu{3}, Takahiro Yamaguchi{2}, Kunihiro Asada{3}

{1}Advantest Corporation, Japan; {2}Advantest Laboratories, Japan; {3}University of Tokyo, Japan

Abstract: This paper presents a design for an on-chip high-speed clocked-comparator for high frequency signal digitization. The comparator consists of two stages, amplification and regenerative, comprising a total of 10 MOS transistors. The design is implemented in 65nm CMOS technology. Also, the paper presents a new cost effective technique for measuring the maximum speed of the clocked comparator. The measurement and simulation results show that the proposed design has an average of 31% higher speed and ~17% less active area than the conventional design.

Session 11 Millimeter-wave and Related Circuits

Time: 13:25-15:30

Room: Conference Room 8

Co-Chairs: Minoru Fujishima (Hiroshima University)

Shuya Kishimoto (NEC Corporation)

11-1 13:25-13:50

A 120-GHz Transmitter and Receiver Chipset with 9-Gbps Data Rate Using 65-nm CMOS Technology

Ryuichi Fujimoto{2}, Mizuki Motoyoshi{3}, Uroschanit Yodprasit{1}, Kyoya Takano{3}, Minoru Fujishima{1}

{1}Hiroshima University, Japan; {2}Semiconductor Technology Academic Research Center, Japan; {3}University of Tokyo, Japan

Abstract: Design and measured results of a 120-GHz transceiver are described in this paper. Simple ASK modulation is adopted for this transceiver. The proposed transceiver is fabricated by using 65-nm CMOS technology. The current consumption is 19.2 mA for the transmitter and 48.2 mA for the receiver. A 9-Gbps PRBS is successfully transferred from the transmitter to the receiver with the bit error rate less than 1.0e-9.

11-2 13:50-14:15

130-GHz Gain-Enhanced SiGe Low Noise Amplifier

Bo Zhang{4}, Yong-Zhong Xiong{1}, Lei Wang{1}, Sanming Hu{1}, Teck-Guan Lim{1}, Y. Q. Zhuang{3}, L.W. Li{2}, Xiao-Jun Yuan{1}

{1}Agency for Science, Technology and Research / IME, Singapore; {2}National University of Singapore, Singapore; {3}Xidian University, China; {4}Xidian University, A-STAR / IME , National University of

Abstract: A 130 GHz low noise amplifier (LNA) in 0.13-μm SiGe BiCMOS technology has been designed and characterized. The gain-boosted cascode topology with 3D grounded-shielding structures is employed. The results showed that the LNA with a chip area of 400 μm× 900 um, gain of ~17.5 dB with a 3-dB bandwidth of ~25 GHz, and noise figure of ~7.7 dB at 130 GHz with total dc power consumption of 31.5 mW has

demonstrated.

11-3 14:15-14:40

A 63 GHz Low-Noise Active Balun with Broadband Phase-Correction Technique in 90 nm CMOS

Hsi-Han Chiang, Fu-Chien Huang, Chao-Shiun Wang, Chorng-Kuang Wang

National Taiwan University, Taiwan

Abstract: This paper presents a low-noise active balun with broadband phase-correction. The proposed phase-correction structure is independent of operation frequency, and effectively suppresses phase deviation of active balun at millimeter-wave (MMW) band. Within the low noise current-reuse pre-amplifier, this active balun circuit can be employed as low-noise amplifier as well. This circuit is fabricated in 90nm low power CMOS technology with core area of 0.275 mm2. The measured phase-error is less than 10 degrees from 50 GHz to 67 GHz, which demonstrates the robust calibration of phase-error at MMW frequency. The measured voltage gain and noise figure at 63 GHz are 17.6 dB and 8.6 dB, respectively. The measured IIP3 is around -7 dBm. The core power consumption is 19 mW from 1.4 V supply voltage.

11-4 14:40-15:05

A 60 GHz Heterodyne Quadrature Transmitter with a New Simplified Architecture in 90nm CMOS

James Brinkhoff{3}, Fujiang Lin{1}, Kai Kang{1}, Duy Dong Pham{1}, Chun-Huat Heng{2}

{1}Agency for Science, Technology and Research / IME, Singapore; {2}National University of Singapore, Singapore; {3}Sapphicon Semiconductor, Australia

Abstract: A 60 GHz heterodyne up-convertor consuming only 29 mW, together with a PA consuming 84 mW, is presented. It takes advantage of sub-harmonic mixing and a sliding IF architecture, using a single LO around 20 GHz, thus relaxing millimeter-wave LO design. This also allowed LO buffers to be eliminated, which minimizes area and power consumption. The I/Q up-converter includes a quadrature VCO, resistive IF mixers, IF amplifier and RF sub-harmonic mixer. It achieves a tuning range of 8.8 % and a conversion gain of 13.1 dB. The 60 GHz power amplifier delivers 9.8 dBm, has 9.7 % PAE and 20 dB gain.

11-5 15:05-15:17

A Compact, Fully Differential D-Band CMOS Amplifier in 65nm CMOS

Zhiwei Xu{1}, Qun Jane Gu{3}, I-Ning Ku{2}, Mau-Chung Chang{2}

{1}HRL Laboratories, United States; {2}University of California, Los Angeles, United States; {3}University of Florida, United States

Abstract: A fully differential D-band CMOS amplifier has been demonstrated in 65nm CMOS. It validates a maximum 20dB power gain and has positive gain over 38GHz frequency range from 126GHz to 164GHz. With stacking circuit architecture, the amplifier can tolerate up to 2V supply without reliability concern. It also delivers over 5.7dBm saturated output power with P1dB of 5dBm under 2V supply. The amplifier features a 3-stage common-source cascode architecture with on-chip inter-stage matching. The chip occupies 0.05 mm2 area and draws 39mA and 51mA from 1.4V and 2V supplies, respectively. To our best knowledge, this amplifier achieves the highest power gain for CMOS amplifiers beyond 100GHz and paves the way for integrated D-band radar and passive imaging system applications.

11-6 15:17-15:29

0.6V Voltage Doubler and Clocked Comparator for Correlation-Based Impulse Radio UWB Receiver in 65nm CMOS

Lechang Liu, Takayasu Sakurai, Makoto Takamiya

University of Tokyo, Japan

Abstract: This paper presents a 0.6-V voltage doubler and a 0.6-V clocked comparator in 65nm CMOS. For the multi-phase sampling application, such as charge-domain correlator for impulse UWB receivers or analog-to-digital converter, the proposed voltage doubler can reduce the power consumption and the chip area by half compared to the conventional one. The non-overlapping complementary clock generator used in the conventional voltage doubler can be eliminated by simply swapping the input clock order. The proposed 0.6-V clocked comparator can operate at 100-MHz clock with the proposed voltage booster.

Session 12 Communication and Media Signal Processing

Time: 13:25-15:30

Room: Conference Room 9

Co-Chairs: Zhenyu Liu (Tsinghua University)

Tomohisa Wada (University of the Ryukyus)

12-1 13:25-13:50

A 92mW 76.8GOPS Vector Matching Processor with Parallel Huffman Decoder and Query Re-Ordering Buffer for Real-Time Object Recognition

Seungjin Lee, Joonsoo Kwon, Jinwook Oh, Junyoung Park, Hoi-Jun Yoo

Korea Advanced Institute of Science and Technology, Korea, South

Abstract: A vector matching processor with memory bandwidth optimizations is proposed to achieve real-time matching of 128 dimensional SIFT features extracted from VGA video. The main bottleneck of feature-vector matching is the off-chip database access. We employ the locality sensitive hashing (LSH) algorithm which reduces the number of database comparisons required to match each query. In addition, database compression using Huffman coding increases the effective external bandwidth. Dedicated parallel Huffman decoder hardware ensures fast decompression of the database. A flexible query re-ordering buffer exploits overlapping accesses between queries by enabling out-of-order query processing to minimize redundant off-chip access. As a result, the 76.8 GOPS feature matching processor implemented in a 0.13μm CMOS process achieves 43200 queries/second on a 100 object database while consuming peak power of 92mW.

12-2 13:50-14:15

A 5.7Gbps Row-Based Layered Scheduling LDPC Decoder for IEEE 802.15.3c Applications

Shiang-Yu Hung, Shao-Wei Yen, Chih-Lung Chen, Hsie-Chia Chang, Shyh-Jye Jou, Chen-Yi Lee

National Chiao Tung University, Taiwan

Abstract: A LDPC decoder chip supporting four code rates of IEEE 802.15.3c applications is presented. The row-based layered scheduling with normalized min-sum algorithm is proposed to reduce the iteration number. In addition, reconfigurable 8/16/32-input sorter is designed to deal with four code rates decoding. Both of the reallocation of sorter inputs and pre-coding routing network are proposed to eliminate the number of multiplexer inputs by 64%. Fabricated in the 65 nm 1P10M CMOS process, this test chip can achieve over 5.76 Gbps throughput for the highest code rate code, while the hardware efficiency and power efficiency are 3.68 Gbps/mm2 and 89 pJ/bit, respectively.

12-3 14:15-14:40

A 15.8 pJ/Bit/iter Quasi-Cyclic LDPC Decoder for IEEE 802.11n in 90 nm CMOS

Christoph Roth, Pascal Meinerzhagen, Christoph Studer, Andreas Burg

ETH Zurich, Switzerland

Abstract: We present a low-power quasi-cyclic low density parity check (LDPC) decoder that meets the throughput requirements of the highest-rate (600 Mbps) modes of the IEEE 802.11n WLAN standard. The design is based on the layered offset-min-sum algorithm and is runtime-programmable to process different code matrices (including all rates and block lengths specified by IEEE 802.11n). The register-transfer-level implementation has been optimized for best energy efficiency. The corresponding 90 nm CMOS ASIC has a core area of 1.77 mm2 and achieves a maximum throughput of 680 Mbps at 346 MHz clock frequency and 10 decoding iterations. The measured energy efficiency is 15.8 pJ/bit/iteration at a nominal operating voltage of 1.0 V.

12-4 14:40-14:52

A 5.35 mm2 10GBASE-T Ethernet LDPC Decoder Chip in 90 nm CMOS

Alessandro Cevrero{1}, Yusuf Leblebici{1}, Paolo Ienne{1}, Andreas Burg{2}

{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}ETH Zurich, Switzerland

Abstract: A partially parallel low density parity check (LDPC) decoder compliant with the IEEE 802.3an standard for 10GBASE-T Ethernet is presented. The design is optimized for minimum silicon area and is based on the layered offset-min-sum algorithm which speeds up the convergence of the message passing decoding algorithm. To avoid routing congestion the decoder architecture employs a novel communication scheme that reduces the critical number of global wires by 50%. The prototype LDPC decoder ASIC, fabricated in 90 nm CMOS, occupies only 5.35 mm2 and achieves a decoding throughput of 11.69 Gb/s at 1.2 V with an energy efficiency of 133 pJ/bit.

12-5 14:52-15:04

A 2x2 - 8x8 Sorted QR Decomposition Processor for MIMO Detection

Jhong-Yu Wang{2}, Ren-Hao Lai{2}, Cheng-Ming Chen{1}, Pang-An Ting{1}, Yuan-Hao Huang{2}

{1}Industrial Technology Research Institute, Taiwan; {2}National Tsing Hua University, Taiwan

Abstract: Due to the growing demand of transmission capacity of the wireless communication system, multiple-input multiple-output orthogonal-frequency-division-multiplexing (MIMO-OFDM) communication system requires more and more MIMO antennas and a large number of OFDM subcarriers. Thus, the QR decomposition becomes one of the computational bottlenecks in the QR-based MIMO detection. The proposed Givens-Rotation-based QR decomposition algorithm features efficient parallel processing with sorting function that resolves the trade-off between the detection performance and hardware utiliztion efficiency. According to the algorithm, we designed and implemented a 2x2-8x8 QR decomposition processor using TSMC 0.18μm 1P6M CMOS technology. The throughput of the QR decomposition processor achieves 6.8x10^4 SQRD per second, which outperforms other works in the literature after being normalized by the MIMO dimension.

12-6 15:04-15:16

A Low-Complexity Heterogeneous Multi-Core Platform for Security SoC

Wei Huang, Jun Han, Shuai Wang, Xiao-Yang Zeng

Fudan University, China

Abstract: This paper presents the design and implementation of a heterogeneous multi-core SoC platform to deal with intensive cyrptography algorithms in different security protocols. And it integrates a MIPS-like general processor, a dedicated package processor for fast data package, and multiple security processors for cryptography. Our platform has a low-complexity hardware cost but more flexibility.

12-7 15:16-15:28

A 2-Gb/S 5.6-mW Digital Equalizer for a Los/NLOS Receiver in the 60GHz Band

Ji-Hoon Park, Brian Richards, Borivoje Nikolic

University of California at Berkeley, United States

Abstract: The wide unlicensed bandwidth of a 60GHz channel presents an attractive opportunity for high data rate and low power personal area networks (PANs). The use of single-carrier modulation is beneficial for efficient transmitter and receiver implementation. Equalization of the long channel response in non-line-of-sight (NLOS) conditions presents a significant challenge. A digital equalizer for 60GHz channels has been designed for both line of sight (LOS) and NLOS channel conditions based on the IEEE WPAN standard. Power consumption is minimized by using parallelized distributed arithmetic (DA). A 2mm x 2mm test chip in 65nm CMOS implements a 6-tap feedforward and 32-tap feedback equalizer that consumes 5.6mW at 2.0Gb/s throughput.

Session 13 Emerging Medical Applications II and MEMS techniques

Time: 15:50-17:55

Room: Crowne Ballroom A

Co-Chairs: Bill Yang Liu (Analog Devices)

Hirofumi Sumi (Sony Corporation)

13-1 15:50-16:15

A Low-Power Mandarin-Specific Hearing Aid Chip

Cheng-Wen Wei, Yu-Ting Kuo, Kuo-Chiang Chang, Cheng-Chun Tsai, Jihi-Yu Lin, Yi Fanjiang, Ming-Hsien Tu, Chih-Wei Liu, Tian-Sheuan Chang, Shyh-Jye Jou

National Chiao Tung University, Taiwan

Abstract: This paper presents a digital hearing aid chip designed for Mandarin user to enhance speech quality and intelligibility. The hearing aid consists of an 18 subbands analysis and synthesis filter bank, insertion gain stage, and three channels wide dynamic range control for the new Mandarin-specific auditory compensation algorithm. A noise reduction block based on multiband spectral subtraction and enhanced entropy voice activity detection is also included to enhance quality. We reduce the power consumption of these algorithms through algorithmic and architecture optimization. In addition, for the data storage requirement, a low power SRAM that can operate at 0.6V and below is developed. Moreover, several strategies such as multi-clock domain, bypass mode, and voltage scaling are also adopted for power reduction. The chip measurement shows that the hearing aid consumes 314uW at 0.6V.

13-2 16:15-16:40

A 2.1 uW Area-Efficient Capacitively-Coupled Chopper Instrumentation Amplifier for ECG Applications in 65 nm CMOS

Qinwen Fan{1}, Fabio Sebastiano{2}, Han Huijsing{1}, Kofi Makinwa{1}

{1}Delft University of Technology, Netherlands; {2}NXP Semiconductors, Netherlands

Abstract: This paper describes a capacitively-coupled chopper instrumentation amplifier for use in electrocardiography (ECG). The amplifier employes a DC servo loop to reject the DC offset generated by the electrode-tissue interface. The high-pass corner frequency established by the servo loop is realized by an area-efficient switched-capacitor integrator. A positive feedback loop is employed to boost the amplifier's input-impedance to 80 Mohm and a ripple reduction loop is used to suppress the chopper ripple. Implemented in a 65 nm CMOS technology, the amplifier draws 2.1 uA from a 1 V supply and occupies 0.2 mm2.

13-3 16:40-16:52

Ultra Low Power Programmable Biomedical SoC for on-Body ECG and EEG Processing

Benjamin Büsze{1}, Frank Bouwens{1}, Mario Konijnenburg{1}, M. De Nil{1}, Maryam Ashouei{1}, J. Hulzink{1}, J. Zhou{1}, Jan Stuyt{1}, J. Huisken{1}, Harmke de Groot{1}, Octavio Santana{2}, A. Abbo{2}, L. Yseboodt{2}, Jef van Meerbergen{2}, Martijn Bennebroek{2}

{1}Holst Centre - IMEC, Netherlands; {2}Philips Research, Netherlands

Abstract: An Ultra Low Power (ULP) biomedical System-on-Chip (SoC) has been developed for efficient ECG/EEG signal processing in a Body Area Network environment. This experimental SoC explores the use of event-driven peripheral modules that autonomously interact with external sensors together with the use of an Application-Specific-Instruction-set-Processor (ASIP) to optimize energy-efficiency during active and sleep periods. The SoC has been manufactured in standard 90nm CMOS process and use has been made of power gating to reduce leakage power that starts to become more dominant in advanced technologies. When running an ECG algorithm that is capable of reliably detecting the QRS complex in an ambulatory environment, an average power consumption of 10 μW has been measured at 0.7 V supply.

13-4 16:52-17:04

118-dB Dynamic Range, Continuous-Time, Opened-Loop Capacitance to Voltage Converter Readout for Capacitive MEMS Accelerometer

Kevin Chai{1}, Dong Han{1}, Ravinder Pal Singh{1}, Duy Dong Pham{1}, Chin Pang{1}, Jianwen Luo{1}, David Nuttman{2}, Minkyu Je{1}

{1}Agency for Science, Technology and Research / IME, Singapore; {2}Phsical Logic, Israel

Abstract: This paper presents a high performance AFE interface circuit for capacitive MEMS accelerometer. The AFE is implemented in a CT, chopper stabilized, trancapacitance CVC topology with a VGA and an LPF with 300 Hz bandwidth. The noise analysis of each blocks of the AFE is also presented in this paper. The AFE achieved a minimum noise resolution of 27 nV / rtHz. Long term stability showed an input offset with an Allan deviation floor of 60 nVrms . The AFE achieved a nonlinearity of +/- 1 % using a slow input ramp signal.

Session 14 Over-sampled Data Converters

Time: 15:50-17:55

Room: Crowne Ballroom B

Co-Chairs: Zhongyuan Chang (IDT Shanghai)

Yuichi Okuda (Renesas Electronics Corp.)

14-1 15:50-16:15

A 20MHz Bandwidth Continuous-Time ΣΔ Modulator with Jitter Immunity Improved Full-Clock Period SCR (FSCR) DAC and High Speed DWA

Jun-Gi Jo, Jinho Noh, Changsik Yoo

Hanyang University, Korea, South

Abstract: A 20MHz bandwidth continuous-time ΣΔ modulator with third-order active-RC loop filter and 4-bit quantizer is implemented in a 0.13μm CMOS process. The immunity to clock jitter is greatly improved by employing full clock period switched-capacitor-resistor (FSCR) DAC for feedback. A new data weighted averaging (DWA) technique is adopted to remove the timing bottleneck at 640MHz clock frequency. The modulator achieves 63.9dB peak-SNDR. Dynamic range is 68dB and decreases by only 2.3dB when RMS clock jitter is 15ps. The power consumption is 58mW from a 1.2V supply.

14-2 16:15-16:40

A 1.2, 78dB HDSP ADC with 3.1V Input Signal Range

Omid Rajaee{2}, Seiji Takeuchi{1}, Mitsuru Aniya{1}, Koichi Hamashita{1}, Un-Ku Moon{2}

{1}Asahi-Kasei Microdevices, Japan; {2}oregon state university, United States

Abstract: A low power, high resolution two-step hybrid delta- sigma/pipelined modulator (HDSP) is presented. The feedback architecture of the HDSP modulator is modified to allow higher orders of noise shaping. The pipelined quantizer is simplified. Finally, the input signal range of the HDSP modulator is extended beyond the supply voltage. The prototype chip is implemented in a 0.18μm CMOS process. With a 1.56 MHz bandwidth, 2.6 mW analog power consumption and 1.2 V analog supply voltage, the measured dynamic range and SNDR of this prototype IC are 78dB and 75dB.

14-3 16:40-17:05

A 1V 350μW 92dB SNDR 24 Khz ΔΣ Modulator in 0.18μm CMOS

Liyuan Liu, Dongmei Li, Liangdong Chen, Chun Zhang, Shaojun Wei, Zhihua Wang

Tsinghua University, China

Abstract: This paper presents a high precision multi-bit audio ΔΣ modulator working under 1V supply. We propose a kind of asynchronous 4-bit successive approximation quantizer without fast clock generation. Feed-forward topology with digital summing is adopted to relax the OTA design requirement. Power efficient single stage OTA is adopted to drive the large sampling capacitor with low power. Fabricated in 0.18μm standard CMOS, the modulator achieves 92dB SNDR with 24 kHz bandwidth and consumes only 350μW. The active core die area is 0.64mm2.

14-4 17:05-17:30

A Low-Power Continuous-Time Delta-Sigma Modulator for Electret Microphone Applications

Hashem Zare-Hoseini{1}, Izzet Kale{2}, Richard Morling{2}

{1}Cambridge Silicon Radio, United Kingdom; {2}University of Westminster, United Kingdom

Abstract: A continuous-time delta-sigma modulator that maybe used as an interface for Electret microphones is presented. The third order modulator comprises a single-ended-to-differential-converter integrated inside the loop-filter with a single-ended high-impedance input, an RC integrator on the first stage and Gm-C integrators for the other stages. Gm-C integrators comprise highly-linear low-power transconductances. The modulator has been designed and fabricated in the TSMC 0.18μm technology for audio application (300Hz-10kHz) with a single supply voltage of 1.8V and a single-ended input signal with a peak of 125mV. The measured dynamic range of the modulator is 86dB with a power consumption of 240uA.

14-5 17:30-17:42

A Regulator-Free 84dB DR Audio-Band ADC for Compact Digital Microphones

Huy-Binh Le, Sang-Gug Lee, Seung-Tak Ryu

Korea Advanced Institute of Science and Technology, Korea, South

Abstract: A 20kHz audio-band ADC with a single power-supply pad is implemented for a digital electret microphone. The designed low-noise preamplifier not only relaxes the ADC design requirement but also provides an excellent interface for the electret capacitor. A low power 4th-order switched-capacitor Sigma-Delta modulator converts the analog signal into 1b digital. Under the single power-supply pad, the switching noise effect on the signal quality is estimated via post simulations with simplified parasitic models. Performance degradation is minimized by time-domain noise isolation (TDNI) with sufficient time-spacing between the sampling edge and the output transition. A prototype ADC was implemented in a 0.18 μm CMOS process. It operates under a minimum supply voltage of 1.6 V with total current of 420 uA. Operating at 2.56 MHz clock frequency, it achieves 84 dB dynamic range and a 64 dB peak signal-to-(noise + distortion) ratio. The measured power supply rejection at a 100 mVpp 217 Hz square wave is -72 dB without any supply regulation.

14-6 **17:42-17:54**

Power Optimization of High Performance Delta-Sigma Modulators for Portable Measurement Applications

Jian Xu{2}, Xiaobo Wu{2}, Hanqing Wang{2}, Junyi Shen{2}, Bill Liu{1}

{1}Analog Devices, Inc., China; {2}Zhejiang University, China

Abstract: Power optimization of two high performance Delta-Sigma modulators for portable measurement applications is presented. One modulator is a single-bit topology with 89.8dB peak SNDR and 20uW power at a 1.5V supply. A new power efficient current mirror Class-AB OTA is introduced here. The other modulator adopts MBSO technique to achieve 80.5dB peak SNDR and consume only 9uW at a 1.8V supply. Especially, a new fully switched-off SO with 50% power saving and double FOM is proposed. Besides, a novel resonator idea applicable to SO technique is adopted to realize a coefficient of 1/100 with 75% power and 70% area reduction. Both modulators are fabricated in a low cost 0.35uW CMOS process with a bandwidth of 1 kHz. The measured results show high FOM of the designed modulators.

Session 15 **Memory**

Time: 15:50-17:55

Room: Conference Room 8

Co-Chairs: Kazuhiko Kajigaya (Elpida Memory Inc.)

Yufeng Xie (Fudan University)

15-1 **15:50-16:15**

A Digitized Replica Bitline Delay Technique for Random-Variation-Tolerant Timing Generation of SRAM Sense Amplifiers

Yusuke Niki, Atsushi Kawasumi, Azuma Suzuki, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Fumihiko Tachibana, Yuki Fujimura, Tomoaki Yabe

Toshiba Corporation, Japan

Abstract: A digitized replica bitline delay technique has been proposed for random-variation-tolerant timing generation of SRAM sense amplifiers. The sense timing variation attributable to the random variation of transistor threshold voltage is reduced by sufficient count of multiple replica cells, and replica bitline delay is digitized and multiplied for adjusting it to the target sense timing. The variation of the generated timing was 34% smaller than that with a conventional technique and cycle time was reduced by 16% at the supply voltage of 0.6V in 40nm CMOS technology with this scheme.

15-2 16:15-16:40

Highly Reliable Reference Bitline Bias Designs for 64Mb and 128Mb Chain FeRAMs

Ryu Ogiwara, Daisaburo Takashima, Sumiko Doumae, Shinichiro Shiratake, Ryousuke Takizawa, Hidehiro Shiga

Toshiba Corp., Japan

Abstract: This paper demonstrates the new reference bitline bias designs for 64Mb and 128Mb chain FeRAMs. A bias generator for 64Mb compensates cell signal level shift of "1" and "0" data due to temperature variation, and improves signal margin by ±22mV. A unique reference circuit called "elevator circuit" for 128Mb also compensates array voltage fluctuation as well as signal level shift with temperature variation. The reference bitline bias varies with temperature variation and improves cell signal window by ±40mV at low 1.8V VDD, and varies with array voltage VAA variation and improves cell signal window by ± 44mV at 1.5V ±0.2V VAA.

15-3 16:40-17:05

A 5.42nW/Kb Retention Power Logic-Compatible Embedded DRAM with 2T Dual-Vt Gain Cell for Low Power Sensing Applications

Yoonmyung Lee, Mao-Ter Chen, Junsun Park, Dennis Sylvester, David Blaauw

University of Michigan, United States

Abstract: A logic-compatible 2T dual-Vt embedded DRAM (eDRAM) is proposed for ultra-small sensing systems to achieve 8x longer retention time, 5x lower refresh power and 30% reduced area compared with the lowest power eDRAM previously reported. With an area-efficient single inverter sensing scheme designed for R/W speed compatibility with ultra-low power processors, 58% array efficiency is maintained for memories as small as 2kb and for as few as 32 bits per bitline.

15-4 17:05-17:30

A Fully CMOS-Compitible 672-Bit EEPROM for Passive RFID Tag Application

Jong-Min Baek{2}, Jung-Hoon Chun{2}, Kee-Won Kwon{2}, Jihong Kim{1}, Myung Ho Yoo{1}

{1}Samsung TECHWIN Co., LTD, Korea, South; {2}Sungkyunkwan University, Korea, South

Abstract: This paper presents a 672-bit electrically erasable programmable read-only memory (EEPROM) which can be fabricated using the conventional 0.13 μm CMOS process. The write voltages are lowered to 6 V and -4 V using planar cell structure on the isolated p-wells. The amount of electrons removed from the floating gate is regulated by real time monitoring to improve the Vth variation of erased cells. The read and write power dissipations are 2.1 uW and 26 uW, respectively, at room temperature.