ADVANCE PROGRAM

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

ISSCC

UNIVERSITY OF PENNSYLVANIA

2002 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 3, 4, 5, 6, 7

CONFERENCE THEME:
ICs FOR INFORMATION TECHNOLOGIES

SAN FRANCISCO MARRIOTT HOTEL

SUNDAY ALL-DAY: 1 WORKSHOP: Telecom Access Circuits; 7 TUTORIALS 2 SPECIAL EVENING SESSIONS: Inductance (for Digital); Low-Power Design

WEB REGISTRATION: Hotel, Conference: 1 Short Course, 7 Tutorials, 2 Workshops

5-DAY PROGRAM

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

CONFERENCE HIGHLIGHTS

On Sunday, February 3rd, the day before the official opening of the Conference, ISSCC 2002 offers a choice of up to 3 of a total of 7 Tutorials. The SSCTC Workshop on *Analog Telecom Access Circuits and Concepts* is also offered during the day on Sunday. New for 2002, two special-topics evening sessions addressing next-generation circuit design challenges will be offered on Sunday starting at 7:30PM: *Inductance: Implications and Solutions for High-Speed Digital Circuits,* and *Low-Voltage Design for Portable Systems*. These sessions offer leading experts in the field presenting tutorial background and state-of-the-art design strategies in a workshop format and are open to all ISSCC attendees.

On Monday, February 4th, ISSCC 2002 offers three plenary papers followed by five parallel sessions of technical papers. There will be a Social Hour for all registrants from 5:00PM to 6:30PM in the Golden Gate Hall (on the level above the Ballroom). Evening panel discussions will be held on Monday and on Tuesday evenings from 8:00PM to 10:00PM. Technical sessions continue on Tuesday and Wednesday.

On Thursday, February 7th, ISSCC 2002 offers an ISSCC Microprocessor Design Workshop on *High-Frequency Clocking: Issues and Solutions for Clocking High-Frequency Microprocessors.* The ISSCC Short Course on *Wideband Communications* will also be held on Thursday. Three sessions of the Short Course will be offered with staggered starting times; these will be filled on a first-come, first-served basis.

Use of the ISSCC web-registration site is strongly encouraged. You will be provided with immediate confirmation on registration for Tutorials, SSCTC Workshop, ISSCC Workshop and ISSCC Short Course if you use web registration either through the link on the ISSCC website (www.isscc.org) or directly to the ISSCC registration site (www.seminarsource.com/isscc2002).

CONFERENCE INFORMATION

The **timing of papers permits session-hopping** without missing important material. This Program gives you the starting time for each paper. Taking of **pictures and videos** during sessions is **not permitted**. A printed supplement with speakers' visuals will be sent to all registered attendees within one month of the conclusion of ISSCC 2002.

A CDROM containing both the ISSCC 2002 Digest of Technical Papers and the Visuals Supplement will be mailed in late Spring to speakers and all attendees paying the member or non-member Conference registration fee.

Conference Information: Courtesy Associates, Fax: 202-973-8722; email: isscc@courtesyassoc.com.

Press Information: Kenneth C. Smith, University of Toronto, Phone: 416-978-5033; Fax: 416-971-2286; email: lcfujino@cs.com

Registration: SeminarSource, **FAX: 1-619-293-7332 or 1-619-293-0793**; **Telephone: 1-619-293-0684 or 1-888-288-1827.**

Sponsorship: ISSCC 2002 is sponsored by the IEEE Solid-State Circuits Society. Co-sponsors are the IEEE San Francisco Section and Bay Area Council, and the University of Pennsylvania.

Website: See **http://www.isscc.org**

CONTENTS

TUTORIALS

**T1: Specifications and Figures of Merit for Mixed-Signal Circuits—
A Guide to Understanding Where the Numbers Come from and
What They Mean.**

This tutorial explores specifications of mixed-signal circuits featured at ISSCC. An overview is provided of what the specification means, what makes the specification important for a given circuit, what is easy and what is difficult, and what to watch for when specs are quoted. Different "Figures of Merit" (where specifications are combined) are considered. Performance benchmarks from past (and present) ISSCCs are provided. Specifications of A/D converters, D/A converters, amplifiers, filters, VCOs and phase-locked loops are discussed.

Instructor: David Robertson is Product Line Director of the High Speed Converter Group at Analog Devices, Inc. He received BA and BE from Dartmouth College, in 1984 and 1985 respectively, and since 1985 has worked at Analog Devices as a design and product engineer on a wide variety of D/A and A/D converters on complementary bipolar, BiCMOS and CMOS processes. He holds 14 patents on converter and mixed-signal circuits, has participated in two Best Panel ISSCC Evening Panel Sessions, and is co-author of a paper that received the JSSC 1997 Best Paper Award.

T2: Design for Reliability in CMOS VLSI

As VLSI continues to scale, the likelihood of chip failure increases dramatically. At the same time, consumers expect electronic systems will be increasingly reliable. Rather than being confined to technical conferences and publications, reliability failures of high-profile computer systems now make headline news. This tutorial reviews the most common failure mechanisms and terms used to describe them. It describes three categories of reliability: (1) hard failures such as electromigration and gate-oxide breakdown, (2) soft failures induced by alpha particles and cosmic ray neutron hits, and (3) circuit failures caused by mechanisms such as leakage sensitivity and thermal hot spots. For each of these failure mechanisms, strategies are considered for analysis and design-around.

Instructor: David Greenhill is Senior Engineer of Sun Microsystems UltraSparc design team in Sunnyvale, CA. In 1986, he graduated from Imperial College, London, with Physics BSc. From 1986 to 1992, he worked for INMOS in Bristol, England, on CMOS VLSI design, color look-up tables, video controllers, and transputer microprocessor design. He joined Sun Microsystems in 1992 and worked on the UltraSparcI and UltraSparcII designs. He is currently Chief Engineer for the implementation of UltraSparcV. His interests include high-performance CMOS circuit design and technology, CAD and reliability of high-performance multiprocessor computer systems. He is involved in circuit analysis and design tradeoffs for reliability in these systems. He has been a member of the ISSCC Program Committee since 1997.

T3: High-Dynamic-Range Image Sensors

This tutorial provides a framework for analyzing performance of image sensor dynamic range (DR) extension techniques and for comparing their effectiveness. A brief introduction to conventional image sensors, such as CCDs, CMOS APS and DPS is provided. A model is given for the signal path through an image sensor from input photocurrent to output voltage, including signal integration, dark current, temporal noise, and FPN. The model is used to define DR and SNR. Techniques for extending image sensor DR, including well-capacity adjusting, spatially-varying pixel exposure, time to saturation, and multiple capture are described. These techniques are compared, based on SNR. As DR is extended, some of these techniques suffer from higher loss in SNR than others, which limits their effective DR extension. Comparisons based on other critera such as spatial resolution and implementation complexity are discussed. Other types of high-DR sensors, e.g., logarithmic sensors and silicon retina, are discussed. Recent research in the area is covered.

Instructor: Abbas El Gamal received BS EE from Cairo Univ. in 1972, MS in statistics and PhD in EE from Stanford in 1977 and 1978, respectively. From 78-80 he was Asst. Prof. of EE at Univ. of Southern California. He joined Stanford in 1981, where he is now Prof. of EE. From 1984-8, on leave from Stanford, he was Director of LSI Logic Research Lab, cofounder and Chief Scientist of Actel. From 1990-1995 he was a cofounder and Chief Technical Officer of Silicon Architects (now part of Synopsys). He is principal investigator on the Stanford Programmable Digital Camera Project. His research interests include: CMOS image sensors and digital camera design, image processing, network information theory, and electrically-configurable VLSI design and CAD. He has authored or coauthored over 100 papers and 25 patents in these areas. He serves on the board of directors and advisory boards of several IC and CAD companies. He is Fellow of the IEEE and member of the ISSCC Program Committee.

T4: Ferroelectric Memory Design (FeRAM 101)

FeRAMs are nonvolatile memories that compete favorably today with EEPROMs and Flash memories in terms of write speed and power consumption. This tutorial covers the basics of ferroelectric materials, ferroelectric capacitors as circuit elements, ferroelectric memory cell circuits and their read/write operations, reference generation, and FeRAM architectures.

Instructor: Ali Sheikholeslami is an Asst. Prof. of ECE at the Univ. of Toronto. His research interests are VLSI memory design (including SRAM, DRAM, and content-addressable memories), ferroelectric memory design (circuit design and modeling), multiple-valued memories, and high-speed signaling. He has several journal and conference papers and two US patents in the area of ferroelectric memories.

TUTORIALS

T5: Architectures and Design Methods for Cryptography

As electronic systems evolve from centralized to distributed, communicating devices, the need for security and encryption grows. This tutorial introduces the basics of cryptographic algorithms, the specialized mathematics involved, and the protocols commonly used today (e.g., SSL and IPsec). The tutorial then maps the various functions and protocols to VLSI architectures and describes different implementation techniques.

Instructor: Ingrid Verbauwhede, Univ. of California, Los Angeles, received PhD from K. U. Leuven, Belgium in 1991. From 1992-1994, she was visiting post-doc researcher at U.C. Berkeley. From 1994 to 1998, she was Principal Engineer at TCSI and ATMEL, and in 1998, joined UCLA as Assoc. Prof.. Her current interest is architecture design, design methods and VLSI implementation of specialized processors for wireless communication, networking and encryption.

Instructor: Jim Goodman, Lumic Electronics, Ottawa, Canada, received PhD from MIT in 2000, where his research focused on reconfigurable energy-efficient VLSI architectures for cryptography. From 2000 to 2001 he was Senior IC Architect at Chrysalis-ITS, developing next-generation network security processors. He is currently Senior Mixed Signal Architect at Lumic Electronics, developing low-power multimedia processors.

T6: Introduction to Wireless-Receiver Design

An introduction to integrated receivers focuses on performance requirements for GSM cellular handset applications: (1) Overview of radio standards for sensitivity, blocking, AM suppression, and intermodulation. (2) Comparison of heterodyne, direct conversion, and low-IF receiver architectures. (3) Discussion of design specifications and tradeoffs.

Instructor: G. Tyson Tuttle, Silicon Labs, Austin TX holds an MS from UCLA and a BS from John Hopkins Univ., both in EE. He has held positions at Crystal Semiconductor and Broadcom Corp. focusing on high-speed mixed-signal circuit design for hard disk drive read channel and Ethernet applications. He joined Silicon Labs in 1997 where he is currently Product Manager for CMOS cellular wireless transceiver ICs. He holds 6 patents, is author or co-author of 6 technical publications, and is a member of IEEE.

T7: CMOS Optical-Front-End Circuits

This tutorial provides analysis of CMOS integration techniques and their limitations for optical-front-end circuits: (1) Discussion of transimpedance amplifiers and their optimization for speed and sensitivity. (2) Description of decision networks for data-recovery and its problems. (3) Examples and implementations of CMOS Gb/s circuits.

Instructor: Michel Steyaert received his PhD in Electronics from Katholieke Universiteit Leuven in 1987. In 1988 he was Visiting Asst. Prof. at the University of California, Los Angeles. From 1989-1996 he was NFWO Senior Research Associate at the ESAT Lab., K. U. Leuven, where he is now Professor. His research interests are high-frequency analog integrated circuits for high-frequency signal processing and for telecommunication circuits.

SSCTC WORKSHOP ON ANALOG TELECOM

W1: Analog Telecom-Access Circuits and Concepts
IEEE Solid State Circuits and Technology Committee Workshop

Organizing Chair: Jan Sevenhans, Alcatel Belgium, IEEE Fellow

Committee: Paul Davis, Consultant; Trudy Stetzler, TI; Franz Dielacher, Infineon, Villach; Cormac Conroy, Berkana Wireless; Behzad Razavi, UCLA; Michiel Steyaert, KULeuven; Russ Apfel, Legerity; Anantha Chandrakasan, MIT; Stan Schuster, IBM, Bryan Ackland, Agere

The analog design community faces challenges of requirements for analog front-end building blocks such as high-voltage high-performance high-efficiency line drivers, high-resolution high-speed A/D and D/A converters, and upstream/downstream filters.

The major success of DSL technology worldwide places all telecom manufacturers under pressure for next-generation DSL products: increasing density of the lines per board, reducing power consumption per line and maximizing loop reach and robustness against disturbances such as RFI and bridge taps.

DMT signalling has opened golden gates on copper cable but leaves the system with a power bottleneck in the line drivers because of the high crest factor. Class A/B amplifiers, still in ADSL production lines, will soon be replaced with Class G, Class H, Class K and other high-efficiency power amplifier concepts re-invented today, going back to the future and remembering audio low-power high-efficiency concepts.

Loop-reach requirement push analog designers to achieve 14b-resolution A/D and D/A converters in high-volume-production highly-integrated analog front ends. Sigma-delta pipelined and various subranging architectures at the interface between analog and digital are revisited in advanced research programs. FDM upstream/downstream filtering is reconsidered to avoid carrier attenuation in the filter overlap region and the consequent loss of loop reach.

Speakers from telecom and silicon industry and from university research centers bring attendees up to date on the analog challenges of this emerging access application.

W1 (Continued)

Topics	Time
Welcome & Introduction	8:30-8:45
Trade Offs in ADSL Analog Front-End Requirements **Peter Reusens**, Alcatel, Antwerp, Belgium	8:45-9:30
Analog Design Challenges in ADSL Filter and Low-Noise Circuits. **Samuel Sheng**, LSI Logic, San Jose, CA	9:30-10:15
BREAK	15 min
ADSL Transceivers : Optimizing Power, Cost, Function and Performance **Russell Apfel**, Legerity, Austin, TX	10:30-11:15
ADSL Line Transceivers, Power and RX Integration Trends **Marco Corsi**, Texas Instruments, Dallas, TX	11:15-12:00
LUNCH	12:00-2:00
Silicon Technologies and Circuit Topologies for High Efficiency in ADSL Line Drivers **Domenico Rossi**, STMicroelectronics, Agrate, Italy	2:00-2:45
Line Drivers for xDSL **Tim Piessens**, K.U. Leuven, Leuven, Belgium	2:45-3:30
AFE Design for VDSL: a Case Study **Joerg Hauptman**, Infineon, Villach, Austria	3:30-4:15
BREAK	15 min
Concluding panel: DSL Analog Strategy of the Future.	4:30-5:30
Conclusion	5:30

SPECIAL TOPIC EVENING SESSIONS

SE1: Inductance: Implications and Solutions for High-Speed Digital Circuits

Co-Organizer/Co-Chair: William J Bowhill, Intel Corp., Shrewsbury, MA
Co-Organizer: Anantha Chandrakasan, MIT, Cambridge, MA
Co-Chair: Stephen Kosonocky, IBM, Yorktown Heights, NY

Technology scaling is realizing designs containing hundreds of millions of transistors capable of multi-GHz operation. For high-slew-rate signaling with low-resistance interconnects, on-chip inductance is no longer negligible. This session provides a comprehensive overview and describes practical approaches an IC designer can use to include inductance effects in chip designs.

The session begins with an overview of the extraction and analysis issues related to on-chip inductance effects, followed by a description of a partial-element equivalent circuit (PEEC) interconnect model and how these can be used for construction of a comprehensive model that includes portions of the power and ground grid surrounding the signal net and return path.

Techniques for managing the effects of inductance in the context of general on-chip busses are also described which provide the IC designer with the necessary methods, rules of thumb, and back-end tool checks to both constrain their effects in the front-end design phase and verify their correctness in the back-end prior to tape out.

A special section dedicated to clock network modeling describes clock distribution strategies which now require well-optimized and controlled on-chip transmission line design. This includes a description of a full-wave PEEC interconnect analysis tool combined with 3D visualization for studying high-frequency effects.

Scaling trends in VLSI have created significant challenges for chip power delivery and distribution as supply voltages have decreased. Accurate modeling of the power distribution network becomes important, which includes information about the entire distribution network, decoupling capacitors hierarchies, board and package planes, vias, and bumps. The final session describes constructs to build power distribution models, the trade-offs and some design solutions to typical problems.

Topics	Time
Inductance Extraction and Modeling	7:30 PM
David Blaauw, Univ. of Michigan	
Kaushik Gala, Motorola Inc., Austin, TX	
On-chip Signaling	8:00 PM
Shannon Morton, Silicon Graphics, Boston, MA	
Clock Distribution	8:30 PM
Phillip Restle, IBM, Yorktown Heights, NY	
Xuejue Huang, Univ. California, Berkeley, CA	
The Chip Electrical Interface	9:00 PM
Claude Gauthier, Sun Microsystems, Sunnyvale, CA.	
Brian Amick, Sun Microsystems, Austin, TX	

SE2: Low-Voltage Design for Portable Systems

Organizer/Co-Chair: Wanda Gass, Texas Instruments, Dallas, TX, USA
Co-Chair: Thucydides Xanthopoulos, Cavium Networks, Marlboro, MA, USA

The processing requirements of portable devices are increasing at a fast pace as new algorithms, higher data rates and new system features are introduced. Technology scaling, in addition to low- power requirements for battery-powered devices, make low-voltage operation a design requirement.

In the past, there has been reliance on process and technology improvements to support increased circuit performance and lower power dissipation. Further technology-driven gains will come at an increased cost, necessitating better design practices.

Analog and RF designers are continuously challenged to design circuits using very low voltages, while still maintaining large dynamic ranges. New architectures and innovative uses of passive elements will be required to satisfy stringent product specifications.

On the digital side, the challenge is to continue improving performance as well as maintaining low leakage. Back biasing techniques in addition to device stacking, multiple threshold device usage and supply voltage gating can control standby and active leakage currents in deep sub-micron processes.

In addition, low-voltage operation reduces noise margins, and smaller feature sizes increase susceptibility to various noise sources. The resulting noise effects require accurate modeling and design considerations to ensure robust circuit operation.

The panelists enumerate and describe the challenges that lie ahead as application demand for performance, small feature sizes, and long battery life pose conflicting requirements to circuit and system designers. In addition, they address potential solutions to the aforementioned issues.

Topics	Time
Technology, Architecture and Applications **Robert Brodersen**, Prof., Univ. of California, Berkeley, CA, USA	7:30 PM
When MOSFET Switches Become MOSFET Dimmers **Dennis Buss**, Vice President, Texas Instruments, Dallas, TX, USA	8:00 PM
RF Circuits at Low Voltage **Asad Abidi**, Professor, Univ. of California, Los Angeles, CA, USA	8:30 PM
Leakage Reduction in Digital CMOS Circuits **Shekhar Borkar**, Intel Fellow and Director, Intel Corp, Hillsboro, OR, USA	9:00 PM
Robustness of Digital Circuits @ Low Voltage Harry Veendrick, Research Fellow, Philips, Eindhoven, The Netherlands	9:30 PM

SESSION 1   SALON 7-9

PLENARY SESSION – INVITED PAPERS

Chair:　　　　　　　　　**Tim Tredwell**, Eastman Kodak Research
　　　　　　　　　　　　　　Labs, Rochester, NY
　　　　　　　　　　　　　　ISSCC Executive-Committee Chair
Associate Chair:　　　　**Willy Sansen**, Katholieke Universiteit
　　　　　　　　　　　　　　Leuven, Leuven, Belgium
　　　　　　　　　　　　　　ISSCC Program-Committee Chair

FORMAL OPENING OF CONFERENCE　　　　　**8:30 AM**

1.1　Technology in the Internet Age　　　　　**8:40 AM**
　　　Dennis Buss, Texas Instruments, Dallas, Texas, USA

Internet electronic products have requirements different from those of personal computers (PCs). The increasing importance of Internet electronics is driving changes in development of IC technology. One important characteristic of the Internet Age is computational disaggregation. Whereas, over the past 20 years, PCs have been characterized by ever-increasing computation capabilities, emerging Internet electronic products are characterized by sufficient computation to achieve the function in a small, often portable, form factor. The imperative for lower cost, which enables penetration into mass markets, is a second area where Internet electronic products differ from PCs. Disaggregation and cost requirements are driving an unprecedented degree of system-on-a-chip (SoC) integration. In the Internet Age, SoC integration means more than integrating different digital cores. It also means integrating functions that are realized today in different technologies: logic, memory, analog, power management, passives and radio or wireline driver, depending on the product. Because SoC integration is motivated primarily by cost, diverse functions must be integrated together in standard CMOS with minimal cost addition. Cost-effective embedded memory technology also needs to be developed. Current examples of SoC integration include cell phones, cable/DSL modems, and internet audio. These representative examples, together with others, are driving changes in the way ICs are developed. In the latter half of the decade, it is likely that SoC integration will expand to include MEMS, microphotonics, and on-chip energy sources. Moore's Law scaling will continue at least through the end of this decade, but SoC integration will become an increasingly important technology imperative for continued cost reduction throughout the Internet Age.

ISSCC, SSCS, JSSC, & IEEE AWARD PRESENTATIONS 9:30 AM

　　　　　　　　　　　　　　　　　　　　　BREAK   10:00 AM

1.2 Semiconductor Memories for IT   10:15 AM
C. G. Hwang, Samsung Semiconductor Memory, Yongin City, Korea

Information technology (IT) emerged from the 1970s based on main-frame computers. Since then, PCs and the Internet world have drastically expanded the IT industry along with rapid growth of network and communication technology. For almost all platforms, semiconductor memories have been a key enabling technology.

In the PC era, DRAM density increase has been driven by rapid expansion of applications with advanced operating systems. In the future, servers will continue driving high-density DRAM requirements, and the maximum memory size of servers will be one of the key performance parameters. 512Mb DRAM will be widely available in 2002 and 16Gb DRAM is expected to appear within the next 10 years.

Performance of semiconductor memories will be driven by graphics applications and network systems. 1Gb/s/pin DRAM will be popular in 2002 and 2Gb/s/pin in 2004 for high-end graphics applications. Random-access times in the range of 5ns for SRAM and 20ns for DRAM range and 1Gb/s/pin DRAM will be available in 2002, and even faster (frequency, latency) memories will be required for high-end network systems such as OC-768-based switches and routers and beyond.

Mobile platforms, especially 3G phones and PDAs, are driving low-voltage low-power memories. Standby power of DRAM and pseudo-SRAM has been reduced drastically over the last 2 years. 1.8V DRAM will be in volume production in 2002 and 1.0V DRAM is expected in 2005 for longer battery life and moving-picture capability of mobile applications. The small-form-factor requirement of mobile phones and consumer applications such as PDA, and DSC will expedite various multi-chip-package solutions such as SRAM+Flash, DRAM+Flash, and SRAM+DRAM+Flash. Recent digital convergence and the rapid reduction of $/MB of mass storage flash memory increased the usage of flash memory in various mobile and consumer applications.

Semiconductor Memory will continue to follow Moore's law for at least the next 10 years and will be lead by mass storage flash memory technology. Memory requirement of various IT platforms will continue to increase the trend of MB/system and MB/person.

1.3 Ambient Intelligence: the Next Paradigm for   11:05 AM
Consumer Electronics:
How will it Affect Silicon?
Fred Boekhorst, Philips Research, Eindhoven, The Netherlands

Ambient Intelligence refers to an environment where the user experience is what matters. People want to have fun, feel free, enjoy life, feel secure, be in control and be productive. This experience is not linked to one particular device but is realized by a network of devices present in the environment that will provide us these experiences in an intelligent way.

Ambient Intelligence is introduced as a new paradigm in consumer electronics. Some of the technologies required for Ambient Intelligence are covered, with a focus on IC consequences. Ongoing work in three fields is described: ubiquitous radio, intuitive user/system interfaces and three-dimensional visual displays. These three fields highlight the diverse nature of Ambient Intelligence technologies as well as the resulting requirements for ICs. Considerations with respect to an introduction timeline of Ambient Intelligence are given.

BREAK   11:55 AM

IMAGE SENSORS

Chair: Charles V. Stancampiano, Eastman Kodak, Rochester, NY
Associate Chair: Yoshiaki D. Hagiwara, Sony Corp., Tokyo, Japan

2.1   A 1/1.8" 3M-pixel FT-CCD with On-Chip Horizontal Sub-Sampling for DSC Applications

1:30 PM

L. Le Cam[1], J. Bosiers[1], A. Kleimann[1], H. van Kuijk[1], J. Maas[1],
M. Beenhakkers[1], H. Peek[1], P. van de Rijt[1], A. Theuwissen[1,2]
[1]Philips Semiconductors, Eindhoven, The Netherlands
[2]Delft Univ. of Technology, The Netherlands

A 1/1.8" 3M-pixel frame-transfer CCD (FT-CCD) has on-chip horizontal sub-sampling. It allows an additional preview mode where the image extraction rate is doubled (up to 60 images/s) while keeping the classic readout frequency of 25MHz. High-sensitivity video clips, fast auto-focus, and auto-exposure is achieved on digital still cameras.

2.2   Single-Chip CMOS Image Sensor for Mobile Applications

2:00 PM

K. Yoon[1], C. Kim[1], B. Lee[2], D. Lee[1]
[1]Hynix Semiconductor Inc., Ichon Korea
[2]National Semiconductor, Santa Clara, CA

A CIF CMOS Image sensor contains fundamental color signal processing functions on-chip. The analog line memory, which can be accessed twice, enables simple color-interpolation and other signal processing in a small chip. At 30frames/s, the sensor consumes 20mW at 3.0V supply.

2.3   Single Chip for Imaging, Color Segmentation, Histogramming, and Pattern Matching

2:30 PM

R. Etienne-Cummings[1,2], P. Pouliquen[1,2], M. Anthony Lewis[2]
[1]Johns Hopkins Univ., Baltimore, MD
[2]Iguana Robotics, Inc., Baltimore, MD

128(H)x64(V) x RGB CMOS imager is integrated with region-of-interest selection, RGB-to-HSI transformation, HSI-based pixel segmentation, 36-bins x 12b HSI histogramming, and sum-of-absolute-difference template matching. 32 learned color templates are stored and compared to each frame. At 30frames/s, it uses 1mW.

BREAK   3:00 PM

2.4   138dB-Dynamic-Range CMOS Image Sensor with New Pixel Architecture

3:15 PM

D. Stoppa, A. Simoni, L. Gonzo, M. Gottardi, G. Dalla Betta
Loc. Pante' di Povo, Trento, Italy

A 128x64 pixel image sensor in 0.35μm 3.3V CMOS technology achieves 138dB dynamic range by adapting single-pixel integration time to the local illumination conditions. Video frame rate is achieved with 0.2% rms temporal noise and 14mW power in a test chip.

2.5   1.5M Pixel Imager with Localized Hole-Modulation Method
3:45 PM

T. Miida, K. Kawajiri, H. Terakago, T. Endo, S. Yamamoto, T. Okazaki, A. Nishimura
Innotech Corp., Yokohama, Japan

A 1.5Mpixel imager with 4.2μm square pixel is composed of a single MOSFET and a pinned photo-diode. A localized high-density p-region near the source of MOSFET converts the accumulated hole number to source voltage. Low random noise, low dark signal, high sensitivity with good color reproduction and resolution are achieved.

2.6   A 1.0V V_{DD} CMOS Active-Pixel Image Sensor with Complementary-Pixel Architecture Fabricated with a 0.25μm CMOS Process
4:00 PM

C. Xu, M. Chan
Hong Kong Univ. of Science & Technology, Clear Water Bay, Hong Kong

A 128x128 complementary CMOS active-pixel sensor (CAPS) is fabricated in 0.25μm CMOS for low -voltage application. A single-slope with correlated double sampling (CDS) is used in the readout circuit. The chip operates at a V_{DD} as low as 0.8V with 15dB added dynamic range compared with conventional CMOS APS.

2.7   A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of >100 Frames
4:15 PM

T. Goji Etoh[1,2], D. Poggemenn[2], A. Ruckelshausen[2], A. Theuwissen[3,6], G. Kreider[3], H.-O. Folkerts[3], H. Mutoh[4], Y. Kondo[5], H. Maruno[5], K. Takubo[5], H. Soya[5], K. Takehara[1], T. Okinaka[1], Y. Takano[1], T. Reisinger[1,2], C. Lohmann[1,2]
[1]Kinki Univ., Higashi-Osaka, Japan
[2]Univ. of Applied Sciences, Osnabrueck, Germany
[3]Philips Semiconductors, The Netherlands
[4]Link Research Corp., Japan
[5]Shimadzu Corp., Japan
[6]Delft Univ. of Technology, The Netherlands

A single-chip CCD image sensor captures >100 successive images at >1Mframes/s. The pixel count of the test chip is 312 x 260 (=81,120) pixels. Charge handling capacity is 40k electrons. Grey levels are 10b. Fill factor is 13%. On-chip overwriting mechanism makes possible continuous recording of the latest image signals, draining the old ones to the substrate.

2.8   A 35mm-Film Format CMOS Image Sensor for Camera-Back Applications
4:30 PM

J. Hurwitz, M. Panaghiston, K. Findlater, R. Henderson, T. Bailey
STMicroelectronics, Edinburgh, Scotland, UK

A 5V 1120x1808 pixel 35mm-film format CMOS image sensor for camera-back use, fabricated in 0.5μm 2P3M technology, includes integrated light -detection circuitry using non-destructive pixel read and consumes <50μW. Reticle stitching is employed for the large format. Dynamic range is 66dB and peak SNR is 55dB.

CONCLUSION   4:45 PM

SESSION 3   SALON 7

DIGITAL SIGNAL PROCESSORS, CIRCUITS, AND SYSTEMS

Chair: Willie Anderson, Analog Devices, Austin, TX
Associate Chair: Steve Morein, ATI Research, Marlborough, MA

3.1   A Packet-Memory-Integrated 44Gb/s Switching Processor with 10Gb Port and 12 1Gb Ports

1:30 PM

M. Lau, S. Shieh, P. Wang, B. Smith, M. Yuan, D. Lee, J. Gaba, J. Chao, B. Shung, C. Shih
Broadcom Corp., San Jose, CA

A 44Gb/s switching processor chip has 1MB embedded packet memory. With a 10Gb and 12 1Gb ports, this chip is useful for LAN/WAN bridging applications. Wirespeed switching performance is demonstrated using a shared buffer switching architecture. This 0.18µm CMOS processor integrates a 10Gb port with an XGMII interface.

3.2   A 6GOPS General-Purpose DSP with an Enhanced Instruction Set for Wireless Communication

2:00 PM

F. Lange, A. Olofsson, M. Jalfon, H. Meirov, A. Kadry, D. Agur, O. Chalak, T. Ben-Nun Glass, R. Holzer, O. Raikhman, D. Agur, Z. Greenfield
Analog Devices, Herzelia, Israel

A 6GOPS DSP implements the TigerSharc architecture with an instruction set enhanced for wireless communication. It is implemented in a 0.13µm process with 8 layers of copper interconnect and operates at 250MHz with 1W power dissipation under nominal conditions.

3.3   A 600MHz VLIW DSP

2:30 PM

S. Agarwala, P. Koeppen, T. Anderson, A. Hill, M. Ales, L. Simar, R. Damodaran, L. Nardini, P. Wiley, S. Mullinnix, J. Leach, A. Lell, M. Gill, J. Golston, D. Hoyle, A. Rajagopal, A. Chachad, M. Agarwala, R. Castille, N. Common, J. Apostol, H. Mahmood, M. Krishnan, D. Bui
Texas Instruments, Dallas, TX

A 600MHz VLIW DSP delivers 4800MIPS, 2400 (16b) or 4800 (8b) million multiply accumulates at 0.3mW/MMAC (16b). The chip has 64M transistors and dissipates 718mW at 600MHz and 1.2V, and 200mW at 300MHz and 0.9V. It has an 8-way VLIW DSP core, a 2-level memory system, and an I/O bandwidth of 2.4GB/s.

BREAK   3:00 PM

3.4   A 175mV Multiply-Accumulate Unit Using an Adaptive Supply Voltage and Body Bias (ASB) Architecture

3:15 PM

M. Miyazaki[1,2], J. Kao[1], A. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Hitachi Ltd., Tokyo, Japan

The power dissipation of a digital circuit is minimized by simultaneous control of power supply voltage and body bias. The technique minimizes power dissipation for varying processing rates through dynamic adjustment of V_{dd} and V_{bb}. A 16b MAC operates at 166kHz and 14nW at 175mV V_{dd}. A ring oscillator operates at 0.1V.

3.5   A 1.3GSample/s Full-Rate Self-Timed 10-Tap FIR with Variable Latency and Clocked Interfaces

3:45 PM

J. Tierno[1], A. Rylyakov[1], S. Rylov[1], M. Singh[2], P. Ampadu[3], S. Nowick[2], M. Immediato[1], S. Gowda[1]
[1]IBM, Yorktown Heights, NY
[2]Columbia Univ., New York, NY
[3]Cornell Univ., Ithaca, NY

A 6b 10-tap digital FIR has a self-timed datapath, clocked interfaces, and variable latency. The $0.45mm^2$ circuit in 0.18μm CMOS is operational form 1.2V to 2.1V power supply, and has 80mW dissipation at 300MSample/s and 4 cycles of latency, and 500mW at 1.3GSample/s and 7 cycles of latency.

3.6   A GSM/GPRS Mixed-Signal Baseband IC

4:15 PM

D. Redmond, M. Fitzgibbon, A. Bannon, D. Hobbs, C. Zhao, K. Kase, J. Chan, M. Priel, K. Traylor, K. Tilley
Motorola, Austin, TX

A dual-core baseband processor IC for GSM/GPRS cellular phone applications is built in a 0.13μm CMOS process with 5 levels of copper interconnect and contains a high level of mixed signal integration which includes: 1GHz CMOS synthesizer, 10b general-purpose ADC, two 14b ADCs, power amplifier controller, and 13b voice CODEC.

3.7   A 0.55nV/√Hz Gigabit Fully-Differential CMOS Preamplifier for MR/GMR Read Application

4:45 PM

Z. Zheng, S. Lam, S. Sutardja
Marvell Semiconductor, Inc., Sunnyvale, CA

A low-noise Gb fully-differential preamp in 0.25μm CMOS has a variable gain with constant 850MHz bandwidth, and has a variable bandwidth with constant gain. Noise is <0.55nV/√Hz. The power consumption is 600mW. The die of a 4-channel IC is $<4.2mm^2$.

CONCLUSION   5:15 PM

BACKPLANE INTERCONNECTS AND CLOCK MULTIPLIERS

Chair: Wai Lee, Texas Instruments, Dallas, TX
Associate Chair: Mehmet Soyuer, IBM, Yorktown Heights, NY

4.1   A 1.5V 86mW/ch 8-Channel 622-2500Mb/s/ch CMOS SerDes Macrocell with Selectable MUX/DEMUX Ratio   1:30 PM

F. Yang, J. O'Neill, P. Larsson, D. Inglis, J. Othmer
Agere Systems, Holmdel, NJ

An 8-channel serial link transceiver realizes 20Gb/s full duplex total I/O throughput with <700mW dissipation from a 1.5V supply and occupies $2mm^2$ in 0.16µm CMOS. An analog DLL allows tracking of frequency offset up to 400ppm. The receiver, employing an integrate-and-dump front-end, achieves a 30mVpp sensitivity.

4.2   Quad 3.125Gb/s/channel Transceiver with Analog Phase Rotators   2:00 PM

D. Zheng, X. Jin, E. Cheung, M. Rana, G. Song, Y. Jiang, Y. Sutu, B. Wu
BitBlitz Communications, Fremont, CA

A $0.18µm^2$ CMOS quad transceiver provides 12.5Gb/s full-duplex raw data throughput at 200mW/channel consumption. An analog phase rotator in CDR eliminates quantization error of digital phase interpolation techniques, resulting in <17ps peak-peak output jitter.

4.3   A 62Gb/s Backplane-Interconnect ASIC Based on 3.1Gb/s Serial-Link Technology   2:30 PM

P. Landman[1], A. Yee[1], R. Gu[1], B. Parthasarathy[1], V. Gupta[1],
S. Ramaswamy[1], L. Dyson[1], P. Bosshart[1], J. Reynolds[1], M. Frännhagen[2],
P. Fremrot[2], S. Johansson[2], K. Lewis[2], W. Lee[1]
[1]Texas Instruments, Dallas, TX
[2]Turin Networks, Petaluma, CA

A backplane interconnect ASIC with 62Gb/s full-duplex aggregate throughput uses 3.1Gb/s serial link technology organized as 20 bidirectional channels to realize bandwidth. The chip operates with <5×10⁻¹⁷ aggregate BER and is fabricated in a 0.18µm CMOS technology, dissipating 9W in a 768-pin flipchip BGA package.

BREAK   3:00 PM

4.4   An 800Mb/s Physical-Layer LSI with Hybrid Port Architecture for Consumer Electronics Networking

3:15 PM

T. Yoshikawa, T. Yoshida, T. Ebuchi, Y. Arima, T. Iwata, K. Nishimura,
H. Kimura, Y. Komatsu, H. Yamauchi
Matsushita Electric, Osaka, Japan

A physical layer LSI has one DS-port and two βports in accordance with IEEE1394-2000 and P1394b Draft 1.01 respectively. The 0.25µm CMOS LSI realizes 800Mb/s and 1.2km peer-to-peer IEEE1394 networking through βport. Each βport requires 180mW active power and is trea ted as ASIC macro for future large system integration.

4.5   A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly-Integrated Data-Communication Chips

3:45 PM

R. Farjad-rad, W. Dally, J. Poulton, H. Ng, T. Stone, R. Nathan
Velio Communications, Milpitas, CA

The MDLL, in 0.18µm CMOS, has 0.05mm^2 active area and 200MHz to 2GHz speed range. The complete synthesizer, including the output clock buffers, dissipates 12mW from a 1.8V supply at 2.0GHz. This MDLL architecture is used as a clock multiplier in a highly-integrated chip, and has jitter of 1.73ps (rms) and 15.6ps (pk-pk) at 2GHz.

4.6   A Multiple-Crystal-Interface PLL with VCO Realignment to Reduce Phase Noise

4:15 PM

S. Ye[1], L. Jansson[2], I. Galton[1]
[1]Univ. of California, San Diego, CA
[2]Silicon Wave, San Diego, CA

A phase realignment technique is applied to a ring oscillator VCO in a 3V 6.8mW CMOS PLL that converts most of the popular crystal reference frequencies to a 32MHz baseband clock and RF PLL reference. The peak in-band phase noise at 20kHz offset is -102dBc/Hz with the technique enabled, and -92dBc/Hz with the technique disabled.

4.7   A Multichip-on-Oxide 1.0Gb/s Fully-Differential CMOS Transimpedance Amplifier for Optical Interconnect Applications

4:45 PM

J. Lee[1], S. Song[1], S. Min Park[1], C. Nam[2], Y. Kwon[1], H. Yoo[1]
[1]Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea
[2]Telephus, Taejon, Korea

A 1.0Gb/s 80dBΩ fully-differential TIA uses 0.25µm CMOS and multichip-on-oxide (MCO) process. MCO enables integration of PD, TIA, and planar inductors of Q=21.1 for shunt peaking on an oxidized silicon substrate. Interchannel crosstalk and power dissipation are <-40dB and 27mW, respectively. MCO and TIA chips are 5x5mm^2 and 0.7x1mm^2, respectively.

4.8   45GHz SiGe Active Frequency Multiplier

5:00 PM

S. Hackl[1,2], J. Boeck[1], G. Ritzberger[1,2], M. Wurzer[1], H. Knapp[1],
L. Treitinger[1], A. L. Scholtz[2]
[1]Infineon Technologies AG, Munich, Germany
[2]Technical Univ. of Vienna, Vienna, Austria

A frequency quadrupler for frequencies up to 45GHz uses a pre-production 0.4µm SiGe bipolar technology. Gain is achieved at   -15dBm input power between 24 and 45GHz with maximum of 7.3dB at 44GHz. The circuit draws 84mA from a single 5V supply.

CONCLUSION   5:15 PM

SESSION 5   SALON 9

WIRELESS NETWORKING TRANSCEIVERS

Chair: Mary Jo Nettles, Mobilian, San Diego, CA
Associate Chair: Tom Schiltz, Linear Technology Corp., Colorado Springs, CO

5.1   A Bluetooth Radio in 0.18μm CMOS.

1:30 PM

P. van Zeijl[1], J. Eikenbroek[1], P. Vervoort[1], S. Setty[2], J. Tangenberg[1], G. Shipton[2], E. Kooistra[1], I. Keekstra[1], D. Belot[3]
[1]Ericsson Eurolab, Emmen, The Netherlands
[2]Ericsson Microelectronics, Swindon, United Kingdom
[3]STMicroelectronics, Crolles, France

A Bluetooth radio in 0.18μm CMOS technol   ogy works on 2.5-3.0V, dissipating 75mW in RX and 90mW in TX. RX uses a 2MHz IF with an active poly-phase bandpass filter. The fractional-N PLL uses a VCO running at 5GHz. TX uses IQ modulation. Special attention is paid to Si-crosstalk because this radio is combined with baseband circuitry. Silicon area is 5.5mm^2.

5.2   A Direct-Conversion Single-Chip Radio-Modem for Bluetooth

2:00 PM

G. Chang[1], L. Jansson[1], K. Wang[1], J. Grilo[1], R. Montemayor[1], C. Hull[2], M. Lane[1], A. X. Estrada[1], M. Anderson[1], I. Galton[1], S.V. Kishore[1]
[1]Silicon Wave Corp., San Diego, CA
[2]now at National Semiconductor, San Diego, CA

A fully-integrated radio-modem using a direct-conversion receiver architecture achieves -83dBm sensitivity at 0.1% BER, +40dBm IIP2, and -5dB and -40dB adjacent and alternate channel blocking C/I, respectively. The radio consumes 39mA in receive and 37mA in transmit mode with a 2.7V supply. The 19.5mm^2 chip uses a 0.35μm 27GHz f$_T$ SOI BiCMOS process.

5.3   Design of a Low-Cost Integrated 0.25μm CMOS Bluetooth SOC in 16.5mm^2 Silicon Area

2:30 PM

J. Cheah, E. Kwek, E. Low, C. Quek, M. Choke, C. Yong, R. Enright, J. Hirbawi, A. Lee, H. Xie, L. Wei, L. Luong, J. Pan, S-T. Yang, W. Ngai, A. Lau, L. Chew
Transilica, San Diego, CA

A complete 0.25μm CMOS SOC bluetooth solution adopts a two -die in a single MCM chip packaging approach with minimum product cost as the most important design goal while maintaining competitive power consumption and RF performance.

BREAK   3:00 PM

5.4   A 5GHz CMOS Transceiver for IEEE 802.11a Wireless LAN

3:15 PM

D. Su[1], M. Zargari[1], P. Yue[1], S. Rabii[1], D. Weber[1], B. Kaczynski[1],
S. Mehta[1], K. Singh[1], S. Mendis[1], B. Wooley[2]
[1]Atheros Communications, Sunnyvale, CA
[2]Stanford Univ., Stanford, CA

A 5GHz transceiver comprising the RF and analog circuits of an IEEE 802.11a-complaint WLAN using a 0.25µm CMOS technology occupies 22mm^2. The IC has 22dBm maximum transmitted power, 8dB overall receive-chain noise figure, and -112dBc/Hz synthesizer phase noise at 1MHz offset.

5.5   A 2.4GHz RF Transceiver with Digital Channel-Selection Filter for Bluetooth

3:45 PM

M. Kokubo, M. Shida, T. Ishikawa, H. Sonoda, K. Yamamoto,
T. Matsuura, M. Matsuoka, T. Endo, T. Kobayashi, K. Oosaki, T. Henmi,
J. Kudoh, H. Miyagawa
Central Research Lab., Hitachi Ltd, Tokyo, Japan

An RF transceiver chip for Bluetooth that uses a digital channel-selection filter is 3.3x3.4mm^2, realized by decrease of the analog area using the digital channel selection filter. The test chip uses 0.35µm BiCMOS.

5.6   Single-Chip 5.8GHz Electronic-Toll-Collection Transceiver IC with PLL and Demodulation Circuits

4:15 PM

T. Masuda[1], K. Ohhata[2], N. Shiramizu[2], T. Maruyama[3], S. Hanazawa[3],
M. Kudoh[3], Y. Tanba[3], Y. Takeuchi[3], H. Shimamoto[2], T. Nagashima[4],
K. Washio[2]
Hitachi, Ltd., [1]Kokubunji, Tokyo/ [3]Ome, Tokyo/ [4]Yokohama, Kanagawa, Japan
[2]Hitachi Device Engineering, Co. Ltd., Tokyo Japan

A single-chip 5.8GHz ETC transceiver IC with PLL and demodulator uses SiGe HBT/CMOS. The fully-integrated ETC chip includes a 31dB-gain RX stage, an ASK demodulator, and a high-precision RSSI. The PLL is constructed with a varactor-tuned LC-VCO and a low-power BiCMOS synthesizer. The TX stage incorporates a transformer-transferred single-ended PA.

CONCLUSION   4:45 PM

SESSION 6 SALON 10-15

NON-VOLATILE MEMORIES AND SRAM

Chair: Jagdish Pathak, Sub-Micron Circuits, San Jose, CA
Associate Chair: Ban-Pak Wong, Sun Microsystems, Palo Alto, CA

6.1 A 512Mb, NROM Data Storage Memory with 8MB/s Data Rate
1:30 PM

E. Maayan[1], R. Dvir[1], J. Shor[1], D. Avni[1], B. Eitan[1], E. Stein[2], Z. Cohen[3], M. Meyassed[3], H. Palm[3], Y. Alpern[3].
[1]Saifun Semiconductors, Netanya, Israel
[2]Infineon Technologies, Düsseldorf, Germany
[3]Ingentix Semiconductor, Netanya, Israel

The NROM technology is applied to EEPROM, Flash, and data storage product lines. All the products are based on the two-bit-per-cell core technology, using common design concepts, algorithms, circuits, and the same process architecture. Differing product requirements emphasize versatility of the concept.

6.2 A 44mm^2 4-Bank 8-Word Page-Read 64Mb Flash Memory with Flexible Block Redundancy and Fast Accurate Word-Line Voltage Controller
2:00 PM

T. Tanzawa[1], A. Umezawa[1], T. Taura[1], H. Shiga[1], T. Hara[1], Y. Takano[1], T. Miyaba[2], N. Tokiwa[2], K. Watanabe[1], H. Watanabe[1], K. Masuda[1], K. Naruke[1], H. Kato[1], S. Atsumi[1]
[1]Toshiba Corp., Yokohama, Japan
[2]Toshiba Mircoelectronics Corp., Kawasaki, Japan

Combining a negative-gate channel-erasing NOR flash memory technology with an aggressively-scaled NAND flash process technology results in a 64Mb NOR flash memory with 0.27µm^2 cell and 44mm^2 chip. The flash memory provides 4 independent banks for flexible dual operation and unique block redundancy for yield.

6.3 A 1.8V 1Gb NAND Flash Memory with 0.12µm Process Technology
2:30 PM

J. Lee, H. Im, D. Byeon, K. Lee, D. Chae, K. Lee, Y. Lim, J. Lee, J. Choi, Y. Seo, J. Lee, K. Suh
Samsung Electronics, Yongin, Korea

A 1.8V 1Gb flash memory uses a 0.12µm STI process technology. A charge pump operates at <1.8V. A center-placed row decoder is digitized in one block pitch by applying 32-cell NAND structure. A page buffer, containing two latches, supports cache-program to improve program speed to 7MB/s.

BREAK 3:00 PM

6.4   A 125mm² 1Gb NAND Flash Memory with 10MB/s Program Throughput   3:15 PM

H. Nakamura[1], K. Imamiya[1], T. Himeno[1], T. Yamamura[1], T. Ikehashi[1], K. Takeuchi[1], K. Kanda[1], K. Hosono[1], T. Futatsuyama[1], K. Kawai[1], R. Shirota[1], K. Shimizu[1], N. Arai[1], F. Arai[1], K. Hatakeyama[1], H. Hazama[1], M. Saito[1], H. Meguro[1], K. Conley[2], K. Quader[2], J. Chen[2]
[1]Toshiba, Yokohama, Japan
[2]Sandisk, Sunnyvale, CA

A 125mm² 1Gb NAND flash uses 0.13μm CMOS. The cell is 0.077μm². Chip architecture is changed to reduce chip size and to realize 10.6MB/s throughput for program and 20MB/s for read. An on-chip page copy function provides 9.4MB/s throughput for garbage collection.

6.5   A Low-Power ROM using Charge Recycling and Charge Sharing   3:45 PM

B-D. Yang, L-S. Kim
KAIST, Taejon, Korea

A charge-recycling predecoder (CRPD), a charge-recycling word line decoder (CRWD), and a charge-sharing bit line (CSBL) reduce power in a memory. The CRPD and the CRWD recycle the charge used in predecoder lines and word lines. The CSBL reduces the bit line swing voltage. A 128kb ROM in a 0.35μm CMOS process consumes 8.63mW at 100MHz and 3.3V.

6.6   The 16kB Single-Cycle-Read-Access Cache on a Next-Generation 64b Itanium Microprocessor

4:15 PM

D. E Bradley[1], P. Mahoney[2], B. Stackhouse[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel Corp., Fort Collins, CO

A 16kB four-ported physically addressed cache operates at 1.2GHz with 19.2GB/s peak bandwidth. Circuit and microarchitectural techniques are optimized to allow a single-cycle read access latency. The cache occupies 3.2x1.8mm² in a 0.18μm process.

6.7   An On-Chip 3MB Subarray-Based 3rd-Level Cache for a Next-Generation 64b Itanium Microprocessor

4:45 PM

D. Weiss[1], J. Wuu[1], V. Chin[2]
[1]Hewlett-Packard, Fort Collins, CO
[2]Intel Corp., Santa Clara, CA

This 3MB on-chip level-three cache employs subarray design style, and achieves 85% array efficiency. Characterized to operate up to 1.2GHz, the cache allows a store and a load in every four core cycles, and provides a total bandwidth of 64GB/s at 1.0GHz.

CONCLUSION   5:15 PM

DISCUSSION SESSIONS

E1   Software Radio: Cool or to be Cooled?
(Salon 1-6)
Organizer/ Moderator: Michel S.Steyaert, Katholieke Universiteit
        Leuven, Belgium

All system designers dream of flexibility and easy, fast system adjustment. They dream of performing wireless transceiver functions in software. This would mean no nasty analog circuits. However, more analog functions are appearing. Is it possible to put A/D and/or D/A converter immediately before or after the antenna? Will this result in an unacceptable power drain, or will the solution enable more-efficient transmission techniques?

Panelists:

> **Qiuting Huang**, ETH Zurich, Lab, Switzerland
> **Raf Roovers**, Philips Research, Eindhoven, The Netherlands
> **Franz Dielacher**, Infineon Technologies, Villach, Austria
> **Bram Nauta**, Univ. of Twente, Enschede, The Netherlands
> **Simon Atkinson**, Analog Devices Inc., Wilmington, MA
> **Hiroshi Tsurumi**, Toshiba Corp., Corp. R&D Ctr., Kawasaki, Japan

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**E2   When Will Optical Interconnects Appear on
        High-Performance Microprocessors?**
(Salon 7)
Organizer: Stefanos Sidiropoulos, Aeluros Inc, Palo Alto, CA
Moderator: Ian Young, Intel Corp., Hillsboro, OR

Performance of modern processors is limited not by intrinsic transistor speed, but by bandwidth and latency of internal and external interconnects. Optical interconnect technology promises virtually unlimited bandwidth. Will large-scale digital chips be forced to use optical interconnects on-chip and to the rest of the system? Will on-chip copper interconnects with mixed-signal I/O and DSP techniques enable microprocessors to remain purely electrical chips? Are the cost/performance advantages of opto-electronics attractive enough to overcome the inertia of a mature industry?

Panelists:

> **Alina Deutsch**, IBM T. J. Watson Research Center, Yorktown Heights, NY
> **Karl Joachim Ebeling**, Infineon Technologies AG, Munich, Germany
> **Mark Horowitz**, Stanford Univ., Stanford, CA
> **David A. Miller**, Stanford Univ., Stanford CA
> **Sam Naffziger**, Hewlet Packard, Fort Collins, CO
> **Mitsumasa Koyanagi**, Tohoku Univ., Japan
> **Christer Svensson**, Linkoping Univ., Sweden

E3   **Does Moore's Law Apply to Analog?:**
Past, Present, and Future Implications of Technology
Progress and Higher Levels of Integration for Mixed-Signal
Circuits

(Salon 8)

Co-organizer: Venu Gopinathan, Broadcom Corp., Irvine, CA
Co-organizer, Moderator: David Robertson, Analog Devices,
    Wilmington, MA

Digital ICs have been governed by an increase in integration density obeying Moore's Law. Does the same law benefit the analog domain? Mixed-signal circuits care about SNR and dynamic range. Power dissipation is more than cv^2f. Are constantly-shrinking lithographies a boon or a curse? What are the important issues for integration of mixed-signal circuits? What are the hard and soft limits? Will designs hit a wall in deep sub-micron where mixed-signal integration no longer makes sense?

Panelists:

Kerry Bernstein, IBM, Essex Junction, VT
Lew Counts, Analog Devices, Wilmington, MA
Steven J. Hillenius, Agere Systems, Murray Hill, NJ.
Masao Hotta, Hitachi Ltd., Tokyo, Japan
Ted Tewksbury, Maxim Integrated Products, N. Chelmsford, MA.
Maarten Vertregt, Philips Research Labs, Eindhoven, The Netherlands
Bruce Wooley, Stanford Univ., Stanford, CA

E4   **Have Universities Killed Research - or Has Industry**
Corrupted It?

(Salon 9)

Organizer: Bud Taddiken, Microtune, Plano, TX
Moderator: Thomas H. Lee, Stanford Univ., Stanford, CA

Discussion covers ways to improve university/industry interactions for research. Is industry getting what it needs from university research? Is academia getting what it needs or wants? Industry says that it wants long-range fundamental research, but seems more interested in paying for short-range applied research. Is it just money for students? Are there pure motives to build on?

Panelists:

Hugo J. De Man, KU Leuven/IMEC, Leuven, Belgium
Herbert Eichfeld, Infineon Technologies AG, Munich, Germany
Teresa H. Meng, Stanford Univ., Stanford CA
J. Chris Ruddell, Consultant, Fremont, CA
Eric Swanson, Consultant, Buda, TX

SESSION 7   SALON 1-6

BASEBAND COMMUNICATIONS

Chair: Lars Thon, Atheros Communications, Sunnyvale, CA
Associate Chair: Ivo Bolsens, Xilinx Inc., San Jose, CA

7.1   A Unified Turbo / Viterbi Channel Decoder for 3GPP Mobile Wireless in 0.18µm CMOS

8:30 AM

M. Bickerstaff, D. Garrett, T. Prokop, C. Thomas, B. Widdup, G. Zhou,
C. Nicol, R. Yan
Lucent Technologies, North Ryde, Australia

A 3GPP-compliant 4.1Mb/s channel decoder supports data and voice calls in a unified Turbo/Viterbi architecture with hardware interleaver memory and pattern computation. The $9mm^2$ chip in 0.18µm 1.8V 6LM CMOS operates at 110MHz and consumes 306mW when decoding 2Mb/s data and voice calls.

7.2   An Integrated 802.11a Baseband and MAC Processor

9:00 AM

B. Baas, E. Cooper, J. Gilbert, G. Hsieh, P. Husted, A. Lokanathan,
J. Kuskin, D. McCracken, W. McFarland, T. Meng, D. Nakahira, S. Ng,
M. Rattehalli, J. Smith, R. Subramanian, J. S. Thomson, L. Thon,
Y. Wang, R. Yu, X. Zhang
Atheros Communications, Sunnyvale, CA

An 0.25µm CMOS mixed -signal baseband and MAC processor for the IEEE 802.11a WLAN standard in 0.25µm CMOS occupies $6.8 \times 6.8mm^2$ and contains 4.0M transistors in a 196-pin BGA package. Power consumption for transmit and receive is 326mW and 452mW. Additional data rates up to 108Mb/s are supported.

7.3   A 10Gb/s and 40Gb/s Forward-Error-Correction Device for Optical Communications

9:30 AM

L. Song, M. Yu, M. Shaffer
Agere Systems, Holmdel, NJ

Two forward error-correcting devices for OC-48/192/768 are implemented in 1.5V 0.6µm CMOS. A 10Gb/s (or Quad2.5 Gb/s) device with 424k -gate Reed-Solomon core consumes 343mW. A 40Gb/s device contains 364k-gates and consumes 361mW.

BREAK   10:00 AM

7.4   IIR Digital Filter for ΔΣ Decimation, Channel Selection, and Square-Root-Raised-Cosine Nyquist Filtering

10:15 AM

S. Mirabbasi, K. Martin
Univ. of Toronto, Toronto, Canada

A 1.8V 0.18μm CMOS ΔΣ decimation filter also performs channel-selection and an approximate root-raised-cosine Nyquist pulse-shaping. The $0.1mm^2$ IIR structure consumes 6.4mW (26.8mW) at 64MHz (240MHz) oversampling frequency.

7.5   A 300MHz Quadrature Direct Digital Synthesizer/Mixer in 0.25μm CMOS

10:45 AM

A. Torosyan[1], A. Willson, Jr.[2]
UCLA, [1]Glendale/ [2]Los Angeles, CA

A 0.25μm quadrature direct digital frequency synthesizer/mixer has 32b frequency control word, 0.07Hz tuning resolution, 12b inputs and 13b outputs offering 90.3dBc spurious-free dynamic range. The 4180 cell core occupies $0.36mm^2$. Power dissipation is <400mW at 300 MHz.

7.6   Direct Digital Frequency Synthesizers using High-Order Polynomial Approximation

11:15 AM

D. De Caro, E. Napoli, A. G.M. Strollo
Univ. of Napoli, Napoli, Italy

Two 80MHz 0.35μm 3.3V CMOS ROM-less DDFS using polynomial approximation are compared with Cordic-based circuits. A 60dBc SFDR DDFS uses 2nd-order polynomials and $0.18mm^2$, with 15mW dissipation. An 80dBc SFDR DDFS uses 3rd-order polynomials and $0.44mm^2$, with 35mW dissipation.

CONCLUSION   11:45 AM

SESSION 8   SALON 7

HIGH SPEED TIMING

Chair: Stefanos Sidiropoulos, Aeluros Inc., Palo Alto, CA
Associate Chair: Paul Landman, Texas Instruments, Dallas, TX

8.1   Jitter Optimization Based on Phase-Locked-Loop Design Parameters

8:30 AM

M. Mansuri, C-K Yang
Univ. of California, Los Angeles, CA

A tunable PLL allows independent optimization of loop parameters. The effects of varying PLL parameters (damping factor and bandwidth) on timing jitter is derived analytically and verified experimentally.

8.2   A Self-Regulating VCO with Supply Sensitivity <0.15%-delay/1%-supply

9:00 AM

I. Hwang[1], S-M. Kang[2]
[1]Univ. of Illinois at Urbana-Champaign, Urbana, IL
[2]Univ. of California, Santa-Cruz, CA

A self-regulating VCO has supply sensitivity <0.15%-delay/1%-supply. The design uses a differential delay cell that contains an nMOS transmission gate for delay adjustment and a built-in feedback circuit for power-supply rejection. The charge-pump PLL embedded with this VCO has 40ps peak-to-peak jitter at 450MHz output with VCO at 900MHz.

8.3   Low-Power Small-Area ±7.28ps Jitter 1GHz DLL-Based Clock Generator

9:30 AM

C. Kim[1], I. Hwang[2], S-M. Kang[3]
[1]IBM, Austin, TX
[2]Univ. of Illinois, Urbana, IL
[3]Univ. of California, Santa Cruz, CA

A 1GHz DLL-based clock generator in 0.35μm CMOS occupies 0.08mm^2. It has fast locking time and no jitter-accumulation problem. A phase detector with reset circuitry and a frequency multiplier overcome the limited locking range and frequency multiplication problem of conventional DLL-based systems. Measured peak-to-peak jitter is ±7.28ps.

BREAK   10:00 AM

8.4   The Clock Distribution of the POWER4 Microprocessor

10:15 AM

P. Restle[1], C. Carter[2], J. Eckhardt[3], B. Krauter[2], B. McCredie[2],
K. Jenkins[1], A. Weger[1], A. Mule[4]
[1]IBM, Yorktown Heights, NY/ [2]Austin, TX/ [3]Poughkeepsie, NY
[4]Georgia Institute of Technology, Atlanta, GA

The clock distribution on the Power4 supplies a single critical 1.5GHz clock from one SOI-optimized PLL to 15,200 pins on a large chip with 20ps skew and 35ps jitter. The network contains 64 tuned trees driving a single grid, and specialized tools to achieve targets on schedule with no adjustment circuitry.

8.5   The Core Clock System for a Next-Generation Itanium Processor

10:45 AM

S. Wells[1], F. Anderson[2], E. Berta[1]
[1]HP, Fort Collins, CO
[2]Intel, Fort Collins, CO

A PLL generates a high-frequency core clock for a 1GHz processor by multiplying up the system clock. The clock is distributed across the 19x14mm core via a shielded, balanced, H-tree to the final pulsed gated buffers with <62ps measured skew. Test features include phase shrinking and regional skew manipulation.

8.6   A Low-Power RISC Microprocessor using Dual PLLs in a 0.13μm SOI Technology with Copper Interconnect and Low-k BEOL Dielectric

11:15 AM

S. Geissler, D. Appenzeller, E. Cohen, S. Charlebois, P. Kartschoke,
P. McCormick, N. Rohrer, G. Salem, P. Sandon, B. Singer, T. Vonreyn,
J. Zimmerman
IBM, Essex Junction, VT

Microprocessors achieving clock frequencies >1GHz for mobile applications require solutions to maintain long battery life. Circuit and architecture solutions for dynamic frequency switching between multiple PLLs, DC power reduction methods, and impact of low-k dielectric on timing and power are discussed.

CONCLUSION   11:45 AM

SESSION 9   SALON 8

DRAM AND FERROELECTRIC MEMORIES

Chair: Mark Bauer, Intel, Folsom, CA
Associate Chair: T. S. Jung, Samsung Electronics, Yongin, Kyungki, Korea

9.1   Memory Design Using One-Transistor Gain Cell on SOI

8:30 AM

T. Ohsawa, K. Fujita, T. Higashi, Y. Iwata, T. Kajiyama, Y. Asao, K. Sunouchi
Toshiba Corp., Yokohama, Japan

A 512kb DRAM has a $7F^2$ one-transistor gain cell (F=0.18µm) on SOI. The array driving method makes selective write possible. Basic operation is verified by device simulation and hardware measurement. Simulations show 40ns access time. Non-destructive readout and Cb/Cs-free signal development improve cell efficiency.

9.2   An Offset-Cancellation Bit-Line Sensing Scheme for Low-Voltage DRAM Applications

9:00 AM

S. Hong, S. H. Kim, S. J. Kim, J. Wee, J. Chung
Hynix Semiconductor Inc., Ichon, Korea

Offset-cancellation provides low-voltage DRAM operation. The offset cancelling bit-line sense amplifers are pitch-matched to the conventional 0.16µm DRAM cell array without process modifications. Results indicate better refresh characteristics than conventional bit-line sense amplifiers even at 1.5V.

9.3   A 300MHz Multi-Banked eDRAM Macro Featuring GND Sense Bit-Line Twisting and Direct Reference-Cell Write

9:30 AM

J. Barth, D. Anand, J. Dreibelbis, E. Nelson
IBM, Essex Junction, VT

A 0.12µm growable eDRAM macro has GND sense, bit   -line twisting, direct reference cell write, a flexible multi-banking protocol, and column redundancy to support multi-banking. The protocol supports simultaneous activate, read/write and pre-charge to three different banks. Hardware measurements verify 300MHz operation, 6.6ns tacc, and 10ns trc.

BREAK   10:00 AM

9.4   A Hierarchy Bitline-Boost Scheme for Sub-1.5V Operation and Short Precharge Time on High-Density FeRAM

10:15 AM

H-B. Kang, H-W. Kye, G-I. Lee, J-H. Park, J-H. Kim, S-S. Lee, S-K. Hong, Y-J. Park, J-Y. Chung
Hynix Semiconductor Inc., Ichon, Korea

This work develops three concepts: low-voltage operation with boost voltage control of bitline and plateline, reduced bitline capacitance with multiple divided sub cell array, and increased chip performance with write operation sharing both active and precharge time period. A 256kb test chip with $3.0 \times 1.0 \mu m^2$ 1T1C memory cells in 0.25µm desig n roles is expected to achieve 180ns access and 70ns precharge at 1.5V based on internal probing.

9.5   A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage

10:45 AM

T. Nishihara, Y. Ito
Sony Corp., Kanagawa, Japan

A memory unit consists of multiple ferroelectric capacitors that store individual bits and share one access transistor. Disturb degradation and cross-talk effects are suppressed to an acceptable level. The capacitors can be multi-stacked, increasing packing density by a number of times.

9.6   A 0.25µm 3.0V 1T1C 32Mb Nonvolatile Ferroelectric RAM with ATD and CFLSA

11:15 AM

M-K. Choi, B-G. Jeon, N. Jang, B-J. Min, Y-J. Song, S-Y. Lee, H-H. Kim, D-J. Jung, H-J. Joo, K. Kim
Samsung Electronics, Yongin-City, Korea

A nonvolatile 32Mb ferroelectric random-access memory with 0.25µm design rules uses ATD control for SRAM applications and a common-plate folded bit-line cell scheme with current forcing latched sense amp for low noise level without cell area penalty.

CONCLUSION   11:45 AM

SESSION 10   SALON 9

HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

Chair: Venu Gopinathan, Broadcom Corp.
Associate Chair: K. Nagaraj, Texas Instruments

10.1   A 4GSample/s 8b ADC in 0.35µm CMOS

8:30 AM

K. Poulton[1], R. Neff[1], A.Muto[1], W. Liu[1], A. Burstein[2], M. Heshami[3]
[1]Agilent Technologies, Palo Alto, CA
[2]Volterra, Fremont, CA
[3]Virata, Cupertino, CA

A 4GSample/s 8b ADC in 0.35µm CMOS achieves accuracy of 7 effective bits at DC and 6.1 effective bits for 1GHz input, while dissipating 4.6W. It uses 32 current-mode pipelines driven by 32 interleaved clocks with 1.1ps rms accuracy.

10.2   A 6b 1.6GSample/s Flash ADC in 0.18µm CMOS Using Averaging Termination

9:00 AM

P. Scholtens, M. Vertregt
Philips, Eindhoven, The Netherlands

A 1.6GSample/s 6b flash analog-to-digital converter in 0.18µm CMOS for storage read channels is described. The array of amplifiers and averaging resistors is terminated with less overrange while maintaining full-scale linearity. Consuming 340mW, it achieves 5.7 effective bits at DC and 5 effective bits at 660MHz.

10.3   A 7b 450MSample/s 50mW CMOS ADC in 0.3mm^2

9:30 AM

K. Sushihara, A. Matsuzawa
Matsushita Electric Industrial Co., Osaka, Japan

A 7b 450MSample/s CMOS ADC in 0.18µm technology is used for the embedded digital read channel system in DVD SOC. A dynamic comparator and an interpolation circuit composed with gate-width-weighted transistors consumes 50mW and occupies 0.3mm^2.

BREAK   10:00 AM

10.4 A 10b 120MSample/s Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration

10:15 AM

S. Jamal[1], D. Fu[2], P. Hurst[3], S. Lewis[3]
[1]Marvell Semiconductor Inc., Sunnyvale, CA
[2]Maxim Integrated Products, Sunnyvale, CA
[3]Univ. of California at Davis, Davis, CA

Digital calibration using adaptive signal processing corrects offset mismatch, gain mismatch, and sample-time error between time-interleaved channels in a 10b 120MSample/s pipelined ADC. With background calibration, peak SNDR is 56.8dB and power dissipation is 234mW from 3.3V. Active area is 12.5mm^2 in 0.35μm CMOS.

10.5 A 16mW 30MSample/s 10b Pipelined A/D Converter Using a Pseudo-Differential Architecture

10:45 AM

D. Miyazaki, M. Furuta, S. Kawahito
Shizuoka Univ., Hamamatsu, Japan

A 16mW 2V 30MSample/s 10b pipelined A/D converter in 0.3μm CMOS uses a pseudo-differential architecture and a capacitor cross-coupled S/H stage. SNDR and the SFDR at 30MHz input are 54dB and 67dB, respectively.

10.6 A 1.2V 10b 20MSample/s Non-Binary Successive-Approximation ADC in 0.13μm CMOS

11:15 AM

F. Kuttner
Infineon Technologies, Villach, Austria

A successive-approximation ADC with non-binary code achieves 55dB SNR at sampling frequencies up to 20MHz. The converter, with on-chip driver for analog input and reference input, measures 0.08mm^2 in a standard 0.13μm CMOS process and consumes 12mW from a single 1.2V supply.

CONCLUSION   11:45 AM

TD: RF/HIGH-SPEED TECHNOLOGIES

Chair: John R. Long, Univ. of Toronto, Toronto, Ontario, Canada
Associate Chair: Takayuki Kawahara, Hitachi, Ltd., Kokobunji, Tokyo, Japan

11.1 0.13µm 210GHz-f_T SiGe HBTs - Expanding the Horizons of SiGe BiCMOS Applications

8:30 AM

A. Joseph[1], D. Coolbaugh[1], D. Harame[1], G. Freeman[2], S. Subbanna[2], M. Doherty[4], J. Dunn[1], C. Dickey[1], D. Greenberg[3], R. Groves[2], M. Meghelli[3], A. Rylyakov[3], M. Sorna[2], O. Schreiber[5], D. Herman[3], and T. Tanji[5]
[1]IBM, Essex Junction, VT/ [2]Hopewell Junction, NY/ [3]Yorktown Heights, NY/ [4]San Diego, CA/ [5]Edina, MN

SiGe BiCMOS is in its fourth lithographic generation since introduction of the 0.5µm. The key component is the SiGe -base HBT whose performance (f_T, f_{MAX}) is improved to >200GHz in the 0.13µm generation. Evolution and future directions of SiGe BiCMOS technology and product applications are reviewed.

11.2 An On-Chip 100GHz Sampling 8-channel Sampling-Oscilloscope Macro with Embedded Sampling-Clock Generator

9:00 AM

M. Takamiya[1], M. Mizuno[1], K. Nakamura[2]
[1]NEC Corp., Kanagawa, Japan
[2]Kyushu Institute of Technology, Iuzuka, Japan

An on-chip 8-channel sampling oscilloscope macro for signal integrity checking uses a 0.13µm CMOS process. It contains a phase-interpolated sampling clock generator for 100GHz sampling, charge-sharing sampling heads with -0.3V to Vdd+0.3V input range, and ESD-tolerant decoupling capacitors for noise-immune measurement.

11.3 High-Q FBAR Filters in a Wafer-Level Chip-Scale Package

9:30 AM

R. C. Ruby, A. Barfknecht, C. Han, Y. Desai, F. Geefay, G. Gan, M. Gat, T. Verhoeven
Agilent, Newark, CA

Wafer-level chip-scale packaged RF filters use thin-film bulk acoustic resonator technology. The 1x1mm^2 high-Q filter is hermetically sealed as two thin layers of silicon for ~12mil height. The full-band 1900MHz Tx filter mounted in a PCS power module has a 12MHz roll-off, and replaces external split-band SAW filters and their accompanying switches.

11.4   Polylithic Integration of SAW Devices using a Quartz-on-Silicon Process for Single-Chip Radio

9:45 AM

Y. Ku[1], Y. Eo[2]
[1]KAIST, Taejon, Korea
[2]LG Electronics Institute of Technology, Korea

A digitally temperature-compensated SAW oscillator uses Polylithic IC technology on a quartz-on-silicon wafer. The oscillator shows -115dBc/Hz phase noise at 10kHz offset, 7.5mW power consumption, and 4.5ppm frequency stability.

BREAK   10:00 AM

11.5   A Superconducting Bandpass ΔΣ Modulator with 2.23GHz Center Frequency and 42.6GHz Sampling

10:15 AM

J. F. Bulzacchelli[1], H-S. Lee[1], J. Misewich[2], M. Ketchen[2]
[1]Massachusettes Institute of Technology, Cambridge, MA
[2]IBM, Yorktown Heights, NY

A superconducting bandpass ΔΣ modulator employing a 2.23GHz microstrip resonator and a single flux quantum comparator clocked at 42.6GHz achieves 49dB peak SNR over a 20.8MHz bandwidth.   At 40.2GHz clock rate, in-band noise over a 19.6MHz bandwidth is -57dBFS. The test chip with integrated acquisition memory contains 4065 Josephson junctions and dissipates 1.9mW at T=4.2K.

11.6   A 43Gb/s Full-Rate-Clock 4:1 Multiplexer in InP-based HEMT Technology

10:45 AM

Y. Nakasha[1], T. Suzuki[1], H. Kano[1], A. Ohya[2], K. Sawada[1], K. Makiyama[1], T. Takahashi[1], M. Nishi[2], T. Hirose[1], Y. Watanabe[1]
[1]Fujitsu Labs Ltd., Atsugi, Kanagawa, Japan
[2]Fujistu Quantum Devices, Ltd., Showa, Nakagoma, Japan

A 43Gb/s 4:1 multiplexer in 0.13μm InP-based HEMT technology contains a 52Gb/s static D-FF and a phase adjuster giving the D-FF 360º effective phase margin. Microwave techniques and optimization of layout enable 43Gb/s operation with 43GHz full-rate clock. Power dissipation is 7.9W at -5.2V.

11.7   A 90Gb/s 2:1 Multiplexer IC in InP-based HEMT Technology

11:15 AM

T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, K. Imanishi, T. Hirose, Y. Watanabe
Fujitsu Labs Ltd., Atsugi, Kanagawa, Japan

A 90Gb/s 2:1 multiplexer IC uses 0.13μm -gate InP-based HEMT technology. Parallel 2-ch input data are serialized, and the differential outputs are $0.7V_{pp}$. The die is $1.9x1.8mm^2$ and consumes 1.3W from a -5.2V supply.

CONCLUSION   11:45 AM

TD: DIGITAL DIRECTIONS

Chair: Krste Asanovic, MIT, Cambridge, MA
Associate Chair: George Smarandiov, Atmel, San Jose, CA

12.1   Cellular Supercomputing with System-On-A-Chip

1:30 PM

A. Gara
IBM, Yorktown Heights, NY

System-on-a-chip technology allows a level of integration that can be leveraged to develop inexpensive high-performance, low-power computing nodes. When used in aggregate, this approach promises to challenge conventional supercomputer architectures in the high-performance computing arena. Systems under consideration reach into the hundreds of thousand nodes per machine. Architecture for these systems are described.

12.2   Dynamic Microarchitecture Adaptation via Co-Designed Virtual Machines   2:00 PM

J. Smith, A. Dhodapkar
Univ. of Wisconsin, Madison, WI

Co-designed virtual machines provide hardware designers with a hidden layer of software that can be used to manage configurable hardware units. A reconfiguration algorithm based on a mechanism for identifying recurring program phases provides power savings in caches and predictors up to 60%, without significantly affecting performance.

12.3   PicoRadios for Wireless Sensor Networks: The Next Challenge in Ultra-Low-Power Design   2:30 PM

J. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, T. Tuan
Univ. of California Berkeley, Berkeley, CA

Challenges and opportunities in design of integrated wireless sensor and actuator nodes, to be used in self-configuring ad-hoc networks, are described. To be viable, the node must be smaller than a couple of mm^3, cost <$1, and consume <100µW, allowing for energy scavenging from the environment.

BREAK   3:00 PM

12.4   Ovonic Unified Memory - A High-Performance Non-volatile Memory Technology for Stand-Alone Memory and Embedded Applications   3:15 PM

M. Gill[1], T. Lowrey[2], J. Park[3]
[1]Intel, Santa Clara, CA
[2]Ovonyx Inc., Santa Clara, CA
[3]Azalea Microelectronics Corp., Santa Clara, CA

Development status of Ovonic unified memory (OUM), a phase-change non-volatile semiconductor memory technology is discussed. Using 0.18µm 3V CMOS, cells from $5F^2$ to $8F^2$ are built in a charge-pump-free 4Mb development vehicle. Direct overwrite, 10ns reset times, 50ns set times, and 1.0×10^{12} cycling are achieved. Ten-year data retention is projected at 120°C.

12.5   Digital Logic Using Molecular Electronics

3:45 PM

S. Goldstein, D. Rosewater
Carnegie Mellon Univ., Pittsburgh, PA

A reconfigurable architecture is based on chemically-assembled electronic nanotechnology (CAEN). A molecular latch based on molecular RTDs provides I/O-isolation, voltage restoration, and fan-out using only 2-terminal devices.

12.6   Programmable Single-Electron-Transistor Logic for Low-Power Intelligent Si LSI

4:15 PM

K. Uchida[1], J. Koga[1], R. Ohba[1], A. Toriumi[2]
[1]Toshiba Corp., Yokohama, Japan
[2]Univ. of Tokyo, Tokyo, Japan

Room-temperature-operating single-electron devices work not only as single-electron transistors (SETs) but also as nonvolatile single-electron memories. It is demonstrated that the combination of Coulomb oscillations with the nonvolatile memory functions offers high programmability for LSIs. The power and delay of a programmable SET logic are estimated.

12.7   Ferroelectric-Based Functional Pass-Gate for Fine-Grain Pipelined VLSI Computation

4:45 PM

T. Hanyu[1], H. Kimura[1], M. Kameyama[1], Y. Fujimori[2], T. Nakamura[2], H. Takasu[2]
[1]Tohoku Univ., Sendai, Japan
[2]Rohm Co. Ltd., Kyoto, Japan

The state-transition scheme of remnant polarization in a ferroelectric capacitor performs storage and switching functions simultaneously with a functional pass-gate. As an example of fine-grain pipelined VLSI computation, a 250MHz 54×54b pipelined multiplier has 2.5W estimated power dissipation in a 0.6μm ferroelectric/CMOS technology.

12.8   A Diagonal-Interconnect Architecture and Its Application to RISC Core Design

5:00 PM

M. Igarashi[1], T. Mitsuhashi[1], A. Le[2], S. Kazi[2], Y-T. Lin[3], A. Fujimura[3], S. Teig[3]
[1]Toshiba, Kawasaki, Japan
[2]ArTile Microsystems, Inc., San Jose, CA
[3]Simplex Solutions, Inc, Sunnyvale, CA

Applying a design methodology based on an interconnect architecture characterized by pervasive use of diagonal wiring to a 128b RISC processor core design, results in 19.8% path delay reduction and 10% area reduction, compared to the conventional orthogonal interconnect architecture.

CONCLUSION   5:15 PM

SESSION 13   SALON 7

OVERSAMPLING A/D CONVERTERS

Chair: Brian Brandt, Maxim Integrated Products, Chelmsford, MA
Associate Chair: Bill Redman-White, Philips Semiconductor, San Jose, CA

13.1 A 1MHz-Bandwidth Second-Order Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for Low-IF Radio Receivers

1:30 PM

F. Henkel[1], U. Langmann[1], A. Hanke[2], S. Heinen[2], E. Wagner[2]
[1]Ruhr-Universität, Bochum, Germany
[2]Infineon Technologies AG, Düsseldorf, Germany

A 2nd-order continuous-time quadrature bandpass ΣΔ modulator with 1MHz IF clocked at 100MHz digitizes I and Q inputs with SNDR of 56.2dB for 1MHz bandwidth inputs. The 0.65µm BiCMOS chip consumes 21.8mW at 2.7V, and operates with a clock-frequency range of 25-100MHz.

13.2 A 50mW Bandpass ΣΔ ADC with 333kHz BW and 90dB DR
2:00 PM

R. Schreier[1], J. Lloyd[1], L. Singer[1], D. Paterson[1], M. Timko[1], M. Hensley[1], G. Patterson[1], K. Behel[1], J. Zhou[1], W. Martin[2]
[1]Analog Devices, Wilmington, MA
[2]Motorola, Ft. Lauderdale, FL

A mixer plus multi-bit bandpass ΣΔ ADC achieves 89dB and 77dB SNR in 35kHz and 333kHz bandwidths at 273MHz IF while consuming 16mA from a 3V supply. The 6th-order ADC combines continuous-time LC and active RC resonators with a discrete-time switched-capacitor resonator, and includes AGC capability.

13.3 A Dual-Mode 80MHz Bandpass ΣΔ Modulator for a GSM/WCDMA IF-Receiver

2:30 PM

T. Salo[1], T. Hollman[2], S. Lindfors[3], K. Halonen[1]
[1]Helsinki Univ. of Technology, Otakaari, Finland
[2]Texas Instruments, Espoo, Otaniemi Finland
[3]Aalborg Univ., Aalborg, Denmark

A band-pass ΔΣ modulator operating at 80MHz combines frequency down-conversion with A/D conversion. The two SC resonators are implemented using a single Op-Amp. A single-bit quantizer and feedback is used for GSM, but 4-bit quantizer is used for WCDMA. Measured peak SNRs are 80dB for 270kHz B/W (GSM), and 48dB for 3.84MHz B/W (WCDMA).

BREAK   3:00 PM

13.4   A 1.8V 14b ΣΔ A/D Converter with 4MSample/s Conversion

3:15 PM

R. Jiang[1], T. Fiez[2]
[1]Maxim Integrated Products, Hillsboro, OR
[2]Oregon State Univ., Corvallis, OR

A fifth-order single-stag e ΔΣ modulator achieves 14b resolution with 8x OSR and 4MHz conversion bandwidth in a 1.8V 0.18µm CMOS process. The DC gain of the internal op amps is 43dB. It occupies 1.3X2.2mm^2 and consumes 102mW analog power and 47mW digital power.

13.5   A 3.3mW ΣΔ Modulator for UMTS in 0.18µm CMOS with 70dB Dynamic Range in 2MHz Bandwidth

3:45 PM

R. Van Veldhoven[1], K. Philips[1], B. Minnis[2]
[1]Philips, Eindhoven, The Netherlands
[2]Philips, Redhill, UK

A 4th-order, continuous-time, ΣΔ modulator with 1.5b quantizer and feedback DAC for a UMTS receiver has 70dB DNR in a 2MHz band and -74dB THD at full scale. An IC including two modulators, a PLL and an oscillator dissipates 11.5mW at 1.8V. Active area is 0.41mm^2 in 0.18µm, 1 poly and 5-metal-layer CMOS technology.

13.6   A 64MHz ΣΔ ADC with 105dB IM3 Distortion using a Linearized Sampling Network

4:15 PM

S. Gupta, T. Brooks, V. Fong
Broadcom Corp., Irvine, CA

A ΣΔ ADC with 105dB distortion up to 1.5MHz signal bandwidth uses a linear sampling network in a 2-1-1 modulator. Operating at 64MHz clock frequency, the measured SNR in a 1.1MHz bandwidth is 88dB. The area, including bypass capacitors, is 2.6mm^2. The power consumed is 230mW, including references and decimation filter.

13.7   A 3V ΣΔ Receiver with Sampling Rate Enhancement for CDMA Baseband-Processor IC

4:45 PM

E. Liu, M. Chen, M. Pan
LSI Logic, Milpitas, CA

A 3V ΔΣ CDMA baseband receiver has a 4th -order single-loop modulator that enhances the effective sampling rate without increasing the actual rate, achieves 62dB DR, consumes 22mW, and occupies 1.3mm^2 in 0.25µm CMOS. The 8M transistor 10.5x10.5mm^2 chip integrates receiver, transmitter, voice codec, 10b ADC and DAC, PLL, 32kHz oscillator, two DSP, memory, and ARM.

CONCLUSION   5:15 PM

SESSION 14   SALON 8

CELLULAR RF WIRELESS

Chair: William Camp, Sony Ericsson Mobile Communications, Research Triangle Park, NC
Associate Chair: Tony Montalvo, Analog Devices, Inc., Raleigh, NC

14.1   A Dual-Band Direct-Conversion Transceiver IC for GSM
1:30 PM

S. Dow, B. Ball Weber, L. Chou, D. Eickbusch, J. Irwin, G. Kurtzman, P. Manapragada, J. Paramesh, G. Black, R. Wollscheid, D. Moeller, K. Johnson
Motorola, Austin, TX

The transceiver IC, in SiGe:C BiCMOS, contains dual LNAs, dual quadrature mixers, baseband filtering, RX and TX VCOs, and transmit buffers. The IC has GSM band performance of 67.5dB gain, 2.3dB NF, +49dBm IIP2, -9dBm IIP3 50dB image rejection, and TX noise <-162dBc/Hz at 20MHz.

14.2   A Single-Chip Quad-Band (850/900/1800/1900MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer.   2:00 PM

A. Molnar, R. Magoon, G. Hatcher, J. Zachan, W. Rhee, M. Damgaard, W. Domino, N. Vakilian
Conexant Systems Inc., Newport Beach, CA

A monolithic IC integrates all the active RF functions of a quad band GSM handset except for the PA. A direct-conversion receiver (900MHz NF 3.0dB, IIP2 +65dBm) and an up conversion loop transmitter (900MHz spectrum at 400kHz -65dBc, phase noise at 20MHz -164dBc/Hz) use a fractional-N PLL and fully-integrated transmit and UHF VCOs.

14.3   A Highly-Integrated Tri-Band/Quad-Mode SiGe BiCMOS RF-to-Baseband Receiver for Wireless CDMA/WCDMA/AMPS Applications with GPS Capability   2:30 PM

V. Aparin, P. Gazzerro, J. Zhou, B. Sun, S. Szabo, E. Zeisel, T. Segoria, S. Ciccarelli, C. Persico
QUALCOMM Inc., San Diego, CA

A 0.5µm SiGe BiCMOS single -chip receiver integrates three front-ends (LNA, RF-to-IF mixer, VGA) for the cellular, PCS/IMT and GPS frequency bands, a shared I/Q demodulator, IF VCO, and UHF LO buffers. It has 2.0dB NF and –0.6dBm IIP3 in the cellular CDMA mode and 2.3dB NF and –7dBm IIP3 in the PCS mode with <150mW at 3V.

BREAK   3:00 PM

14.4   A GSM/EDGE/WCDMA Modulator with On-Chip D/A Converter for Base Station   3:15 PM

J. Vankka, J. Ketola, O. Väänänen, J. Sommarek, M. Kosunen, K. Halonen
Helsinki Univ. of Technology, Espoo, Finland

A modulator with a 14b on-chip D/A converter occupies 22.09mm^2 in 0.35µm CMOS and dissipates1.7W at 3.3V with a 110MHz clock. A digital programmable up/down unit enables power ramping on a time-slot basis. The modulator fulfills the spectrum, phase and EVM specifications of GSM, EDGE and WCDMA.

14.5   A Highly-Integrated SiGe BiCMOS WCDMA Transmitter IC

3:45 PM

A. Bellaouar, M. Frechette, A. Fridi, S. Embabi
Texas Instruments, Dallas, TX

A highly-integrated SiGe BiCMOS WCDMA transmitter IC consists of VHF, UHF chains, and synthesizers. At 6dBm output power, it consumes 79mA at 2.7V, with a 5% rms EVM and -42dBc ACLR at 5MHz offset. In-band and receive-band output noise are -128 and -135dBm/Hz, respectively. Fully-integrated PLLs use on-chip VCO tanks, and require no off-chip loop filters.

14.6   A 0.18µm CMOS Direct-Conversion Receiver Front-End for UMTS

4:15 PM

F. Svelto, P. Rossi, F. Gatta, D. Manstretta, R. Castello
Università di Pavia, Pavia, Italy

The IC contains LNA, quadrature mixers and VGAs, realized in 0.18µm CMOS. It has +48.8dBm IIP2, -6dBm in band IIP3 (+1dBm out of band II3), 6.2dB DSB NF integrated in a 10kHz-1.92MHz band and draws 15mA from a 1.8V supply.

14.7   An 18mW 1800MHz Quadrature-Demodulator in 0.18µm CMOS

4:45 PM

D. Pfaff, Q. Huang
ETH Zurich, Zurich, Switzerland

The demodulator consists of a 3.6GHz VCO, a 3.8mA current-mode divider for the I/Q generation and two single-ended input, double-balanced mixers. The IC consumes 10mA at 1.8V, and has -114dBc phase noise at 100kHz offset, 40dB image rejection, 14dB DSB noise figure and 8.5dBm IIP3.

14.8   A 2GHz Direct-Conversion WCDMA Modulator in 0.25µm CMOS

5:00 PM

G. Brenna, D. Tschopp, D. Pfaff, Q. Huang
ETH Zurich, Zurich, Switzerland

A modulator IC delivers -8dBm maximum output power. Gain is programmable over a 78dB range in 1dB steps with 0.3dB accuracy. Consuming 41mA from a 2.5V supply, the modulator achieves a 15dBm OIP3, 50dBm OIP2, 36dB rejection of unwanted sideband, 47dB carrier suppression and -148dBc/Hz out-of-band-noise.

CONCLUSION   5:15 PM

TIMETABLE OF ISSCC 2002 SESSIONS

Sunday, February 3rd

ISSCC 2002 TUTORIALS

8:00 AM	T1: Specifications and Figures of Merit for Mixed-Signal Circuits T2: Design for Reliability in CMOS VLSI T3: High-Dynamic-Range Image Sensors T4: Ferroelectric-Memory Design (FeRAM 101)	T5: Architectures and Design Methods for Cryptography T6: Introduction to Wireless-Receiver Design T7: CMOS Optical-Front-End Circuits

SSCTC WORKSHOP

8:30 AM	SSCTC Workshop on Analog Telecom-Access Circuits and Concepts (Salon 7)

SPECIAL TOPIC EVENING SESSIONS: NEXT-GENERATION CIRCUIT-DESIGN CHALLENGES

7:30 PM	SE1: Inductance: Implications and Solutions for High-Speed Digital Circuits (Salon 1-6)	SE2: Low-Voltage Design for Portable Systems (Salon 7)

Monday, February 4th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 1: Plenary Session (Salons 7-9)				
1:30 PM	Session 2: Image Sensors (Salon 1-6)	Session 3: Digital Signal Processors, Circuits and Systems (Salon 7)	Session 4: Backplane Interconnect (Salon 8)	Session 5: Wireless-Networking Transceivers (Salon 9)	Session 6: Non-Volatile Memories and SRAM (Salon 10-15)
5:00 PM	Author Interviews and Social Hour (Golden Gate Hall)				

ISSCC 2002 DISCUSSION SESSIONS

8:00 PM	E1: Software Radio: Cool or to be Cooled? (Salon 1-6)	E2: When Will Optical Interconnects Appear on High-Performance Microprocessors? (Salon 7)	E3: Does Moore's Law Apply to Analog? (Salon 8)	E4: Have Universities Killed Research or Has Industry Corrupted It? (Salon 9)

Tuesday, February 5th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 7: Baseband Communications (Salon 1-6)	Session 8: High-Speed Timing (Salon 7)	Session 9: DRAM and Ferroelectric Memories (Salon 8)	Session 10: High-Speed ADCs (Salon 9)	Session 11: TD: RF/High-Speed Technologies (Salon 10-15)
1:30 PM	Session 12: TD: Digital Directions (Salon 1-6)	Session 13: Oversampling A/D Converters (Salon 7)	Session 14: Cellular RF Wireless (Salon 8)	Session 15: Gigabit Communications (Salon 9)	Session 16: High-Speed Circuit Techniques and I/O (Salon 10-15)
5:15 PM	Author Interviews (Golden Gate Hall)				

ISSCC 2002 DISCUSSION SESSIONS

8:00 PM	E5: Low-Voltage Design or the End of MOSFET Scaling? (Salon 1-6)	E6: SOI: Solution or Indigestion? (Salon 7)	E7: What Caused the Telecom Crash ? (Salon 8)	E8: Solid-State Circuits: System or Circuit Innovation? (Salon 9)

Wednesday, February 6th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 17: Advanced RF Techniques (Salon 1-6)	Session 18: Converter Techniques (Salon 7)	Session 19: DSL and Wireline Circuits (Salon 8)	Session 20: Microprocessors (Salon 9)	Session 21: TD: Sensors and Microsystems (Salon 10-15)
1:30 PM	Session 22: Multimedia Signal Processing (Salon 1-6)	Session 23: Analog Techniques (Salon 7)	Session 24: RF Systems (Salon 8)	Session 25: Processor Building Blocks (Salon 9)	Session 26: MEMS and Displays (Salon 10-15)
5:15 PM	Author Interviews (Ballroom Foyer South)				

Thursday, February 7th

ISSCC 2002 SHORT COURSE

8:00 AM	ISSCC 2002 Short Course: Wideband Communications (Sessions at 8:00 AM, 10:00 AM, and 1:30 PM) (Salons 1-6, Nob Hill, Golden Gate A)

ISSCC 2002 MICROPROCESSOR DESIGN WORKSHOP

8:00 AM	Microprocessor Design Workshop (Salon 7)

SESSION 15   SALON 9

GIGABIT COMMUNICATIONS

Chair: Yuriy Greshishev, Nortel Networks, Ottawa, Canada
Associate Chair: Roger Minear, Agere Systems, Reading, PA

15.1   OC-192 Transmitter in Standard 0.18µm CMOS   1:30 PM
M. Green, A. Momtaz, K. Vakilian, X. Wang, K. Jen, D. Chung, J. Cao,
M. Caresosa, A. Hairapetian, I. Fujimori, Y. Cai
Broadcom Corp., Irvine, CA

A fully-integrated SONET OC-192 transmitter IC using a standard CMOS process consists of an input data register, FIFO, CMU, and 16:1 multiplexer to give a 10Gb/s serial output. A higher FEC rate, 10.7Gb/s, is supported. This chip, using a 0.18µm process, exceeds SONET requirements, dissipating 450mW.

15.2   SONET OC-192 Receiver in Standard 0.18µm CMOS   2:00 PM
J. Cao, A. Momtaz, K. Vakilian, M. Green, D. Chung, K. Jen,
M. Caresosa, B. Tan, I. Fujimori, A. Hairapetian
Broadcom Corp., Irvine, CA

A fully-integrated OC-192 multi-rate (9.95Gb/s - 10.71Gb/s) receiver uses standard 0.18µm CMOS. The circuit consists of an input amplifier, CDR, 1:16 demux and 18 LVDS drivers. The chip exceeds SONET jitter tolerance spec by >100%. Recovered 10Gb/s clock jitter is <4mUI(rms). The input sensitivity is <50mV with 870mW at 1.8V.

15.3   A 9.9G-10.8Gb/s Rate-Adaptive Clock and Data-Recovery with
**   No External Reference Clock for WDM Optical-Fiber**
**   Transmission   2:30 PM**
H. Noguchi, T. Tateyama, M. Okamoto, H. Uchida, M. Kimura, K.
Takahashi
NEC Corp., Kawasaki, Japan

A 9.9-10.8Gb/s rate adaptive clock and data recovery circuit with 1:16 DMUX are integrated in 0.5µm SiGe BiCMOS. A dual   -input voltage-controlled oscillator incorporates a fast and a slow tracking loop with a DC gain enhancer. The chip exhibits 2mUIrms jitter generation and 0.45UIpp jitter tolerance in a 4-80MHz range. Power dissipation is 1.45W from a 3.3V supply.

BREAK   3:00 PM

15.4   A 10Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18µm
**   CMOS**
**   3:15 PM**
J. Rogers, J. Long
Univ. of Toronto, Toronto, Canada

A monolithic 10Gb/s clock/data recovery and 1:2 demultiplexer is implemented in 0.18µm CMOS. The quadrature LC delay line oscillator has 110MHz tuning range and 60MHz/V sensitivity to power-supply pulling. The circuit meets SONET OC-192 requirements with 1ps rms measured jitter. The $1.9 \times 1.5 mm^2$ IC consumes 285mW from a 1.8V supply.

15.5   A 5Gb/s 0.25µm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit

3:45 PM

S. Lee[1], M. Hwang[1], Y. Choi[1], S. Kim[1], Y. Moon[1], B. Lee[1], D. Jeong[1], W. Kim[1], Y. June Park[1], G. Ahn[2]
[1]Seoul National Univ., Seoul, Korea
[2]Silicon Image Inc., Sunnyvale, CA

A variable-interval oversampling clock/data recovery circuit (CDR) provides robust operation under varying jitter conditions. An eye-measuring loop in the CDR enables data recovery at maximum eye-opening, responding to the amount and shape of jitter. The CDR in 0.25µm CMOS shows <10^{-13} BER for 2^7-1 PRBS at 5GBaud.

15.6   A 622Mb/s Fully-Integrated Optical-Communication Receiver IC with a Wide-Dynamic-Range Input

4:15 PM

T. Takeshita, T. Nishimura
SONY, Kanagawa, Japan

An optical receiver IC for 622Mb/s that integrates transimpedance amplifier, post amplifier, and clock recovery uses a BiCMOS process. The one-chip receiver achieves dynamic range sensitivity from -29.4 to 0dBm. A PLL circuit without reference-clock tolerates input with duty-cycle distortion from 70 to 130%.

15.7   50Gb/s SiGe BiCMOS 4:1 Multiplexer and 1:4 Demultiplexer for Serial-Communication Systems

4:45 PM

M. Meghelli, A. Rylyakov, L. Shan
IBM, Yorktown Heights, NY

SiGe BiCMOS 4:1 multiplexer and 1:4 demultiplexer ICs targeting SONET OC-768 applications are packaged to enable bit-error-rate testing by connecting their serial interfaces. Operation is error-free for both circuits at data rates >50Gb/s and -3.6V supply.

CONCLUSION   5:15 PM

SESSION 16   SALON 10-15

HIGH-SPEED CIRCUIT TECHNIQUES AND I/O

Chair: Héctor Sánchez, Motorola, Inc., Austin, TX
Associate Chair: C. K. Ken Yang, Univ. of California, Los Angeles, CA

16.1 A 100Gb/s Transceiver with GND-VDD Common-Mode Receiver and Flexible Multi-Channel Aligner

1:30 PM

K. Tanaka, M. Fukaishi, M. Takeuchi, N. Yoshida, K. Minami, K. Yamaguchi, H. Uchida, Y. Morishita, T. Sakamoto, M. Soda, M. Kurisu, T. Saeki
NEC Corp., Kanagawa, Japan

A 5Gb/s 20 channel transceiver uses 0.13μm 1.5V CMOS t   echnology. The sampling amplifier recovers ±100mV 90ps data over 0-1.5V common-mode range. A flexible multi-channel aligner and full-digital CDR architecture are used.

16.2 An Integrated 9-channel Time Digitizer with 30ps Resolution

2:00 PM

A. Mäntyniemi, T. Rahkonen, J. Kostamovaara
Univ. of Oulu, Oulu, Finland

An integrated 9-channel time digitizer with 30ps rms resolution, 496μs range, and 50mW power consumption in 0.6μm CMOS uses a three-   stage delay line interpolation and delay-generation principle that divides the 66MHz clock period into 512 bins using only 45 delay elements.

16.3 Adaptive-Supply Serial Links with Sub-1V Operation and Per-Pin Clock Recovery

2:30 PM

J. Kim, M. A. Horowitz
Stanford Univ., Stanford, CA

Adaptive power-supply regulation is extended to serial links, by using 5:1 multiplexing and low-voltage transceivers for power saving, and by scaling link properties with bit rate, especially in per-pin clock recovery PLL/DLLs. The serial link operates at 0.45-3.5Gb/s for 0.9-2.5V supply and dissipates 9.2-197mW.

BREAK   3:00 PM

16.4   1.1V 1GHz Communications Router with On-Chip Body Bias in 150nm CMOS

3:15 PM

S. Narendra, M. Haycock, R. Mooney, V. Govindarajulu, V. Erraguntala, H. Wilson, S. Vangal, A. Pangal, E. Seligman, R. Nair, N. Borkar, J. Hofsheier, S. Menon, B. Bloechel, G. Dermer, S. Borkar, V. De
Intel Corp., Hillsboro, OR

A router chip, that incorporates on-chip forward body biasing capability with 2% area overhead, achieves 1GHz operation at 1.1V supply in a 150nm logic technology, compared to 1.25V required for the orginal design having no body bias. Switching power is 23% less and chip leakage is reduced by 3.5x in standby mode by withdrawing forward bias.

16.5   A 1V CMOS PLL in High-Leakage CMOS Operating from 10 to 700MHz

3:45 PM

R. Holzer
Analog Devices Inc, Herzlia, Israel

A PLL uses 0.13µm logic process where leakage currents are high. The loop capacitor is implemented by a structure of poly and 9 metal layers. The VCO is implemented with common-mode feedback to compensate for leakage currents. Maximum VCO frequency is 1400MHz. Typical power is 7mW at 200MHz. RMS jitter is 25.4ps at 360MHz.

16.6   Methodology and Experimental Verification for Substrate-Noise Reduction in CMOS Mixed-Signal ICs with Synchronous Digital Circuits

4:15 PM

M. Badaroglu[1,2], M. van Heijningen[1], V. Gravot[1], J. Compiet[1], S. Donnay[1], M. Engels[1], G. Gielen[2], H. De Man[1,2]
[1]IMEC, Leuven, Belgium
[2]K.U. Leuven, Leuven, Belgium

An efficient substrate-noise-reduction technique for synchronous CMOS circuits shows >2x noise reduction with penalties of 3% area and 4% power increase in a 5k-gate synchronous CMOS circuit fabricated in a 0.35µm CMOS process on an epi-type substrate.

CONCLUSION   4:45 PM

DISCUSSION SESSIONS

E5   Low-Voltage Design or the End of MOSFET Scaling?
(Salon 1-6)
Organizer: Akira Matsuzawa, Matsushita Electric Industrial Co., Ltd.,
        Osaka, Japan
Co-Organizer: Kunihiko Iizuka, Sharp, Nara, Japan
Moderator: Takayasu Sakurai, Univ. of Tokyo, Tokyo, Japan

CMOS feature size continues to shrink for digital circuits, and mass production in 0.1μm is in sight. Yet, the trend of decreasing supply voltage in deep sub-micron processes tends to make analog and memory circuit design harder. The panel focuses on two issues. (1) How low-voltage can CMOS circuit designs be? (2) Without scaling, is it possible to continue improving performance and reducing cost of CMOS LSI?

Panelists:

> **Asad Abidi**, Univ. of California, Los Angels, CA
> **Daniel Senderowicz**, SynchroDesign, Berkeley, CA
> **Akira Matsuzawa**, Matsushita Electric Industrial Co., Ltd.,
> Osaka, Japan
> **Alex Shubat**, Virage Logic Corp, Fremont, CA,
> **Junichi Miyamoto**, Toshiba Corp., Yokohama, Japan
> **Shekhar Y. Borkar**, Intel, Hillsboro, OR

E6   SOI: Solution or Indigestion?
(Salon 7)
Organizer/Moderator: Sreedhar Natarajan, Texas Instruments Inc.,
Dallas, TX

Introduction of SOI as an alternative to bulk has been limited to niche markets. The demand for low power/voltage and high performance suggests SOI is suitable for memory applications. SOI advantages, particularly reduced junction capacitance, isolation, SER etc., offer performance improvement. This is balanced against SOI disadvantages like parasitic leakages, power supply distribution and sense amplifier floating-body effects. Acceptance of SOI as a mainstream technology requires overcoming its disadvantages and achieving high-performance high-density RAMs.

Panelists:

> **Geordie Braceras**, IBM Microelectronics, Essex Junction, VT
> **Tadaaki Yamauchi**, Mitsubishi Electric Corp., Hyogo, Japan
> **Toshiro Hiramoto**, Univ. of Tokyo, Tokyo, Japan
> **Betty Prince**, Memory Strategies International, Austin, TX
> **Eric Dupont Nivet**, SOISIC, Grenoble, France
> **James Burns**, MIT Lincoln Labs, Lexington, MA

E7   **What Caused The Telecom Crash: Technology, Business or Demand?**

(Salon 8)

Organizer: Larry DeVito, Analog Devices, Wilmington, MA
Moderator: Rick Walker, Agilent Technologies, Palo Alto, CA

What limits growth of the global communication network: electronics, optics, demand, or business model? Is there no limit? Some claim the backbone has excess capacity, while others build faster OC-768 DWDM optical switching networks. Slow deployment of ADSL and cable modems limits bandwidth demand, yet some blame unsophisticated business models for unrealistic demand forecasts. For example, household computers are now installed at a slowing rate, reducing growth of telecom demand. Yet the business forecasts were building for an exponentially increasing market.

Panelists:

> **Scott Blackstone**, Analog Devices, Cambridge, MA
> **Don Clarke**, BTexact Technologies, Martlesham, Ipswich, UK
> **Jay Liebowitz**, RHK Consulting, Waltham MA
> **Yuriy M.Greshishchev**, Nortel Networks, Ottawa, ON, Canada
> **John W. Jarve**, Menlo Ventures, Menlo Park, CA
> **Andrew M. Odlyzko**, Univ. of Minnesota, South Minneapolis, MN
> **Toshitaka Tsuda**, Fujitsu Labs Ltd., Nakahara, Kawasaki, Japan

E8   **Solid-State Circuits: System or Circuit Innovation?**

(Salon 9)

Organizer: Bill Bidermann, Pixim Inc., Mountain View CA
Moderator: Ralph Etienne-Cummings, Johns Hopkins Univ., Baltimore MD

With standard-cell ASIC design and readily-available IP blocks, many who call themselves "VLSI designers" have less and less to do with transistor-level circuit design. One might hold that all the circuits themselves are dredged-up versions of past innovations. Those struggling with the requirements of scaling, high performance, and low power seem unable to satisfy the demand for circuit innovation. Black-box system design or transistor-level design - which is the order of the day?

Panelists:

> **Barrie Gilbert**, Analog Devices, Beaverton, OR
> **Thomas H. Lee**, Stanford Univ., Stanford CA
> **Andreas Andreou**, Johns Hopkins Univ., Baltimore MD
> **Wlodek Kurjanowi**, ATMOS Corp., Kanata, Ontario, Canada
> **Bruce Gieseke**, AMD, Sunnyvale, CA

ADVANCED RF TECHNIQUES

Chair: Paul C. Davis, Consultant, Reading, PA
Associate Chair: Ken R. Cioffi, Tropian, Cupertino, CA

17.1   A Low-Noise Transformer-Based 1.7GHz VCO   8:30 AM
M. Straayer[1], J. Cabanillas[2], G. Rebeiz[1]
[1]Univ. of Michigan, Ann Arbor, MI
[2]Univ. of Barcelona, Barcelona, Spain

A low-noise transformer-based CMOS 0.35µm VCO operates at 1.7GHz. The VCO core consumes 4.5mA from 2.5V, and results in phase noise of -116, -137 and -142dBc/Hz at 100k, 600k and 1MHz from the carrier, respectively. The tuning range is 107MHz for 0-2.5V tuning voltage. The oscillator is based on a transformer-type resonator.

17.2   A CMOS Differential Noise-Shifting Colpitts VCO   8:45 AM
R. Aparicio, A. Hajimiri
Caltech, Pasadena, CA

A 0.35µm VCO uses current switching to increase voltage swing, lower phase noise by cyclostationary noise alignment, and improve start-up reliability. A CMOS VCO in a 3-metal, 0.35µm process has -139dBc/Hz phase noise at 3MHz offset from a 1.8GHz carrier and 30% of continuous tuning using inductors with Q of 6 and 4mA dc current.

17.3   A Low-Phase-Noise Low-Phase-Error 1.8GHz Quadrature
**   CMOS VCO   9:00 AM**
P. Andreani
Lund Univ., Lund, Sweden

A 1.8GHz quadrature VCO in standard 0.35µm CMOS with three metal layers shows -140dBc/Hz phase noise or less across an 18% tuning range, while drawing 25mA from a 2V power supply. The quadrature phase error between the VCO outputs is at most 0.25°.

17.4   Adaptive Biasing of a 5.8GHz CMOS Oscillator   9:15 AM
D. Hitko, C. Sodini
MIT, Cambridge, MA

A key concept for VCOs in next-generation RF links is to allow phase noise performance to be scaled back to save power in times of reduced demand. A 5.8GHz VCO and biasing circuitry in 0.5µm CMOS have performance adjustable from -107dBc/Hz (1MHz offset) with 6.2mW dissipated to -121dBc/Hz using 70mW.

17.5   A 2.4GHz 0.18µm CMOS Self-Biased Cascode Power
**   Amplifier with 23dBm Output Power   9:30 AM**
T. Sowlati[1], D. Leenaerts[2]
[1]Philips Research USA, Briarcliff Manor, NY
[2]Philips Research, Eindhoven, The Netherlands

A two-stage self-biased cascode power amplifier in 0.18µm CMOS process for Class 1 Bluetooth application provides 23dBm output power with 31dB gain and 42% PAE at 2.4GHz. The power amplifier die occupies 0.46mm^2.

BREAK   10:00 AM

17.6   A Wideband Linear Amplitude Modulator for Polar Transmitters Based on the Concept of Interleaving-Delta Modulation

10:15 AM

P. Nagle[1], P. Burton[1], E. Heaney[2], F. McGrath[3]
[1]Univ. of Limerick, Limerick, Ireland
[2]M/A-COM, Blackrock, Ireland
[3]M/A-COM, Lowell, MA

A wideband amplitude modulator for use with an RF polar transmitter is based on interleaving delta modulation to improve linearity and reduce switching loss, filter size, and EMI. A 0.35µm CMOS 0.35mm^2 chip verifies the iDM concept.

17.7   Wireless 1.25Gb/s Transceiver Module at 60GHz-Band
10:45 AM

K. Ohata[1], K. Maruhashi[1], M. Ito[1], S. Kishimoto[1], K. Ikuina[1], T. Hashiguchi[1], N. Takahashi[2], S. Iwanaga[1]
[1]NEC Corp., Otsu, Japan
[2]NEC Engineering Ltd., Kawasaki, Japan

A 1.25Gb/s 60GHz-band compact transceiver module uses ASK modulation. CPW MMICs and planar filters are flip-chip mounted in TX and RX LTCC MCMs. The transmitter exhibits 9.6dBm output power. The receiver shows -50dBm minimum received power for 1.25Gb/s error-free transmission. The transceiver module is 82x53x7mm^3 (30cc).

17.8   A 1V 1mW 51GHz Fully-Integrated VCO in Standard CMOS
11:15 AM

M. Tiebout, H. Wohlmuth, W. Simbuerger
Infineon Technologies, Munich, Germany

A fully-integrated 51GHz VCO is implemented in 0.12µm standard CMOS with 6 metal levels. Core power consumption is 1mW at 1V supply due to the optimized high-inductance tank. The tuning range is 1.4GHz. Measured phase noise is -85dBc/Hz at 1MHz offset.

17.9   25GHz Static Frequency Divider and 25Gb/s Multiplexer in 0.12µm CMOS

11:30 AM

H. Knapp, H. Wohlmuth, M. Wurzer, M. Rest
Infineon Technologies, Munich, Germany

A static 2:1 frequency divider operating up to 25.4GHz at 41mA and a 25Gb/s 2:1 multiplexer at 29mA implemented in current-mode logic have differential 50Ω inputs and outputs. They are fabricated in a 0.12µm CMOS process and operate from a 1.5V supply.

CONCLUSION   11:45 AM

CONVERTER TECHNIQUES

Chair: Scott Willingham, Silicon Labs, Austin, TX
Associate Chair: David Johns, Univ. of Toronto, Toronto, Ontario, Canada

18.1   A 1.5V 2.4/2.9mW 79/50dB DR ΣΔ Modulator for GSM/WCDMA in a 0.13µm Digital Process

8:30 AM

G. Gomez, B. Haroun
Texas Instruments, Inc., Dallas, TX

A 2nd order multi-level ΣΔ A/D converter for low-power multi-standard wireless receivers, in a single-poly 0.13µm digital CMOS process, has 79/50dB dynamic range for GSM/WCDMA. The $0.2mm^2$ chip consumes 2.4/2.9mW at 1.5V.

18.2   An Embedded 0.8V/480µW 6b/22MHz Flash ADC in 0.13µm Digital-CMOS Process using Nonlinear Double-Interpolation Technique

9:00 AM

J. (H.-C.) Lin[1], B. Haroun[2]
[1]Texas Instruments, Inc., Dallas, TX
[2]Texas Instruments, Inc., Plano, TX

For high-data-rate wireless communication, a 0.8V 480µW 6b 22MSample/s flash-interpolation ADC is fabricated in 0.13µm digital CMOS. The circuit achieves 33dB SNDR and 47dB SFDR using a nonlinear double interpolation technique.

18.3   A 0.7V MOSFET-Only Switched-Opamp ΣΔ Modulator

9:30 AM

J. Sauerbrey[1], T. Tille[2], D. Schmitt-Landsiedel[2], R. Thewes[1]
[1]Infineon Technologies AG, Munich, Germany
[2]Technical Univ. of Munich, Munich, Germany

A 0.7V MOSFET-only switched-opamp ΣΔ modulator for speech applications achieves 67dB SNDR, and 75dB dynamic range. The circuit, occupying $0.08mm^2$ in 0.18µm CM OS, does not use voltage boosting or low-V_T devices. All capacitors are compensated MOS devices.

BREAK   10:00 AM

18.4   A 30mW 12b 21MSample/s Pipelined CMOS ADC

10:15 AM

S. Kulhalli, V. Penkota, R. Asv
Texas Instruments, Bangalore, Karnataka, India

A 0.6µm double -poly CMOS 12b ADC uses a number of different techniques to obtain low power. The ADC achieves 68dB SNR at 21MSample/s, consuming 30mW at 2.7V. Die area is 2.56mm^2.

18.5   A Self-calibrated Pipeline ADC with 200MHz IF-Sampling Frontend

10:45 AM

M. Waltari, L. Sumanen, T. Korhonen, K. Halonen
Helsinki Univ. of Technology, Espoo, Finland

A 13b 50MSample/s pipeline ADC with digital self-calibration and IF-sampling frontend, using a 0.35µm BiCMOS process, achieves 76.5dB SFDR at 194MHz input. The chip occupies 6mm^2 and dissipates 715mW from a 2.9V supply.

18.6   A 33mW 14b 2.5MSample/s ΣΔ Converter in 0.25µm Digital CMOS

11:15 AM

R. Reutemann, P. Balmelli, Q. Huang
ETH Zurich, Zurich, Switzerland

The IC consists of a 5th-order single-loop tri-level ΣΔ modulator and a multistage digital filter. Measured dynamic range is 86dB over 1MHz bandwidth. With 79dB peak SNDR, the chip consumes 33mW and occupies 1.5mm^2.

CONCLUSION   11:45 AM

SESSION 19   SALON 8

DSL AND WIRELINE CIRCUITS

Chair: Franz Dielacher, Infineon Technologies, Villach, Austria
Associate Chair: Cormac Conroy, Berkana Wireless, San Jose, CA

19.1   A 744mW ADSL CO Supply-on-Demand (SOD) Driver

8:30 AM

J. W. Pierdomenico, S. Wurcer, B. Day
Analog Devices, Wilmington, MA

A ±6V ADSL CO driver delivers 20.4dBm power into a 100Ω load with 5.3 crest factor using internally pumped power supplies. In a 1:1.1 transformer reference design, 1E-08 BER is measured while driving 8.16Mb/s down a 6.5kft line. Data rates up to 8Mb/s are measured. The device uses a 26V SOI bipolar process with 744mW of total supply.

19.2   A 710mW ADSL CO Driver with 75dB MTPR

9:00 AM

F. Sabouri, R. Shariatdoust
Analog Devices, Somerset, NJ

A bipolar ADSL line driver for central office achieves 75dB MTPR. Employing a single-active-termination topology, it has 710mW total dissipation including 20.4dBm delivered to the line. Class-AB biasing makes the 4mA quiescent current independent of process, temperature, and supply variations.

19.3   A 0.5μm CMOS ADSL Line Driver with Digital Adaptive Bias

9:30 AM

M. Ingels[1], S. Bojja[2], P. Wouters[2]
[1]Alcatel Microelectronics, Zaventem, Belgium
[2]Alcatel Microelectronics, Raleigh, NC

A 5V 0.5μm CMOS line driver has distortion <   -65dB in the ADSL upstream band for a 4V peak to peak differential output swing on a 12.5Ω load. The quiescent current is controlled digitally with a dedicated algorithm that corrects for offsets and process variations. The driver is integrated in a complete ADSL CPE analog front-end.

BREAK   9:45 AM

19.4 A 1.8V 450mW VDSL-4Band Analog Front-End IC in 0.18μm CMOS

10:15 AM

H. Weinberger, A. Wiesbauer, M. Clara, C. Fleischhacker, T. Pötscher, B. Seger
Infineon Technologies, Villach, Austria

A highly-integrated AFE chip for VDSL-4band in 0.18μm CMOS draws 450mW from a single 1.8V supply. The 12MHz bandwidth transceiver employs an 11b ADC, a 12b DAC, automatically tuned anti-aliasing and reconstruction filters, and programmable gain amplifiers. Beside the basic transceiver circuitry, it also provides clock generation and a wake-up circuitry on a 7.5mm^2 die.

19.5 Analog Front End for DMT-Based VDSL

10:45 AM

W. A. P. De Wilde[1], N. Scantamburlo[2], M. Combe[3], J. Van Leeuwe[1], K. Doorackers[1], Y. Mazoyer[3], C. Renous[3], R. Petigny[3], A. Bonin[3], B. Bayracki[2], B. Belhi[3], E. Moons[1], J. Sevenhans[1]
[1]Alcatel, Antwerpen, Belgium
[2]Alcatel, Padova, Italy
[3]STMicroelectronics, Grenoble, France

A 12MHz 760mW analog front end for DMT-based VDSL integrates all active components except line driver in a single BiCMOS 0.35μm ASIC. When fully active, the ASIC dissipates 480mW at 3.3V supply, providing resolution equivalent to 12b without trimming.

19.6 A Low-Power Integrated Tuner for Cable-Telephony Applications

11:15 AM

C. Ling, R. Montemayor, A. Cicalini, K. Wang, L. Jansson, L. Mucke, P. Trihka, S. V. Kishore
Silicon Wave, San Diego, CA

A fully-integrated dual-conversion tuner for cable telephony in a 27GHz 0.35μm SOI BiCMOS process receives signals from 200 to 880MHz and produces a 44MHz IF. The 13mm^2 IC has 7.3dB NF, <-78dBc/Hz total phase noise at 10kHz offset, spurs below 42dBc for 137 5dBmV channels, 60dB gain, and 68dB gain range, drawing 168mA from 3V.

CONCLUSION   11:45 AM

MICROPROCESSORS

Chair: Glenn Giacalone, C-Port Corp., North Andover, MA
Associate Chair: Simon Segars, Arm, Ltd., Cambridge, England

20.1   An 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading

8:30 AM

R. Preston, R. Badeau, D. Bailey, S. Bell, L. Biro, W. Bowhill, D. Dever,
S. Felix, R. Gammack, V. Germini, M. Gowan, P. Gronowski, D. Jackson,
S. Mehta, S. Morton, J. Pickholtz, M. Reilly, M. Smith
Compaq Computer Corp., Shrewsbury, MA

A 250M transistor microprocessor implements the Alpha instruction set and features 8-wide superscalar issue and simultaneous multithreading in a 0.125µm SOI process. Performance is estimated at over three times that of the previous design.

20.2   A Single-Chip Programmable Platform Based on a Multithreaded Processor and Configurable Logic Clusters

9:00 AM

Y-D. Bae, S-I. Park, Y. Yi, I-C. Park
KAIST, Taejon, Korea

A configurable platform chip integrates most hardware blocks required in embedded system chip design, such as a 32b multithreaded RISC processor, configurable logic clusters, FIFO memories and control circuitry. The multithreaded processor has fast task switching and configurable logic are grouped into clusters for IP-based design.

20.3   Implementation of a Third-Generation 1.1GHz 64b Microprocessor

9:30 AM

G. Konstadinidis, K. Normoyle, S. Wong, S. Bhutani, H. Stuimer,
T. Johnson, A. Smith, D. Y. Cheung, F. Romano, S. Yu, S. Oh,
V. Melamed, S. Narayanan, D. Bunsey, C. Khieu, K. J. Wu, R. Schmitt,
A. Dumlao, M. Sutera, J. Chau
Sun Microsystems, Palo Alto, CA

A third-generation 1.1GHz 64b microprocessor provides 1MB on-chip L2$, 4GB/s off chip memory bandwidth and a 200MHz JBUS interface that supports 1 to 4 processors. The 90M transistor chip is implemented in a 7-level metal copper 0.13µm CMOS process, and dissipates 53W at 1.3V and 1.1GHz

BREAK   10:00 AM

20.4   A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor

10:15 AM

K. J Nowka[1], G. Carpenter[1], E. Mac Donald[2], H. Ngo[1], B. Brock[1], K. Ishii[3], T. Nguyen[1], J. Burns[1]
[1]IBM Austin Research Lab., Austin, TX
[2]IBM Microelectronics Division, Austin, TX
[3]IBM Microelectronics Division, Yasu, Japan

A 32b PowerPC™ system-on-a-chip supporting dynamic voltage supply and dynamic frequency scaling operates from 366MHz at 1.8V and 600mW down to 150MHz at 1.0V and 53mW in a 0.18μm CMOS process. Maximum supply change without PLL relock is 10mV/ms. Processor state save/restore enables a deep-sleep state.

20.5   A 400MHz 32b Embedded Microprocessor Core with 4.0GB/s Cross-Bar Bus Switch for SoC

10:45 AM

M. Nakajima, T. Yamamoto, S. Ozaki, T. Sezaki, T. Kanakogi, T. Furuzono, T. Sakamoto, T. Aruga, M. Sumita, M. Tsutsumi, A. Ueda, T. Ichinomiya
Matsushita Electric Industrial Co., Nagaoka, Japan

A 32b RISC microprocessor core for Digital TV SoC occupies 14.8mm² in 0.13μm CMOS with six Cu layers. The core runs at 400MHz with average dissipation of 500mW at 1.35V. The integrated 4.0GB/s 3 x 4 cross-bar bus switch improves sustained system performance efficiency by 1.75 times.

20.6   The Implementation of the Next-Generation 646 Itanium™ Microprocessor

11:15 AM

S. D Naffziger[1], G. Hammond[2]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

The processor incorporates over 220M transistors on a 465mm² die and operates at >1.2GHz with an 8-stage pipeline in a 0.18μm process. It has three levels of on-chip cache totaling over 3.3MB providing >32GB/s bandwidth at each level.

CONCLUSION   11:45 AM

SESSION 21   SALON 10-15

TD: SENSORS AND MICROSYSTEMS

Chair: Werner Weber, Infineon Technologies, Munich, Germany
Associate Chair: Wai L. Lee, Cirrus Logic, Inc., Austin, TX

21.1   0.25µm CMOS and BiCMOS Single-Chip Direct-Conversion Doppler Radar for Remote Sensing of Vital Signs   8:30 AM

A. Droitcour[1], O. Boric-Lubecke[2], V. M Lubecke[2], J. Lin[2]
[1]Stanford Univ., Stanford, CA
[2]Lucent Technologies, Murray Hill, NJ

A fully-integrated direct conversion Doppler radar detects heart and respiration movement at a distance of 50cm. The 1.6GHz transceiver is in both CMOS and BiCMOS, with each chip occupying 14mm^2 using a 0.25µm silicon processes. The effects o   n system sensitivity of phase noise at small offset frequencies with range correlation are assessed.

21.2   Sensor Arrays for Fully-Electronic DNA Detection on CMOS   9:00 AM

R. Thewes[1], F. Hofmann[1], A. Frey[1], B. Holzapfl[1], M. Schienle[1],
C. Paulus[1], P. Schindler[1], J. Zapf[2], C. Kassel[2], M. Stanzel[2], A. Hengerer[2],
R. Hintsche[3], E. Nebling[3], J. Albers[3], J. Hassman[4], J. Schülein[4],
W. Goemann[5], W. Gumbrecht[2]
[1]Infineon Technologies AG, Munich, Germany
[2]Siemens AG, Munich / Erlangen, Germany
[3]Fraunhofer Gesellschaft, Itzehoe, Germany
[4]November AG, Erlangen, Germany
[5]Eppendorf Instrumente GmbH, Hamburg, Germany

A 16x8 DNA sensor array chip with fully-electronic readout is based on an extended CMOS process. Requirements concerning the integration of bio-compatible interface-, sensor- and transducer-materials into standard-CMOS-environment and circuitry design issues are discussed.

21.3   A 500dpi Capacitive CMOS Fingerprint Sensor with Pixel-Level Adaptive Image Enhancement   9:30 AM

K. Lee, E. Yoon
Korea Advanced Institute of Science and Technology, Taejon, Korea

A 500dpi capacitive CMOS fingerprint sensor with pixel-level adaptation image enhancement uses virtually-grounded metal shields to suppress parasitic capacitances and capacitive switching networks to generate local threshold level. A 210×100 sensor in 0.6µm CMOS consumes 40mW at 5V supply.

21.4   A 500dpi 224x256Pixel Single-Chip Fingerprint-Identification LSI with Pixel-Parallel Image Enhancement and Rotation Schemes   9:45 AM

S. Shigematsu, K. Fujii, H. Morimura, T. Hatano, M. Nakanishi, T. Adachi, N. Ikeda, T. Shimamura, K. Machida, Y. Okazaki, H. Kyuragi
NTT, Atsugi, Kanagawa, Japan

A 500-dpi 224x256-pixel single-chip fingerprint identification LSI adapts the sensing circuit to a finger and performs pixel-parallel image processing and rotation in a pixel array. A test chip achieves 2ms 10mW sensing, 41ms 19.2mW identification, and practical identification accuracy at 2.5V, 5MHz.

BREAK   10:00 AM

21.5   Micromachined e-Jet for IC-Chip Cooling   10:15 AM
T. Chou, K. Najafi, M. Muller, L. Bernal, P. Washabaugh, B. Amir Parviz
Univ. of Michigan, Ann Arbor, MI

A micromachined acoustic ejector (MACE) chip contains electrostatically-driven Helmholtz resonators, which generate small air jets. A 1.6x1.6cm^2 prototype contains 25 e-jets with 1m/s measured velocity. Results show that a 15-jet device located ~1cm above a 100°C surface dissipates >6W/m^{2}K. Future generations are being designed with higher jet velocity.

21.6   Microelectromechanical Scanning Devices for Optical-
         Networking Applications   10:45 AM
M. Wu[1], D. Hah[1], P. Patterson[1], H. Toshiyoshi[2]
[1]UCLA, Los Angeles, CA
[2]Univ. of Tokyo, Tokyo, Japan

The state-of-the-art of optical MEMS devices for optical networking applications is reviewed, and a scanning micromirror with angular vertical comb (AVC) actuators is introduced. The AVC scanner uses a single etching process and is completely self-aligned. It has 50% larger scan angle than conventional vertical comb devices. Resonant frequency is 630Hz.

21.7   3-D Integrable Optoelectronic Devices for
         Telecommunications ICs   11:15 AM
P. Dainesi[1], A. Ionescu[1], L. Thevenaz[1], P. Robert[1], K. Banerjee[2],
P. Fluckiger[1], C. Hibert[1], G. Racine[1], P. Renaud[1], M. Declercq[1]
[1]EPFL, Lausanne, Switzerland
[2]Stanford Univ., Stanford, CA

3-D integrable SOI optoelectronic devices include telecommunication optical switches with 5MHz bandwidth and unbalanced Mach Zehnder interferometers for filtering. Thermal compensation provides efficient modulation over 100kHz-1MHz and addresses 3-D IC thermal issues.

21.8   A DC-to-250MHz Low-Noise Current Pre-Amplifier with
         Integrated Photo-Diodes in 0.6μm CBiMOS, for Optical-
         Storage Systems
                                                    11:30 AM
G. de Jong, J. R. Bergervoet, J. H. Brekelmans, J. F. van Mil
Philips, Eindhoven, The Netherlands

An opto-electronic IC contains pre-amplifiers and integrated photo-diodes for optical-storage systems (CD, DVD, and DVR). The pre-amps exhibit low-noise (4.6 nV/$\sqrt{}$Hz) and the diodes have 0.25pF junction -capacitance. The IC uses a standard 0.6μm CBiMOS process for a high-performance low-cost solution.

CONCLUSION   11:45 AM

MULTIMEDIA SIGNAL PROCESSING

Chair: Stephen Fischer, Intel Corp., Sacramento, CA
Associate Chair: Takao Yamazaki, Sony Corp., San Jose, CA

22.1   A 27MHz 11.1mW MPEG-4 Video-Decoder LSI for Mobile Application

1:30 PM

M. Ohashi[1], T. Hashimoto[1], S. Kuromaru[1], M. Matsuo[1], T. Mori-iwa[1],
K. Ishida[1], T. Nakamura[1], M. Hamada[1], Y. Sugisawa[1], M. Arita[1],
T. Kimura[1], H. Miyajima[1], H. Tomita[1], M. Hoshino[1], H. Fujimoto[1],
K. Watada[1], T. Fukunaga[1], J. Michiyama[1], T. Nishi[1], H. Ito[2], Y. Kohashi[1],
T. Kondo[1], A. Inoue[1]
[1]Matsushita Electric Industrial Co., Ltd., Iizuka, Japan
[2]Matsushita Communication Industrial Co., Ltd., Yokosuka, Japan

A single-chip MPEG-4 video decoder LSI with integrated 896kb embedded SRAM frame buffer and embedded video display engine consumes 11.1mW at 27MHz operation. The chip achieves QCIF 15Hz H.263 and Simple@L1 decoding capability on 37.26mm^2 die using 0.18μm 1.5V quad-metal CMOS technology.

22.2   A 131mW MPEG-4 Video LSI with 9mW Error-Resilient Codec Core Based on a Fast Motion Estimation Algorithm

2:00 PM

H. Nakayama, T. Yoshitake, H. Komazaki, Y. Watanabe, H. Araki,
K. Morioka, J. Li, L. Peilin, S. Lee, H. Kubosawa, Y. Otobe
Fujitsu Labs Ltd., Kawasaki, Kanagawa Japan

An MPEG4 video codec core based on a scene-adaptive motion estimation algorithm, is integrated into 5.296x5.296mm^2 die using 0.18μm quad-metal technology. The power dissipation during codec operation of the device is 131mW for QCIF format at 15 frames/s at 13.5MHz using a 1.5V supply.

22.3   A 133MHz 170mW 10μA Standby-Application Processor for 3G Cellular Phones

2:30 PM

T. Yamada, N. Irie, J. Nishimoto, Y. Kondoh, T. Nakazawa, K. Yamada,
K. Tatezawa, T. Irita, S. Tamaki, H. Yagi, M. Furuyama, K. Ogura,
H. Watanabe, R. Satomura, K. Hirose, F. Arakawa, T. Hattori, I. Kudo,
I. Kawasaki, K. Uchiyama
Hitachi Ltd., Kokubunji-shi, Japan

An application processor for 3G cellular phones, using 0.18μm CMOS technology, includes a single CPU and DSP core with an on-chip 128kB SRAM. It enables software-based 15frames/s MPEG-4 encoding of QCIF Simple @L1 at 70MHz and 140mW. Standby current of the processor is <10μA in a partially-powered standby mode using separate power lines.

BREAK   3:00 PM

22.4 A 0.8W HDTV Video Processor with Simultaneous Decoding of Two MPEG2-MP@HL Streams and Capable of 30 frames/s Reverse Playback

3:15 PM

H. Yamauchi, S. Okada, K. Taketa, T. Mori, S. Okada, T. Watanabe, Y. Harada, Y. Matsushita
Sanyo Electric Co., Ltd., Anpachi-Gun, Japan

A HDTV video processor with decoding/display of two MPEG MP@HL streams and reverse playback with smooth 30frames/s without frame skip uses a 0.18µm 5 -layer process in 6.86x6.86mm^2 and 5.7M transistors. It is for home multimedia and mobile TV applications. It operates at 135MHz and 0.8W at 1.8V.

22.5 An 8-way VLIW Embedded Multimedia Processor built in a 7-layer Metal 0.11µm CMOS Technology

3:45 PM

H. Okano, A. Suga, T. Shiota, Y. Takebe, Y. Nakamura, N. Higaki, H. Kimura, H. Miyake, T. Satoh, K. Kawasaki, R. Sasagawa, W. Shibamoto, M. Sasaki, N. Ando, T. Yamana, Y. Asada, T. Satoh, T. Sukemura, S. Ando, H. Takahashi, I. Fukushi, S. Tago, F. Hayakawa, T. Kamigata, S. Imai, A. Satoh
Fujitsu Ltd., Kawasaki, Kanagawa Japan

A 533MHz 2.5W 2132MIPS 12.8GOPS 2.1GFLOPS 8-way VLIW embedded multimedia processor occupies a 7.8x7.8mm^2 die in a 7-layer metal 0.11µm CMOS at 1.2V. VLIW, SIMD, dynamic branch prediction, non-aligned dual load/store mechanism and a crosstalk-aware design flow contribute to performance.

22.6 A Single-Chip Text-To-Speech Synthesis Device Utilizing Analog Non-Volatile Multi-Level Flash Storage.

4:15 PM

G. Jackson[1], S. Awsare[1], M. Chang[1], W. Chen[1], R. Doan[1], L. Gaddy[1], P. Holzmann[1], D. Kahn[2], R. Lin[1], M. Macchi[2], A. Raina[1], H. Saar[1], J. Wu[1], B. Yang[1]
[1]Winbond Electronics Corp. America, San Jose, CA
[2]Espeech Corp., Gillette, NJ

A single-chip solution for text-to-speech synthesis uses analog non-volatile multi-level storage of a corpus of natural speech elements. An embedded micro-controller performs the algorithmic tasks of text-to-speech synthesis. The 80mm^2 chip fabricated in 0.5µm Flash CMOS operates at 24MHz and 3.0V at 90mW.

CONCLUSION 4:45 PM

ANALOG TECHNIQUES

Chair: Ken Poulton, Agilent, Palo Alto, CA
Associate Chair: Venu Gopinathan, Broadcom, Irvine, CA

23.1   A 2.5V 57MHz 15-Tap SC Bandpass Interpolating Filter with 320MHz Output Sampling Rate in 0.35µm CMOS

1:30 PM

S-P. U[1], R. Martins[1], J. Franca[2]
[1]Univ. of Macau, Macau, China
[2]Chipidea Microelectronics, S.A., Lisbon, Portugal

A 57MHz SC bandpass interpolating filter with 320MSample/s output is realized in 0.35µm CMOS for DDFS system. 15   -tap FIR response is achieved with sampling rate increase and frequency upconversion by translating 22MHz 80MSample/s input to 56MHz 320MSample/s output. Dynamic range is 69dB (1%THD) and 61dB (1%IM3). The filter dissipates 120mW analog and 16mW digital at 2.5V supply.

23.2   1W 0.8µm BiCMOS Adaptive-Q Current-Controlled Class-AB Power Amplifier for Portable Sound Equipment

2:00 PM

J. Hwang, H. Lee
Fairchild Semiconductor, Puchon, Korea

An AQC class-AB amplifier with low THD and quiescent power consumption uses 0.8µm 10V BiCMOS process, occupying 1.8x1.6mm ^{2}. It has <0.3% THD+N over audio frequency rang e driving 1W into 8Ω. It consumes 2.6mA at quiescent condition and has 65.1% power efficiency.

23.3   Analog-Processing Circuits for a 1.1V 270µA Mixed-Signal Hearing-Aid Chip

2:30 PM

J. Fattaruso[1], J. Hochschild[1], W. Sjursen[2], L. Fang[1], D. Gata[1], C. Branch[1], J. Holmes[1], Z. Jiang[1], S. Chen[1], K. Ling[1], E. Petilli[3], M. Skorcz[1], R. Dickerson[1], W. Severin[1]
[1]Texas Instruments, Dallas, TX
[2]Songbird Hearing, NJ
[3]Intrinsix, NJ

A compressing preamplifier, ADC, DAC, output driver and clock oscillator are implemented in a mixed-signal BiCMOS hearing-aid chip with digital filtering. 2.8µV input noise floor over the audio band and   0.02% THD are achieved with 270µA total battery current.

BREAK   3:00 PM

23.4   A 3µV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing

3:15 PM

A. Tang
Analog Devices, Inc., San Jose, CA

A 3µV offset op -amp uses both autozeroing and chopping to give 20nV/√Hz input noise at DC with low energy at the chopping frequency. The design includes additional circuitry for reduced switching transients. The power consumption is 4mW from a 5V supply. Die area is 0.6x1.12mm^2 using a 0.6µm DPDM CMOS process.

23.5   A 10µV-Offset 8kHz-Bandwidth 4th-Order Chopped ΣΔ A/D Converter for Battery Management

3:45 PM

P. G. Blanken, S. Menten
Philips, Eindhoven, The Netherlands

A chopped 4th-order continuous-time 1b ΣΔ A/D Con verter with 10µV offset and 8kHz bandwidth is for battery current measurement. Chopping at 16kHz, the circuit has a 0.1V input range, a 68dB SNR, and a 1MHz output bit rate. Area is 0.45x0.4mm^2 in 0.35µm CMOS. Current consumption is 30µA at 2.5-4V.

23.6   A Pseudo-CCM/DCM SIMO Switching Converter with Freewheel Switching

4:15 PM

D. Ma, W. Ki, C. Tsui
The Hong Kong Univ. of Science & Technology, Hong Kong, China

A single-inductor multiple-output switching converter operates in pseudo-CCM/DCM. It requires freewheeling of the inductor current during the instants when the n switch and all output p switches are off. It is fabricated in a 0.5µm CMOS n -well process with Voa = 2.5V and Vob = 3.0V. With 1µH inductor, converter efficiency is 84.7% at 1MHz.

23.7   A Method for Reducing the Effects of Random Mismatch in CMOS Bandgap References

4:45 PM

V. Ceekala, L. Douglas Lewicki, J. Weiser, D. Varadarajan, J. Mohan
National Semiconductor Corp., Santa Clara, CA

A method for reducing the effects of random mismatches in CMOS bandgap references reduces effects of CMOS current-mirror offsets and input-referred offsets of CMOS opamps. The circuit is fabricated in a 0.18µm CMOS process. Measured 3 sigma output voltage distribution is ~1%.

CONCLUSION   5:15 PM

RF SYSTEMS

Chair: Thomas H. Lee, Stanford Univ., Stanford, CA
Associate Chair: Ernesto Perea, STMicroelectronics, Grenoble, France

24.1   A Fully-Integrated GPS Receiver Front-End with 40mW Power Consumption

1:30 PM

M. Steyaert, P. Coppejans, W. De Cock, P. Leroux, P. Vancorenland
KU Leuven, Leuven, Belgium

A 0.25µm CMOS quadrature complex bandpass low -IF GPS receiver includes an LNA, PLL, mixer and a continuous-time $\Delta\Sigma$ ADC. The chip has -130dBm input sensitivity, 62dB DR, and -32dB IMRR, while consuming 40mW from 2V supply. The chip is 9mm^2.

24.2   A 27mW GPS Receiver in 0.35µm CMOS

2:00 PM

F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour,
A. Kheirkhahi, M. Nariman, S. Bhatia, M. Conta
Valence Semiconductor, Invine, CA

A pure-CMOS 1.575GHz radio integrates a receiver and a synthesizer for GPS application. The receiver path uses a quadrature single-downconversion architecture with an on-chip image reject LPF. It has 4dB NF and -17dBm IIP3 and operates over a range of 2.2V to 3.6V supply and -40 to 85°C. It consumes 27mW from 2.2V supply.

24.3   A CMOS Broadband-Tuner IC

2:30 PM

L. Connell, N. Hollenbeck, M. Bushman, D. McCarthy, S. Bergstedt,
R. Cieslak, J. Caldwell
Motorola, Schaumburg, IL

A single-chip dual-conversion tuner in 0.35µm CMOS incorporates both a 50-860MHz LNA and a digital CMOS synthesizer with a -173dBc/Hz phase-noise floor. The synthesizer generates 100mA switching currents at a 12.5MHz rate and all associated in-band spurs are suppressed <0.5µVrms input referred. Th e 5mm^2 die consumes 1.5W from a 5V supply.

BREAK 3:00 PM

24.4 A 1V 2GHz CMOS Up-Converter using Self-Switching Mixers

3:15 PM

T. Umeda, S. Otaka, K. Kojima, T. Itakura
Toshiba Corp., Kawasaki, Kanagawa, Japan

A 2GHz up-converter uses 0.25µm CMOS. Curren t adding and self-switching mixers are used for 1V operation. A -40dBc LO leakage within a 20mV offset is achieved using a DC offset canceller. The measurement results at 1V supply are 6.7dB conversion gain, 6.5dBm OIP3, ±2dB gain deviation from -33 to 75°, and 49mW consumption.

24.5 A CMOS IF Sampling Circuit with Reduced Aliasing for Wireless Applications

3:45 PM

S. Levantino[1], C. Samori[1], M. Banu[2], J. Glas[2], V. Boccuzzi[2]
[1]Politecnico de Milano, Milan, Italy
[2]Agere Systems, Murray Hill, NJ

An IF-sampling technique rejects even-order alias channels. A 0.25µm CMOS test chip demonstrates 2dB anti-aliasing rejection, 70dB dynamic range, and -121dBm/Hz noise floor, for a 377MHz IF GSM signal, with 52MHz sampling rate.

24.6 Noise Cancelling in Wideband CMOS LNAs

4:15 PM

F. Bruccoleri, E. Klumperink, B. Nauta
Univ. of Twente, Enschede, The Netherlands

A noise-cancelling technique in a wideband LNA achieves low noise figure (NF) and source impedance matching without global feedback. The 0.25µm LNA provides < 2.4dB NF from 0.01-2GHz, total voltage gain is 13.7dB, −3dB bandwidth is 0.01-1.6GHz, S_{12} is <−36dB and S_{11} is <-10dB. IIP2 is 12dBm, and IIP3 is 0dBm drawing 14mA at 2.5V.

CONCLUSION 4:45 PM

PROCESSOR BUILDING BLOCKS

Chair: Vojin Oklobdzija, Univ. of California, Davis, CA
Associate Chair: Ronald P. Preston, Intel, Shrewsbury, MA

25.1   A 6.5GHz 130nm Single-Ended Dynamic ALU and Instruction-Scheduler Loop

1:30 PM

M. Anders, S. K. Mathew, B. Bloechel, R. Krishnamurthy, K. Soumyanath, S. Borkar
Intel Corp., Hillsboro, OR

32b Han-Carlson ALU and 8-entry x 2-ALU instruction scheduler loop for 6.5GHz single-cycle integer execution at 1.2V and 25°C use dual-Vt CMOS technology. A single-ended, leakage-tolerant dynamic scheme enables up to 9-wide ORs with 23% critical path speed improvement, 40% active leakage power reduction compared to Koggie-Stone implementation, dense layout occupying $44,100\mu m^2$, and performance scalable to 8GHz at 1.5V, 25°C

25.2   5GHz 32b Integer-Execution Core in 130nm Dual-V_T CMOS

2:00 PM

S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, S. Narendra, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, V. De, S. Thompson, S. Borkar
Intel Corp., Hillsboro, OR

A 32b integer execution core implements 12 instructions. Circuit and body bias techniques together increase the core clock frequency to 5GHz. In a 130nm six-metal dual-V_T CMOS process, the $2.3mm^2$ prototype contains 160k transistors, with RF-ALU units dissipating 515mW at 1.6V.

25.3   A Dual-Issue Floating-Point Coprocessor with SIMD Architecture and Fast 3D Functions

2:30 PM

R. Rogenmoser, L. O'Donnell, S. Nishimoto
Broadcom Corp., Santa Clara, CA

A floating-point coprocessor is part of a MIPS64 dual-processor SOC. It consists of a 32x64b register file and two pipes each with a multiplier, an adder, and a fast 3D approximation unit. It operates up to 1GHz at 1.3W, measures $4.74mm^2$ in 0.13μmCMOS, and has peak performance of 8GFlops per CPU and 16GFlops on the dual-processor SOC.

BREAK   3:00 PM

25.4   A 34-Word 64b 10R/6W Write-Through Self-Timed Dual-Supply-Voltage Register File

3:15 PM

N. Tzartzanis[1], W. Walker[1], H. Nguyen[1], A. Inoue[2]
[1]Fujitsu Laboratories of America, Sunnyvale, CA
[2]Fujitsu Laboratories Ltd., Kawasaki, Japan

A register file leverages from a replica-based control unit to improve reliability, operate in a wide voltage range, and support two supply voltages. The main power supply can be stepped down to reduce power, or shut off for sleep mode. Access time is 1.4ns and power dissipation is 220mW at 500MHz in 1.2V, 0.11µm CMOS.

25.5   The High-Bandwidth 256kB 2nd-Level Cache on an Itanium Microprocessor

3:45 PM

T. Grutkowski[1], R. Riedlinger[2]
[1]Intel, Santa Clara, CA
[2]Hewlett Packard, Fort Collins, CO

A second-level 256kB unified cache is incorporated into a 1.2GHz next-generation Itanium Microprocessor. The datapath structures provide a non-blocking, out-of-order interface to the processor core achieving a minimum 5-cycle latency with a stand-alone bandwidth of 72GB/s.

25.6   The Fully-Bypassed 6-Issue Integer-Integer Datapath and Register File on an Itanium Microprocessor

4:15 PM

E. Fetzer[1], J. Orton[2]
[1]Hewlett-Packard, Fort Collins, CO
[2]Intel Corp., Santa Clara, CA

A 6-issue integer datapath with a 20 ported 128x65b register file in a 0.18µm process operates up to 1.2GHz at 1.5V. Operands bypass through 4 stages, from 34 locations, using ½ clock for execution and ½ clock for bypass. Each result is available for the next instruction.

25.7   Adaptive Body-Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage

4:45 PM

J. Tschanz[1], J. Kao[2], S. Narendra[1], R. Nair[1], D. Antoniadis[2],
A. Chandrakasan[2], V. De[1]
[1]Intel Corp., Hillsboro, OR
[2]Massachusetts Institute of Technology, Cambridge, MA

Measurements on a 150nm CMOS test chip show that on-chip bidirectional adaptive body biasing compensates effectively for die-to-die parameter variation to meet both frequency and leakage requirements. An enhancement of this technique to correct for within-die variations triples the accepted die count in the highest frequency bin.

CONCLUSION   5:15 PM

MEMS AND DISPLAYS

Chair: A. Akinwande, MIT, Cambridge, MA
Associate Chair: Clark Ngyugen, Univ. of Michigan, Ann Arbor, MI

**26.1   A Single-Chip Surface-Micromachined Integrated Gyroscope
          with 50°/hour root Allan Variance**

1:30 PM

J. Geen, S. Sherman, J. Chang, S. Lewis
Analog Devices, Cambridge, MA

A MEMS surface-micromachined gyroscope integrated on a single $3x3mm^2$ chip with a 3µm BiCMOS process has 4µm   -thick polysilicon structure, 5V 6mA power supply, 0.05°/√s spot noise, 12.5mV/°/s, >30,000g shock survival, and -55 to 85°C operating range.

**26.2   A Low-Noise Low-Offset Chopper-Stabilized Capacitive-
          Readout Amplifier for CMOS MEMS Accelerometers**

2:00 PM

J. Wu, L. Richard Carley
Carnegie Mellon Univ., Pittsburgh, PA

A CMOS chopper-stabilized amplifier with both DC and AC offset cancellation, for capacitive readout of motion in MEMS structures, achieves 40nV/√Hz noise floor , 10mV DC offset, and 40dB sensor offset reduction. The amplifier, integrated into a CMOS-MEMS accelerometer, achieves 50µg/√Hz noise floor.

26.3   CMOS Single-Chip Multisensor Gas-Detection System

2:30 PM

C. Hagleitner, N. Kerness, D. Lange, A. Hierlemann, O. Brand, H. Baltes
ETH Zurich, Zurich, Switzerland

A single-chip chemical microsensor system fabricated in industrial 0.8µm CMOS technology includes three different polymer-coated micromachined transducers. The chip forms an integral part of a handheld unit to detect volatile organics. On-chip circuitry includes signal conditioning, A/D-converters, filters, digital controller, and serial bus interface (I^2C).

BREAK   3:00 PM

26.4   A Smart CMOS Wind Sensor

3:15 PM

K. Makinwa, J. Huijsing
Delft Univ. of Technology, Delft, The Netherlands

A 2-D thermal flow sensor for the measurement of wind speed and direction is integrated with interface electronics on a single chip. Three thermal ΣΔ modulators control and digitize the flow   -dependent heat distribution in the sensor. Errors in wind speed and direction are <±3% and <±2° respectively. The 16mm^2 chip uses a standard CMOS process.

26.5   A 1/4-inch QVGA Color-Imaging and 3-D-Sensing CMOS Sensor with Analog Frame Memory

3:45 PM

T. Sugiyama[1], S. Yoshimura[2], R. Suzuki[1], H. Sumi[1]
[1]Sony, Atsugi-shi, Japan
[2]Sony-Kihara Research Center, Shinagawa, Japan

A 320x240 color imaging CMOS sensor with a current-copier cell array and comparators for column-parallel processing accomplishes video rate depth acquisition. The sensor dissipates 82mW for 3.3kframe/s 3-D sensing with 2.5mm depth resolution, and 36mW for 30frames/s imaging with a single CDS circuit for FPN reduction at 3.3V.

26.6   An 852x600 Pixel OLED-on-Silicon Color Microdisplay Chip using CMOS Sub-Threshold-Voltage-Scaling Current Driver

4:15 PM

H. Lin[1], E. Naviasky[1], J. Ebner[1], W. Evans[1], P. Farrell[1], M. Hufford[1], G. Levy[1], D. Wheeler[1], B. Allison[1], O. Prache[2]
[1]Tality Corp., Columbia, MD
[2]eMagin Corp., Hopewell Junction, NY

A 16.28x14.2mm^2 852x600x3-pixel OLED-on-silicon color microdisplay is implemented in a 0.35µm 3.3V/4.0V CMOS process. Using sub-threshold-voltage-scaling, the pixel current is modulated between 250pA and 25nA. The 10M-transistor system supports 15 video modes consuming 200mW for 56.25MHz full-motion video.

26.7   A 30MSample/s 12b 110mW Video Analog Front-End for Digital Camera

4:45 PM

B. Ahuja, E. Hoffman, R. Gower, C. Rogers, T. Salcedo
EXAR, Fremont, CA

A highly-integrated 30MSample/s video analog front end for >2M pixels camera with 36dB of programmable pixel-by-pixel gain achieves 73dB SNR. Dynamic bias techniques in a 12b pipeline ADC result in 48mW power with 0.4LSB DNL. The die is 7.6mm^2 in 0.35µm CMOS with 110mW power at 2.7V.

CONCLUSION   5:15 PM

SHORT COURSE

WIDEBAND COMMUNICATIONS

This Short Course is intended to jumpstart engineers in the design and development of CMOS circuits for wideband optical and gigabit Ethernet communication applications. Course completion provides an overall perspective of system tradeoffs along with detailed circuit design strategies for key circuit building blocks. Topics covered include an overview of transceiver architectures and key metrics of wideband amplifiers, chip-to-chip communication and clock and data recovery.

For Registration, please check off the "ISSCC 2002 Short Course" on your registration form (see pg. 72). **Sign-in** is at San Francisco Marriott Hotel, Level B-2, beginning at 8:00 AM.

The Short Course is offered three times on Thursday, February 7.
> The first session is scheduled for **8:00AM to 4:30PM**.
> The second session is scheduled for **10:00AM to 6:30PM**.
> The third session is scheduled for **1:30PM to 9:30PM**.

CD of the Short Course & Relevant Papers: Short Course registrants will receive a CD-ROM of the Short Course with relevant papers and background material. The CD-ROM includes: (1) The four Short Course presentations in PDF format for printing hard copies of the slides, (2) Bibliographies of relevant papers for all four presentations, and (3) PDF copies of relevant background material and important papers in the field (about 10-20 papers per presentation).

OUTLINE

HIGH-SPEED DSP-BASED TRANSCEIVERS
(8:00-9:30AM), (10:00-11:30AM), (1:30-3:00PM)

This first segment of the short course describes standard techniques used in high-speed DSP-based transceivers, such as modulation, equalization, Viterbi detection, and forward error correction, with special emphasis on architecture and VLSI implementation. It then studies two specific design cases: Gigabit Ethernet over unshielded twisted pair, and a DSP-based optical transceiver.
Instructor: Kamran Azadet received PhD from ENST Paris in 1994. Since 1994 he has been with Bell Labs/Holmdel NJ, working on color digital CMOS cameras, and high-speed transceivers. He was a member of the IEEE 802.3ab Gigabit Ethernet 1000BaseT and 10 Gigabit Ethernet 802.3ae standard committees. He is currently director of the high-speed Communications VLSI Research Department of Agere Systems in Holmdel. He was a co-recipient of the 1998 IEEE Journal of Solid-State Best Paper Award for a paper on a color digital CMOS camera.

WIDEBAND AMPLIFIERS
(10:00-11:30AM), (12:00-1:30PM), (3:30-5:00PM)

Amplifiers used in fiber optic receivers and transmitters must satisfy a wide range of requirements. The design challenges are compounded by packaging, power supply and interface aspects. The opto-electronic devices that the chips are coupled with are examined and system requirements are translated into circuit specifications such as bandwidth, dynamic range, group delay and drive capability. The design of a 10Gb/s driver for un-cooled laser applications serves as an example.

Instructor: Hans Ransijn received the EE Degree from Delft Univ. of Technology, Netherlands in 1982. He co-founded a semi-custom IC design house DICE (Delft Integrated Circuit Engineering) and worked as a Technical Staff Member with the CATV department of the Dutch PTT in 1983. From 1983-1985 he was with the Space Research Organization Netherlands (SRON), where he designed analog front ends for space-borne instrumentation. In 1985 he joined AT&T Bell Labs in Reading, PA, now Agere Systems, where he is working on high-speed physical-layer circuits for 10 and 40Gb/s fiber-optic communication systems.

CHIP-TO-CHIP COMMUNICATION
(1:00-2:30PM), (3:00-4:30PM), (5:30-7:00PM)

Chip-to-chip I/O performance is projected to exceed Tb/s of aggregate bandwidth. Serious circuit design issues emerge in building low area, high-speed (multi-Gb/s), low power, and noise robust I/O busses. Designs of transmitters and receivers for parallel I/O busses are described emphasizing low-cost design techniques to achieve low jitter and high signal integrity (noise filtering and equalization).

Instructor: C.K. Ken Yang received BS and PhD in EE from Stanford Univ. in 1992 and 1998, respectively. He joined Rambus Inc. during a leave of absence for one year in 1993 to design a 500MB/s memory interface on a 16Mb DRAM. In 1999, he joined the UCLA Dept. of EE as an Assistant Professor. His research on high-performance mixed-mode circuit design primarily focuses on high-speed clock and data recovery for large VLSI systems.

CLOCK AND DATA RECOVERY FOR SERIAL DATA COMMUNICATIONS
(3:00-4:30PM), (5:00-6:30PM), (8:00-9:30PM)

Techniques for data transmission over serial optical and electrical links are presented with the common distortions that occur over such links. Topics including eye diagrams, jitter tolerance, jitter transfer function, and jitter generation are introduced along with data encoding for run length control, framing, and DC-balance. The talk describes monolithic clock recovery emphasizing bang-bang PLL design and components such as data-driven phase/frequency detectors, charge pumps, ring oscillators, and multi-phase sampling structures.

Instructor: Richard Walker received BS in Engineering and Applied Science from the California Institute of Technology in 1982, and MS in Computer Science from California State Univ., Chico, CA in 1992. Rick joined Agilent Labs (formerly Hewlett-Packard) in 1981, where he is currently a Principal Project Engineer. His interests include broadband-cable modem design, solid-state laser characterization, bang-bang phase-locked-loop theory, 64b/66b 10GbE linecode design, and gigabit-rate serial data transmission. He holds 13 US patents.

WORKSHOP ON MICROPROCESSOR DESIGN

ISSCC Microprocessor Design Workshop:
W2: High-Frequency Clocking – Issues and Solutions for Clocking High-Frequency Microprocessors

Organizing Committee: Chair: Sam Naffziger, Hewlett Packard, John Maneatis, True Circuits, Inc, Kerry Bernstein, IBM, Ron Preston, Intel, Simon Segars, ARM, Hector Sanchez, Motorola, Ian Young, Intel

This Workshop encourages open interchange in a closed forum. Attendance is limited and pre-registration is required.
The general goal is to discuss important technical issues and directions in design of next-generation microprocessors.

This year, the Workshop addresses issues of high-frequency clocking on a variety of levels: architecture, circuit, process technology, and chip to chip interconnection.

As frequencies have driven relentlessly up into the multi-GHz range, the problem of getting that multi-GHz clock to all parts of the chip has become increasingly difficult. This Workshop seeks to enable designers of next generation processors to deal effectively with these difficulties by addressing the following issues:

- **Clock partitioning**: As processor complexity grows, the span of the clock must increase to cover all the additional circuitry. When combined with larger wire delays and increased variability, many processor architects are looking at ways to partition the design into smaller quanta, each of which can operate in its own, somewhat independent clock domain. Topic 3 examines some of these tradeoffs.

- **Asynchronous methods**: One solution to distributing the high frequency global clock is to eliminate it by resorting to largely asynchronous circuit implementations. Some of the methods of design and analysis of such systems are presented in topic 5.

- **Process variability**: As transistor and interconnect geometries continue to shrink, designers are faced with the increased impacts of not only wire RC delays, but the increased variability of these wires and circuits. The net result is that it is much harder to reliably deliver a synchronous clock to all corners of the die. Topics 2, 6 and 7 seek to enable designers to analyze and understand this variability and deal with the implications for clock distribution.

- **Skew management**: The increased uncertainty in actual clock arrival time across the chip has resulted in designers seeking out new ways to either reduce the clock skew with active circuitry or make the clocked storage elements less sensitive to the effects of skew. Some of these approaches are discussed under topics 4 and 7.

The workshop wraps up with representatives from both academia and industry painting pictures of what it will take to produce and consume reliable clocks for 10 to 20GHz processors. The path to achieving those clock frequencies in the next few years will certainly traverse many of the methods discussed in this workshop.

Thursday, February 7th 8:30 AM

1. Workshop Introduction and Overview of Clocking

8:30

Sam Naffziger, Hewlett-Packard

2. Process Technology Scaling Trends.

(9:00

Krishna Saraswat, Stanford University

Break 9:45

3. Clocking Impacts on Architecture - future directions

10:00

Matt Reilly (Intel)

4. Design of Sequential Elements

11:00

Vojin Oklobdzjia (University of California, Davis)

Lunch 12:00

5. Clock tolerant architectures - Asynchronous methods and issues

1:00

Simon Moore, Cambridge University

6. Manufacturing components of delay variation

2:00

Sani Nasif (IBM)

7. Clock skew components and methodologies for analysis and design.

2:30

David Harris, Harvey Mudd College

Break 3:30

8. i) Clocking solutions for 10-20GHz processors

3:45

Tom Chen, Colorado State University

8. ii) Architecture implications for Clocking in 10-20GHz processors

4:15

Dave Sager, Intel

Workshop Discussion, All speakers **4:45**

Conclusion **5:15**

CONFERENCE REGISTRATION

This year ISSCC will again offer online registration. This is the fastest most convenient way to register and will give you immediate confirmation of whether or not you have a place in the Tutorial and Short Course sessions of your choice, as well as the ISSCC Microprocessor Design Workshop and SSCTC Analog Telecom Access Circuits and Concepts Workshop. If you register online using a credit card, your registration is processed immediately, and your written confirmation can be downloaded and printed for your record keeping. If you register by fax or mail, you will not receive confirmation for several days. **Registration forms received without full payment will not be processed until payment is received at SeminarSource.**

To register online, go to the ISSCC website (www.isscc.org) or go directly to registration via www.seminarsource.com/isscc2002. All payments must be made in U.S. Dollars, by credit card or check. Checks are to be made payable to "**SeminarSource/ISSCC**." Payments by credit card will appear on your monthly statement as a charge from "SSource-ISSCC2002."

The deadline for receipt of Early Registration fees is **December 28, 2001. After December 28th and on or before January 18, 2002,** registrations will be processed only at the Late Registration rates**. As of January 19th, you must pay the onsite/highest registration fees.** Because of limited seating capacity in the meeting rooms and hotel fire regulations, onsite registration may be limited. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2002.

For those who wish to register by fax or mail, the Advance Registration form can be found at the center of this booklet. Please read the explanations and instructions on the back of the form carefully.

Full Conference registration includes one copy each of the Digest of Technical Papers, the Visuals Supplement (mailed in March) and the 2002 Conference CD-ROM (mailed in June). Students receive a Digest and CD-ROM. All students must present their student ID at the Conference Registration Desk to receive the student rate. Anyone registering at the IEEE Member rate must also provide his/her IEEE Membership number.

The Onsite and Advance Registration Desks at ISSCC 2002 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except presenting authors, must pick up their registration materials at these desks as soon as they arrive at the hotel. **The Presenting Author for each paper must go directly to the Twin Peaks to register and to collect their materials.**

REGISTRATION HOURS:

Saturday, 2/2:	4:00 PM to 7:00 PM (**Tutorial and Workshop Attendees Only**)
Sunday, 2/3:	6:30 AM to 1:30 PM (**Tutorial and Workshop Attendees Only**)
	4:00 PM to 7:00 PM
Monday, 2/4:	7:00 AM to 3:00 PM
Tuesday, 2/5:	8:00 AM to 3:00 PM
Wednesday, 2/6:	8:00 AM to 12:00 Noon
Thursday, 2/7:	7:00 AM to 1:00 PM (**Short Course and Workshop Only**)

INFORMATION

NEXT ISSCC DATES AND LOCATION
ISSCC 2003 will be held on February 9-13, 2003 at the San Francisco Marriott Hotel.

FURTHER INFORMATION
Visit the website at: http://www.isscc.org
To be placed on the Conference Mailing List, please contact the Conference Office, c/o Courtesy Associates, 2000 L Street, N.W. - Suite 710, Washington, DC 20036; Email: isscc@courtesyassoc.com; Fax: 202-973-8722.

HOTEL RESERVATIONS
This year, ISSCC participants can again make their hotel reservations online. To do this, go to the website (www.isscc.org) and click on the Hotel Reservation link to the San Francisco Marriott. To receive the special ISSCC group rates, you must enter the proper "Group Code" for ISSCC: SSCSSCA = single @ $184; or double @ $204; SSCSSCB = triple @ $224; SSCSSCC = quad @ $244. The dates of your reservation must fall within the period of January 31-February 8, 2002. All online reservations require the use of a credit card. Once made and confirmed, your online reservation can be changed only by calling 1-800-228-9290 (toll free) or 415-442-6755. Reservation changes can also be made by faxing the Marriott directly at 415-442-0141. Online reservations are confirmed immediately, while you are online. We suggest that you **print the page containing your confirmation number and reservation details and bring it with you** when you travel to ISSCC.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet. **Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax.**

Reservations must be received at the San Francisco Marriott no later than Friday, January 11, 2002 to obtain the special ISSCC rates. A limited number of rooms is available at these rates. Once this limit is reached and/or after Friday, January 11th, the group rate will no longer be available. After the 11th, reservation requests will be filled at the best available rate.

CONFERENCE PUBLICATIONS
Additional ISSCC publications can be purchased at the Conference Registration Desk. Prices are lower for purchases collected onsite that do not have to be shipped to the purchaser.

TECHNICAL-BOOK DISPLAY
A number of technical publishers have a collection of professional books and textbooks on display. These books are available for sale or to order onsite. The book display is in the Golden Gate Hall, located one level above the ballroom and technical sessions. The Book Display will be open on Monday from 12:00 Noon - 6:30 PM; on Tuesday from 9:30 AM to 5:30 PM; and on Wednesday from 9:30 AM to 1:00 PM.

INFORMATION

ISSCC AND JSSC DIGITAL-ARCHIVE DVD

In August 2001 the Solid-State Circuits Society (SSCS) released a new *Digital-Archive-2000* DVD. It includes the complete collection of *ISSCC Digests* and *Slide Supplements* and the complete collection of IEEE *Journal of Solid-State Circuits* issues. Specific features of the Digital-Archive-DVD include:

- A Master Index of the 1956-2000 ISSCC publication and the 1966-2000 JSSC publication, including
    - Author, title, issue, and subject indexes
    - Abstracts, references, and citations for each article
- PDFs of all papers of the 1956-2000 *ISSCC Digests* and PDFs of the *ISSCC Slide Supplements*
- PDFs of all papers from the 1966-2000 *JSSC*

The abstracts and papers are fully searchable using the Acrobat search engine included with the DVD. As a new feature, the search results can now be sorted by date. All references and citations to ISSCC or JSSC articles are automatically linked to those articles retrieved, allowing instant access to references and citations.

The DVD Digital Archive is priced at \$120 for members and \$240 for non-members. It may be ordered on the advance-registration form. DVDs ordered with your advance registration form will be waiting for you at registration. You may also purchase a DVD on-site at the IEEE book desk in Golden Gate Hall.

IEEE AND SOCIETY MEMBERSHIP

If you have never been a member of the IEEE and would like to sample its subscriptions and advantages, bring your ISSCC registration receipt showing that you registered as a non-member, to the IEEE Membership Desk located in Golden Gate Hall. Special new-member-only rates are offered during ISSCC 2002. Receive \$25 off a full year of IEEE membership and free membership in both the Solid-State Circuits Society and the Electron Devices Society. IEEE membership allows access to IEEE *Xplore^{tm}*.

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As well, low member-rates are available to purchase SSCS products such as the CD of the 2000 ISSCC Short Course on *Circuits and Devices for RF Wireless Networks* and the *Digital-Archive-2000* DVD described above.

Current or formal IEEE members should can or add membership in a Society by telephoning 1-800-678-IEEE, or using their IEEE WEB account.

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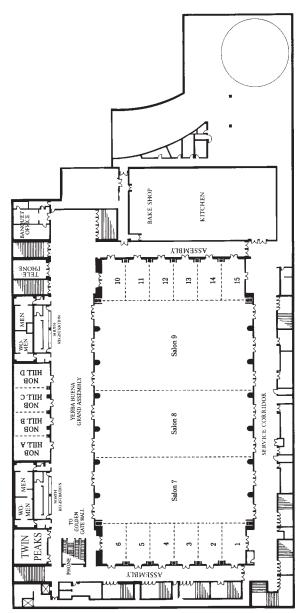
COMMITTEES

CONFERENCE SPACE LAYOUT

The Conference Book Display and Social Hour will be held in Golden Gate Hall. The layout appears below:

CONFERENCE SPACE LAYOUT

All Conference Technical Paper Sessons are in the Yerba Buena Ballroom at the San Francisco Marriott Hotel. The layout appears below: