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Welcome to the 24th annual Custom Integrated Circuits Conference, CICC 2002. The CICC is the leading international conference for integrated circuit development where first time advancements are published and presented. CICC provides a unique forum for all individuals involved with IC development to meet and share information about the most recent advances in system architectures, circuit and computer-aided design and process technology. CICC's goal is to offer attendees a total educational experience balanced between paper presentations, exhibits, panels, tutorials and interesting networking events. You are cordially invited to participate in CICC 2002, as we convene this year in Orlando, Florida at the Caribe Royale Resort Suites.

The conference starts with three educational sessions on Sunday, May 12th, 2002. These sessions are taught by practicing experts working at the leading edge of their field. The topics for these sessions are: Advanced RF, Advanced Data Converter Design and Test Techniques, High-Performance and Low-voltage Design Challenges and Techniques.

On Monday morning, the technical program begins with the keynote speaker, Christine King, CEO of AMI Semiconductor. Christine will discuss the challenge facing the semiconductor industry to balance cost, performance, power, productivity and time to market in "Smart Management of ASIC Requirements and Technology (SMART)".

The technical program offers exceptional technical papers that provide the latest and most significant developments in the IC industry. This year, more than 250 technical papers were submitted, of which 108 were selected and organized into 21 sessions. Topics for these sessions include: Analog, Wireless & Wired Communications, Custom & Low Power Circuits, System-on-a-Chip/IP, Embedded Memories, Simulation & Modeling, Fabrication, Programmable Devices, DSPs and Test & Reliability. As always, the technical sessions are highlighted by invited and tutorial papers presented by leading experts from industry and academia. This year we have had the good fortune of many excellent publications.

Jeff Oppold
General Chair

Monday afternoon the Exhibitor Preview Sessions kick off the opening of the Exhibits Hall. Here many of our Exhibitors will present overviews of new products and services. During the Monday evening Exhibitors' Reception you will find refreshments and professional networking at its very best! As always, our exhibits area will include booths and software demonstrations from prominent corporations in the industry.

Phil Diodato
Conference Chair

You will not want to miss this year's conference luncheon. Our honored guest speaker is Dr. Eugene Trinh, Director of the Physical Sciences Research Division in the Biological and Physical Research Enterprise at NASA. Dr. Trinh was a member of the Space Shuttle Columbia's crew in 1992. The title of his talk will be "Accomplishments and Promises of Research in Low-gravity." This promises to be a fascinating and educational experience.

Larry Starr
Technical Program Chair

On Tuesday afternoon and evening, three spirited panel discussions are scheduled featuring experts who are sure to offer strong opinion on the following three panels: "Design Challenges in Wireless LANs", "Will the Next Great Killer Technology Application Please Stand Up!!", and "Can Scaling Continue at the same rate below 0.10μm? What is the end of CMOS…and What is Next?" These panel discussions are always entertaining and enlightening, and you are sure to come away with information and insights of the not-too-distant future. There will also be a special in-session educational tutorial presented during Session 10 entitled "Delta-Sigma Converters for Wireless Transceivers" taught by Dr. Ian Galton of the University of California.

We extend our thanks to all the authors who spent many hours on the preparation of their submitted papers. We also wish to thank the CICC Technical Program Committee and our dedicated conference staff for all of their hard work and support. It is their diligent efforts that keep CICC as the best place to discover the latest in integrated circuit innovations, newest product announcements, and to debate the most effective business strategies. See you in Orlando!

EDUCATIONAL SESSIONS

Sunday, May 12

Chairperson: Trudy Stetzler, Texas Instruments

Ed. Session 1 - Advanced RF: From Devices to Systems
Grand Caribbean Ballroom I

Organizer: Francesco Svelto, Università di Pavia
Co-organizer: Larry Nagel, Omega Enterprises

E1-1 RF Performance and Modeling of CMOS Devices

8:00-9:50 Dirk B.M. Klaassen, Philips Research Laboratories

Continuous down-scaling of CMOS process technologies has resulted in a strong improvement of the RF performance of MOS devices. Consequently, CMOS has become a viable option for analog RF applications and RF system-on-a-chip. In order to allow for versatile RF circuit design in CMOS technologies, a number of issues, which traditionally get little or no attention in compact MOS modeling for digital or low-frequency analog circuit design, have to be taken into account: impedances and power gain, output impedance and bulk resistance, input impedance and gate resistance, non-quasi-static (or transit time) effects, power gain, noise, 1/f (or flicker) noise, thermal noise, induced gate noise and distortion.

This presentation focuses on the discussion of these issues for CMOS devices, while in addition an overview will be given of the present state-of-the-art of compact modeling. This part will be followed by a discussion, using both simulations and measurements of layout effects on the RF performance of CMOS devices. Finally, the performance and modeling of passive devices such as varicaps (or varactors) and inductors will be discussed.

E1-2 RFIC Receiver Circuits

10:10-12:00 John R. Long, Delft University of Technology

This lecture addresses the design of RFIC receiver circuits in CMOS and BiCMOS technologies from antenna to base-band. Major IC building blocks such as low-noise preamplifiers, down-converting mixers, voltage-controlled oscillators, image-reject down-converters and frequency scalers are considered. Technology evaluation for RF performance, selection of an appropriate circuit topology and the relationship between the circuit and systems specifications as preliminary steps in the design process are outlined. The advantages and limitations of on-chip inductors, transformers and other passives available for RFIC work are discussed. Issues in modeling, simulation and circuit design based on the passive and active components available in standard IC design kits and tools are highlighted within the context of each building block. Co-integration and evaluation of receiver blocks are described, with emphasis on topics such as physical layout, package parasitics, off-chip matching, test fixturing and chip evaluation at RF.

E1-3 Key Issues in Transmitter Blocks

1:00-2:50 Earl McCune, Tropian Inc.

This presentation will focus on higher order issues for transmitter blocks not generally seen in textbooks. These are grouped into three areas: 1) effects of error sources in quadrature modulators and demodulators, 2) issues with on-channel RF signal processing (direct conversion/modulation), and 3) successful implementation of RF circuitry in the presence of local digital CMOS.

E1-4 From RF System to Silicon

3:10-5:00 Asad A. Abidi, University of California, Los Angeles

Expertise in RF circuits traditionally concentrates on the design and optimization of individual circuit blocks, such as better amplifiers, mixers, or oscillators. Yet in the context of single-chip transceivers, the importance of the right architecture of receiver or transmitter usually has a much greater impact on performance and power consumption than improvements in any given circuit. Without sufficient thought to the architecture, even the best circuits may lead to an inferior end result. The practical problems of on-chip interconnections and buffering at RF are often overlooked.

In this presentation, we will use various examples to show this process at work. The examples include an adaptive 2.4 GHz linear receiver for wireless LAN, a 900 MHz receiver and transmitter for GSM, and a 900 MHz very low power receiver for paging usage.

Ed. Session 2 - Advanced Data Converter Design and Test Techniques

Grand Caribbean Ballroom II

Organizer: Doug Garrity, Motorola
Co-organizer: David Allee, Arizona State University

E2-1 8:00-9:50 **Introduction to Delta-Sigma Data Converters**
Bob Adams, Analog Devices

Noise-shaping converters have by now completely displaced data-acquisition converters in applications where spectral performance is the key performance metric. This talk will start with the basics of noise-shaping converter theory and progress to more advanced and recent topics such as mismatch-shaping schemes that are used in modern multi-bit noise-shapers. Practical aspects of noise-shaping converter design will also be covered.

E2-2 10:10-12:00 **Multi-bit Mismatch-Shaping DACs for High-Performance Delta-Sigma Data Conversion**
Ian Galton, UC San Diego

Mismatch-shaping DACs have become widely used in high-performance delta-sigma data converters. By suppressing the signal-band portion of the error introduced by inevitable component mismatches, mismatch-shaping DACs have made the use of multi-bit quantization in delta-sigma modulators practical. Relative to single-bit quantization, which was the norm prior to the availability of mismatch-shaping DACs, multi-bit quantization significantly relaxes the performance required of the analog circuitry thereby increasing the data conversion performance that can be achieved for a given power consumption and circuit area. This tutorial will present a detailed explanation of mismatch-shaping DACs and their application to high-performance delta-sigma data converters at both the signal processing and circuit levels. After a brief review of delta-sigma modulation, the tutorial will provide a practical explanation of the signal processing principle underlying the ability of mismatch-shaping DACs to shape mismatch error without knowledge of the mismatches, a survey of alternative mismatch-shaping DAC topologies, a detailed circuit-level description of highly efficient first-order and second-order mismatch-shaping DACs, and the system and analog circuit level delta-sigma modulator design implications of mismatch-shaping DACs. Examples of state-of-the-art delta-sigma data converters will be presented as case studies.

E2-3 1:00-2:50 **Practical Aspects of Nyquist-Rate Switched-Capacitor ADC's**
David Nairn, Analog Devices

System- and circuit-level issues for switched-capacitor (SC), Nyquist rate analog-to-digital converters (ADCs) will be discussed. After a brief review of the common SC ADC architectures, flash, successive approximation, cyclic and pipelined, the trade-offs between the architectures will be considered. Then, system-level issues such as noise and accuracy in conjunction with their effects on partitioning and scaling will be considered for the ADCs. Following this, the discussion will focus on specific circuit and design issues related to subcomponents such as switches, capacitors, op amps and comparators. Where appropriate, example circuits will be analyzed and good layout practices will be considered.

E2-4 3:10-5:00 **State of the Art Lab Characterization Methods for High-Speed ADCs and DACs**
Steve Reine, Analog Devices

High Speed ADCs and DACs are making the distance, often spoken of as bits to the antenna, shorter in each new generation of converters. Cutting-edge digital communications systems require novel and unique characterization methods for ADCs and DACs. Converter characteristics are now defined in terms of radio and broadband communications technology. Spectral characteristics become key, while time-domain effects take on new meaning. Generation of high-speed analog and digital test signals requires that generators be capable of synthesizing high dynamic range multi-carrier and wideband signals.

Ed. Session 3 - High-Performance and Low-Voltage Design Challenges and Techniques

Grand Caribbean Ballroom III

Organizer: Ram Krishnamurthy, Intel Corporation
Co-organizer: Sreedhar Natarajan, Texas Instruments

E3-1 Low-power Circuits & XScale

8:00-9:50 Larry Clark, Intel Corporation

Low-power circuit design is increasing in importance with the proliferation of battery-powered devices and increasingly difficult integrated circuit thermal management. This tutorial will provide an overview of low-power design including process selection, circuit and logic design techniques, clocking, voltage scaling, dynamic voltage adjustment, and leakage management. Examples of techniques used in the industry, as well as details of those used in the XScale Microarchitecture(TM) will be discussed. The XScale microprocessor is capable of operation at 800MHz dissipating 900mW down to 200MHz dissipating 50mW and is capable of changing frequency and voltage on the fly. Standby power of 100uW is enabled by leakage suppression circuitry while retaining state. Application needs and the efficacy of power reduction approaches in addressing them will also be described and compared. Issues with future process scaling and the resulting power implications will conclude the tutorial.

E3-2 Leakage Control & Leakage Tolerant Circuits

10:10-12:00 Prof. Kaushik Roy, Purdue University

This tutorial presents advanced challenges and solutions for leakage control and leakage tolerant VLSI systems. Circuit and CAD techniques for leakage control and tolerance, e.g., stacked CMOS with gated-Vdd, Multiple-Vt, Dynamic-Vt, MTCMOS, VTCMOS, and SCCMOS techniques and their bulk and SOI implementations are discussed. Ultra-low-voltage digital subthreshold logic techniques and some of their medical applications, e.g., bursty vs. non-bursty modes are described.

E3-3 SOI Design Challenges

1:00-2:50 Andrew Marshall, Texas Instruments

Silicon-on-insulator (SOI) material has become an increasingly popular technology for IC design and manufacturing. Performance improvement, reduced power, component isolation and an increase in circuit density are some of the obvious benefits. Many of these advantages, however, have trade-offs , including bipolar leakage effects of the SOI MOS devices, thermal issues, transistor matching difficulties and the history and kink effects for some SOI technologies.

A brief overview of the SOI process is given and a comparison is made between SOI and bulk material. The challenge of modeling SOI devices is explored and some concepts for successful SOI circuit layout are introduced, including a review of various options for the reduction of thermal self-heating effects. Following discussion of digital design techniques, SOI feasibility to SRAM and DRAM memory designs is considered. In addition analog circuit design techniques are discussed. By way of conclusion, low-power design and trends in SOI development are addressed.

E3-4 Low-power Memory Design

3:10-5:00 Dr. Betty Prince, Memory Strategies International Inc.

This session will review issues for low-power memory design including the trend toward portable systems; reliability in nanometer scale geometries; managing high speed operation in standalone memories such as DDR DRAMs and SRAMs; and controlling high speed, heat generating operations in integrated memories such as cache and CAM. Methodology discussed will include reducing power consumption in the memory peripheral circuitry and in the array architecture, and managing memory mode to minimize power. Power issues with non-volatile memories will also be discussed such as use of high-voltage generators on chip.

EXHIBITS

CICC once again combines its outstanding technical program with a variety of exhibitors. Exhibits will include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications. The Exhibit Hall will be the site for Monday's Exhibitors' Reception and Tuesday evening's Happy Hour.

Partial Listing of Exhibitors:

Adelante Technologies
ATMOS
Avant! Corporation
IMS, A Credence Company
John Wiley and Sons
Kluwer Academic Publishers
Mentor Graphics
Nassda Corporation
Neolinear, Inc.
Rubicad Corporation
Simplex Solutions
Synopsys, Inc.

EXHIBIT HOURS

Royal Palms I & II
Monday, May 13
2:00 pm - 8:00 pm
1:00 pm - 2:00 pm Exhibitor Preview Session
5:30 pm - 8:00 pm Exhibitors' Reception
Tuesday, May 14
2:00 pm - 7:00 pm
5:30 pm - 7:00 pm Happy Hour

EXHIBITORS' PREVIEW SESSIONS

Monday, May 13, 1:00 pm - 2:00 pm

PREVIEW SESSION 1
Boca I

1:00 **Accent -** Outsourcing SoC Design Safety and Profitably
1:20 **Adelante Technologies** - TBD
1:40 **Simplex** - SoC Verification and the Mixed-Signal Challenge

PREVIEW SESSION 2
Boca II

1:00 **Nassda** - Full-chip Verification of Power-Net IR Drop Enables Nanometer Silicon
1:10 **Synopsys** - Multi-Level Mixed-Signal Circuit Simulation with NanoSim
1:20 **Rubicad -** TBD
1:30 **John Wiley and Sons** - TBD

TECHNICAL SESSIONS

Monday, May 13 - Wednesday, May 15

Session 1 – Keynote Presentation
Grand Caribbean Ballroom I
Monday Morning, May 13

8:00 **Welcome/Opening Remarks**
Awards Presentations
Keynote Speaker Introduction
Jeff Oppold, General Chairman

8:20 **KEYNOTE ADDRESS**
"Smart Management of ASIC Requirements and Technology (SMART)", C. King, President & CEO, AMI Semiconductor

Complex issues such as time-to-market, productivity, cost, performance and power continue to challenge the semiconductor industry. Today the focus is on finding the best overall solution to fit individual applications and to meet specific market needs. Many applications require and benefit from the highly advanced system-on-a-chip designs enabled by the unprecedented silicon potential of ever-shrinking technologies. For example, high-performance graphics processors in computers and game systems have evolved to extreme examples of integration, but are very specific to a given architecture. Routers and datapath systems, on the other hand, must be configurable to different I/O and network requirements and are benefiting from a combination of medium-density ASICs, standard products and FPGAs where the same "leading-edge" technology is not essential. Today's engineers are striving to balance the tradeoffs of these two approaches to find the smartest overall solution. What will the impact of this SMART mind set be on the semiconductor industry in the year 2002 and beyond?

Christine King was named president and chief executive officer of AMI Semiconductor (AMIS) on Sept. 10, 2001, becoming the first woman CEO of a semiconductor company.

Prior to joining AMIS, King spent 23 years at IBM where she was most recently vice president of Semiconductor Products for IBM Microelectronics, a multi-billion dollar business. Her extensive experience at IBM includes launching IBM's ASIC business in 1993 and growing it to be the number one ASIC business in the world with $1.7 billion in revenue, as reported by Gartner Dataquest. She also launched IBM's networking business in 1998.

Session 2 – Reconfigurable Hot SoCs
Grand Caribbean Ballroom I
Monday Morning, May 13

Chair: Jim Lipman Co-Chair: Ric Williams

Following an invited reconfigurable-logic tutorial are two papers on embedded configurable-processor designs. One paper describes unique code-decompression circuits to reduce code size while the other combines an extensible core with an embedded FPGA.

10:00 am **Introduction**

10:05 am **Reconfigurable Logic in SoC Systems (Invited),** J.
2-1 Greenbaum, Chameleon Systems, Inc., San Jose, CA

10:55 am 2-2 **1-Cycle Code Decompression Circuitry for Performance Increase of Xtensa-1040-based Embedded Systems,** H. Lekatsas, J. Henkel and V. Jakkula, NEC USA, Inc., Princeton, NJ

11:20 am 2-3 **A Reconfigurable System featuring Dynamically Extensible Embedded Microprocessor, FPGA and Customisable I/O,** M. Borgatti, F. Lertora, B. Forêt and L. Calì, STMicroelectronics, Agrate Brianza, Italy

Session 3 – Modeling and Optimization Techniques

Grand Caribbean Ballroom II
Monday Morning, May 13

Chair: Yuhua Cheng Co-Chair: Hidetoshi Onodera

Join this session for new modeling and design methodology ideas for high-speed interconnects, noise and delay optimization, compact model compilation, and multi-objective generic optimization techniques for analog/RF circuits.

10:00 am **Introduction**

10:05 am 3-1 **Loop-based Interconnect Modeling and Optimization Approach for Multi-GHz Clock Network Design,** X. Huang, P. Restle*, T. Bucelot*, Y. Cao and T.-J. King, University of California, Berkeley, CA and *IBM T.J. Watson Research Center, Yorktown Heights, NY

10:30 am 3-2 **A Signal Integrity-Driven Buffer Insertion Technique for Post-Routing Noise and Delay Optimization,** K. Chakraborty, D. Long, J. Fishburn, K. Singhal*, L. Ye* and C. Ortiz*, Agere Systems, Murray Hill, NJ and *Allentown, PA

10:55 am 3-3 **ADMS - Automatic Device Model Synthesizer,** L. Lemaitre, C. McAndrew* and S. Hamm**, Motorola, Geneva, Switzerland and *Tempe, AZ and **Austin, TX

11:20 am 3-4 **Watson: A Multi-Objective Design Space Exploration Tool for Analog and RF IC Design,** B. De Smedt and G. Gielen, Katholieke Universiteit, Leuven, Belgium

Session 4 – Copper Wired Communications

Grand Caribbean Ballroom III
Monday Morning, May 13

Chair: Dave Rich Co-Chair: Sang-Soo Lee

This session addresses trends in DSL and wired-communications systems, focusing on ICs for analog-line interfaces and data-synchronization applications.

10:00 am **Introduction**

10:05 am 4-1 **Integration and System Design Trends of ADSL Analog Front Ends and Hybrid Line Interfaces (Invited),** S.-S. Lee, LSI Logic, San Jose, CA

10:55 am 4-2 **A Central Office Combined ADSL-VDSL Line Driver Solution in .35µm CMOS,** T. Piessens and M. Steyaert, Katholieke Universiteit, Leuven, Belgium

11:20 am 4-3 **A 6MHz-130MHz DLL with a Fixed Latency of One Clock Cycle Delay,** H.-H. Chang, J.-W. Lin and S.-I. Liu, National Taiwan University, Taipei, Taiwan, ROC

Session 5 – Innovations in Programmable Logic: Architectures and Applications

Grand Caribbean Ballroom I
Monday Afternoon, May 13

Chair: Steve Wilton Co-Chair: Trevor Bauer

What do chess, virtual silicon, and analog circuitry have in common? Programmable logic can do it all.

2:00 pm **Introduction**

2:05 pm 5-1 **An Architecture for a Programmable Mixed-Signal Device,** M. Mar, B. Sullam and E. Blom, Cypress MicroSystems, Inc., Bothell, WA

2:30 pm 5-2 **Nearest Neighbour Interconnect Architecture in Deep Submicron FPGAs,** A. Roopchansingh and J. Rose, University of Toronto, Toronto, ON, Canada

2:55 pm 5-3 **PipeRench: A Virtualized Programmable Datapath in 0.18 Micron Technology,** H. Schmit, D. Whelihan, A. Tsai, M. Moe, B. Levine and R. Taylor, Carnegie Mellon University, Pittsburgh, PA

3:20 pm **Break**

3:35 pm 5-4 **The Architecture of Dual-Mode FPGA Embedded System Blocks,** E. Lin and S. Wilton, University of British Columbia, Vancouver, BC, Canada

4:00 pm 5-5 **An FPGA Based Move Generator for the Game of Chess,** M. Boulé and Z. Zilic, McGill University, Montréal, PQ, Canada

Session 6 – Design Approaches for Testability and Reliability

Grand Caribbean Ballroom II
Monday Afternoon, May 13

Chair: Mark Young Co-Chair: Mike Zachariah

The importance of designing for test and reliability is the focus of papers in electrostatic discharge, burn-in, timing measurement, and soft-errors.

2:00 pm **Introduction**

2:05 pm 6-1 **A Deep Sub-Micron Timing Measurement Circuit Using a Single-Stage Vernier Delay Line,** A. Chan and G. Roberts, McGill University, Montréal, PQ, Canada

2:30 pm 6-2 **A Burn-In Tolerant Dynamic Circuit Technique,** A. Alvandpour, R. Krishnamurthy, S. Borkar, A. Rahman and

C. Webb, Intel Corporation, Hillsboro, OR

2:55 pm 6-3 **Managing Soft Errors in ASICs,** L. Wissel, S. Pheasant, R. Loughran, C. LeBlanc and B. Klaasen, IBM Microelectronics, Essex Junction, VT

3:20 pm **Break**

3:35 pm 6-4 **High Voltage Tolerant ESD Design for Analog Applications in Deep Submicron CMOS Technologies,** C.-H. Chen, Y.-K. Fang, C.-C. Tsai*, S. Tu*, M.K.L. Chen* and M.-C. Chang*, National Cheng Kung University, Tainan, Taiwan, ROC and *TSMC, Hsinchu, Taiwan, ROC

4:00 pm 6-5 **The Embedded SCR NMOS and Low Capacitance ESD Protection Device for Self-Protection Scheme and RF Application,** J.-H. Lee, Y.-H. Wu, K.-R. Peng, R.-Y. Chang, T.-L. Yu and T.-C. Ong, TSMC, Hsin-Chu, Taiwan, ROC

Session 7 – Advances in Embedded Memory

Grand Caribbean Ballroom III
Monday Afternoon, May 13

Chair: Sreedhar Natarajan Co-Chair: Cormac O'Connell

This session describes novel memory architectures including 1T capacitor-less DRAM, molecular memory, and low-power sequential-access memory. Also featured are ROM-compression algorithms for continuous data and self-adaptive FLASH programming.

2:00 pm **Introduction**

2:05 pm 7-1 **A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs,** P. Fazan*·**, S. Okhonin**, M. Nagoga** and J.-M. Sallese**, *Innovative Silicon Solutions, Le Landeron, Switzerland and **Swiss Federal Institute of Technology, Lausanne, Switzerland

2:30 pm 7-2 **An Interpolating Sense Circuit for Molecular Memory,** Y. Nishida and W. Liu, North Carolina State University, Raleigh, NC

2:55 pm 7-3 **A 16kb 1T1C FeRAM Testchip Using Current-Based Reference Scheme,** J. Siu, Y. Eslami, A. Sheikholeslami, P. Gulak, T. Endo* and S. Kawashima*, University of Toronto, Toronto, ON, Canada and *Fujitsu Laboratories, Ltd., Atsugi, Japan

3:20 pm **Break**

3:35 pm 7-4 **Low-Power Sequential Access Memory Design,** J.-S. Moon, W. Athas*, P. Beerel and J. Draper**, University of Southern California, Los Angeles, CA, *Apple Computer, Inc., Cupertino, CA and **University of Southern California, Marina del Rey, CA

4:00 pm 7-5 **A Self Adaptive Programming Method with 5 mV Accuracy for Multi-level Storage in FLASH,** L. Engh, A. Kordesch and C.-M. Liu, Winbond Electronics Corporation America, San Jose, CA

4:25 pm 7-6 **A ROM Compression Method for Continuous Data,** B.-D. Yang and L.-S. Kim, KAIST, Daejeon, Korea

Session 8 – Low Power Circuits and I/O

Grand Caribbean Ballroom IV
Monday Afternoon, May 13

Chair: Takayasu Sakurai Co-Chair: Thaddeus Gabara

Microprocessors, filter, and flip-flop designers will appreciate the low-power and high-performance solutions discussed in this session, which also describes AC coupling for high-density I/O circuits.

2:00 pm **Introduction**

2:05 pm 8-1 **High-performance and Low-power Challenges for Sub-70nm Microprocessor Circuits (Invited),** R. Krishnamurthy, A. Alvandpour, V. De and S. Borkar, Intel Corporation, Hillsboro, OR

2:55 pm 8-2 **A New Reduced Clock-Swing Flip-Flop: NAND-type Keeper Flip-Flop (NDKFF),** M. Tokumasu, H. Fujii, M. Ohta, T. Fuse and A. Kameyama, Toshiba Corporation, Kanagawa, Japan

3:20 pm **Break**

3:35 pm 8-3 **4 Gbps High-Density AC Coupled Interconnection (Invited),** S. Mick, J. Wilson and P. Franzon, North Carolina State University, Raleigh, NC

4:25 pm 8-4 **A Low Power Adaptive Filter Using Dynamic Reduced 2's-Complement Representation,** Z. Yu, M.-L. Yu*, K. Azadet* and A.N. Willson, University of California, Los Angeles, CA and *Agere Sys., Holmdel, NJ

Session 9 – Application Specific Signal Processors

Grand Caribbean Ballroom I
Tuesday Morning, May 14

Chair: Ram Krishnamurthy Co-Chair: Masataka Matsui

High-performance signal processing forms the core of many real-world applications. This session describes advances shown in encryption, forward error correction (FEC), imaging, and MPEG2.

8:30 am **Introduction**

8:35 am 9-1 **A 2.29 Gbits/sec, 56 mW Non-Pipelined Rijndael AES Encryption IC in a 1.8V, 0.18 µm CMOS Technology,** H. Kuo, I. Verbauwhede and P. Schaumont, University of California, Los Angeles, CA

9:00 am 9-2 **Burst Mode: A New Acceleration Mode for 128-bit Block Ciphers,** Y. Mitsuyama*, Z. Andales*,***, T. Onoye** and I. Shirakawa*, *Osaka University, Osaka, Japan, **Kyoto University, Kyoto, Japan and ***University of the Philippines at Los Banos, Laguna, Philippines

9:25 am 9-3 **Single-chip FEC Codec LSI using Iterative CSOC Decoder for 10 Gb/s Long-haul Optical Transmission Systems,** K. Seki, K. Mikami, M. Baba, A. Katayama*, H. Tanaka, Y. Hara, M. Kobayashi and N. Okada, NEC Corp., Kanagawa Japan and *NEC

Engineering, Ltd., Kanagawa, Japan

9:50 am **Break**

10:05 am 9-4 **A Vector DSP for Imaging,** J. Redford, B. Bersack, M. Moniz, F. Huettig and D. Fitzgerald, ChipWrights Inc., Newton, MA

10:30 am 9-5 **A Single-Chip MPEG-2 Codec Based on Customizable Media Microprocessor,** S. Ishiwata, T. Yamakage, Y. Tsuboi, T. Shimazawa, T. Kitazawa, S. Michinaka, K. Yahagi, H. Takeda, A. Oue, T. Kodama, N. Matsumoto, T. Kamei, T. Miyamori, G. Ootomo and M. Matsui, Toshiba Corporation, Kanagawa, Japan

10:55 am 9-6 **An Ultra Low Power, Realtime MPEG2 MP@HL Motion Estimation Processor Core with SIMD Datapath Architecture Optimized for Gradient Descent Search Algorithm,** M. Miyama, O. Tooyama, N. Takamatsu, T. Kodake, K. Nakamura, A. Kato, J. Miyakoshi, K. Hashimoto, S. Komatsu*, M. Yagi**, M. Morimoto**, K. Taki** and M. Yoshimoto, Kanazawa University, Kanazawa, Japan, *The University of Tokyo, Japan and **Kobe University, Japan

11:20 am 9-7 **A Low-power Highly-Integrated MPEG1/2 Audio Layer 3 (MP3) Decoder for CD-based Systems,** H. Cloetens, R. Hahn, B. Hooser and F. Lenke, Motorola, Munich, Germany

Session 10 – Oversampled Data Converters

Grand Caribbean Ballroom II
Tuesday Morning, May 14

Chair: Pat Rakers Co-Chair: Douglas Garrity

This session comprises papers describing low-power and multi-bit techniques for the development of oversampled analog-to-digital converters for lowpass and bandpass applications.

8:30 am **Introduction**

8:35 am 10-1 **Delta-Sigma Data Converters for Wireless Transceivers,** a special Educational Session by Ian Galton, University of California

9:25 am 10-2 **An 80MHZ 8th-Order Bandpass $\Delta\Sigma$-Modulator with a 75DB SNDR for IS-95,** T. Salo, S. Lindfors* and K. Halonen, Helsinki University of Technology, Hut, Finland and *Aalborg University, Aalborg, Denmark

9:50 am **Break**

10:05 am 10-3 **Digital Techniques for Improved $\Delta\Sigma$ Data Conversion (Invited),** J. Silva, X. Wang, P. Kiss, U. Moon and G. Temes, Oregon State University, Corvallis, OR

10:55 am 10-4 **A Multi-Bit Sigma-Delta ADC for Multi-Mode Receivers,** M. Miller and C. Petrie, Motorola, Schaumburg, IL

11:20 am 10-5 **Sub-Sampling Sigma-Delta Modulator for Baseband Processing,** S. Chandrasekaran and W. Black, Iowa State University, Ames, IA

Session 11 – Modeling for RF Design

Grand Caribbean Ballroom III
Tuesday Morning, May 14

Chair: Larry Nagel Co-Chair: Colin McAndrew

Key issues in RF design are noise and integrated inductors. This session covers RF noise, analysis of the effect of noise on oscillators, and improved models and designs for on-chip inductors.

8:30 am **Introduction**

8:35 am 11-1 **MOSFET Modeling for Low Noise, RF Circuit Design (Invited),** M.J. Deen, C.-H. Chen and Y. Cheng*, McMaster University, Hamilton, ON, Canada and *Conexant Systems, Newport Beach, CA

9:25 am 11-2 **Modeling the Gate-Related High-Frequency and Noise Characteristics of Deep-Submicron MOSFETs,** R. Kraus and G. Knoblinger*, University of Bundeswehr Munich, Neubiberg, Germany and *Infineon Technologies AG, Munich, Germany

9:50 am **Break**

10:05 am 11-3 **Virtual Damping in Oscillators,** D. Ham and A. Hajimiri, California Institute of Technology, Pasadena, CA

10:30 am 11-4 **Frequency-Independent Equivalent Circuit Model for On-Chip Spiral Inductors,** Y. Cao, R. Groves*, N. Zamdmer*, J.-O. Plouchart*, R. Wachnik*, X. Huang, T.-J. King and C. Hu, University of California, Berkeley, CA, and *IBM Microelectronics Divison, Hopewell Junction, NY

10:55 am 11-5 **Modeling and Optimization of Inductors with Patterned Ground Shields for a High Performance Fully Integrated Switched Tuning VCO,** F. Rotella and J. Zachan, Conexant Systems, Inc., Newport Beach, CA

Session 12 – Receiver Architectures

Grand Caribbean Ballroom IV
Tuesday Morning, May 14

Chair: Oliver Werther Co-Chair: Francesco Svelto

Highly integrated direct, dual and low IF receiver architectures used in wireless applications are discussed in this session. Also covered are techniques to improve key parameters (e.g., image rejection and 2^{nd} -order nonlinearity).

8:30 am **Introduction**

8:35 am 12-1 **Dual Mixer Downconversion Architecture Using Complex Mixing Signals: Enabling Solutions for Software Defined Radios (Invited),** T. Manku, C. Snyder, M. Ting, Y. Ling, J. Khajehpour, B. Kung and L. Wong, SiRiFIC Wireless Corporation, Waterloo, ON, Canada

9:25 am **A Quadrature Direct Digital Downconverter,** P.

12-2 Vancorenland, P. Coppejans, W. De Cock, M. Steyaert and Katholieke Universiteit Leuven, Heverlee, Belgium

9:50 am **Break**

10:05 am 12-3 **A Direct Conversion Receiver for the 3G WCDMA Standard,** R. Gharpurey, N. Yanduru, F. Dantoni, P. Litmanen, G. Sirna, T. Mayhugh, C. Lin, I. Deng, P. Fontaine and F. Lin, Texas Instruments, Inc., Dallas, TX

10:30 am 12-4 **Analysis and Optimization of IIP2 in CMOS Direct Down-Converters,** D. Manstretta and F. Svelto, University of Pavia, Pavia, Italy

10:55 am 12-5 **A Monolithic CMOS Low-IF Bluetooth Receiver,** W. Sheng, B. Xia, A. Emira, C. Xin, S.T. Moon, A. Valero-Lopez and E. Sanchez-Sinencio, Texas A&M University, College Station, TX

11:20 am 12-6 **A Self-Calibration Technique for Mismatches in Image-Reject Receivers,** M. Elmala and S. Embabi*, Texas A&M University, College Station, TX and *Texas Instruments, Inc., Dallas, TX

Session 13 – Sensors and Imaging

Grand Caribbean Ballroom I
Tuesday Afternoon, May 14

Chair: Tadahiro Kuroda Co-Chair: John Wright

Real-world interfaces present significant design challenges. This session explores sensor and display interfaces.

2:00 pm **Introduction**

2:05 pm 13-1 **A 402-Output TFT-LCD Driver IC with Power-Controlling Function by Selecting Number of Colors,** T. Itakura, H. Minamizaki, T. Saito and T. Kuroda, Toshiba Corporation, Kawasaki, Japan

2:30 pm 13-2 **A 500-dpi Cellular-Logic Processing Array for Fingerprint-Image Enhancement and Verification,** K. Fujii, M. Nakanishi, S. Shigematsu, H. Morimura, T. Hatano, N. Ikeda, T. Shimamura, Y. Okazaki and H. Kyuragi, NTT Laboratories, Kanagawa, Japan

2:55 pm 13-3 **High Dynamic Range CMOS Image Sensor with Conditional Reset,** S.-H. Yang and K.-R. Cho, Chungbuk National University, Chungbuk, Korea

3:20 pm 13-4 **SOI Hall Effect Sensor Operating up to 270°C,** L. Portmann, H. Ballan* and M. Declercq, Swiss Federal Institute of Technology, Lausanne, Switzerland and *Eurmicros GmbH, Lausanne, Switzerland

Session 14 – Enhancement Techniques for Integrated Passives

Grand Caribbean Ballroom II
Tuesday Afternoon, May 14

Chair: Jean-Baptiste Begueret Co-Chair: Trudy Stetzler

Non-ideal behavior and parasitic effects of passive integrated components, especially inductors, are often a limiting factor in RF design. This session discusses several techniques and advanced models to address these problems.

2:00 pm **Introduction**

2:05 pm 14-1 **On-Chip RF Spiral Inductors and Bandpass Filters Using Active Magnetic Energy Recovery,** Y.-C. Wu and M.F. Chang, University of California, Los Angeles, CA

2:30 pm 14-2 **A 0.18µm CMOS, High Q-Enhanced Bandpass Filter with Direct Digital Tuning,** C. DeVries and R. Mason, Carleton University, Ottawa, ON, Canada

2:55 pm 14-3 **A 2.1GHz 1.3V 5mW Programmable Q-Enhancement LC Bandpass Biquad in 0.35µm CMOS,** F. Dülger, E. Sánchez-Sinencio and J. Silva-Martínez, Texas A&M University, College Station, TX

3:20 pm 14-4 **A 2GHz Quadrature Hybrid Implemented in CMOS Technology,** R. Frye, S. Kapur and R. Melville, Agere Systems, Murray Hill, NJ

Session 15 – Afternoon Panel Session

Grand Caribbean Ballroom III
Tuesday, May 14, 2:00 pm - 4:00 pm

"Design Challenges in Wireless LANs"

Organizers: **David Rich**, Lafayette College
Jim Lipman, TechOnLine

Moderator: **Jim Lipman**, TechOnLine

Panelists:

Johan Akesson
Ericsson Technology

Reza Rofougaran
Broadcom

Eric Hansen
Innovative Wireless Technologies

David Su
Atheros Communications

Cormac O'Connell
SiGe Semiconductor Inc.

Bruce Tuch
Agere Systems

Bluetooth and 802.11 wireless network systems have become commercial realities, with products currently shipping. However, the designer's job is far from finished. Both standards are evolving to higher data rates and lower power consumption. Furthermore, for products to ship in significant volume designers need to reduce the cost of building wireless LANs.

Come hear experts summarize the current state and next generation of the WLAN standards. Our panelists will discuss whether 802.11 and Bluetooth are complementary or competitive technologies. Designers who have developed chips for these systems will discuss issues involved in designing custom ICs for low-cost wireless LAN applications. These issues will include:

- The process technology required for building competitive systems. Can designs be completed in standard CMOS or do you need specialized technologies such as SOI and SiGe bipolar?
- The optimal system architectures for low-cost realizations of wireless LANs.
- The potential of using similar architectures to implement both a Bluetooth and 802.11 system.
- The level of integration that can be achieved between the RF and baseband digital processor along with the ability to move RF passive components from the PC board to the chip.
- The importance of involving circuit designers in the standard-setting process to insure low-cost system realization of wireless LANs.

Session 16 – Evening Panel Session
Grand Caribbean Ballroom III
Tuesday, May 14, 8:00 pm

"Will the Next Great Killer Technology Application Please Stand Up!!"

Organizers: **Brian, Fitzgerald,** ChipWrights, Inc.
Rakesh Kumar, Technology Connexions

Moderator: **Rakesh, Kumar,** Technology Connexions

Panelists:
Brian Fitzgerald, CEO
ChipWrights, Inc.

David Bursky, Editor
EDN Magizine

Doug Palmer, CTO
Path One Networks

Robert Guernsey, Director of
Silicon Technology Strategy
IBM Microelectronics

Ali Hajimiri
CalTech

Everyone talks about the next 'killer app', the thing that will change the face of technology and in many ways, the direction of our careers. Or has it been the other way around? That is to say; the technology facilitates the killer app, thereby creating the next great leap in high tech.

What technologies on the drawing board have the potential to fundamentally change our industry and, ultimately, obsolete the very semiconductor electronics in which we are all expert. Will we feel a 'rift in the force", a killer technology that disrupts our very livelihood , or will the progress be 'more of the same'?

And how about the customers, the consumers of new technology? What problem do they really want us to solve for them? Without them, isn't a new technology only going to become the latest 'technological monument' to its inventor and nothing more?

Who will lead the charge in the new millennium? Will it be the industry leaders with their R & D? Or will it be a few of the many masses of high-tech startups that will rise to the top. And how about the economy of this past year; is that affecting innovation?

Come listen to what a panel of experts have to say. The panelists are a blend of people with varied backgrounds from the semiconductor industry who will try to shed light on this important issue.

What are the opinions of the panel members? What is your opinion?

Session 17 – Evening Panel Session

Grand Caribbean Ballroom IV
Tuesday, May 14, 8:00 pm

"Can Scaling Continue at the Same Rate Below 0.1µm? What is the End of CMOS…and What is Next?"

Organizers: **Rich Liu,** Macronix International Ltd.
Sreedhar Natarajan, Texas Instruments Inc.

Moderator: **Sreedhar Natarajan,** Texas Instruments Inc.

Panelists:

Shekhar Borkar, Director of Circuit Research Lab, Intel Corporation

Seiichiro Kawamura, Executive Director, AIST

Dr. Dennis Buss, VP of Silicon Technology Dev., Texas Instruments

Jagdish Pathak, President Sub Micron Circuits Inc.

Steve Hillenius, Director of Device & Module R&D, Agere Systems

Dr. Krishna Sarawat, Professor, Stanford University

In the last decade we have seen an acceleration in the rate of scaling. While the need for improving performance and lowering the cost per function continue to be strong driving forces, there are many technological and application challenges that threaten to disrupt this scaling curve. Direct-tunneling gate leakage current will start dominating the total standby current in SRAM and interconnects are not going to scale down with technology. Will these compromise future low-power and high-performance applications? Feature sizes are already well below lithography wavelengths--will new lithography tools and photoresist development schedules meet the future challenges? The cost of masks is already escalating and will become prohibitive for ASICs in the future. How will this change the shape of the custom IC market? The power supply voltage is scaling toward a sub-one-volt regime--how will this affect the mixed-signal devices? Finally, will the prohibitive cost of 300-mm fabs and technology development drive toward more consolidation and foundry-based process and manufacturing? Will this change the landscape from a score of large integrated IC houses to numerous smaller fabless design houses?

Session 18 – SoC Design Methodologies

Grand Caribbean Ballroom I
Wednesday Morning, May 15

Chair: Michele Taliercio Co-Chair: Thomas Zimmermann

This session discusses IP, Bus, EMI, and packaging constraints which impact SoC realization. Complementing this are two real-life applications covering voice telephony and MP3.

8:30 am **Introduction**

8:35 am 18-1 **A Design Methodology for Low EMI-Noise Microprocessor with Accurate Estimation-Reduction-Verification,** H. Tsujikawa, K. Shimazaki, S. Hirano, M. Ohki, T. Yoneda and H. Benno, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan

9:00 am 18-2 **Design Integration, DFT, and Verification Methodology for an MPEG 1/2 Audio Layer 3 (MP3) SoC Device,** B. Birkl, B. Hooser, M. Janssens, F. Lenke and V. Vorisek, Motorola, Munich, Germany

9:25 am **18-3** **A Design Methodology for Integrating IP into SoC Systems,** P. Coussy, A Baganne and E. Martin, Université de Bretagne Sud, Lorient, France

9:50 am **Break**

10:05 am **18-4** **A Voice Processing and Control Module for Cable Telephony Applications,** J. Nabicht, J. Pitz, P. Siniscalchi, C. Betty, S. Maggiotto, D. Richardson, S. DeSoto, S. Sridharan, S. Vemulapalli, K. Downs, D. Gata, A. Dweik, D. Guidry, K. Muskoff, B. Beckham and G. Westphal, Texas Instruments, Inc., Dallas, TX

10:30 am **18-5** **NECoBus: A High-End SoC Bus with a Portable and Low-Latency Wrapper-Based Interface Mechanism,** K. Anjo, A. Okamura, T. Kajiwara*, N. Mizushima, M. Omori and Y. Kuroda, NEC Corporation and *NEC Micro Systems Ltd., Kanagawa, Japan

10:55 am **18-6** **System-on-Chip (SoC) Requires IC & Package Co-Design and Co-Verification,** A. Fontanelli, S. Arrigoni, D. Raccagni and M. Rosin, STMicroelectronics, Agrate Brianza, Italy

Session 19 – Analog Techniques

Grand Caribbean Ballroom II
Wednesday Morning, May 15

Chair: David Allee Co-Chair: Tatsuji Matsuura

This session covers significant advances in compensation methods for multistage amplifiers, and genetic algorithms and optimization techniques for improving filter performance.

8:30 am **Introduction**

8:35 am **19-1** **Active-Feedback Frequency Compensation for Low-Power Multi-Stage Amplifiers,** H. Lee and P. Mok, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong

9:00 am **19-2** **Nested Feed-Forward Gm-Stage and Nulling Resistor Plus Nested-Miller Compensation for Multistage Amplifiers,** X. Peng and W. Sansen, Katholieke Universiteit, Leuven, Belgium

9:25 am **19-3** **Three Stage Amplifier with Positive Feedback Compensation Scheme,** J. Ramos and M. Steyaert, Katholieke Universiteit, Leuven, Belgium

9:50 am **Break**

10:05 am **19-4** **A High Gain CMOS Operational Amplifier with Negative Conductance Gain Enhancement,** J. Yan and R. Geiger, Iowa State University, Ames, IA

10:30 am **19-5** **A Noninvasive Channel-Select Filter for a CMOS Bluetooth Receiver,** A. Zolfaghari and B. Razavi, University of California, Los Angeles, CA

10:55 am **19-6** **An AI-Calibrated IF Filter: A Yield Enhancement Method with Area and Power Dissipation Reductions,** M. Murakawa, T. Adachi*, Y. Nino*, E. Takahashi, Y. Kasai, K. Takasuka* and T. Higuchi, AIST, Japan and *Asahi Kasei Microsystems, Japan

11:20 am 19-7 **A 1.2Gbps SOI-BiCMOS Write Driver for Hard Disk Drives,** H. Yoshizawa, Y. Kobayashi, M. Yoshinaga, Y. Ookuma, K. Maio and K. Irikura*, Hitachi, Ltd., Tokyo, Japan and *Hitachi ULSI System Co., Ltd., Tokyo, Japan

Session 20 – Multi Gigabit Systems and Circuits

Grand Caribbean Ballroom III
Wednesday Morning, May 15

Chair: Jafar Savoj Co-Chair: Johan Van Der Tang

Addressing the need for high data-rate networks, this session focuses on circuits and systems for multi-gigabit optical and backplane communications.

8:30 am **Introduction**

8:35 am 20-1 **A 10Gbase Ethernet Transceiver (LAN PHY) in a 1.8V, 0.18µm SOI/CMOS Technology,** T. Yoshimura, K. Ueda, J. Takasoh, Y. Wada, T. Oka, H. Kondoh, O. Chiba, Y. Azekawa and M. Ishiwaki, Mitsubishi Electric Corporation, Itami, Japan

9:00 am 20-2 **A 2.5 Gbps CMOS Optical Receiver Analog Front-End,** W.-Z. Chen and C.-H. Lu, National Central University, Chung-Li, Taiwan, ROC

9:25 am 20-3 **An Adaptive PAM-4 5Gb/s Backplane Transceiver in 0.25µm CMOS,** J. Sonntag, J. Stonick, J. Gorecki, B. Beale, B. Check, X.-M. Gong, J. Guiliano, K. Lee, B. Lefferts, D. Martin, U.-K. Moon, A. Sengir, S. Titus, G.-Y. Wei, D. Weinlader and Y. Yang, Accelerant Networks, Inc., Beaverton, OR

9:50 am **Break**

10:05 am 20-4 **The Role of Monolithic Transmission Lines in High-Speed Integrated Circuits (Invited),** B. Razavi, University of California, Los Angeles, CA

10:55 am 20-5 **Single Reference Continuous Rate Clock and Data Recovery from 30MBit/s to 3.2GBit/s,** J.-P. Frambach, R. Heijna and R. Krösschell, Philips Semiconductors, Nijmegen, The Netherlands

Session 21 – DSP for Communications

Grand Caribbean Ballroom IV
Wednesday Morning, May 15

Chair: Elliot Gould Co-Chair: Bryan Ackland

Designers need high-performance, low-power DSP to build next-generation, high-speed data-communication systems. This session describes new architectures for 3G terminals and basestations, along with a high-performance crossbar switch.

8:30 am **Introduction**

8:35 am 21-1 **Integrated Circuits for 3GPP Mobile Wireless Systems (Invited),** C. Nichol and M. Cooke, Bell Labs, Lucent Technologies, North Ryde, Australia

9:25 am **A 80 Mb/s Low-power Scalable Turbo Codec Core,**
21-2 A. Giulietti, B. Bougard, V. Derudder, S. Dupont, J.-W. Weijers and L. Van der Perre, IMEC, Leuven, Belgium

9:50 am **Break**

10:05 am **600Mhz DSP for Baseband Processing in 3G Base**
21-3 **Stations,** T. Wolf, D. Hocevar, A. Gatherer, P. Geremia* and A. Laine*, Texas Instruments, Inc., Dallas, TX and *Texas Instruments, Inc., Nice, France

10:30 am **A Low-Power W-CDMA Demodulator using**
21-4 **Specially-Designed Micro-DSPs,** H. Igura, M. Hirata*, J. Yamada, M. Yamashina and S. Ono*, NEC Corporation, Kanagawa, Japan and *NEC Networks, Yokohama, Japan

10:55 am **Piece-wise Parabolic Interpolation for Direct Digital**
21-5 **Frequency Synthesis,** A. Eltawil and B. Daneshrad, University of California, Los Angeles, CA

11:20 am **FLEXBAR: A Crossbar Switching Fabric with**
21-6 **Improved Performance and Utilization,** J. Chang, S. Ravi* and A. Raghunathan*, Stanford University, Palo Alto, CA and *NEC USA, Inc., Princeton, NJ

Session 22 – Wireless Networking

Grand Caribbean Ballroom I
Wednesday Afternoon, May 15

Chair: Earl McCune Co-Chair: Andrea Boni

This session addresses practical issues including an invited paper on ESD design for RF integrated circuits. Additional topics include LNA, signal generation, and demodulation.

1:30 pm **Introduction**

1:35 pm **ESD Protection Design for RF Integrated Circuits:**
22-1 **New Challenges (Invited),** A.Z. Wang, H.G. Feng, R.Y. Zhan, G. Chen and Q. Wu, Illinois Institute of Technology, Chicago, IL

2:25 pm **A 1V 0.9dB NF Low Noise Amplifier for 5-6GHz**
22-2 **WLAN in 0.18µm CMOS,** D. Cassan and J. Long, University of Toronto, Toronto, ON, Canada

2:50 pm **A Low-Voltage Multi-GHz VCO with 58% Tuning**
22-3 **Range in SOI CMOS,** N. Fong, J.-O. Plouchart*, N. Zamdmer**, D. Liu*, L. Wagner**, C. Plett and G. Tarr, Carleton University, Ottawa, ON, Canada, *IBM T.J. Watson Research Center, Yorktown Heights, NY and **IBM Microelectronics SRDC, Hopewell Junction, NY

3:15 pm **Break**

3:30 pm **A 1.8GHz CMOS Fractional-N Frequency**
22-4 **Synthesizer with Randomized Multi-Phase VCO,** C.-H. Heng and B.-S. Song*, University of Illinois, Urbana, IL and *University of California, San Diego, La Jolla, CA

3:55 pm **A 2MHz GFSK IQ Receiver for Bluetooth with DC-**
22-5 **Tolerant Bit Slicer,** B.-S. Song, T. Cho*, D. Kang* and S. Dow*, University of California, San Diego, La Jolla, CA and *Wireless Interface Technologies, Inc., San Diego, CA

Session 23 – Nyquist Converters and Techniques

Grand Caribbean Ballroom II
Wednesday Afternoon, May 15

Chair: David Nairn Co-Chair: Richard Carley

Four papers cover state-of-the-art ADCs for low-voltage performance. In addition, two papers address mismatch issues and one discusses bandgap performance.

1:30 pm **Introduction**

1:35 pm
23-1 **A 1.8V Fully Embedded 10b 160MS/s Two-Step ADC in 0.18µm CMOS,** M. Clara, A. Weisbauer and F. Kuttner, Infineon Technologies AG, Villach, Austria

2:00 pm
23-2 **A 2.5V 10b 120 MSample/s CMOS Pipelined ADC with High SFDR,** S.-M. Yoo, T.-H. Oh, J.-W. Moon, S.-H. Lee and U.-K. Moon*, Sogang University, Seoul, Korea and *Oregon State University, Corvallis, OR

2:25 pm
23-3 **A 8-bit 200 MS/s Interpolating/Averaging CMOS A/D Converter,** J. Vandenbussche, K. Uyttenhove, E. Lauwers, M. Steyaert and G. Gielen, Katholieke Universiteit Leuven, Heverlee, Belgium

2:50 pm
23-4 **Understanding MOSFET Mismatch for Analog Design,** P.G. Drennan and C.C. McAndrew, Motorola, Inc., Tempe, AZ

3:15 pm **Break**

3:30 pm
23-5 **Spatial Averaging and Ordering in Matched Element Arrays,** K. Krishna, W. Bright, D. Dye*, K. Muhammad and Y. Hu, Texas Instruments, Inc., Dallas, TX and *Database Drafting, Inc., Dallas, TX

3:55 pm
23-6 **A 2-V 23-µA 5.3-ppm/°C 4th-Order Curvature-Compensated CMOS Bandgap Reference,** K. Leung, P. Mok and C. Leung, The Hong Kong University of Science and Technology, Hong Kong, China

4:20 pm
23-7 **Low-Voltage Pipelined ADC Using Opamp-Reset Switching Technique,** D.-Y. Chang, L. Wu* and U.-K. Moon, Oregon State University, Corvallis, OR and *Marvell, Sunnyvale, CA

Session 24 – Directions in Process and Integration

Grand Caribbean Ballroom III
Wednesday Afternoon, May 15

Chair: David Sunderland Co-Chair: Rich Liu

This session presents papers related to strategic directions in semiconductor process technology and integration, including challenges of and alternatives to CMOS scaling. Circuit designers will find these tutorials valuable in planning future products.

1:30 pm **Introduction**

1:35 pm 24-1 **Technology Trends and Challenges for CMOS/System LSIs for the Next 10-15 Years (Invited),** S. Kawamura, Advanced Semiconductor Research Center, Tsukuba, Japan

2:25 pm 24-2 **Application-Dependent Scaling Tradeoffs and Optimization in the SoC Era,** C. Diaz, M.-C. Chang, T. Ong and J. Sun, TSMC, Taiwan, ROC

2:50 pm 24-3 **Modularized Low Temperature LNO/PZT/LNO Ferroelectric Capacitor-Over-Interconnect (COI) FeRAM for Advanced SOC (ASOC) Application,** S. Lung, D. Lin, S. Chen, G. Weng, C. Liu*, S. Lai, C. Tsai, T. Wu* and R. Liu, Macronix International, Hsinchu, Taiwan, ROC and *National Tsing-Hua University, Hsinchu, Taiwan, ROC

3:15 pm **Break**

3:30 pm 24-4 **High Speed, Low Power, Optoelectronic InP-Based HBT Integrated Circuits (Invited),** M. Sokolich, HRL Laboratories LLC, Malibu, CA

4:20 pm 24-5 **Sea of Leads (SoL) Characterization and Design for Compatibility with Board-Level Optical Waveguide Interconnection,** M. Bakir, H. Reed, A. Mule, P. Kohl, K. Martin and J. Meindl, Georgia Institute of Technology, Atlanta, GA

Session 25 – Modeling for Signal Integrity

Grand Caribbean Ballroom IV
Wednesday Afternoon, May 15

Chair: Steffen Rochel Co-Chair: Jamil Kawa

This session focuses on modeling and measurement techniques aimed at characterizing signal integrity in circuits. Presentations cover IR drop, substrate noise, and lossy interconnect.

1:30 pm **Introduction**

1:35 pm 25-1 **A Comprehensive Geometry-Dependent Macro-model for Substrate Noise Coupling in Heavily Doped CMOS Processes,** D. Öziş, T. Fiez and K. Mayaram, Oregon State University, Corvallis, OR

2:00 pm 25-2 **Modeling Substrate Noise Generation in CMOS Digital Integrated Circuits,** M. Nagata, T. Morie and A. Iwata, Hiroshima University, Higashi-Hiroshima, Japan

2:25 pm 25-3 **The Effect of Supply and Substrate Noise on Jitter in Ring Oscillators,** N. Barton, D. Öziş, T. Fiez and K. Mayaram, Oregon State University, Corvallis, OR

2:50 pm 25-4 **Passive Closed-Form Time-Domain Macromodels for On-Chip Distributed RC Interconnects,** A. Dounavis, R. Achar and M. Nakhla, Carleton University, Ottawa, ON, Canada

3:15 pm **Break**

3:30 pm 25-5 **Delay and Power Model for Current-mode Signaling in Deep Submicron Global Interconnects,** R. Bashirullah, W. Liu and R. Cavin*, North Carolina State University, Raleigh, NC and *Semiconductor Research Corporation, Research Triangle Park, NC

3:55 pm 25-6 **A Comprehensive Study of Energy Dissipation in Lossy Transmission Lines Driven by CMOS Inverters,** P. Heydari, S. Abbaspour* and M. Pedram*, University of California, Irvine, CA and *University of Southern California, Los Angeles, CA

4:20 pm 25-7 **Measurement Results of On-Chip IR-Drop,** K. Kobayashi, J. Yamaguchi and H. Onodera, Kyoto University, Kyoto, Japan

GENERAL INFORMATION

LOCATION Caribe Royale Resort Suites
8101 World Center Drive
Orlando, FL 32821
(407) 238-8000
www.cariberoyale.com

REGISTRATION

Payment of the Technical Session registration fee entitles the registrant to entrance to all Technical Sessions, the Exhibit Hall, Exhibitor Preview Sessions, Exhibitor's Reception, Tuesday Happy Hour and one copy of the Conference Proceedings. Single day registration entitles the registrant to that day's events and one copy of the Conference Proceedings. Technical session registration does not include entrance to the Educational Sessions.

Payment of the Educational Sessions registration fee entitles the registrant to entrance to the Educational Sessions, lunch on Sunday, and one copy of the Educational Sessions Workbook. Educational Session registration does not include entrance to the Technical Sessions, Exhibits or a copy of the Conference Proceedings.

To register for the conference fill out the registration form in the center of this booklet and fax or mail the form and payment to be received by **MAY 1**.

Advance registration forms MUST be received by Wednesday, May 1
After that date you must register onsite at the conference.

Make checks payable to CICC 2002 in US dollars on a US bank. We also accept **VISA** and **MasterCard only**. CICC is not able to accept American Express charges. Requests for cancellations must be received by May 8, 2002 to qualify for a refund.

The Registration Center, located in the Grand Caribbean Foyer, will be open as follows:

Registration for Educational Sessions Only

Sunday, May 12	7:00 am - 2:00 pm

Registration for Technical Sessions

Sunday, May 12	2:00 pm - 5:00 pm
Monday, May 13	7:30 am - 5:00 pm
Tuesday, May 14	8:00 am - 5:00 pm
Wednesday, May 15	8:00 am - 3:00 pm

HOTEL ACCOMMODATIONS

The Caribe Royale Resort Suites is located at 8101 World Center Drive, Orlando, FL. The Caribe Royale is an "all suites" hotel. Every room has a bedroom and a living/dining room. Parking at the Hotel is free. The hotel is only 1.5 miles from the Walt Disney World Resorts®, features five restaurants, offers a complimentary Full American Breakfast Buffet daily and includes an outdoor swimming pool with a waterslide and a hot tub.

Room rates are $156/Queen Double, $166/Standard King, $176/King Deluxe, $281/Executive Suite, $281/Villa. To make hotel reservations call the hotel at (407) 238-8000 or fill out the Housing Reservation Form and mail or fax (407)-238-8088 it to the Caribe Royale by April 17, 2002 to qualify for a room at our special rate. Reservations can also be made online at www.cariberoyale.com

Use the password "IEEE" for the CICC registration rate.

You will receive a reservation confirmation directly from the hotel. It is the responsibility of each participant to make changes or cancellations directly with the hotel no later than 72 hours prior to scheduled arrival. No refunds will be given by the hotel for changes or cancellations with less than 72 hours notification.

EDUCATIONAL SESSIONS

On Sunday, May 12, the CICC sponsors three Educational Sessions. These Sessions are:

1. Advanced RF: From Devices to Systems
2. Advanced Data Converter Design and Test Techniques
3. High-Performance & Low-Voltage Design Challenges & Techniques

To register, complete the Advance Registration Form for receipt by **May 1**

EXHIBITORS' RECEPTION

Monday Evening, May 13, 5:30 pm - 8:00 pm
Royal Palms I & II

The CICC social event this year is an Exhibitors' Reception sponsored by the CICC 2002 Exhibits Committee, held in the Exhibit Hall. All conference attendees are cordially invited! Enjoy the evening by browsing around the exhibit area, talking with the exhibitors' staff, seeing old friends and meeting new ones. Join us at the Exhibitors' Reception to celebrate!

CICC LUNCHEON

Tuesday, May 14, 12:00 pm - 1:30 pm
Royal Palm III

Science in Space:
Accomplishments and Promises in Low-Gravity
Dr. Eugene Trinh, NASA

Ground-based short-duration capabilities, the Space Shuttle, and the International Space Station facilities have provided low-gravity research platforms on which to conduct unique scientific and technology development investigations. Using gravitational acceleration level as a parameter, scientists in the US and around the world have been able to tackle long standing problems which have long defied solution because of the overwhelming masking effect introduced by gravity. Previously obtained results, ongoing on-orbit research, and future program directions will be discussed in such areas as gravitational effects on fluid and transport phenomena, colloidal physics, cellular biotechnology, and fundamental atomic physics.

Born September 14, 1950, in Saigon, Vietnam; Dr. Trinh was raised from the age of two in Paris, France and has lived in the United States since 1968. Currently a resident of Culver City, California, Eugene H. Trinh is Director of the Physical Sciences Research Division in the Biological and Physical Research Enterprise at NASA Headquarters in Washington, DC. Dr. Trinh was one of two science payload specialists on the first United States Microgravity Laboratory (USML-1) Space Shuttle flight. This Spacelab mission was launched on June 25 1992, and it lasted a record 14 days

EVENING PANEL DISCUSSIONS

On Tuesday evening, May 14, beginning at 8:00 pm, the CICC will offer two evening panel discussions on timely issues:

1. Will the Next Great Killer Technology Application Please Stand Up!
2. Can Scaling Continue at the Same Rate Below 0.1µm? What is the End of CMOS…and What is Next?

CONFERENCE PROCEEDINGS

The proceedings contains papers on each presentation. Conference registrants will receive one copy of the Proceedings. Additional copies will be available at the conference registration desk, IEEE member: $60, Non-member: $70. After the conference, order the Proceedings through: Single Copy Sales, IEEE Service Center, 445 Hoes Lanes, Box 1331, Piscataway, NJ, 08855-1331, Customer Service Department (toll free): 800-678-4333. The IEEE catalogue number is 02CH37285.

AUTHOR INTERVIEWS

There will be author interviews each day of the conference immediately following the afternoon sessions in Royal Palm III. This additional forum provides an opportunity for relaxed discussions with your colleagues outside the strict time constrains of the regular sessions.

SPONSOR EVENTS

CICC acknowledges the generous support of our conference sponsors

Accent, The SoC Design Company, for the CD ROM
AMI for the T-Shirts
Cadence Design Systems for the Happy Hour
IBM for the Exhibitors' Reception
Intel Corporation for the Tuesday Morning coffee break
LSI Logic for the Monday Afternoon coffee break
Synopsys for the Tote Bag
Tanner EDA for the Lanyards

CICC SPECIAL PARK DISCOUNTS

DISNEY© Park Hopper Convention Tickets

Save through advance purchase of your Park Hopper Meeting/Convention tickets. These tickets are created just for CICC attendees and are not available at the front gates. See attached Flyer for details.

AIRLINE DISCOUNT PROGRAM

Special discounted airfares for the Custom Integrated Circuits Conference on May 12-15, 2002 in Orlando, Florida have been negotiated by IEEE Global Travel Services. Discounts are as high as 20% off the lowest published airfares with American, Continental, and United Airlines. If Saturday night stays or super-saver airfares are not applicable, deeply discounted airfares are available. Discount code A606098 entitles attendees to receive special rates that have also been negotiated with Avis Rental Car Company.

Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Global Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (800-879-4333); and outside of the US and Canada, call (732) 562-5387. Or, you may visit their on-line travel service web site at www.ieeetravelonline.org. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere.

You may also your fax requirements to the IEEE Global Travel Services at (732) 562-8815. When faxing, please be sure to include your travel dates, departure, and return times, and phone and fax numbers. Or, you may e-mail your request to the department's e-mail address at travel-team@ieee.org. A Travel Counselor will contact you promptly.

AIRPORT TRANSPORTATION

The Caribe Royale is 18 miles from the Orlando International Airport. Mears Shuttle Service provides shuttle service from the airport to the hotel. Arrangements can be made at Ground Transportation or call (407) 839-1570 for more information. The cost is approximately $16.00/one way or $28.00/round-trip. Taxi service is also available from the airport at an estimated cost of $35.00.

BADGES

Badges are required for admittance to all sessions and the exhibit hall. Please wear your badge at all times while attending the conference so that you will not be delayed entry to a session.

FOR FURTHER INFORMATION CONTACT

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