Technical Sessions
Monday, September 20 – Wednesday, September 22, 2010

Session 1 – Keynote Presentation

Monday Morning, September 20
Oak Ballroom

8:15 **Welcome and Opening Remarks**

Awards Presentations

Keynote Speaker Introduction
Jacqueline Snyder, General Chairman

Keynote Presentation
Green Chips: A New Era for the Semiconductor Industry
René Penning de Vries, NXP Semiconductors

The need to minimize the use of fossil fuels to generate electrical energy has been the topic of extensive discussions in the last couple of years. Next to replacement of fossil fuels by alternatives, there is increasing awareness that scrutiny of existing technology and applications can have an immediate, and profound impact. In the presentation the focus will be on the use of high performance mixed signal technologies to minimize energy usage in various applications, such as static and dynamic power of chargers, lighting by CFL and LED technique, as well as various applications in the car.

René Penning de Vries is Senior Vice President and Chief Technology Officer of NXP Semiconductors BV. René is responsible for the product creation processes at NXP, focusing on the key areas of innovation, technology and research. René previously held the position of CTO at Philips Semiconductors prior to the formation of NXP in 2006. He started working for Philips Research in 1984. His career evolved from various technical and managerial roles in CMOS development, into management of platform and design technology as well IP creation. Later, system technology and research were added to his portfolio. During his career, René worked and lived in the US, France and in Singapore, where he was VP of Technology in SSMC.

Session 2 – Advanced Embedded Memories

Monday Morning, September 20
Oak Ballroom

Chair: Vikas Chandra, ARM
Co-Chair: Muhammad Khellah, Intel Corporation

Several new DRAM and SRAM approaches are presented. High speed DRAM, SRAM with Vmin and read/write stability improvement, low energy consumption are discussed.

10:00 **Introduction**

10:05 02-1 **A 45nm SOI Compiled Embedded DRAM with Random Cycle Times Down to 1.3ns (INVITED),** *Mark Jacunski, Darren Anand, Robert Busch, John Fifield, Matthew Lanahan, Paul Lane, Adrian Paparelli, Gary Pomichter, Dale Pontius, Michael Roberge, Stephen Sliva, IBM Systems and Technology Group*

A family of eDRAMs fabricated in 45nm SOI technology is presented. The fast eDRAM has 64 b/BL and achieves a random cycle time of 1.3ns for VDD=1.0V and typical process. The dense eDRAM has 128 b/BL and operates in multi-bank modes up to 1.67GHz.

10:30 02-2 **Improving SRAM Vmin and Yield by Using Variation-aware BTI Stress,** *Jiajing Wang, Satyanand Nalam*, Zhenyu Qi*, Randy Mann*, Mircea Stan*, Benton Calhoun*, Intel Corporation, *University of Virginia*

We propose a novel method that exploits BTI to partially offset variation and thus improve SRAM Vmin and yield. We show correlation between a bitcell's power-up state and its static noise margin. By applying stress with periodic re-power-up, device mismatch can be compensated by BTI induced changes. The proposed method has no extra design and area cost. It can be applied during burn-in test to offset manufacturing variation and/or used during the lifetime of the chip to offset variation from real-time aging and hence continue to improve the margins. Simulations in 45nm show that write, read, and hold Vmin at 6σ can be reduced by 128, 75, and 91 mV, respectively. Measurements from a 16Kb 45nm SRAM demonstrate the improvement of Vmin and yield.

10:55 02-3 **Technology-Circuit Co-Design of Asymmetric SRAM Cells for Read Stability Improvement,** *Jae-Joon Kim, Rahul Rao, Keunwoo Kim, IBM T. J. Watson Research Center*

We present asymmetric SRAM cell design approaches to improve read stability over conventional symmetric SRAM Cell. We show that selective threshold voltage control is more effective than adjusting transistor size for read stability improvement in an asymmetric SRAM cell. We implement statistical DC noise margin monitors and present the hardware measurement data as well as the DC/AC simulation data to support the claims.

11:20 02-4 **7T SRAM Enabling Low-Energy Simultaneous Block Copy,** *Shunsuke Okumura, Shusuke Yoshimoto, Kosuke Yamaguchi, Yohei Nakata, Hiroshi Kawaguchi, Masahiko Yoshimoto, Kobe University*

This paper proposes a 7T SRAM that implements block-level simultaneous copying feature. The proposed SRAM can be used for data transfer between local memories such as checkpoint data storage and transactional memory. In the proposed SRAM, 16-kb data can be copied in 33.3 ns at 1.2V. The proposed scheme reduces energy consumption in copying by 92.7% compared to the conventional read-modify-write manner.

11:45 02-5 **A 32nm 0.5V-Supply Dual-Read 6T SRAM,** *Jente Kuang, Jeremy Schaub, Fadi Gebara, Dieter Wendel, Sudesh Saroop, Tuyet Nguyen, Thomas Fröhnel, Antje Müller, Christopher Durham, Rolf Sautter, Bryan Lloyd, Bryan Robbins, Jürgen Pille, Sani Nassif, Kevin Nowka, IBM*

We report a high-performance dual read port 8-way set associative 6T SRAM with a one clock cycle access latency, in a 32nm metal-gate partially depleted (PD) SOI technology, for low-voltage applications. The hardware exhibits robust operation at 348MHz and 0.5V with a read

and write power of 3.33 and 1.97mW, respectively, per 4.5KB active array with both read ports accessed at the highest activity data pattern. At 0.6V, an access speed of 1.2GHz is observed.

Session 3 – Technology Variability Modeling

Monday Morning, September 20
Fir Ballroom

Chair: Colin McAndrew, Freescale Semiconductor, Inc.
Co-Chair: Frank Liu, IBM Austin Research Lab

Statistical modeling of device mismatch and variability is critical in scaled integrated circuits.

10:00 **Introduction**

10:05 03-1 **Modeling and Simulation of Transistor and Circuit Variability and Reliability (INVITED),** *Asen Asenov, Binjie Cheng, Daryoosh Dideban, Urban Kovac, Negin Moezi, Campbell Millar, Gareth Roy, Andrew Brown, Scott Roy, University of Glasgow*

Statistical variability associated with discreteness of charge and granularity of matter is one of limiting factors for CMOS scaling and integration. The major MOSFET statistical variability sources and corresponding physical simulations are discussed in detail. Direct statistical parameter extraction approach is presented and the scalability of 6T and 8T SRAM of bulk CMOS technology is investigated. The standard statistical parameter generation approaches are benchmarked and a newly developed parameter generation approach based on nonlinear power method is outlined.

10:55 03-2 **Technology Variability from a Design Perspective (INVITED),** *Borivoje Nikolić, Bastien Giraud, Zheng Guo*, Liang-Teck Pang**, Ji-Hoon Park, Seng Oon Toh, University of California, Berkeley, *Intel Corp, **IBM T.J. Watson Research Center*

Increased variability in process technology and devices requires added margins in the design to guarantee the desired yield. Variability is characterized with respect to the distribution of its components, spatial and temporal characteristics and impact on specific circuit topologies. Approaches to variability characterization and modeling for digital logic and SRAM are reviewed in this paper. Transistor and ring oscillator arrays are designed to isolate specific systematic and random variability components in the design. Distributions of SRAM design margins are measured by padded-out cells and minimum operating voltages for the entire array. Correlations between various components of variability are essential for adding appropriate margins to the design.

11:45 03-3 **Statistical Modeling and Post Manufacturing Configuration for Scaled Analog CMOS,** *Gokce Keskin, Jonathan Proesel, Larry Pileggi, Carnegie Mellon University*

Process variations in advanced CMOS process nodes limit the benefits of scaling for analog designs. In the presence of increasing random intra-die variations, mismatch becomes a significant design challenge in circuits such as comparators. In this paper we describe and demonstrate the details of a statistical element selection (SES) methodology that relies on choosing a subset of selectable circuit elements (e.g., input transistors in a comparator) to achieve the desired specification (e.g., offset). Silicon results from a 65nm test chip demonstrate that SES can achieve an order of magnitude better matching than both redundancy and Pelgrom-model sizing given the same core circuit area.

Session 4 – Advanced and Specialty IC Technologies

Monday Morning, September 20
Pine Ballroom

Chair: Takamaro Kikkawa, Hiroshima University
Co-Chair: Rich Liu, Macronix International, Co., Ltd.

This session discusses challenges in 3D IC integration, monitoring and managing process variability, and foundry issues beyond mainstream IC technology.

10:00 **Introduction**

10:05 04-1 **Three-Dimensional Integration Technology Using Through-Si Via Based on Reconfigured Wafer-to-Wafer Bonding (INVITED),** *Mitsumasa Koyanagi, Takafumi Fukushima, Tetsu Tanaka, Tohoku University*

Three-dimensional (3-D) integration technologies using through-silicon vias (TSV's) are described. We have developed a 3-D integration technology using TSV's based on a wafer-to-wafer bonding method for the fabrication of new 3-D LSIs. A 3-D image sensor chip, 3-D shared memory chip, 3-D artificial retina chip and 3-D microprocessor test chip have been fabricated by using this technology. In addition, we have developed a new 3-D integration technology based on a reconfigured wafer-to-wafer bonding method called a super-chip integration. A number of known good dies (KGDs) are simultaneously aligned and bonded onto lower chips or wafers with high alignment accuracy by using a new self-assembly technique in a super-chip integration.

10:55 04-2 **Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS,** *Vivek Joshi, Michael Wieckowski, Gregory Chen, David Blaauw, Dennis Sylvester, University of Michigan*

This paper analyzes the impact of double patterning lithography (DPL) on 6T SRAM variability. A test chip is implemented in a 45nm CMOS process that uses DPL. Measurements from 75 die demonstrate a significant impact of DPL on SRAM failures. Extensive analysis demonstrates that DPL induced mismatch considerably increases functional failures in SRAM cells, and degrades yield. We also propose a DPL-aware sizing technique to mitigate yield losses.

11:20 04-3 **Parameter-Specific Ring Oscillator for Process Monitoring at the 45 nm Node,** *Lynn Wang, Nuo Xu, Seng Oon Toh, Andrew R. Neureuther, Tsu-Jae King Liu, Borivoje Nikolic, University of California, Berkeley*

Parameter-specific ring oscillator (RO) experimental results are reported, demonstrating the ability to electronically distinguish and quantify sources of variations from gate lithography focus, gate-to-active overlay, nitride contact etch stop layer (CESL) strain, and shallow trench isolation (STI) stress. A 2% RO frequency change due to gate focus variations, a three-four nm overlay error, a 20% increase in RO frequency per 1 um increase in length of diffusion (LOD), and a 3% speed-up per 0.3 um change in STI width are measured. Typical standard-deviation/mean (σ/μ) among 36 ROs within-chip is 0.2-0.3%.

11:45 04-4 **Specialty Foundry Technology and Design Enablement for RF, High Performance Analog, and Power (INVITED),** *Samir Chaudhry, Marco Racanelli, TowerJazz*

The large customer breadth of the Specialty Foundry is driving process technology and design

enablement innovation that is hard to replicate within an integrated device manufacturer (IDM) which serves a more focused customer base. In this paper we will review Specialty Foundry technology in the areas of RF, high-performance analog, and power. We will also review novel design enablement tools available from the Specialty Foundry that leverage the tight interaction between EDA, models, and process technology to improve time to market and yield of highly integrated analog products.

Session 5 – RF Transceivers

Monday Morning, September 20
Cedar Ballroom

Chair: Aristotele Hadjichristos, Qualcomm
Co-Chair: John Rogers , Carleton University

This session will present explosive advances in transceivers for an epic range of applications spanning over 100GHz of spectrum. New circuit and architectural techniques are addressed.

10:00 **Introduction**

10:05 05-1 **Highly Integrated and Tunable RF Front-Ends for Reconfigurable Multi-Band Transceivers (INVITED),** *Hooman Darabi, Broadcom Corp.*

Architectural and circuit techniques to integrate the RF front-end passive components, namely the SAW filters and duplexers that are traditionally implemented off chip, are presented. Intended for software defined radios, tunable high-Q filters allow the integration of highly reconfigurable transceiver front-ends that are robust to in-band and out-of-band blockers. Furthermore, duplexer techniques based on electrical balance concept are introduced to enable highly integrated and programmable radios for full duplex applications such as 3/4G transceivers.

10:55 05-2 **A 1.2 mm^2 Fully Integrated GPS Radio with Cellular/WiFi Co-existence,** *Paul Yu, Todd Sepke, Belal Helal, Shervin Shekarchian, Danilo Gerna, Konstantinos Sarrigeorgidis, Lydi Smaini, Arnab Mitra, James Li, Brian Brunn, Greg Uehara, Thomas Cho, Marvell Semiconductor*

This paper presents a fully integrated GPS receiver with 2.4 dB NF, 1.2mm^2 area, and 13 mA of current in 55 nm CMOS. NF degrades by only 0.1/0.5/0.1 dB in the presence of GSM, DCS, and WiFi blockers respectively. By using current mode operation, push-pull topology, current reuse techniques, and modular Gm-TIA stages, the area is about half and power is about 1/3 of previously published GPS receivers while having similar or better co-existence performance.

11:20 05-3 **A Flexible 500MHz to 3.6GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21MS/s SAR ADC,** *David Lin, Li Li, Shahin Farahani*, Michael Flynn, University of Michigan, Ann Arbor, *Freescale Semiconductor*

A flexible, digital-dominant wireless receiver is implemented in 65nm CMOS. The receive chain consists of a wideband LNA, mixers, and baseband amplifiers. A 7b 21MS/s SAR ADC with embedded, configurable DT FIR/IIR filtering rejects aliasing interferers. Interleaving of sampling and SAR in the ADC maximizes the conversion rate. The receiver achieves -92dBm sensitivity, +33dB and +39dB adjacent and alternate channel interferer rejection with 802.15.4 packets, respectively, and -83dBm sensitivity, +41dB, +20MHz interferer rejection with 802.11 packets.

11:45 05-4 **D-Band CMOS Transmitter and Receiver for Giga-Bit/sec Wireless Data Link,** *Zhiwei Xu, Qun Jane Gu, Yi-Cheng Wu, Adrian Tang, Yu-Ling Lin*, Ho-Hsian Chen*, Chewnpu Jou*, Mau-*

*Chung Frank Chang, UCLA, *TSMC*

A 140GHz transmitter and receiver for Giga-Bit/sec data communication have been designed, fabricated and demonstrated in 65nm CMOS. The chip uses ASK modulation to realize this non-coherent data link and achieve compact design and low power operation. Over 2.5Gbps data link has been validated and the chipset occupies 0.03mm^2/0.12mm^2 and burns 115mW/120mW for TX/RX respectively.

Session 6 – Analog Technologies

Monday Afternoon, September 20
Oak Ballroom

Chair: Eric Naviasky, Cadence
Co-Chari: Ken Suyama, Epoch Microelectronics

This session is a potpourri of analog techniques spanning from asynchronous data acquisition and class D amplification to filters for RF applications, ring oscillators and PLL's and a novel TDC.

1:30 **Introduction**

1:35 06-1 **Event-Driven Data Acquisition and Continuous-Time Digital Signal Processing (INVITED),** *Yannis Tsividis, Columbia University*

This paper reviews research in event-driven data acquisition and associated digital signal processing. The approaches considered can potentially offer significant energy and bandwidth savings with certain important classes of signals, in which activity varies significantly with time. An extensive bibliography is provided.

2:25 06-2 **A Self-Oscillating Class D Audio Amplifier with 0.0012% THD+N and 116.5 dB Dynamic Range,** *Jingxue Lu, Ranjit Gharpurey, University of Texas at Austin*

A low distortion third-order self-oscillating class D audio amplifier is integrated in a 0.7-um CMOS process. It can deliver 1.4 W into an 8 ohm load with 5 V power supply. The presented amplifier eliminates the requirement for a high quality carrier. It achieves a dynamic range (DR) of 116.5 dB, and a peak THD+N of 0.0012% for a 1 kHz sinusoidal input. The efficiency is 84.5%. The area of the amplifier is 6 mm^2.

2:50 06-3 **Dynamic Push-Pull Operational Amplifier for AMLCD Common Voltage Driver Using Minimum Current Limiting Circuit,** *Seungchul Jung, Young-Jin Woo, Tae-Kyu Nam*, Jin-Yong Jeon, Gyu-Ha Cho**, Gyu-Hyeong Cho, KAIST, *Silicon Works, **JDA Technology*

This paper reports a Class AB output stage based on a complementary common source with a minimum current limiting circuit. The non-active transistor in the output stage remains slightly turned on to react immediately for the opposite operation. The quiescent current of the output stage is defined by the proposed minimum current limiting circuit. This operational amplifier is designed for an AMLCD common voltage driver and fabricated by MagnaChip 18V 0.35μm CMOS process. The operation range of the supply voltage is from 5V to 16V and the total quiescent current is independent of temperature variation from -40ºC to 120ºC. On a single 8V supply, the operational amplifier has 1.37mA quiescent current including the bias generation block. The offset voltage is measured from -3.2mV to 5.4mV for 80 samples. The maximum transient current capacity is measured 200mA. The bandwidth is 15MHz with 62º phase margin and the slew-rate is measured 29.9V/μs (rising) and 45.0V/μs (falling).

3:15 BREAK

3:30 06-4 **A 5.8-mW, 20-MHz, 4th-Order Programmable Elliptic Filter Achieving Over -80-dB IM3,** *Peiyuan Wan, Yun Chiu, Pingfen Lin*, University of Illinois at Urbana-Champaign, *Beijing University of Technology*

Frequency compensation of an active-RC elliptic filter is enabled for the first time by employing a derivative-free architecture. In conjunction with a built-in automatic unity-gain bandwidth tracking scheme, the prototype 4th-order active-RC elliptic low-pass filter (LPF) measures a digitally programmable bandwidth of 14-23MHz, a two-tone IM3 at 6MHz consistently better than -80dB with a full-scale input of over 800mVpp, a 1-dB in-band ripple and 45-dB stop-band rejection, all across wide temperature and voltage ranges. The LPF dissipates 5.8mW from a 1.2-V supply and occupies 0.1mm^2 in 0.13-um CMOS.

3:55 06-5 **A Low-Noise Analog Baseband in 65nm CMOS,** *Hassan Elwan, Ahmet Tekin*, Kenneth Pedrotti*, Newport Media Inc., * University of California, Santa Cruz*

In this paper, a universal receiver baseband approach is introduced. The chain includes a post-mixer noise shaping blocker pre-filter, a programmable-gain post mixer amplifier (PMA) with blocker suppression, a differential ramp-based linear-in-dB variable gain amplifier and a Sallen-Key output buffer. The 1.2-V chain is implemented in a 65-nm CMOS process, occupying a die area of 0.45 mm^2. While the device can be tuned across a bandwidth of 700-KHz to 5.2-MHz with 20 KHz resolution, it is tested for two distinct mobile-TV applications; Integrated Services Digital Broadcasting-Terrestrial ISDB-T (3-Segment fc=700 KHz) and Digital Video Broadcasting-Terrestrial/Handheld (DVB-T/H fc=3.8 MHz).

4:20 06-6 **A 1.6mW 1.6ps-rms-Jitter 2.5GHz Digital PLL with 0.7-to-3.5GHz Frequency Range in 90nm CMOS,** *Wenjing Yin, Rajesh Inti, Pavan Kumar Hanumolu, Oregon State University*

A digital phase-locked loop (DPLL) employs a linear proportional path, a double integral path, bandwidth and tuning range tracking, and a novel delta-sigma digital to analog converter to achieve low jitter, wide operating range and low power. The prototype DPLL fabricated in a 90nm CMOS process operates from 0.7 to 3.5GHz. At 2.5GHz, the proposed DPLL consumes only 1.6mW power from a 1V supply and achieves 1.6ps and 11.6ps of long-term r.m.s and peak-to-peak jitter, respectively.

4:45 06-7 **A 2.4ps Resolution 2.1mW Second-Order Noise-Shaped Time-to-Digital Converter with 3.2ns Range in 1MHz Bandwidth,** *Brian Young, Sunwoo Kwon*, Amr Elshazly, Pavan Kumar Hanumolu, Oregon State University, *Dongbu HiTek*

A time-to-digital converter (TDC) employs a phase-reference second-order continuous-time delta-sigma modulator to achieve high resolution and low power. The modulator operates on the phase of the input signal and generates an equivalent noise-shaped one-bit output data stream. Fabricated in an LP 90nm CMOS process, the prototype TDC achieves better than 2.4ps resolution over a 3.2ns range in a 1MHz signal bandwidth while consuming 2.1mW from a 1.2V supply.

5:10 06-8 **High-Speed CMOS Ring Oscillators with Low Supply Sensitivity,** *Xiaoyan Gui, Michael Green, University of California, Irvine*

A novel circuit topology for CMOS CML ring oscillators that reduces the supply sensitivity is presented. It is shown that this technique causes only a slight reduction in the maximum frequency of the oscillator and maintains the same random jitter generation while greatly reducing the sinusoidal jitter caused by power supply variation. Measurement results from a prototype chip fabricated in 0.18μm CMOS process verify the effectiveness of the proposed technique.

Session 7 – Biomedical Sensors and Systems

Monday Afternoon, September 20
Fir Ballroom

Chair: Ken Szajda, LSI Corporation
Co-Chair: Steve Garverick, Case Western Reserve University

This session covers work that pushes the limit of biosensors and their interface electronics in terms of very low power, extended functionality and high performance.

1:30 **Introduction**

1:35 07-1 **Smart CMOS Substrates for Bioelectronic Interfaces: Overview and Trends (INVITED),** *Marco Tartagni, University of Bologna*

The paper will overview the recent trends of smart CMOS substrates hosting arrays of biosensor interfaces. It will review figures of merit and will discuss the design trade-offs and the trends with respect to the scaling in both sensing and actuation.

2:25 07-2 **A Low-Power Multi-band ECoG/EEG Interface IC,** *Fan Zhang, Apurva Mishra, Andrew G. Richardson, Stavros Zanos, Brian P. Otis, University of Washington*

We present a 6.4 microwatt core electrocorticography (ECoG)/electroencephalography (EEG) processing integrated circuit with a 0.4 microvolt rms noise floor intended for emerging brain-computer interface applications. This chip conditions the signal and simultaneously extracts energy in four fully-programmable frequency bands. Measured results from in-vivo ECoG recording from the primary motor cortex of an awake monkey are presented.

2:50 07-3 **A Programmable Pulse UWB Transmitter with 34% Energy Efficiency for Multichannel Neuro-Recording Systems,** *Henrique Miranda, Teresa Meng*, *Stanford University*

This paper describes configurable, 3.6 to 7.5 GHz pulse UWB transmitter IC targeted for neurological implants with high data rate requirements. Each cycle of the RF pulse is digitally programmable in amplitude and duration, enabling a very flexible shaping of the transmitted PSD signal, without the use of an output filter. The transmitter achieves a maximum of 34% of energy efficiency when drawing 8.5 pJ/bit from the supply, with 13 uW of constant static power. This transmitter was implemented in 65nm CMOS and measures 1.0 mm x 0.7 mm. A 32-channel recording experiment using this chip is also reported.

3:15 BREAK

3:30 07-4 **An Inside Body Power and Bidirectional Data Transfer IC Module Pair,** *Edward Lee, Alfred Mann Foundation*

An IC module pair connected with 3 wires was proposed for an implant that consisted of a master unit (MU) and a small, light-weight satellite unit (SU). Power was delivered from the MU to the SU using a 3-phase signal, and converted to DC in the SU by a passive MOS AC-DC converter. Data transfer between the two units was achieved by modulating the amplitudes and the positions of the rising and falling edges of the 3-phase signal. A bidirectional data rate in the range of MB/s and an overall power efficiency of 90.2% for a 3.2mW load were achieved in a 0.18µm CMOS process.

3:55 07-5 **192-Channel CMOS Neurochemical Microarray,** *Meisam Honarvar Nazari, Hamed Mazhab-Jafari, Lian Leng, Axel Guenther, Roman Genov, University of Toronto*

A 16×12-channel neurochemical microarray is presented. Each channel acquires bidirectional currents down to pico-amperes proportional to the concentration of a neurochemical. By combining the current-to-frequency and the single-slope analog-to-digital converter (ADC) 110dB of dynamic range is achieved. The ADC in each channel generates a 16-bit output in less than a millisecond. The microarray with flat and 3D gold electrodes and an on-chip microfluidic network is experimentally validated in in-situ recording of neurotransmitter dopamine.

4:20 07-6 **A Frequency-Shift-Based CMOS Magnetic Biosensor with Spatially Uniform Sensor Transducer Gain,** *Hua Wang, Constantine Sideris, Ali Hajimiri, California Institute of Technology*

This paper presents a scalable and ultrasensitive magnetic biosensing scheme based on on-chip LC resonance frequency-shifting. The sensor transducer gain is demonstrated as being location-dependent on the sensing surface and proportional to the local polarization magnetic field strength |B|2 generated by the sensing inductor. To improve the gain uniformity, a bowl-shape stacked coil together with floating shimming metal is proposed for the inductor design. As an implementation example, a 16-cell sensor array is designed in a 45nm CMOS process. The spatially uniform sensor gain of the array is verified by testing micron-size magnetic particles randomly placed on the sensing surface. The Correlated-Double-Counting (CDC) noise cancellation scheme is also implemented in the presented design, which achieves a noise suppression of 10.6dB with no power overhead. Overall, the presented sensor demonstrates a dynamic range of at least 85.4dB.

Session 8 – Advanced Wireline Techniques

Monday Afternoon, September 20
Pine Ballroom

Chair: Ed Van Tuijl, Axiom-IC Twente
Co-Chair: Afshin Momtaz, Broadcom

This session presents multi-GHz wireline transceivers, emphasizing equalization, high performance, and low power techniques.

1:30 **Introduction**

1:35 08-1 **Gain and Equalization Adaptation to Optimize the Vertical Eye Opening in a Wireline Receiver,** *Dustin Dunwell, Anothony Chan Carusone, University of Toronto*

Control signals for an equalizer and variable gain amplifier are optimized by examining the PDF of received data, which is obtained from the DC output of an analog sampler. Measured results show that the adaptation scheme functions correctly over channels of varying lengths at speeds from 2 to 10 Gb/s.

2:00 08-2 **Equalizer Design and Performance Trade-offs in ADC-based Serial Links (INVITED),** *Jaeha Kim, Jihong Ren,Brian Leibowitz, Patrick Satarzadeh, Ali-Azam Abbasfar, Jared Zerbe, Rambus, Inc.*

This paper analyzes the performance benefit of using non-uniform quantization in ADC-based backplane receivers. The optimal way of placing the ADC quantization thresholds is not what minimizes the quantization error, especially with limited ADC resolution. The proposed reduced-slicer partial-response DFE receiver achieves the BER of 3~4-bit uniform ADCs with only 4 data slicers.

2:50 08-3 **A Combined Anti-Aliasing Filter and 2-tap FFE in 65-nm CMOS for 2x Blind 2-10 Gb/s ADC-Based Receivers,** *Tina Tahmoureszadeh, Siamak Sarvari, Ali Sheikholeslami, Hirotaka Tamura*, Yasumoto Tomita*, Masaya Kibune*, University of Toronto, *Fujitsu Laboratories Limited*

This paper presents a combined anti-aliasing filter and 2-tap feed-forward equalizer (AAF/FFE) as an analog front-end (AFE) for 2x blind ADC-based receivers. The front-end optimizes the channel/filter characteristics for data-rates of 2-10 Gb/s. The AAF bandwidth scales with the data-rate and the 2-tap FFE is designed without the need for noise-sensitive analog delay cells. The AAF/FFE is implemented in 65-nm CMOS, occupies 0.013 mm^2, and consumes 2.4 mW at 10 Gb/s.

3:15 BREAK

3:30 08-4 **A 5Gb/s 2×2 MIMO Crosstalk Cancellation Scheme for High-Speed I/Os,** *Taehyoun Oh, Ramesh Harjani, University of Minnesota*

We describe a multiple-input multiple-output crosstalk cancellation (MIMO-XTC) architecture, particularly applicable to single-ended I/O. The MIMO architecture efficiently cancels crosstalk and improves jitter and eye-opening at the same time. A continuous-time prototype design was fabricated using a 130nm CMOS process and occupies 0.03mm^2 of die area. The XTC equalizer performance has been verified for a variety of FR4 channel spacings and data rates. Measured eye diagrams show that the jitter_pp reduces by 67%UI and the vertical eye opening increases by 58.2% at 5Gb/s. The prototype MIMO-XTC circuit consumes 2.8 mW/Gbps/lane which is roughly two times lower than other XTC schemes.

3:55 08-5 **A 6Gb/s Receiver With Discrete-Time Based Channel Filtering For Wireline FDM Communications,** *Tsutomu Takeya, Kazuhisa Sunaga*, Koichi Yamaguchi*, Hideyuki Sugita*, Yoichi Yoshida, Masayuki Mizuno*, Tadahiro Kuroda, Keio University , *NEC Corporation*

We present a 6Gb/s wireline receiver having frequency division multiplexing (FDM) with four frequency sub-channels. Its discrete-time filter consumes less power than a conventional filter and provides channel filtering of FDM signals. Improved I/Q-based phase detection makes possible low-power symbol-rate clock recovery. The receiver achieves BER<10^-12 over a 25cm low-ε channel, while consuming 250mW from a 1.4V supply.

4:20 08-6 **A Slew-Rate Controlled Transmitter to Compensate for the Crosstalk-Induced Jitter of Coupled Microstrip Lines,** *Hae-Kang Jung, Soo-Min Lee, Jae-Yoon Sim, Hong-June Park, POSTECH*

A single-ended transmitter eliminates the crosstalk-induced jitter at the receiver by controlling the slew rates of the signal at the transmitter for the even and odd modes of two parallel coupled microstrip lines. The transmitter chip in a 0.18 μm CMOS process reduces the total RX jitter by about 38 ps (53%) for the data rates from 2.6 to 5 Gbps, and increases the horizontal eye-opening (BER < 1E-12) by about 21% at 5 Gbps.

4:45 08-7 **Digital Link Pre-emphasis with Dynamic Driver Impedance Modulation,** *Ranko Sredojevic, Vladimir Stojanovic, Massachusetts Institute of Technology*

Digital impedance-modulating equalizer overcomes the power overhead of equalization in voltage-mode drivers. Compact, fully-digital RAM-DAC implementation compensates duty-cycle distortion and driver nonlinearity. A 90nm CMOS testchip shows small signal degradation from dynamic modulation of transmitter impedance, achieving 100mV receiver eye with 2pJ/bit at 4Gb/s over wide variety of 20'' backplanes.

Session 9 - Forum 1
3D Integration Infrastructure

Monday Afternoon, September 20
Cedar Ballroom

Chair: David Sunderland, Boeing Space & Intelligence Systems

Vertically stacked integrated circuits, enabled by Through-Silicon Via (TSV) technology, appear poised to provide significant improvements in density and performance. But is the design, assembly and test infrastructure ready to support this innovation in mainstream products? We explore this issue with four Invited talks.

1:35 9-1 **3D Integration Infrastructure: Requirements to Support High Volume Production,** *W. R. Bottoms, Third Millennium Test Solutions, Santa Clara, CA*

This presentation reviews the status of 3D technology integration and product development, and discusses a variety of potential "roadblocks" to the adoption of 3D for the mainstream. Meeting the challenges posed by these roadblocks will require new materials, new equipment, new process technologies and even new production flows. The known solutions and the potential solutions in development will be discussed.

2:25 9-2 **3D IC – TSV & Micro-bump Modeling and Design Implementation Tools,** *Vassilios Gerousis, Cadence, San Jose, CA*

This talk will explore 3D IC physical modeling, physical design methodology and physical design tools. It will first provide the basic modeling features of 3D IC to allow the specification and the integration of multiple chips in either a vertical stack or a silicon interposer. The second part of the talk will focus on design implementation and analysis of the 3D IC interconnect components and how those are integrated in a design flow.

3:30 9-3 **3D Packaging Evolution from an OSAT Perspective,** *Raj Pendse, STATSChipPAC, Fremont, CA*

This presentation illustrates parallel developments in the three areas of packaging technology, i.e. traditional die and package stacking on substrates, fan-in and fan-out wafer level packaging and 3D Si integration, and the role of the Out-Sourced Assembly and Test (OSAT) industry in supporting this evolution. Latest developments in the key elements of 3D Si integration such as wafer thinning, micro bumping, micro bonding and logical hand off points among Si and package foundries are presented.

4:20 9-4 **Challenges and Emerging Solutions for Testing TSV-Based Three-Dimensional Stacked ICs,** *Erik Jan Marinissen, IMEC, Leuven, Belgium*

This presentation focuses on the challenges of testing 3D-SICs, and describes for which challenges solutions are already available or emerging. It provides an overview of the manufacturing steps of TSV-based 3D-SICs, as far as relevant for testing. Subsequently, it discusses test flows for wafer probing and packaged-device tests, the challenges with respect to test contents and wafer-level probe access, and the on-chip design-for-test (DFT) infrastructure required for 3D-SICs.

Poster Session

Monday Evening, September 20
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

M-1 **Amorphous Silicon 7 Bit Digital-to-Analog Converter on PEN,** *Aritra Dey, Hongjiang Song*, Tofayel Ahmed*, Sameer Venugopal, David Allee, Flexible Display Center at Arizona State University, *Intel Corp, Arizona*

A 7-bit switched capacitor D/A converter (DAC) is built using only n-channel amorphous silicon hydride (a-Si:H) thin film transistors (TFTs) and capacitors. The circuit is fabricated on both polyethelene napthalate (PEN) and glass using a low temperature process, compatible with flexible plastic substrates. Switched capacitor architectures are chosen as they are less prone to TFT aging because of electrical stress, and also to active device mismatches. The measurements from the fabricated DAC show excellent linearity characteristics, achieving a DNL of less than ±0.6 LSB and INL of less than ±1 LSB without additional calibration, at a conversion rate of 500 Hz.

M-2 **Design of Low-noise CMOS MEMS Accelerometer with Techniques for Thermal Stability and Stable DC Biasing,** *S. S.Tan, C. Y. Liu, L. K. Yeh, Y. H. Chiu, Michael S.-C. Lu, Klaus Y. J. Hsu, National Tsing Hua University*

An integrated high-sensitivity CMOS MEMS capacitive accelerometer with thermal stability has been designed and demonstrated in this work. Issue of obtaining stable DC bias at input terminals is particularly addressed. Sensitivity of 595 mV/g is achieved in the accelerometer and the overall noise floor is 50 μg/√Hz, which corresponds to an effective capacitance noise floor of 0.024 aF/√Hz. The zero-g thermal variation is as low as 1.68 mg/°C.

M-3 **A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors,** *Fred Chen, Anantha Chandrakasan, Vladimir Stojanovic, Massachusetts Institute of Technology*

We present the design and implementation of a new sensor system based on the theory of compressed sensing that addresses the energy and telemetry bandwidth constraints of wireless sensors. A hardware efficient realization demonstrates continuous data acquisition and compression of up to 40x on an EEG signal, while relaxing the noise constraints of the analog frontend by nearly 10x. The hardware is implemented in a 90nm CMOS process and consumes 1.9μW at 0.6V and 20kS/s.

M-4 **Analysis and Demonstration of MEM-Relay Power Gating,** *Hossein Fariborzi, Matthew Spencer*, Vaibhav Karkare**, Jaeseok Jeon*, Rhesa Nathanael*, Chengcheng Wang**, Fred Chen, Hei Kam*, Vincent Pott*, Tsu-Jae King Liu*, Elad Alon*, Vladimir Stojanović, Dejan Marković**, Massachusetts Insitute of Technology, *University of California, Berkeley, ** University of California, Los Angeles*

This paper shows that due to their negligibly low leakage, chips utilizing MEM relay power gates can potentially achieve lower energy than those utilizing CMOS power gates. A simple analysis provides design guidelines and savings estimates for relay designs. Finally, a relay chip successfully power-gating a CMOS chip is demonstrated.

M-5 **An Energy-Efficient SoC for Closed-Loop Medical Monitoring and Intervention,** *Xiaoyu Zhang, Hanjun Jiang, Fule Li, Songyuan Cheng, Chun Zhang, Zhihua Wang, Tsinghua University*

This paper presents an energy-efficient SoC dedicated for portable medical monitoring and intervention systems capable of closed-loop control. The SoC contains a 0.9V/165μW MCU and a dual-band RF block including a 403MHz transceiver for data link and a 915MHz receiver for wake-up link. The data link transceiver is composed of a 200kbps FSK transmitter and a 64kbps OOK receiver, consuming 5.58mW and 3.13mW, respectively. The 915MHz receiver based on wireless energy harvesting gives the SoC the unique power-silent work-on-demand capability, avoiding wasting energy during the idle-listening period. The power consumption of the integrated MCU is reduced by means of acceleration instructions and modules. The implemented work-on-demand MAC protocol with instant response satisfies the requirements of typical medical applications. The SoC is fabricated in 0.18um CMOS technology, and occupies a die area of 5.9mm^2.

M-6 **A Novel Readout IC with High Noise Immunity for Charge-Based Touch Screen Panels,** *Jun-HyeokYang, Seung-Chul Jung, Young-Jin Woo, Jin-Yong Jeon, Sung-Woo Lee, Chang-byung Park, Hyun-Sik Kim, Seung-Tak Ryu, Gyu-Hyeong Cho, KAIST*

The critical issues in charge-based touch screen panels for large size display are noise and speed. To solve these, this paper introduces a 'Delta-integration' scheme. It effectively solves local noise and speed issues. In addition, it can replace a high-resolution ADC with a comparator and counter.

M-7 **Ground Rule Slack Aware Tolerance-Driven Optical Proximity Correction for Local Metal Interconnects,** *Shayak Banerjee, Kanak Agarwal*, Michael Orshansky, University of Texas - Austin, *IBM Research*

The current method of communicating process capabilities to the designer is in the form of ground rules. However, due to constraints on the complexity and number of rules, there may exist shapes that are design-rule clean but difficult to manufacture. This problem is exacerbated in local routes drawn on 1x metal (M1) which allows highly bi-directional shapes at tight spacing. On the other hand, local M1 routes have low parasitic resistance and capacitance as compared to device impedances. Hence there exists an opportunity to perturb these shapes to improve their manufacturability without significant performance impact. We propose to guide this perturbation by the amount of leeway available between the designed values and the ground rules – which we refer to as ground rule slack. In this paper, we utilize ground rule slack to generate tolerance bands for layout features. We further develop a tolerance-driven optical proximity correction (TD-OPC) algorithm which utilizes such tolerance bands to find a lithographically optimal mask solution for manufacturing. Our experiments on sample layouts shows that the use of this methodology helps reduce lithographic hotspots by 59% in comparison to process window optical proximity correction.

M-8 **HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System,** *David Duarte, Paola Zepeda, Suching Hsu, Atul Maheshwari, Greg Taylor, Intel Corp.*

This paper describes the design of a thermal sensor and its accompanying supply voltage regulator, both implemented in a Hi-K, metal-gate, 32nm technology. The designs incorporated built-in run-time variability reduction schemes and silicon data verified the expected performance. The DFT circuits needed to validate circuit performance in HVM are described.

M-9 **Single Event Transient Mitigation in Cache Memory using Transient Error Checking Circuits,** *Xiao Yinyao, Lawrence Clark, Dan Patterson, Keith Holbert, Arizona State University*

Protecting a high performance radiation hardened by design cache from single-event transient induced peripheral circuit errors is presented. A 16 kB cache and test engine, fabricated on an IBM 90 nm bulk CMOS process, irradiated with heavy ions, is used to provide experimental

validation of the design.

M-10 **Elimination of Half Select Disturb in 8T-SRAM by Local Injected Electron Asymmetric Pass Gate Transistor,** *Kentaro Honda, Kousuke Miyaji, Shuhei Tanakamaru, Shinji Miyano*, Ken Takeuchi, University of Tokyo, *Semiconductor Technology Academic Research Center*

An 8T-SRAM cell with asymmetric PG transistor by local electron injection is proposed. Both side injection scheme and SR one side injection scheme are also proposed and analyzed for 6T-SRAM and 8T-SRAM cell. The SR one side injection scheme combined with the 8T-SRAM shows the best characteristics and suppresses half select disturb by 141% without write margin and read speed degradation.

M-11 **Opportunities for PMOS Read and Write Ports in Low Voltage Dual-Port 8T Bit Cell Arrays,** *Bibiche Geuskens, Muhammad Khellah, Jaydeep Kulkarni, Tanay Karnik, Vivek De, Intel Labs*

Strained silicon has enhanced PMOS transistor current much more than NMOS. As such, IDSATN/IDSATP equal to 1 is nearing reality. This work studies the effect of this presumably continuing trend on dual-port 8T bit cell performance. Preference for using NMOS or PMOS in write and read ports is shown to depend on current ratio, VMIN circuit assist and array access type.

M-12 **Radio-Frequency Signal Tracking (RFST) Technique for Improving Efficiency in RF Amplifier Supplying Systems,** *Yu-Huei Lee, Wei-Chan Wu, Pin-Chin Huang, Shih-Wei Wang, Ke-Horng Chen, National Chiao Tung University*

A current mode buck-boost (BB) converter with the RFST technique is proposed to improve the efficiency of radio frequency (RF) power amplifiers (PAs). The fast up/down tracking is implemented to meet the requirement of the RF amplifier supplying systems. Besides, the current mode control with the self-tuning pulse skipping (SPS) mechanism can extend the effective duty cycle to achieve voltage regulation and get high efficiency when the input voltage is close to the output. Through the RFST tracking technique, the tracking speed from 3 V to 2 V and vice versa are 15 μs and 20 μs, respectively. Besides, the recycling energy improves the efficiency to be higher than 85 % under a high switching frequency of 5 MHz.

M-13 **A 1.2A 2MHz Tri-Mode Buck-Boost LED Driver With Feed-Forward Duty Cycle Correction,** *Sarvesh Bang, Damian Swank, Arun Rao, William McIntyre, Qadeer Khan*, Pavan Hanumolu*, National Semiconductor Corporation, *Oregon State University*

A flash LED Buck-Boost driver employs a dual duty cycle control and feed-forward duty cycle correction to achieve high efficiency over the entire Li-On battery voltage range of 3.0 to 5.2V. Fabricated in a 0.5μm CMOS process, the converter uses an external 1μH inductor and a 10μF capacitor and operates at 2MHz switching frequency. The measured peak efficiency is 83% and 87% at 1.2A and 0.6A LED currents, respectively. This achieved efficiency represents an improvement of more than 10% over conventional approaches.

M-14 **0.18-V Input Charge Pump with Forward Body Biasing in Startup Circuit using 65nm CMOS,** *Po-Hung Chen, Koichi Ishida, Xin Zhang, Yasuaki Okuma*, Yoshikatsu Ryu*, Makoto Takamiya, Takayasu Sakurai, The University of Tokyo, *Semiconductor Technology Academic Research Center*

To kick up the boost converter in low operation voltage, a charge pump circuit with forward body biasing is proposed. Because of applying the appropriate forward bias to each MOSFET, the pumping efficiency can be improved more than conventional charge pump without applying forward bias. The experiment results show that the proposed charge pump can improve the output current more than 150% with 1.5% area overhead. The boost converter connected with

the proposed charge pump can kick up the 0.18-V input to 0.74-V output while the conventional one only provides 4.7mV output. With the higher pumping ability and the lower kick-up voltage, the proposed charge pump circuit is more suitable for energy harvesting applications which only provide low voltages.

M-15 **A Novel Wideband 1-π Model with Accurate Substrate Modeling for On-Chip Spiral Inductors,** *Huanhuan Zou, Jun Liu, Jincai Wen, Huang Wang, Lingling Sun, Zhiping Yu, Hangzhou Dianzi University*

This paper presents a novel wideband 1-pi equivalent circuit model for on-chip spiral inductors is presented. A substrate network, consisting of R/L/C, is proposed to model the broadband loss mechanisms in the silicon substrate. The skin and distributed effects for windings have been taken into account. A series of inductors with different geometries are fabricated in standard 0.18-um 1P6M RF CMOS process to verify the model. Excellent agreements have been obtained between the modeled and measured data up to 40 GHz, which verify that the proposed 1-pi model naturally has better wideband prediction capability than published 1-pi or T-models, and simpler topology than 2-pi models for on-chip spiral inductors.

M-16 **Reliability Analysis of Analog Circuits Using Quadratic Lifetime Worst-Case Distance Prediction,** *Xin Pan, Helmut Graeb, Technische Universitaet Muenchen*

This paper proposes an efficient method to predict the lifetime yield of analog circuits considering the joint effects of manufacturing process variations and parameter lifetime degradations. The method uses the idea of worst-case distance, which is an indicator of circuit robustness concerning process variations. The worst-case distance in circuit lifetime is predicted based on a new, quadratic prediction model in time domain. The lifetime yield of the circuit is obtained based on this quadratic model. We prove for the first time that the lifetime yield value is directly applicable to the calculation of reliability function and lifetime distribution of analog circuits, while previous modeling techniques either are only applicable for digital circuits, or require long simulation time. The experimental results show that the proposed method has an average error smaller than 5%, with a speed up of six times in comparison to an iterative optimization based lifetime yield analysis method.

M-17 **A 70 GHz 10.2 mW Self-Demodulator for OOK Modulation in 65-nm CMOS Technology,** *Xia Li, Peter Baltus, Paul van Zeijl*, Dusan Milosevic, Arthur van Roermund, Eindhoven University of Technology, *Philips Research Eindhoven*

A 70.86 to 79.29 GHz low-power self-demodulator for on-off-keying (OOK) modulation is realized in TSMC 65-nm CMOS technology. By using a frequency-sweeping injection-locked oscillator (IJLO), the OOK modulated 70 GHz signal is demodulated by itself in a passive mixer and an 8.43 GHz bandwidth is achieved at 10.2 mW power consumption from a 1-V supply. The conversion gain is 10 dB and constant over the entire bandwidth. The core area of the chip is 0.072 mm^2.

M-18 **A 10 GHz Frequency-Drift Temperature Compensated LC VCO with Fast-Settling Low-Noise Voltage Regulator in 0.13 µm CMOS,** *Hiroshi Akima, Aleksander Dec, Timothy Merkin, Ken Suyama, Epoch Microelectronics, Inc.*

An LC voltage controlled oscillator (VCO) with frequency-drift temperature compensation circuit in 0.13 um CMOS process is presented. The compensation circuit consists of MOS inversion varactor and utilizes negative temperature coefficient of VBE characteristic of BJT. With the compensation circuit, 82 % of improvement in VCO frequency-drift due to temperature is demonstrated in measurement. The VCO is supplied from a fast-settling low-noise voltage regulator.

M-19 **A 43.5mW 77GHz Receiver Front-End in 65nm CMOS suitable for FM-CW Automotive Radar,** *Roc Berenguer, Gui Liu, Abe Akhiyat, Keya Kamtikar, Yang Xu, Illinois Institute of Technology*

A low power 77GHz receiver front-end, suitable for a FM-CW Automotive Radar has been implemented using a 65nm RFCMOS process. It has been designed using direct conversion architecture. The fabricated front-end exhibits a maximum voltage gain of 15dB over the baseband and presents a LNA NF of 7dB which makes it suitable for next generation of collision avoidance systems. The achieved power consumption of the receiver front-end is 43.5mW from a 1.5V supply.

M-20 **A 27mW 2.2dB NF GPS Receiver using a Capacitive Cross-coupled Structure in 65nm CMOS,** *Hyunwon Moon, Seung-Chan Heo, Hwayeal Yu, Jinhyuck Yu, Ji-Soo Chang, Seung-Il Choi, Sangyoub Lee, Woo-Seung Choo, Byeong-Ha Park, Samsung Electronics*

A fully integrated low-IF GPS receiver with minimum external components is implemented in a 65nm CMOS process. It has an integrated LNA and an active complex bandpass filter with a switchable signal bandwidth of 2MHz or 6 MHz to achieve the SNR improvement. To reduce power consumption, the current reusing method and current mode interface technique using a capacitive cross-coupled common-gate structure are applied. The measured noise figure of whole receiver including an external inter-stage SAW filter is 2.2dB. Its current consumption is 15mA at 1.8V supply.

M-21 **A Low Power High Reliability Dual-Path Noise-Cancelling LNA for WSN Applications,** *Ming-Yeh Hsu, Chao-Shiun Wang, Chorng-Kuang Wang, National Taiwan University*

This paper presents a dual-path noise-cancelling (DPNC) LNA, which is designed for low power wireless sensor network (WSN) applications and operates at 2.4GHz band. The proposed DPNC LNA can effectively cancel internal circuit noise while consuming less power by gm-boosted technique. The measured voltage gain and NF are 22dB and 3.7dB, respectively. IIP3 is +8dBm and consumes 1.2mW with a 1.0V single supply. Fabricating in the 0.18μm standard CMOS process, the LNA occupies an active area of 0.3mm^2.

M-22 **W-Band Pulsed Radar Receiver in Low Cost CMOS,** *Ning Zhang, Kenneth O, University of Florida*

A CMOS heterodyne receiver integrating a phase-locked loop that includes a bulk of transmitter functions for W-band pulsed radar is realized using low leakage transistors of a low cost 65-nm bulk CMOS process with 5 thin and 1 thick metal layers used to manufacture cell phone RFIC's. The peak conversion gain of receiver is 7 dB and the minimum NF is 10.8 dB between 78 and 88 GHz in measurement. The entire receiver front-end consumes ~190 mW.

Session 10 – Oversampled Data Converters

Tuesday Morning, September 21
Oak Ballroom

Chair: Don Thelen, ON Semiconductor
Co-Chair: Alessandro Piovaccari, Silicon Laboratories

Delta sigma ADCs continue to improve and are being used in more applications each year. This session includes many novel examples.

9:00 **Introduction**

9:05 10-1 **A 32-Channel Front-End for Wireless HID using Inverse-STF Pre-Filtering Technique,** *Sherif Galal, Jurgen van Engelen*, Jared Welz, Henrik Jensen, Khaled Abdelfattah, Felix Cheung, Sasi Kumar Arunachalam, Xicheng Jiang, Todd Brooks, Broadcom Corp., *Mobius Semiconductor*

A 32-channel front-end circuit for wireless human interface devices (HID) is described. The front-end incorporates a Sigma-Delta ADC combined with an inverse-STF pre-filtering technique to achieve 10.8 ENOB at a conversion rate of 7.5us per channel. Chopping and digital calibration are employed to achieve an offset voltage < 850uV and gain error < 0.17%. The HID front-end measures single-ended rail-to-rail inputs with 1.62V to 3.63V supply range, occupies 0.28mm^2 in 65nm CMOS and consumes 1.8mW from 1.2V supply.

9:30 10-2 **82 dB SNDR 20-Channel Incremental ADC with Optimal Decimation Filter and Digital Correction,** *Wenhuan Yu, Mehmet Aslan*, Gabor Temes, Oregon State University, *National Semiconductor Corporation*

A third-order multi-channel incremental ADC with a 5-level quantizer is presented. An optimal decimation filter is used which minimizes the weighted sum of the thermal and quantization output noises. Digital correction is used to suppress mismatches in the multi-bit DAC.

9:55 10-3 **A +5dBFS Third-Order Extended Dynamic Range Single-Loop ΔΣ Modulator,** *Nima Maghari, Skyler Weaver, Un-Ku Moon, Oregon State University*

A new single-loop delta-sigma modulator with extended dynamic range is proposed. It employs an auxiliary multi-bit quantizer which processes the quantization error of the main quantizer. This addition guarantees improved stability over a wider input signal range. The cancelation of the quantization noise of the main quantizer is done via in-loop digital summation and is immune to opamp DC gain. As a proof of concept, a 3rd order modulator is designed in a 0.18μm CMOS process. This implementation incorporates a 3-level main quantizer, a 9-level auxiliary quantizer and 30dB open-loop opamp gain. Measurement results show that at 1.2V power supply and reference, the input signal can go over +5dBFS without any stability issues, achieving 75dB SNDR and 77.2dB dynamic range at OSR of 16. The clock frequency is 40MHz and the power dissipation is 4.9mW.

10:20 10-4 **A 63 dB 16 mW 20 MHz BW Double-Sampled ΔΣ Analog-to-Digital Converter with an Embedded-Adder Quantizer,** *Jeongseok Chae, Sanghyeon Lee, M. Aniya*, S. Takeuchi*, K. Hamashita*, Pavan Hanumolu, Gabor Temes, Oregon State University, *Asahi Kasei Microdevices*

A wideband ΔΣ ADC using a novel double-sampling scheme with a single set of capacitors and a dynamic embedded-adder quantizer is presented. The proposed quantizer eliminates static currents in the adder of a low-distortion architecture. Fabricated in 0.18 μm CMOS process, the prototype chip operates with a 320 MHz sampling frequency and achieves 63 dB SNDR in a 20 MHz signal band while consuming 16 mW power.

10:45 BREAK

11:05 10-5 **A 69.8 dB SNDR 3rd-order Continuous Time Delta-Sigma Modulator with an Ultimate Low Power Tuning System for a Worldwide Digital TV-Receiver,** *Kazuo Matsukawa, Yosuke Mitani, Masao Takayama, Koji Obata, Yusuke Tokunaga, Shiro Sakiyama, Shiro Dosho, Panasonic Corporation*

This paper presents a 3rd-order continuous time delta-sigma modulator for a worldwide digital TV-receiver whose SNDR is 69.8 dB. An ultimate low power tuning system using RC-relaxation oscillator is developed in order to achieve high yield against PVT variations. A 3rd-order

modulator with modified single opamp resonator contributes to cost reduction by realizing very compact circuit. The mechanism to occur 2nd-order harmonic distortion at current feedback DAC was analyzed and a reduction scheme of the distortion enabled the modulator to achieved FOM of 0.18 pJ/conv-step.

11:30 10-6 **A Robust STF 6mW CT ΔΣ Modulator with 76dB Dynamic Range and 5MHz Bandwidth,** *Mohammad Ranjbar, Omid Oliaei, Robert Jackson*, University of Massachusetts Amherst

A third-order continuous-time delta-sigma modulator achieving 76dB dynamic range over 5MHz signal bandwidth is presented. The modulator has a monotonic lowpass signal transfer function and achieves over 70dB anti-aliasing. The prototype chip implemented in a 130nm CMOS process consumes 6mw power from a single 1.2V supply and occupies 0.56 mm^2 active area.

11:55 10-7 **A 5-MHz 11-bit Delay-Based Self-Oscillating ΣΔ Modulator in 0.025mm^2,** *Bart De Vuyst, Pieter Rombouts, Ghent University*

In this paper a self-oscillating sigma-delta modulator is presented. The self-oscillation is induced here by introducing a controlled delay in the feedback loop of the modulator. A second order CMOS prototype was constructed in a 0.18 um technology. The modulator achieves a dynamic range (DR) of 66 dB for a signal bandwidth of 5 MHz. The power consumption is 6 mW and the chip area of is 0.025 mm^2.

Session 11 – Power Management

Tuesday Morning, September 21
Fir Ballroom

Chair: Cory Arnold, Maxim Integrated Products
Co-Chair: Hoi Lee

Effective power management requires innovative circuits to optimize system cost and efficiency. This session includes advancements in switching regulators, linear regulators, and smart power drivers.

9:00 **Introduction**

9:05 11-1 **Ramp Signal Generation in Voltage Mode CCM Random Switching Frequency Buck Converter for Conductive EMI Reduction,** *Edward N. Y. Ho, Philip K. T. Mok, Hong Kong University of Science and Technology*

An output voltage ripple aware design of different voltage ramp signal of voltage mode CCM random frequency buck converter for conductive EMI reduction has been presented in this paper. Simulation and experimental results with a standard CMOS-0.35μm process verifies the proposed design and analysis. From experimental result, a carefully designed ramp can reduce output voltage ripple by more than 8 times with no influence on the inductor current spectrum spread and without any increment of inductance and capacitance comparing to conventional design.

9:30 11-2 **A 5-MHz 91% Peak-Power-Efficiency Buck Regulator With Auto-Selectable Peak- and Valley-Current Control,** *Mengmeng Du, Hoi Lee, University of Texas at Dallas*

This paper presents a multi-MHz buck regulator for portable applications using an auto-selectable peak- and valley-current control (ASPVCC) scheme. The proposed ASPVCC scheme and the dynamically-biased shunt feedback in the current sensors relax the settling-time requirement of the current sensing and improve the sensing speed. The proposed converter can thus operate at high switching frequencies with a wide range of duty ratios for

reducing the required inductance. Implemented in a 0.35-um CMOS process, the proposed buck converter can operate at 5-MHz with a duty-ratio range of 0.6, use a small-value off-chip inductor of 1 uH, and achieve 91% peak power efficiency.

9:55 11-3 **Fully Integrated On-Chip DC-DC Converter with a 450x Output Range,** *Sudhir Kudva, Ramesh Harjani, University of Minnesota*

This paper presents a technique to efficiently supply power over a wide power range using a fully integrated on-chip converter for dynamic voltage scaling (DVS) based applications. All components, including filter elements, are integrated onchip. To achieve high efficiency the converter adaptively switches between different modes of operation by detecting the output current. The design, implemented in the IBM 130nm CMOS technology achieves a peak efficiency of 74.5% and can operate over a 450X power range (0.6mW to 266mW). This represents the best reported power range for a high-efficiency fully integrated on-chip power converter.

10:20 11-4 **A 140mA 90nm CMOS Low Drop-out Regulator with -56dB Power Supply Rejection at 10MHz,** *Ahmed Amer, Edgar Sánchez-Sinencio, Texas A&M University*

A high power supply rejection (PSR) low drop-out (LDO) voltage regulator employing a supply ripple cancellation adaptive technique is presented. The LDO is implemented in 90nm CMOS process and occupies an active area of 0.015mm^2. Measured PSR is better than -50dB up to 10MHz across the load current range of 140mA with a drop-out voltage of 0.15V and a current efficiency of 99.9%. Load regulation of 6mV for a 140mA current step is measured.

10:45 BREAK

11:05 11-5 **0.5-V Input Digital LDO with 98.7% Current Efficiency and 2.7-µA Quiescent Current in 65nm CMOS,** *Yasuyuki Okuma, Koichi Ishida*, Yoshikatsu Ryu, Xin Zhang*, Po-Hung Chen*, Kazunori Watanabe, Makoto Takamiya*, Takayasu Sakurai*, Semiconductor Technology Academic Research Center, *The University of Tokyo*

A digital LDO is proposed to provide the low noise and tunable power supply voltage to the 0.5-V near-threshold logic circuits. Because the conventional LDO feedback-controlled by the operational amplifier fail to operate at 0.5V, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V operation. The developed digital LDO in 65nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-µA quiescent current at 200-µA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.

11:30 11-6 **Smart Universal Control IC for High Loaded Factor Resonant Converters,** *Yujia Yang, Fabio E. Bisogno, Sadachai Nittayarumphong, Matthias Radecker, Marc Fahlenkamp*, Wolf-Joachim Fischer**, Fraunhofer IZM, *Infineon Technologies AG, **TU Dresden*

This paper presents an adaptive universal control IC with error protection functions for high loaded factor (Q>5) resonant converters . It has a wide frequency tuning range from 25 to 500 kHz. Duty cycle (Dc) tracking and synchronization (SY) are included to ensure zero voltage switching (ZVS). Automatic burst mode (BM) recognition is implemented by external resistive adjustment.The IC has been fabricated with Infineon 0.6 µm B6CA BiCMOS technology.

Session 12 – Low Phase Noise VCOS and ADPLL Building Blocks

Tuesday Morning, September 21
Pine Ballroom

Chair: Julian Tham, Arda Technologies
Co-Chair: Foster Dai, Auburn University

This session focuses on design techniques for GHz range low phase noise voltage-controlled oscillators and building blocks for all digital phase-locked loops.

9:00 **Introduction**

9:05 12-1 **A 4-Port-Inductor-Based VCO Coupling Method for Phase Noise Reduction,** *Zhiming Deng, Ali Niknejad, University of California, Berkeley*

A 4-port-inductor-based VCO coupling technique is introduced to improve VCO phase noise performance. Complete design steps including resonant network design and circuit topology selection are discussed and prototype designs have been demonstrated to verify the analysis. The proposed 12.8 GHz CCVCO design achieves phase noise of -116 dBc/Hz at 1 MHz offset, a tuning range of 31.4%, FOM and FOMT of 184 and 194 respectively.

9:30 12-2 **A 10 GHz Low Phase Noise VCO Employing Current Reuse and Capacitive Power Combining,** *Diptendu Ghosh, Stewart Taylor*, Yulin Tan*, Ranjit Gharpurey, University of Texas at Austin, *Intel Corporation*

A VCO employing capacitive power combining to reduce phase noise is presented. A current reuse technique is utilized to improve the phase noise per unit power metric over conventional LC oscillators. The VCO achieves a phase noise of -148.7 dBc/Hz at 20 MHz offset and a tuning range of 9.15-10.6 GHz while dissipating 30 mW from a 1.3 V supply. Implemented in a 45 nm CMOS technology, it achieves an FOM of 188 dBc/Hz while occupying an area of 0.67 mm^2.

9:55 12-3 **A 475 mV, 4.9 GHz Enhanced Swing Differential Colpitts VCO in 130 nm CMOS with an FoM of 196.2 dBc/Hz,** *Farhad Farhabakhshian, Thomas Brown*, Kartikeya Mayaram*, Terri Fiez*, Maxim Integrated Products, *Oregon State University*

An enhanced swing differential Colpitts VCO operates as low as 400 mV and enables oscillations to go beyond both the supply voltage and ground. Operating at 475 mV, the 4.9 GHz VCO consumes 2.7 mW. The 130 nm CMOS VCO's measured phase noise is -136.2 dBc/Hz at a 3 MHz offset frequency. The resulting FoM of 196.2 dBc/Hz makes it the highest performing integrated LC oscillator published to date.

10:20 12-4 **1.5-GHz CMOS Voltage-Controlled Oscillator Based On Thickness-Field-Excited Piezoelectric AlN Contour-Mode MEMS Resonators,** *Chengjie Zuo, Jan Van der Spiegel, Gianluca Piazza, University of Pennsylvania*

This paper reports on the first demonstration of a 1.5 GHz CMOS VCO based on TFE piezoelectric AlN contour-mode MEMS resonators. The measured phase noise is −85 dBc/Hz at 10 kHz offset frequency and −151 dBc/Hz at 1 MHz offset. This is the highest frequency MEMS oscillator ever reported using a laterally vibrating mechanical resonator. A tunable-supply oscillator design is proposed to enable this novel GHz VCO without using any low-Q tunable component.

10:45 **BREAK**

11:05 12-5 **A 1.56GHz Wide-Tuning All Digital FBAR-Based PLL in 0.13µm CMOS,** *Julie Hu, Richard Ruby*, Brian Otis, University of Washington, *Avago Technologies*

This paper presents the design rationale and measured results of a low power, low jitter, PVT-stable FBAR-based RF synthesizer implemented in 0.13um CMOS. A digitally controlled FBAR oscillator, tuned with a switched-capacitor array, provides 5800ppm of frequency tuning, sufficient to cover a wide range of manufacturing and temperature variations of an FBAR. An all-digital phase-locked loop (ADPLL) is used to stabilize the FBAR DCO. In the ADPLL architecture, we introduce a twostage time-to-digital converter (TDC) to detect phase differences between reference and divider clocks. The solution offers a fine TDC resolution without large and power-hungry TDC circuitry typically used to address in-band phase noise requirements. With the tuning range, the power consumption of 2.8 mW, and an integrated RMS jitter of 0.38ps from 10kHz to 20MHz, the FBAR ADPLL provides a PVT-stable, high quality RF frequency reference for a range of low power, high data rate applications.

11:30 12-6 **Spurious Free Time-to-Digital Conversion in an ADPLL using Short Dithering Sequences,** *Khurram Waheed, Mahbuba Sheba, Robert Bogdan Staszewski*, Fikret Dulger, Socrates Vamvakos, Texas Instruments Inc., *Technische Universiteit Delft*

This paper proposes an enhancement of the digital phase detection mechanism in an all-digital phase locked loop (ADPLL) operable at multi-GHz by randomization of the reference frequency phase by carefully chosen dither sequences. This renders the digital phase detector in the ADPLL free from any phase domain spurious tones as a consequence of ill-conditioned sampling of variable oscillator phase in the time-to-digital converter (TDC). TDC has a typical time quantization in the range of 5 to 30 ps using modern deep sub-micron technologies. This finite dead-band can result in spurious tones, whenever an “integer” relationship arises between the oscillator phase and the TDC sampling process. This anomaly can be resolved using carefully selected spectrum-friendly dithering mechanisms. This work proposes injection of a short sequence dither signal into the reference signal to overcome the quantization introduced limit-cycles. This results in a robust phase tracking and spurious free operation of the ADPLL.

11:55 12-7 **A 3-Dimensional Vernier Ring Time-to-Digital Converter in 0.13µm CMOS,** *Jianjun Yu, Fa Foster Dai, Auburn University*

A 3-dimensional Vernier ring time-to-digital converter (TDC) is presented for the first time that greatly improves the measurement time and power consumption and achieves large detectable range and fine resolution simultaneously. The TDC prototype chip achieves 16.5-ps resolution and an 8-bit detectable range with 0.16 mm^2 die area in a 0.13µm CMOS technology. The power consumption for the entire TDC is only 4.5mW with 1.5V power supply at 15MSps sample rate.

Session 13 - Forum 2
Biomedical and Bio-inspired Systems

Tuesday Morning, September 21
Cedar Ballroom

Chair: Ed Lee, Alfred Mann Foundation

9:00 am 13-1 **Architecting Therapeutic Interface Circuits and Algorithms for the Nervous System,** *Tim Denison, Medtronic*

This talk discusses prototyping sensor, algorithm and actuation technology for interfacing to the nervous system, with a particular focus on creating research tools for exploring treatments for chronic disease. While advances in technology might potentially help improve devices treating neurological conditions, designing a complete system is a complex engineering problem drawing on such diverse fields as applied physics, circuit design, algorithms/classifiers and biology. Fundamental to the design problem is a consideration of the physiology and anatomy of the neural circuits, which helps guide the designer on choosing the most appropriate interface strategy for a given application. Since many of the core operating principles of the nervous system are still being discovered, flexibility and addressing technology validation must also be considered. To put these concepts in context, we will provide an overview of recent work in academics and industry prototyping bi-directional brain-machine interfaces and closed loop systems for preclinical research. These systems seek to provide adaptive neuromodulation of a neural circuit based on detected biomarkers in the nervous system. The applications will highlight how advancements in merging silicon and biological systems might help someday advance the treatment of a variety of neurological disorders.

10:00 am 13-2 **Opportunities for RF integrated circuits in bio-molecular diagnostics,** *Ali Hajimiri, California Institute of Technology*

Silicon integrated circuits have seen a tremendous growth in the last half century. Today, we are at a point where we can integrate an unlimited (practically) number of transistors on a chip with remarkably high yields. We have also spent the last two decades understanding the fundamentals of high-performance RF and mm-wave system integration in silicon, which has led to the tremendous growth in portable RF systems. There is tremendous opportunity in combining these techniques in biological and bio-medical applications and combing them with new developments from the field of molecular machines to create truly novel and practical molecular detection and sensing systems. We will discuss some examples in the field of molecular diagnostics and discuss how silicon integration can enable truly handheld molecular diagnostics devices, where the low cost does not have to come at the price of low performance.

11:00 13-3 **Integrated Circuits for Bio-inspired and Biomedical Systems**, *Rahul Sarpeshkar, Massachusetts Institute of Technology*

Nature is a great analog and digital circuit designer. She has innovated circuits in the biochemical, biomechanical, and bioelectronic domains that operate very robustly with highly imprecise parts and with incredibly low levels of power. I will discuss how analog and bio-inspired circuits and architectures have led to and are leading to novel architectures in sensing and computing, e.g., in ear-inspired radios, architectures for improving operation in noise, neuron-inspired signal-to-symbol conversion, and hybrid analog-digital architectures that are inspired by computations within cells. Such techniques can lead to highly energy-efficient parallel architectures that operate rapidly and precisely and solve computationally intensive tasks. I will provide examples from systems built in my lab for bionic ear processors for the deaf, brain–machine interfaces for the blind and paralyzed, body sensor networks for cardiac monitoring, and in circuits for systems and synthetic biology.

Luncheon Keynote

Tuesday, 12:20 pm, September 21
Sierra Ballroom
Tickets for the luncheon are for sale at the Conference Registration Desk

From Pistons and Gears to Electronics and Software: The Coming Transportation Technology Disruption, *Ian Wright, Wrightspeed*

Electric vehicles have been around for more than a century. Heavy, ugly, slow, expensive, with short range and short life, they have been limited to golf carts and forklifts. From grocery getters to Formula One cars, pistons and gears have been the hot technology. That's about to change. Advances in battery technology, control and power electronics make electric drive the hot technology now. From parcel delivery vans to ultra-high performance cars, electric drive offers higher performance at a 10 times efficiency improvement, and for the first time, shifts transportation away from a total dependence on oil. In this Keynote, Ian Wright explains how this is possible, why it is inevitable, and how much fun it will be for engineers. The implications for vehicle electronics systems architecture are profound.

Ian Wright has over 20 years of experience as an entrepreneur and an operating executive. Since co-founding Tesla Motors in 2003, Ian has focused on electric drive system technology for vehicles. He founded Wrightspeed in 2005, building the world's fastest street-legal electric car as an early demonstrator. It's still unbeaten in 2010. Wrightspeed builds Range-Extended Electric Vehicle drive systems for high fuel consumption vehicles. Prior to Tesla, Ian was a co-founder or senior executive in several networking technology startups, including Altamar Networks (optical switching and ultra-long-haul transmission), QPSX (802.6 MAN), and Scitec (T1 TDMs.) He has also worked for some larger companies: DEC, NET (ATM switches) and Cisco (the terabit router project, for which he holds two patents.) Ian has broad interests in engineering from microelectronics through racecars and aeronautics. He has been a successful amateur racing driver, and is now an active pilot and owner of an experimental airplane. These interests extend to the social, economic, and policy implications of technology; in 2008 he was invited to consult with the NZ Government on the feasibility and implications of electrification of the vehicle fleet. A native New Zealander, Ian has lived and worked in Auckland, Sydney, and Perth before moving to Silicon Valley in 1993.

Session 14 – Novel Simulation and Modeling Techniques

Tuesday Afternoon, September 21
Oak Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting
Co-Chair: Hong-Ha Vuong, LSI Corporation

This session presents three novel, specialized simulation techniques for analog circuit design. In addition, there are two papers that present novel transmission line models.

2:00 **Introduction**

2:05 **Loop Finder Analysis for Analog Circuits,** *G. Peter Fang, Rod Burt, Ning Dong, Texas*
14-1 *Instruments*

The loop finder (LF) analysis is a newly developed method for automatic loop identification and full chip stability analysis. It allows designers to find local potentially problematic return loops in their analog circuits. Node impedance transfer functions in pole-residue format are utilized to generate second-order continuous-time system that approximate the loops. This method was implemented in our in-house Spice-like simulator and has been very helpful identifying instability problems.

2:30 14-2 **Noise Analysis of Non-Linear Dynamic Integrated Circuits,** *Amir Zjajo, Qin Tang, Michel Berkelaar, Nick van der Meijs, Delft University of Technology*

A time-domain methodology for noise analysis of non-linear dynamic integrated circuits with arbitrary excitations is presented. A non-stationary stochastic noise process is described as an Ito system of stochastic differential equations and a numerical solution for such a set of equations is found. Statistical simulation of specific circuits fabricated in 65 nm CMOS process shows that the proposed numerical methods offer accurate and efficient solution of stochastic differentials for noise analysis of integrated circuits.

2:55 14-3 **Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise,** *Takaaki Okumura, Masanori Hashimoto*, Semiconductor Technology Academic Research Center, *Osaka University*

This paper discusses how to cope with dynamic power supply noise in FF timing estimation. We first review the dependence of setup and hold time on supply voltage, and point out that setup time is more sensitive to supply voltage than hold time and hold time at nominal voltage is reasonably pessimistic. We thus propose a procedure to estimate setup time and clock-to-Q delay taking into account given voltage drop waveforms using an equivalent DC voltage approach. Experimental results show that the proposed procedure estimates setup time and clock-to-Q delay fluctuations well with 5% and 3% errors on average.

3:20 14-4 **Modelling and Measurement on minimum-width Transmission-lines from 10-67 GHz in 65 nm CMOS,** *Paul van Zeijl, Henry van der Zanden, Bob Theunissen, Henk Termeer, Philips Research*

Transmission-line models for high-frequency wideband applications should preferably directly relate to the physical dimensions and effects. Various simulation modes (both linear and non-linear in the frequency- and time-domain) point towards the use of a straightforward model using frequency dependent resistances, inductances, and capacitances. However, not all simulators accept frequency dependent elements. This paper presents the design, characterisation and modelling results of 35, 50 and 70 ohm minimum-width transmission lines and 90 degree corners in the TSMC 65 nm process for high frequency (10-67 GHz) applications using frequency-independent elements.

3:45 14-5 **A Novel Equivalent Circuit For On Chip Transmission Lines Modeling,** *Dajie Zeng, Hongrui Wang*, Dongxu Yang*, Li Zhang*, Yan Wang*, Zhiping Yu*, Yaohui Zhang, Institute of SINANO, Tsinghua University*

Microstrip transmission line (MS), coplanar waveguide transmission line (CPW), grounded coplanar waveguide transmission line (GCPW), slow-wave transmission line with slotted grounded shields (GSCPW), and slow-wave transmission line with slotted floating shields (FSCPW) are widely used in silicon technology. Because the quasi-TEM assumption is still valid in these structures, an equivalent circuit is proposed to model all these structures. In this work, we notice that for some types of transmission lines, say GCPW and GSCPW, the per unit length capacitance increases with frequency. An LC series subcircuit is proposed to model this phenomenon. For CPW, GCPW, GSCPW and FSCPW, the model has very good accuracy and fits the measurement results very well up to the highest measurement frequency (40GHz). For

MS, the results from the 3D EM simulation software are adopted and the model shows a great agreement with the simulation results up to the highest simulation frequency (100GHz).

4:10 BREAK

Session 15 – 3D Design Considerations

Tuesday Afternoon, September 21
Fir Ballroom

Chair: Rakesh Patel, GlobalFoundries
Co-Chair: John Biggs, ARM LTD.

Stacking die introduces stress levels and thermal distribution challenges that are significantly higher than in 2D. This session introduces TSV related design-verification challenges and solutions, as well as mitigating low power techniques.

2:00 **Introduction**

2:05 15-1 **Verifying Electrical/Thermal/Thermo-mechanical Behavior of a 3D Stack – Challenges and Solutions (INVITED),** *Geert Van der Plas, Steven Thijs, Dimitri Linten, Guruprasad Katti, Paresh Limaye, Abdelkarim Mercha, Michele Stucchi, Herman Oprins, Bart Vandevelde, Nikolas Minas, Miro Cupac, Morin Dehan, Marc Nelis, Rahul Agarwal, Wim Dehaene, Youssef Travaly, Eric Beyne, Paul Marchal, IMEC*

We describe the design challenges for a low-cost 130nm 3D CMOS technology with 5µm diameter at 10µm pitch Cu-TSV. We investigate electrical, thermal and thermo-mechanical issues encountered in 3D. The electrical yield and ESD of TSVs is reviewed and designers are advised how to ensure yield and reliability. For thermal and thermo-mechanical we'll indicate based on experimental characterization, the importance of extending the chip package co-design flow with thermo-mechanical simulations of the chip stack. We propose a new design flow which leverages information captured by smart samples.

2:55 15-2 **Simulation Methodology and Flow Integration for 3D IC Stress Management,** *Mark Nakamoto, Riko Radojcic, Wei Zhao, Vinay K. Dasarapu*, Aditya P. Karmarkar*, Xiaopeng Xu*, Qualcomm Inc., *Synopsys Inc.*

This paper describes a method/flow to model stress in 3D packed chip stacks. A new methodology to bridge package and silicon domain simulations is demonstrated using a new data file to facilitate stress information exchange. The flow integration uses equivalent stress conditions to replace sensitive process information and parameterized modules to minimize user interventions for 3D IC stress simulations.

3:20 15-3 **Ultra-Low Power Circuit Techniques for a New Class of Sub-mm^3 Sensor Nodes (INVITED),** *Yoonmyung Lee, Gregory Chen, Scott Hanson, Dennis Sylvester, David Blaauw, University of Michigan*

Bell's Law predicts continual reductions in the size of computing systems. We investigate the status of the next paradigm shift that will usher in ubiquitous computing – sub-mm3 sensor nodes. However, this form factor remains beyond the capabilities of modern integrated circuit design techniques due to battery size. This paper describes new ultra-low power circuit techniques applied to digital processors, memory, power management, and a special focus on standby mode operation, that will bring mm3 sensor nodes to reality.

4:10 BREAK

Session 16 – Optical Communication IC's and PLL's

Tuesday Afternoon, September 21
Pine Ballroom

Chair: Gu-Yeon Wei, Harvard University
Co-Chair: Wei-Zen Chen

This section presents high performance transceivers and drivers for multi-gigabits optical communications and advanced PLL techniques for wireline systems.

2:00 **Introduction**

2:05 16-1 **A 25 Gb/s × 4-channel 74 mW/ch Transimpedance Amplifier in 65 nm CMOS,** *Takashi Takemoto, Fumio Yuki, Hiroki Yamashita, Shinji Tsuji, Tatsuya Saito, Shinji Nishimura, Hitachi, Ltd.*

25 Gb/s × 4-channel transimpedance amplifier has been realized in 65-nm CMOS technology. It achieves transimpedance gain of 69.8 dBΩ, bandwidth of 22.8 GHz, and gains flatness of ±2 dB after equalizing the effect of transmission loss, incorporating gain-stage amplifier with flat frequency response, and 50Ω output driver with an analogue equalizer. Our TIA dissipates only 74 mW/ch and demonstrates the transimpedance bandwidth products per DC power of 952.1 GHzΩ/mW and crosstalk of under -17dB.

2:30 16-2 **Progress and Trends in Multi-Gbps Optical Receivers with CMOS Integrated Photodetectors (INVITED),** *Anthony Chan Carusone, Hemesh Yasotharan, Tony Kao, University of Toronto*

There has been significant recent progress towards the realization of multi-Gbps optical receivers fully integrated into standard CMOS processes. Although CMOS photodetectors exhibit performance inferior to discrete photodetectors, they offer the potential for a low-cost highly-integrated solution that suits growing and emerging applications in short-reach optical communication. Past work has focused on using the pn-junctions and depletion regions available in standard CMOS process flows to eliminate, minimize, or cancel the slowly diffusing photocarriers that usually limit the bandwidth of CMOS photodetectors. However, if considered simply as a form of ISI, the slowly diffusing carriers can be dealt with using the same signal processing tools in wide use for other wireline communication applications, including decision feedback equalization. A combination of spatially-modulated light detection, analog equalization, and modest decision feedback equalization appears to offer a path towards data rates in excess of 10-Gbps using integrated photodetectors. Nanoscale CMOS is particularly well suited to the implementation of such signal processing functions. Measured results of photodetectors implemented in a standard 65-nm CMOS process are presented.

3:20 16-3 **A 40-Gb/s Optical Transceiver Front-end in 45nm SOI CMOS Technology,** *Joohwa Kim, James Buckwalter, University of California-San Diego*

A low-power, 40-Gb/s optical transceiver front-end is demonstrated in a 45 nm silicon on insulator (SOI) CMOS technology. A modulator driver uses floating body devices to realize voltage swing of 2 VPP with a small-signal gain of 7.6 dB over 33 GHz. The optical receiver consists of a transimpedance amplifier (TIA) and post-amplifier with 55-dB·Ω of transimpedance over 30 GHz. The group delay variation is ±3.9 ps over the 3-dB bandwidth and the average input-referred noise density is 20.47 pA/√Hz. The TIA consumes 9 mW from a 1 V supply for a transimpedance figure of merit of 1874.5 Ω/pJ. To the author's knowledge, this represents the lowest power consumption for a transmitter and receiver operating at 40-Gb/s in

a CMOS process.

3:45 16-4 **A 25Gb/s Laser Diode Driver with Mutually Coupled Peaking Inductors for Optical Interconnects,** *Norio Chujo, Tsuneo Kawamata, Kenichi Ohhata*, Toshinobu Ohno*, Hitachi Ltd., *Kagoshima University*

This paper describes a LD driver for optical interconnects. A main driver with mutually coupled peaking inductors and pre-driver with CMOS dual-loop active-feedback makes possible 25Gb/s operation with low power consumption (142mW, 5.7mW/Gb/s) and small area occupation ($95\times115\mu m^2$).

4:10 BREAK

4:25 16-5 **A 16Gbps Laser-Diode Driver with Interwoven Peaking Inductors in 0.18-µm CMOS,** *Takeshi Kuboki, Yusuke Ohtomo*, Akira Tsuchiya, Keiji Kishine**, Hidetoshi Onodera, Kyoto University, *NTT Corporation, **University of Shiga Prefecture*

A laser-diode (LD) driver with interwoven mutually-coupled peaking inductors for high-speed optical networks is presented. Six and four inductors are interwoven into two sets of inductors for area-effective implementation as well as performance enhancement. The proposed circuit is fabricated in CMOS 0.18-µm process. The circuit area is $0.34mm^2$ and the maximum operating speed is 16Gbps. Compared to a conventional LD driver in 0.18-µm CMOS, the proposed circuit achieves 1.6 times faster operation, 26% smaller area with 60% reduction in power consumption under the condition for the same amount of data transmission and the LD driving current.

4:50 16-6 **An Energy-Efficient Ring-Oscillator Digital PLL,** *John Crossley, Eric Naviasky*, Elad Alon, University of California, Berkeley, *Cadence*

A linear but fully digital phase control path and a bang-bang frequency control path enable an energy-efficient digital ring-oscillator PLL architecture. A 65nm CMOS prototype occupies 150µm x 170µm of area and generates a 3GHz clock from a 300MHz reference with 1.13ps rms period jitter while consuming 2mW from a single 1V power supply.

5:15 16-7 **An Offset Phase-Locked Loop Spread Spectrum Clock Generator for SATA III,** *Chin-Yu Lin, Chun-Yu Chiang, Tai-Cheng Lee, National Taiwan University*

A spread spectrum clock generator (SSCG) based on an offset phase-locked loop (OPLL) for the Serial AT Attachment 3 (SATA-III) is presented in this paper. The SSCG can be applied to many systems due to its characteristic of spreading the energy of frequency harmonics and reducing the radiated power per unit bandwidth. In the proposed architecture, a low-frequency spread spectrum signal is synthesized by a direct digital frequency synthesizer (DDFS) and mixed with a high frequency signal to produce a higher modulated reference source. The OPLL is employed to lock its output with the modulated reference to generate the desired spread spectrum clock. This SSCG is fabricated in a 0.13-µm RF CMOS technology and its area is 0.7 x 0.45 mm^2. It reduces main tone power by 16dB while drawing 21.16 mW from a 1.2 V supply.

Session 17 – On Die Test and Debug Enabler at 65nm and Beyond

Tuesday Afternoon, September 21
Cedar Ballroom

Chair: Manoj Sachdev, University of Waterloo
Co-Chair: Gordon Roberts, McGill University

The first two papers discuss how embedded circuits can be used to identify/debug 45 nm silicon. The third paper demonstrates how an antenna matrix can be used to develop the SOC EMI profile.

2:00 **Introduction**

2:05 17-1 **Dynamic Variation Monitor for Measuring the Impact of Voltage Droops on Microprocessor Clock Frequency,** *Keith Bowman, Carlos Tokunaga, James Tschanz, Arijit Raychowdhury, Muhammad Khellah, Bibiche Geuskens, Shih-Lien Lu, Paolo Aseron, Tanay Karnik, Vivek De, Intel Corporation*

A 45nm microprocessor integrates a dynamic variation monitor (DVM) to measure dynamic path-level frequency changes. Measurements reveal the sensitivity of the microprocessor maximum clock frequency (Fmax) to high-frequency voltage droops and demonstrate the DVM capability of tracking Fmax changes to within 1% for a wide range of voltage droop profiles.

2:30 17-2 **Dynamic NBTI Management Using a 45nm Multi-Degradation Sensor,** *Prashant Singh, Eric Karl*, Dennis Sylvester, David Blaauw, University of Michigan, Ann Arbor, *Intel*

We propose a low power unified oxide and NBTI degradation sensor designed in 45nm process node. The cell power consumption is 105 lower than a previously proposed sensor. The unified nature enables efficient reliability monitoring with reduced sensor deployment effort and area overhead. Using the sensor Dynamic NBTI Management (DNM) has been implemented for the first time. DNM trades the excess 'reliability-margin' present in the design, due to better than worst case operating conditions, with performance. For the typical case shown in this paper, DNM allows for an average boost of 90mV in accelerated supply voltage while bringing down the excess NBTI margin of 22.5mV to 8mV where the total NBTI budget was of 66mV.

2:55 17-3 **EMI Camera LSI (EMcam) with 12 x 4 On-Chip Loop Antenna Matrix in 65-nm CMOS to Measure EMI Noise Distribution with 60-µm Spatial Precision,** *Naoki Masunaga, Koichi Ishida, Makoto Takamiya, Takayasu Sakurai, University of Tokyo*

An EMI Camera LSI (EMcam) with a 12 x 4 on-chip 250um x 50um loop antenna matrix in 65nm CMOS is developed. EMcam achieves both the 2D electric scanning and 60um-level spatial precision for the first time. The down-conversion architecture increases the bandwidth of EMcam and enables the measurement of EMI spectrum. Shared IF block scheme is proposed to alleviate the increasing power and area penalty inherent to the matrix measurement. 'Mixer and antenna selector (MAS)' reduces the switches and prevents the EMI attenuation due to the switches. EMI measurement with the smallest 32um x 12um antenna to date is also demonstrated.

Session 18 -Panel Discussion
Will "Digital RF" Replace RFIC Designers in Ten Years?

Tuesday Afternoon, September 21
Cedar Ballroom

4:25pm – 5:30pm

Over the years, RF IC designers have taken pride in their craft as being the "black magic", requiring highly skillful and creative minds to craft the circuits operating at high frequencies. Such art, however, has reached a level of maturity and publications reflect efforts to utilize high frequency sampling and signal processing techniques to replace the traditional analog frontends, and make these circuits more amenable to technology scaling and the possibly of automatic synthesis and placement. A panel of experts discusses the possibility of such techniques becoming mainstream, and replacing the "black magic" trade of RFIC designers in ten years.

Moderator:
Prof. Behzad Razavi, *Professor, UCLA*

Panelists:
Dr. Hooman Darabi, *Sr. Engineering Director, Broadcom Corp.*
Mr. Srenik Mehta, *Engineering Director, Atheros Communications*
Prof. Ali Niknejad, *Professor, UC Berkeley*
Prof. Jacques Rudell, *Professor, University of Washington*
Dr. Khurram Waheed, *Senior Systems Engineer, Freescale Semiconductor*

Poster Session

Tuesday Evening, September 21
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

T-1 **A CMOS Programmable Gain Amplifier with a Novel DC-offset Cancellation Technique,** *Xiaojie Chu, Min Lin, Zheng Gong, Yin Shi, Fa Foster Dai*, Suzhou-CAS Semiconductors Integrated Technology Research Center, *Auburn University*

A programmable gain amplifier with a novel DC offset cancellation technique for IEEE 802.11b/g wireless LAN direct-conversion receiver is presented. An operational amplifier utilizing an improved Miller compensation approach is adopted in this PGA design. A gain tuning range of 0dB to 56dB with 2dB per tuning step is achieved. The DCOC loop is based on a voltage-current negative feedback that includes a switchable bandwidth algorithm to speed up the settling time of DC offset cancellation. The proposed approach requires no external components and demonstrates excellent DC offset cancellation capability in measurement. Fabricated in a 0.13 µm CMOS technology, this PGA dissipates 9.7mW from a 1.2 V supply voltage and occupies an area of 0.17 mm2.

T-2 **A Micropower Delta-Sigma Modulator based on a Self-Biased Super Inverter for Neural Recording Systems,** *Le Wang, Luke Theogarajan, University of California, Santa Barbara*

This paper presents a micropower 2nd order switched-capacitor delta-sigma modulator based on a novel self-biased fully differential super inverter for neural recording systems. The prototype modulator is implemented in a 0.13 µm CMOS process and achieves 68dB DR over the 8 KHz neural signal bandwidth, while consuming only 4.8 µW from 1.2 V supply.

T-3 **A 1.16mW 69dB SNR (1.2MHz BW) Continuous Time ΣΔ ADC with Immunity to Clock Jitter,** *Ganesh Balachandran, Venkatesh Srinivasan, Vijay Rentala, Srinath Ramaswamy, Texas Instruments Inc.*

A low-power jitter tolerant 2nd order active-passive continuous-time sigma-delta ADC in 65nm CMOS is presented. The use of just one active Gm-C integrator and a feed-forward path from the ADC's input to the Gm's output helps reduce power consumption. A FIR filter in the outermost feedback path reduces clock jitter impact. For a -2dBFS input, the ADC clocked at 300MHz achieves a 69dB SNR (10KHz – 1.2MHz BW) while consuming 1.16mW from a 1.4V supply.

T-4 **A 10 bit Piecewise Linear Cascade Interpolation DAC with Loop Gain Ratio Control,** *Sungwoo Lee, Kiduk Kim, Kyusung Park, Changbyung Park, Byunghun Lee, Jinyong Jeon, Seungchul Jung, Jin Huh, Junhyeok Yang, Hyunsik Kim, Gyu-Hyeong Cho, KAIST*

This paper proposes a 10 bit linear interpolation digital-to-analog converter (DAC) with area efficiency and a high resolution for an AMLCD drive. Because this proposed structure

implements a 1 bit interpolation circuit with a control block for a loop gain ratio, it shows a wide voltage range of interpolation as well as superior linearity. The proposed circuit is fabricated with Samsung 90nm CMOS 1.5V / 5V technology. The power dissipation is 7uW/channel, and the chip area of the 10 bit piecewise linear DAC is only 91% of the area of a conventional 8 bit resistor DAC. The INL and DNL properties are +0.8LSB/-0.2LSB and +0.23LSB/-0.23LSB, respectively. The maximum interchannel DVO is 10mV without the application of any offset cancellation techniques.

T-5 **A 9.15mW 0.22mm^2 10b 204MS/s Pipelined SAR ADC in 65nm CMOS,** *Young-DeukJeon, Young-Kyun Cho, Jae-Won Nam, Kwi-Dong Kim, Woo-Yol Lee*, Kuk-Tae Hong*, Jong-Kee Kwon, ETRI, *LG Electronics*

This paper describes a 10b 204MS/s analog-to-digital converter (ADC) employing a pipelined successive approximation register (SAR) architecture for low power consumption and small area. To improve the operation frequency, the pipelined SAR ADC consists of two channels with a proposed asynchronous timing technique. This technique increases the amplification time of a residue opamp. To reduce power and area, the opamp is shared between two channels. A reference buffer with a deglitch circuit reduces the glitch and settling time of reference voltages. The prototype ADC fabricated in a 65nm CMOS process shows a SNDR of 55.2dB and a SFDR of 63.5dB with a 2.4MHz input at 204MS/s. The ADC occupies 0.22mm^2 and dissipates 9.15mW at a 1.0V supply. The FoM of the ADC is 95.4fJ/conversion-step.

T-6 **A 9µW 88dB DR Fully-Clocked Switched-Opamp ΔΣ Modulator with Novel Power and Area Efficient Resonator,** *Jian Xu, Xiaobo Wu, Hanqing Wang, Bill Liu*, Menglian Zhao, Zhejiang University, China, *Analog Devices*

A 9µW 88dB DR switched-opamp (SO) ΔΣ modulator is implemented in a low cost 0.35µm CMOS process. To evaluate the effects of finite voltage gain and 1/f noise clearly, two high efficient methods are introduced. And a new fully switched-off SO with a 50% power saving and double Figure-of-Merit (FOM) over the traditional type is proposed to reduce the total power. Besides, to improve the performance, a novel resonator idea applicable to SO technique is adopted to realize a coefficient of 1/100 with 75% power and 70% area reduction over the conventional design. The FOM of the designed modulator is highest among the collected recent low power modulators.

T-7 **A Low-Supply PLL with Enhanced Cascode Compensation and a Low-Supply-Sensitivity CCO,** *Xiong Liu, Alan Willson, UCLA*

Multiple techniques are proposed to realize a selfcontained low-supply PLL macro that can share a digital supply thereby saving one supply regulator on the board. Enhanced Cascode Compensation features fast and slow loops to regulate the supply noise without the need of a replica. A novel topology for a current controlled oscillator (CCO) improves the supply noise rejection by more than 10 dB. A built-in 0.6V bandgap avoids the need for another 1.8V supply. Implemented in a 0.18-µm CMOS process, the whole PLL consumes less than 4 mW for 800-MHz operation. The measured random jitter is less than 2 ps. These features make it ideal for SoC integration.

T-8 **Realization of 0.7-V Analog Circuits by Adaptive-Vt Operation of FinFET,** *Shin-ichi O'uchi, Kazuhiko Endo, Yongxun Liu, Takashi Matsukawa, Yuki Ishikawa, Junichi Tsukada, Toshihiro Sekigawa, Hanpe Koike, T. Nakagawa, Kunihiro Sakamoto, Meishoku Masahara, National Institute of AIST*

An adaptive-threshold-voltage differential pair and a low-voltage source follower using independent-double-gate- (IDG-) FinFETs are proposed for a low-voltage operational amplifier (op amp). These circuits were implemented by our FinFET technology that enables co-integration of connected-DG- (CDG-) and IDG-FinFETs. The proposed components enable a

two-stage op amp to accept the input below the nominal threshold voltage. More than 40-dB gain and 1-MHz GBW in the 500-mV-wide CM input range under 0.7-V supply voltage was estimated by SPICE simulation. Our preliminary silicon implementation demonstrated 0.7-V operation of the proposed source follower.

T-9 **A Low-power Area-efficient Switching Scheme for Charge-sharing DACs in SAR ADCs,** *Fred Chen, Anantha Chandrakasan, Vladimir Stojanovic, Massachusetts Institute of Technology*

Analysis and experimental results for a new switching scheme and topology for charge-sharing DACs used in SAR ADCs is presented. The SAR algorithm is exploited to develop a switching scheme that reduces the number of required unit capacitors by nearly 10x over conventional charge sharing DACs without the aid of any additional reference voltages. An 8-bit SAR ADC is implemented in a 90nm CMOS process and consumes 700nW at 0.7V and 100kS/s while occupying 0.0135mm^2.

T-10 **A 50-300-MHz Low power and High Linear Active RF Tracking Filter for Digital TV Tuner ICs,** *Yang Sun, Chang-jin Jeong, In-young Lee, Jeong-seon Lee, Sang-gug Lee, Korea Advanced Institute of Science and Technology*

A low power and highly linear CMOS active tracking bandpass filter is presented to overcome a local oscillator harmonic mixing problem for Digital TV tuner ICs. A transconductor linearization technique based on a method of dynamic source degenerated differential pair is adopted to improve the linearity performance. The newly proposed low power high quality factor (Q) biquad and the linearized transconductor with negative resistance load (NRL) enables a low power and high Q RF tracking filter design. The total chip area is 0.25 mm X 0.9 mm. The fabricated tracking filter based on the 0.13 um CMOS process shows 48~300 MHz tracking range with 10~50 MHz bandwidth, more than 38 dB 3rd order harmonic rejection, 6 dB unwanted signal rejection@N+6 channel offset, and a maximum IIP3 of 6 dBm at 5 dB gain while drawing 6.4 mA from a 1.2 V supply.

T-11 **A 2.6Gb/s 1.56mm^2 Near-Optimal MIMO Detector in 0.18µm CMOS,** *Tae-Hwan Kim, In-Cheol Park, KAIST*

This paper presents an ASIC implementation of a multi-Gb/s MIMO detector targeting 4x4 16-QAM systems. A modified Dijkstra's algorithm and a pre-calculation technique are proposed to improve the throughput up to 2.6Gb/s, and the Euclidean norm computation is approximated to reduce the chip area. The entire detector occupies 1.56mm^2 in 0.18µm CMOS. In achieving a BER of 10^{-3}, the performance is only 0.1dB away from that of the optimal detection in terms of SNR.

T-12 **Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory,** *Michael B.Healy, Krit Athikulwongse, Rohan Goel, Mohammed M. Hossain, Dae Hyun Kim, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Moongon Jung, Brian Ouellette, Mohit Pathak, Hemant Sane, Guanhao Shen, Dong Hyuk Woo, Xin Zhao, Gabriel H. Loh, Hsien-Hsin S. Lee, Sung Kyu Lim, Georgia Institute of Technology*

We describe the design and analysis of 3D-MAPS, a 64-core 3D-stacked memory-on-processor running at 277 MHz with 63 GB/s memory bandwidth, sent for fabrication using Tezzaron's 3D stacking technology. We also describe the design flow used to implement it using industrial 2D tools and custom add-ons to handle 3D specifics.

T-13 **A Customized Design of DRAM Controller for On-Chip 3D DRAM Stacking,** *Tao Zhang, Kui Wang*, Yi Feng**, Xiaodi Song*, Lian Duan, Yuan Xie, Xu Cheng**, Youn-Long Lin***, The Pennsylvania State University, *Peking University Unity Microsystems Technology Co. Ltd, **Peking University, ***National Tsing Hua University*

This paper introduces the implementation of 3D on-chip memory controller which is integrated in a 3D SoC architecture to demonstrate the feasibility of 3D memory stacking. It also presents a parallel access policy to improve the bandwidth. In addition, the 3D memory stacking is illustrated in the end of paper. The whole chip has been fabricated in Chartered 130nm process with Tezzaron's 3D bonding technology.

T-14 **A Sub-Threshold FPGA with Low-Swing Dual-V^{DD} Interconnect in 90nm CMOS,** *Joseph Ryan, Benton Calhoun, University of Virginia*

This paper presents a sub-threshold field programmable gGate array (FPGA) that uses a low-swing dual-VDD global interconnect fabric to reduce energy and improve delay. A 90nm chip implements the FPGA with 1134 LUTs, which is 2.7X smaller, 14X faster, and 4.7X less energy than a sub-threshold FPGA using conventional interconnect and 22X less energy than an equivalent FPGA at full VDD.

T-16 **A 34.7-mW Quad-Core MIQP Solver Processor for Robot Control,** *Hiroki Noguchi, Junichi Tani, Yusuke Shimai, Masanori Nishino, Shintaro Izumi, Hiroshi Kawaguchi, Masahiko Yoshimoto, Kobe University*

We propose a quad-core mixed integer quadric programming (MIQP) solver processor. The MIQP solver is applicable to hybrid control systems including real-time control robotics. Using multi-core architecture, fixed-point calculations, and branch-and-bound method with high-dispersion performance while processing a 50-variable problem, our design achieves 34.7-mW operation at a frequency of 52 MHz in measurement results, although a core 2 duo PC requires 3.16 GHz to solve it as rapidly.

T-17 **Data-Dependant Sense-Amplifier Flip-Flop for Low Power Applications,** *Farshad Moradi, Charles Augustine, Ashish Goel, Georgeos Karakonstantis, Tuan Vu Cao*, Dag Wisland*, Hamid Mahmoodi**, Kaushik Roy, Purdue University, *University of Oslo, **San Francisco State University,*

In this paper, we present a new sense amplifier based flip-flop that exploits input data activity, to achieve reduced power consumption. The internal nodes of the proposed flip-flop are charged/discharged only when the input data changes state. Simulations show that the power consumption of proposed flip-flop is reduced by 20% to 70% compared to standard sense-amplifier flip-flop. An FIR-filter based on the proposed flip-flop, implemented in 45nm ST process, shows more than 42% improvement in power consumption (with 5% delay penalty) compared standard sense-amplifier flip-flops

T-18 **A 2.5-8Gb/s Transceiver with 5-Tap DFE and Second Order CDR Against 28-inch channel and 5000ppm SSC in 40nm CMOS Technology,** *Wei-Chih Chen, Chien-Chun Tsai, Chih-Hsien Chang, Yung-Chow Peng, Fu-Lung Hsueh, Tsung-Hsin Yu, Jinn-Yeh Chien, Wen-Hung Huang, Chi-Chang Lu, Mu-Shan Lin, Chin-Ming Fu, Shu-Chun Yang, Chung-Wing Wong, Wan-Te Chen, Chin-Hua Wen, Li-Yueh Wang, Chiang Pu, TSMC*

This paper presents a 2.5-8Gb/s transceiver for PCI Express Gen3.0/2.0/1.0 applications. To overcome channel loss of high bit rate application, a linear equalizer (LEQ) and decision feedback equalizer (DFE) are used to eliminate ISI effect, compensate channel loss, and improve BER performance for 28-inch FR4 channel. The 3-tap feed-forward equalizer (FFE) is used to improve signal quality in transmitter. The resolution of de-emphasis and pre-shoot is up to 1/63 and 1/15. It also performs 0.8UIpp eye opening for 8Gb/s operation. A second order clock and data recovery (CDR) employs digital finite state machine to track phase difference and frequency between clock and data. The CDR can cover 0 to -5000ppm frequency offset of SSC modulation and achieve jitter tolerance of up to 0.2UIpp at 8Gb/s with a BER=10-10 when all specified jitter sources is included. The integrated transceiver operates from 2.5Gb/s to 8Gb/s and consumes 235mA at 8Gb/s current with 0.95V supply voltage. The test-chip is

implemented by flip chip layout and fabricated in TSMC 40nm 0.9V/1.8V CMOS technology. The area of transceiver is 725um x 615um.

T-19 **A Crosstalk-and-ISI Equalizing Receiver in 2-Drop Single-Ended SSTL Memory Channel,** *Jun-Hyun Bae, Young-Soo Sohn*, Seung-Jun Bae*, Kwang-Il Park*, Joo-Sun Choi*, Young-Hyun Jun*, Jae-Yoon Sim, Hong-Jun Park, POSTECH, *Samsung Electronics*

An equalizer circuit which minimizes both crosstalk and ISI is applied to a receiver with a strongly-coupled two-parallel two-drop single-ended microstrip SSTL memory channel. The crosstalk equalizer adds a crosstalk-canceling pulse to a victim receiver signal to make the signal crosstalk-free during the transition interval of an incoming signal. A DFE is used for ISI compensation. The equalization of both crosstalk and ISI increases the data rate for BER < 1E-12 from 2.5Gbps to 3.6Gbps (+44%) with a 0.18μm CMOS process.

T-20 **A 100MHz-to-1GHz Open-Loop ADDLL with Fast Lock-Time for Mobile Applications,** *Mi-Jo Kim, Lee-Sup Kim, KAIST*

This paper presents a fast-lock wide-range all-digital delay locked loops (ADDLL) for mobile applications. The proposed open-loop architecture based on time-to-digital converter (TDC) has a lock time of 3~10 clock cycles. The multi-path delay line is implemented to achieve high resolution in TDC. The frequency range selector is adopted for a wide-range operation. The ADDLL is implemented in a 0.18μm CMOS process and operates from 100MHz to 1GHz.

T-21 **A 16 Gb/s Four-Wire CDMA-Based High Speed I/O Link with Transmitter Timing Adjustment,** *Tzu-Chien Hsueh, Sudhakar Pamarti, University of California, Los Angeles*

A simplified code division multiple access (CDMA) technique has been used to cancel crosstalk in a four-wire signaling high-speed I/O system. To further improve the crosstalk suppression and power efficiency, transmitter (TX) timing adjustment in conjunction with the CDMA-based I/O system is proposed. The integrated transceiver achieves an aggregate 16 Gb/s (5.33 Gb/s/link) data rate and 6 mW/Gb/s/wire power efficiency over four 6" FR4 PCB traces with BER < 1e-12 in a 90 nm standard CMOS technology.

T-22 **Interpolated VCO Design for a Low Bandwidth, Low-Jitter, Self-Bbiased PLL in 45 nm CMOS,** *David Duarte, Suching Hsu*, Keng Wong**, Mingwei Huang, Greg Taylor, Intel Corp *Qualcomm Corp., **Anax Corp.*

A novel self-biased PLL design incorporating a low-gain interpolated inverter-based ring oscillator VCO achieves lower bandwidth and jitter without sacrificing PSRR or area. Charge pump programmability provides an effective mechanism for bandwidth adjustments. Data collected on a high-k, metal gate 45 nm process confirms the suitability of the proposed scheme.

T-23 **Process Variation Tolerant All-Digital Multiphase DLL for DDR3 Interface,** *Heechai Kang, Kyungho Ryu, DongHwan Lee*, Won Lee*, SuHo Kim*, JongRyun Choi*, Seong-Ook Jung, Yonsei University, *Samsung Electronics*

An all-digital multiphase DLL is presented that is robust to delay mismatch due to process variation. Each of four 90° phase shift blocks accurately align each phase to 90° delay using its own ring oscillator and locking delay code. Harmonic locking is protected by a ring oscillator and a counter. An area efficient binary to thermometer converter is proposed to diminish the area overhead due to four delay line controllers. An edge combiner is used for duty cycle correction and clock 2x multiplications. The measured large locking delay code difference between four 90° phase shift delay lines in the proposed DLL implemented in 45nm CMOS process, which corresponds to ±31ps at 800MHz, proves that the DLL corrects significant phase error caused by delay mismatch. Phase shift accuracy errors at 90° and 270° phases are 0.43° and 1.01°,

respectively, and output frequency is 1.6GHz with 50% duty cycle at 800MHz. Power consumption is 3.3mW at 800MHz.

T-24 **Varactor-Based Signal Restoration for Near-Speed-of-Light Surfing Global Interconnect,** *Suwen Yang, Robert Drost, Mark Greenstreet*, Shahriar Mirabbasi*, Frank O'Mahony**, Oracle Corporation, *University of British Columbia, ** Intel Corporation*

We present a varactor-based "near-speed-of-light" interconnect design. The varactors compensate for delay variations enabling a simple, source-synchronous solution for clock-and-data recovery. Furthermore, the varactors provide pulse shaping that reduces ISI. We implemented these interconnects in the TSMC 90 nm CMOS process and present test results for 16 mm long lines.

Session 19 – Nyquist ADCs

Wednesday Morning, September 22
Oak Ballroom

Chair: David Nairn, University of Waterloo
Co-Chair: Takahiro Miki, Renesas Electronics Corp.

The need for speed and minimum power continues to drive advances in ADCs. These papers each adopt a different approach to the speed/power tradeoff.

9:00 **Introduction**

9:05 19-1 **An 8-bit 1.5GS/s Flash ADC Using Post-Manufacturing Statistical Selection,** *Jonathan Proesel, Gokce Keskin, Jean-Olivier Plouchart*, Lawrence Pileggi, Carnegie Mellon University, *IBM TJ Watson Research* Center

An 8-bit, 1.5GS/s flash ADC is presented. Comparators are digitally calibrated using statistical selection. INL of 1.32 LSB and DNL of 1.23 LSB are achieved. Average comparator noise of 5mVrms (1.3 LSB) limits SNDR to 37dB at low frequencies. Total power is 35mW, 20mW in the S&H and 15mW in the ADC core. The figure of merit is 0.42pJ/conv, the best reported for 1+GS/s, 7+-bit ADCs.

9:30 19-2 **Single-Channel, 1.25-GS/s, 6-bit, Loop-Unrolled Asynchronous SAR-ADC in 40nm-CMOS,** *Tao Jiang, Wing Liu*, Freeman Y Zhong*, Charlie Zhong*, Patrick Y Chiang, Oregon State University, *LSI Corporation*

A single channel, loop-unrolled, asynchronous successive approximation (SAR) ADC fabricated in 40nm CMOS is presented. Compared with a conventional SAR structure that exhibits significant delay in the digital feedback logic, the proposed 6b SAR-ADC employs a different comparator for each bit of conversion, with an asynchronous ripple clock generated after each quantization. With the sample rate limited only by the six delays of the C-DAC settling and comparator quantizations, the 40nm-CMOS SAR-ADC achieves a peak SNDR of 32.9dB and 30.5dB at 1GS/s and 1.25GS/s, respectively, consuming 5.28mW and 6.08mW in a core area less than 170um x 85um.

9:55 19-3 **A 550µW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction,** *Sang-Hyun Cho, Chang-Kyo Lee, Jong-Kee Kwon*, Seung-Tak Ryu, KAIST, *ETRI*

A speed-enhanced 10b asynchronous SAR ADC with multistep addition-only digital error correction (ADEC) is presented in this paper. Three virtually divided sub-DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC switch

control. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. A prototype ADC was implemented in CMOS 0.13µm technology. The chip consumes 550µW and achieves a 50.6dB SNDR at 40MS/s under a 1.2V supply. The figure-of-merit (FOM) is 42fJ/conv-step.

10:20 19-4 **A 10b 120MS/s 45nm CMOS ADC Using A Re-Configurable Three-Stage Switched Op-Amp,** *Young-Ju Kim, Kyung-Hoon Lee, Seung-Hak Ji, Yi-Gi Kwon, Seung-Hoon Lee, Kyoung-Jun Moon*, Michael Choi*, Ho-Jin Park*, Byeong-Ha Park*, Sogang University, *Samsung Electronics*

10:45 BREAK

11:05 19-5 **SHA-Less Pipelined ADC Converting 10th Nyquist Band with In-Situ Clock-Skew Calibration,** *Pingli Huang, Szukang Hsien*, Victor Lu, Peiyuan Wan**, Seung-Chul Lee, Wenbo Liu, Bo-Wei Chen^, Yung-Pin Lee^, Wen-Tsao Chen^, Tzu-Yi Yang^, Gin-Kou Ma^, Yun Chiu, UIUC, *Texas Instruments, **Beijing University of Technology, ^Industrial Technology Research Institute*

Conversion from dc to the 10th Nyquist band is enabled in a SHA-less, 10-b, 100-MS/s pipelined ADC by digitally calibrating the clock skew in the 3.5-b front-end stage. The architectural redundancy of a pipelined ADC is exploited to extract skew infor-mation from the first-stage residue output with two out-of-range comparators and some simple digital logic; a gradient-descent algorithm is used to adaptively adjust the timing of the front-end sub-ADC to synchronize with that of the S/H. The 90-nm proto-type consumes 12.2 mW and digitizes inputs up to 480 MHz (limited by testing equipment) without skew errors in ex-periments, whereas the same ADC fails at 130 MHz when the calibration is disabled. The measured SFDR is 71 dB at 20 MHz and 55 dB at 480 MHz.

Session 20 – Modeling of Layout-Dependent Effects and RF Devices

Wednesday Morning, September 22
Fir Ballroom

Chair: Hidetoshi Onodera, Kyoto University
Co-Chair: Brian Chen

This session presents a review of state-of-the-art modeling techniques for integrated RF passive devices, RF LDMOS, and layout-dependent effects in VLSI designs.

9:00 **Introduction**

9:05 20-1 **Layout-Dependent Proximity Effects in Deep Nanoscale CMOS (INVITED),** *John Faricelli, Advanced Micro Devices*

As CMOS scaling extends into the nanoscale regime, designers need to be aware that device behavior depends not only on traditional geometric parameters such as channel length and width, but also on layout implementation details of the device and its surrounding neighborhood. The advent of stress engineering, in which intentional mechanical stress is applied to improve device performance, also adds new geometric dependencies. This paper reviews the major process technology features that cause layout-dependent proximity effects and how to account for these effects in circuit and layout design.

9:55 20-2 **Modeling of Integrated RF Passive Devices (INVITED),** *Sharad Kapur, David Long, Integrand Software, Inc.*

We use an electromagnetic (EM) simulator for modeling integrated RF components. EM simulators such as EMX are fast and accurate enough to provide good models of such components. It is feasible to simulate thousands of possible designs and build scalable component models. Scalable models allow fast choices of optimal components.

10:45 BREAK

11:05 20-3 **On the Modeling of LDMOS RF Power Transistors (INVITED),** *John Wood, Peter Aaen, Freescale Semiconductor Inv.*

In this review we present a technology-independent approach to the construction of a circuit model for high-power radio-frequency (RF) LDMOS FETs. This model is fully nonlinear, with a self-consistent dynamic electrothermal component. We compare and contrast this approach with other MOSFET modeling approaches used for digital and RF CMOS applications.

Session 21 – RF Power Amplifiers

Wednesday Morning, September 22
Pine Ballroom

Chair: Alireza Shirvani, Ralink Technologies
Co-Chair: Rick Booth, Panasonic PWRL

This session discusses integrated RF power amplifiers in CMOS technology and the challenges of achieving high output power, high efficiency, and high frequency operation.

9:00 **Introduction**

9:05 21-1 **Will CMOS Amplifiers Ever Kick-GaAs? (INVITED),** *Peter Zampardi, Skyworks Solutions, Inc.*

In this paper, we present a discussion and comparison of CMOS and GaAs HBT technologies for handset power amplifiers. Our perspective is unique to other comparisons in that we actually have products in both technologies. To understand the application space where each of these technologies makes sense, we discuss current and near-term PA requirements as well as technology and technology support issues. Finally, we aim to dispel some the common misperceptions surrounding these technologies.

9:30 21-2 **A Stacked 6.5-GHz 29.6-dBm Power Amplifier in Standard 65-nm CMOS,** *Maryam Fathi, David K. Su, Bruce A. Wooley, Stanford University*

A stacked amplifier architecture has been used to achieve high RF output power levels in sub-100nm CMOS. The stacking makes it possible to both operate the power amplifier (PA) from a large supply voltage and implement RF power combining. A 6.5-GHz PA has been integrated in a 65-nm standard CMOS technology. The amplifier achieves 29.6-dBm output power with an efficiency of 20.3% at 6.5 GHz when driven from a 4.6-V supply voltage.

9:55 21-3 **A 2.4GHz Mixed-Signal Polar Power Amplifier with Low-Power Integrated Filtering in 65nm CMOS,** *Debopriyo Chowdhury, Lu Ye, Elad Alon, Ali Niknejad, University of California, Berkeley*

A 65nm digitally-modulated polar transmitter incorporates a fully-integrated 2.4GHz efficient switching Inverse Class D power amplifier. Low power digital filtering on the amplitude path helps remove spectral images for coexistence. The transmitter integrates the complete LO distribution network and digital drivers. Operating from a 1-V supply, the PA has 21.8dBm peak

output power with 44% efficiency. Simple static predistortion helps the transmitter meet EVM and mask requirements of 802.11g 54Mbps WLAN standard with 18% average efficiency.

10:20 21-4 **An Integrated 33.5dBm Linear 2.4GHz Power Amplifier in 65nm CMOS for WLAN Applications,** *Ali Afsahi, Lawrence E. Larson, University of California, San Diego*

An integrated linear 2.4GHz CMOS power amplifier is presented. With a 3.3V supply, the PA produces a saturated output power of 33.5dBm with peak drain and power-added efficiencies of 44.2% and 37.6%, respectively and has 40dB small-signal gain. By utilizing gm-linearization and digital pre-distortion, an EVM of -25dB is achieved at 26.4dBm with 22% PAE while transmitting 54Mbs OFDM. The chip is fabricated in standard 65nm CMOS and packaged in a 40-pin QFN package. The PA occupies 2.2mm^2 active area.

10:45 BREAK

11:05 21-5 **Millimeter-Wave 14dBm CMOS Power Amplifier with Input-Output Distributed Transformers,** *Andrea Pallotta, Wissam Eyssa*, Luca Larcher**, Riccardo Brama**, STMicrolectronics S.r.l., *Institute for Advanced Study of Pavia, **University of Modena and Reggio Emilia*

We present a novel fully differential input/output distributed transformer topology used for the design of millimeter-wave power amplifiers. Input/output distributed transformers are used to feed the input signal to four differential couples and to combine their output power. This topology improves the stability and the efficiency of the power amplifier, minimizing the chip area. The PA prototype realized in a standard 65nm CMOS technology, supplied with 1.2V, achieves a 1dB single-ended output power compression point of 14dBm at 56GHz with a PAE of 8.3%, occupying only 0.2mm^2.

11:30 21-6 **A 77 GHz Power Amplifier Using Transformer-Based Power Combiner in 90 nm CMOS,** *Tao-Yao Chang, Chao-Shiun Wang, Chorng-Kuang Wang, National Taiwan University*

A 77 GHz PA with 50 Ω input and output matching has been realized in a general purpose 90 nm CMOS technology. In order to improve the output power and reduce the signal loss, a transformer and a short stub topology are employed respectively. The PA achieves a saturated output power (Pout,sat) of +13.2 dBm and 1dB compressed output power (Pout,1dB) of +11.2 dBm with a peak power-added efficiency (PAE) of 10.4% while operated with a 1.2 V supply.

Session 22 – Tutorial
Silicon Debug in Advanced Technologies

Wednesday Morning, September 22
Cedar Ballroom
This session (3 hours) will discuss debug methods in leading edge technologies for SOCs, FPGAs, and Microprocessors. The discussion will cover first silicon bring-up, pre and post-silicon practices for enhancing silicon debug, speed path debug, and power problem debug.

9:00 **Introduction**
Mike Li, Altera

9:05 22-1 **Using Electrical Test Data for Technology/Design Bring-up,** *Anne Gattiker, IBM Austin Research Lab*

Given the many facets of complexity in today's manufacturing processes and the fact that time-to-market pressures make it necessary to begin design before technology is mature, it is a given that there will be mismatch between design models and manufactured hardware. As a

result it is necessary during bring-up to consider not just model-hardware mismatches, but to prioritize attention on those mismatches that affect the product power and performance. This talk discusses approaches to understanding model-hardware correlation, including use of both embedded test structures and product test data, to identify and prioritize problems and speed bring-up.

9:40 22-2 **Pre and Post-silicon Practices for Enhancing Silicon Debug and Failure Analysis on Deep-Submicron Complex Chips,** *Eric C. Chang, Bergen Hung, Altera*

As process technology continues to scale and chip design complexity increases, silicon debug and failure analysis becomes more challenging which directly impacts development and mask costs, in addition to time to market costs. This presentation describes pre and post-silicon practices that are valuable for enhancing silicon debug and failure analysis. Various DFX (Design-For Verification, Debug, Yield, Manufacturability) and debug techniques, including use of FPGA programmability, is discussed.

10:15 **BREAK**

10:30 22-3 **Speed Debug Challenges for High Performance SOC/Processor,** *T.M. Mak, Intel*

Many SoC applications today require a high level of performance (e.g. smartphones, small office/home office (SOHO) network/servers, network attached storage (NAS)/servers) with operating frequencies going beyond 1 GHz. On-die and overall process variation will create new speed paths that may not be predictable with timing models. This tutorial will introduce some speed path debug techniques that have long been employed by high performance processor designs. Additional debug challenges as a result of 3D TSV integration will also be discussed

11:05 22-4 **Low Power Design Debug,** *Jackie Snyder, Marvell and Raymond Lee, EAG*

Design for low power brings a set of unique debug challenges. First silicon may show disappointing low power state results, which may be process or design related. These designs may have multiple voltage domains and internal supply domains that are switched off or back-biased which can create a number of baffling problems if not treated properly. This talk is a collaborative effort from design and failure analysis labs. We will go over a number of low power design bug types and methodologies for finding the problem devices. We will also discuss device fixturing best practices and DFT modes to allow thermal and emissions FA analysis.

11:40 **Bring Your Questions - Ask the Experts - Group discussion**

Session 23 – Power Optimization and Multi-Processing for SoCs

Wednesday Afternoon, September 22
Fir Ballroom

Chair: Aurangzeb Khan, EverSpin Technologies
Co-Chair: Rick Paul

In this session we present a variety of SoCs implementing multi-processor and power efficient designs, as well as power and security aware techniques.

1:30 **Introduction**

1:35 23-1 **A 0.077 to 0.168 nJ/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine,** *Chih-Chi Cheng, Yi-Min Tsai*, Liang-Gee Chen*, Anantha P. Chandrakasan, Massachusetts Institute of Technology, *National Taiwan University*

3GPP LTE requires a 100 Mbps of peak bandwidth, and the instantaneous throughput demand changes with different applications. Fixed sub-block parallel turbo decoding scheme introduces a bit-error rate (BER) performance drop when the block length is short. In this paper, an LTE turbo decoder implemented on a 0.66 mm^2 die in a 65 nm CMOS technology is presented. An adaptive sub-block parallel (ASP) decoding scheme that improves the BER performance by up to 2.7 dB while maintaining the same parallelism is developed. A DVFS engine combining with an early-termination scheme is also developed. It generates the supply voltage and the clock rate that lead to the lowest energy consumption given the output bandwidth requirement. The measured energy consumption is 0.077~0.168 nJ per bit per iteration and 0.39~0.85 nJ per bit.

2:00 23-2 **A Semi-Passive UHF RFID Tag with On-Chip Temperature Sensor,** *Wenyi Che, Dechao Meng, Xuegui Chang, Wei Chen, Lifang Wang, Yuqing Yang, Conghui Xu, Xi Tan, Na Yan, Hao Min, Fudan University*

A semi-passive UHF temperature sensor tag compatible with ISO 18000-6C protocol Revision-1 is presented in this paper. Novel power management techniques are proposed to prolong battery life, including two-stage wake-up detection, optimized rectifier design for wireless recharge, quasi CC-CV battery charging, and on-chip battery voltage surveillance. Both real-time temperature sensing and temperature log function are implemented with a bandgap based PTAT circuit. It has a -40~100 ℃ sensing range with ±1.6 ℃ accuracy. The tag is fabricated in 0.18 μm CMOS technology with EEPROM. Measured sensitivity and standby current are -23.7 dBm and 150 nA respectively.

2:25 23-3 **Intelligent NoC with Neuro-Fuzzy Bandwidth Regulation for a 51 IP Object Recognition Processor,** *Seungjin Lee, Jinwook Oh, Minsu Kim, Junyoung Park, Joonsoo Kwon, Joo-Young Kim, Hoi-Jun Yoo, KAIST*

Balancing the execution times of concurrent tasks in a multi-core processor is critical to achieving good performance scaling with increasing core count. However, this is difficult when the tasks' execution times are not known in advance. In this work, we propose an intelligent Network-on-Chip that performs bandwidth regulation using weighted round robin packet arbitration to balance the execution times of four Feature Extraction Clusters whose workloads vary depending on the input content. A neuro-fuzzy inference block, named the Intelligent Inference Engine, predicts the workload of each FEC, and assigns a priority weight to each FEC channel. As a result, a 34% reduction in synchronization overhead due to unbalanced execution time was achieved, and the overall execution time was reduced by 11.5%.

2:50 23-4 **Reconfigurable Mobile Stream Processor for Ray Tracing,** *Hong-Yun Kim, Young-Jun Kim, Lee-Sup Kim, Korea Advanced Institute of Science and Technology*

This paper presents a reconfigurable mobile stream processor for ray tracing. The processor is implemented with 16mm^2 area in 0.13μm CMOS technology. The processor adopts a single instruction, multiple thread (SIMT) architecture in order to exploit instruction-level and thread-level parallelism. The SIMT architecture consists of twelve stream processors (SPs). A low hardware utilization caused by a branch divergence in SIMT architecture is addressed by reconfiguring the SPs between scalar SIMT and vector SIMT with negligible hardware overhead. A slim special function unit (SFU) with a table loader reduces the SFU area and look-up table access counts. Reusing previous result for a ray generator reduces its operations by up to 71.9%. The proposed processor achieves a peak performance of 6.3M rays per second while consuming 156mW.

3:15 BREAK

3:30 23-5 **A Dynamic Timing Control Technique Utilizing Time Borrowing and Clock Stretching,** *Kwanyeob Chae, Saibal Mukhopadhyay, Chang-Ho Lee, Joy Laskar*, *Georgia Institute of Technology*

This paper presents an effective method for preventing timing failures of a system by utilizing time borrowing and clock stretching, thereby eliminating a safety margin. A design with the proposed method can effectively reduce power consumption or increase the operating frequency, which extends the dynamic operating margin of pipelined systems.

3:55 23-6 **On Security of Cryptosystem-on-Chip (CoC) in Nano-metric Technology,** *Amir Khatib Zadeh, Catherine Gebotys, University of Waterloo*

Evolution of the security threat posed by power consumption is assessed and a quantitative analysis is validated by real attack on two test chips (180nm and 65nm). The effectiveness of a novel use of high threshold transistor assignment for security of crypto core is proposed in 65nm test chip. The presented approach provides a significant resistance against information leakage for nano-scaled crypto ICs.

Session 24 – MM-Wave and Beyond

Wednesday Afternoon, September 22
Pine Ballroom

Chair: Howard Luong, Hong Kong University of Science and Technology
Co-Chair: Cicero Vaucher, NXP Semiconductors

This session consists of circuits and design techniques for mm-wave applications and beyond, including RF front-end, amplifiers, and VCOS and dividers.

1:30 **Introduction**

1:35 24-1 **A 60-GHz 1.65mW 25.9% Locking Range Multi-Order LC Oscillator Based Injection Locked Frequency Divider in 65nm CMOS,** *Keita Takatsu, Hirotaka Tamura*, Takuji Yamamoto*, Yoshiyasu Doi*, Koichi Kanda*, Takayuki Shibasaki*, Tadahiro Kuroda, Keio University, *Fujitsu Laboratories, Ltd.*

A 60-GHz injection-locked frequency divider (ILFD) fabricated in 65nm CMOS and operating at 1.2V consumes 1.65mW, and has a measured locking range of 25.9% with 0dBm input power without a frequency-adjustment mechanism. The core ILFD area is 0.0157mm^2. The large locking range is attributed to the use of the multi-order LC oscillator topology. To the best of our knowledge, this ILFD achieves the highest FOM (locking range per unit power) in mm-Wave frequency dividers.

2:00 24-2 **A V-Band Divide-by-Three Differential Direct Injection-Locked Frequency Divider in 65-nm CMOS,** *Hsieh-Hung Hsieh, Fu-Lung Hsueh, Chewn-Pu Jou, Fred Kuo, Sean Chen, Tzu-Jin Yeh, Kevin Kai-Wen Tan, Po-Yi Wu, Yu-Ling Lin, Ming-Hsien Tsai, Taiwan Semiconductor Manufacturing Company, Ltd.*

In this paper, a novel circuit topology of CMOS divide-by-three injection-locked frequency divider is demonstrated. By using a differential direct injection pair with a LC-tank oscillator, the proposed circuit can perform the division ratio of three while the wide locking range is obtained. Based on the presented circuit architecture, a V-band frequency divider is implemented in 65-

nm CMOS for demonstration. Operated at a supply voltage of 1.0 V, the divider core consumes a dc power of 5.2 mW. At an incident power of 0 dBm, the fabricated circuit exhibits an input locking range from 58.6 to 67.2 GHz. The measured output power and locked phase noise at a 1-MHz offset are -10 dBm and -127 dBc/Hz, respectively. To the authors' best knowledge, this work is the first CMOS V-band divide-by-three injection-locked frequency divider owning a locking range over 10% without any tuning mechanism reported to date.

2:25 24-3 **V-Band Varactor-less Interpolative-Phase-Tuning Oscillators with Multiphase Outputs,** *Sujiang Rong, Howard C. Luong, The Hong Kong University of Science and Technology*

A novel interpolative-phase-tuning technique is proposed in this work to implement varactor-less multi-phase LC oscillators with wide tuning range and low phase noise at millimeter-wave frequencies. Two phase-tuning CCO prototypes, one with 8-phase 50GHz outputs and another with 4-phase 60GHz outputs, implemented in a 0.13-micro-meter CMOS process and operated at 0.8-V supply, measure phase noise of -127.8dBc/Hz and -120.6dBc/Hz at 10MHz offset, FOMs of 186.4dB and 180.6dB, and FOMTs of 183dB and 179.7dB, respectively, which are much better compared to other state-of-the-art millimeter-wave oscillators using capacitive tuning.

2:50 24-4 **Digital Phase Tightening for Millimeter-Wave Imaging,** *Khoa Nguyen, Anthony Accardi, Helen Kim*, Gregory Wornell, Charles Sodini, Massachusetts Institute of Technology, *Massacusetts Instiute of Technology Lincoln Laboratory*

A new technique called digital phase tightening reduces phase noise from receiver front-end circuits to allow precise phase estimation for digital beamforming in millimeter-wave (MMW) imaging applications. This is achieved by leveraging the large ratio between the MMW carrier frequency and the relatively low frame rates in imaging applications. By mixing down to an intermediate frequency (IF) and then averaging over many samples to estimate the phase, we reduce phase noise and attain phase error of the MMW beamformer in the femtosecond range. A test chip demonstrating the phase tightening concept was designed and fabricated using 0.13µm CMOS, and we show that an RMS error of 3.5fs is feasible with this technique.

3:15 BREAK

3:30 24-5 **A 77-GHz to 90-GHz Bidirectional Amplifier for Half-Duplex Front-Ends,** *Joohwa Kim, Mehmet Parlak, James Buckwalter, University of Califoria, San Diego*

A W-band, bidirectional constructive wave amplifier is proposed that eliminates the need for a T/R switch. The amplifier allows amplification of either a forward or backward traveling wave. The measured amplifier has a peak gain of 16 dB and bandwidth of 14.5 GHz at 90 GHz and the center frequency can be electronically controlled between 77 and 90 GHz. The circuit is fabricated in a 0.12 µm SiGe BiCMOS process, occupies an area of 0.47 mm^2, and consumes approximately 32 mA from a 2 V supply. To the author’s knowledge, this is the first W-band, bidirectional amplifier in a silicon/silicon-germanium process.

3:55 24-6 **280-GHz Schottky Diode Detector in 130-nm Digital CMOS,** *Ruonan Han, Yaming Zhang*, Dominique Coquillat**, Julie Hoy^, Hadley Videlier**, Wojciech Knap**, Elliott Brown^, Kenneth O, University of Florida, *University of Texas at Dallas, **University of Montpellier II, ^University of California, Santa Barbara*

Abstract-A 2×2 array of Schottky-barrier diode detectors with an on-chip patch antenna and a preamplifier is fabricated in a 130-nm logic CMOS process. Each detector cell can detect the 25-kHz modulated 280-GHz radiation signal with a measured responsivity and noise equivalent power (NEP) of 21kV/W and 360pW/sqrt(Hz), respectively. At 4-MHz modulation frequency, NEP should be ~40pW/sqrt(Hz). At supply voltage of 1.2V, the detector consumes 1.6mW. By utilizing the detector, a millimeter-wave image is constructed, demonstrating its potential

application in millimeter-wave and THz imaging.