Technical Sessions
Monday, September 19 – Wednesday, September 21

Session 1 – Keynote Presentation

Monday Morning, September 20
Oak Ballroom

8:15am **Welcome and Opening Remarks**
Awards Presentations
Keynote Speaker Introduction
Rakesh Patel, General Chairman

8:30 am **Keynote Presentation**
James D. Meindl
Nanotechnology Research Center & School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA

Since 1960 silicon microchip technology has advanced in productivity by the astounding factor of one billion times. Concurrently, the performance of microchips, for example a microprocessor chip, has increased by a factor of approximately one million times since the early 1970's. These two concurrent advances are unmatched in technological history. The salient objective of this discussion is to provide an incisive response to the question: what's next?

Reducing the minimum feature size (F) of transistors and interconnects in a microchip or scaling has been the single most potent factor enabling the huge improvements in both productivity and performance of microchips during the past half century. To be more specific, transistor printed gate length has been scaled from 25 μm to 25nm or by a factor of 1000x. However, within the next decade limitations such as gate tunneling current and subthreshold drain-to-source current will demand the introduction of new high permittivity gate insulators and metal gates. These new materials and new device structures such as the vertical FinFET will be necessary to enable continued scaling albeit at a substantially reduced rate. A transition from 193 nm optical lithography to EUV technology will also be necessary to support scaling to the sub-10nm region.

As the advance of intrinsic silicon technology nears a saturation point in the sub-10nm range, opportunities for ancillary technology and especially for three-dimensional (3D) integration will become vigorously pursued. Stacking of low power flash memory chips is now a production technology but stacks of microprocessor and memory chips, for example, in a high performance multi-core processor are not yet in use particularly due to heat removal limitations. However, promising innovative approaches to electrical interconnection and liquid cooling of a stack using electrical and fluidic through-silicon vias have been presented.

Beyond another decade of silicon technology advances, perhaps the most promising prospect that is under intense investigation is graphene, particularly due to its ballistic carrier transport, adjustable energy band gap of nanoribbons and potential for fusion of top-down and bottom-up nanotechnology.

Session 2 -Enhanced Modeling Techniques

Monday Morning, September 19
Oak Ballroom

Chair: Colin McAndrew, Freescale Semiconductor
Co-Chair: Hidetoshi Onodera, Kyoto University

This session presents recent developments in nanowire transistor modeling, on-chip transformer and balun modeling, reliability modeling of large digital systems, and wafer-specific model centering.

10:00 AM **Introduction**

10:05 AM 2-1 **Characterization and Analysis of Gate-All-Around Si Nanowire Transistors for Extreme Scaling (INVITED),** *Ru Huang, Runsheng Wang, Jing Zhuge, Changze Liu, Tao Yu, Xin Huang, Yujie Ai, Jinbin*

Zou, Yuchao Liu, Jiewen Fan, Huailin Liao, Yangyuan Wang, Peking University

The gate-all-around Si nanowire transistor is one of the best candidates for ultimately scaled CMOS devices at the end of roadmap. This paper reviews our recent work on characterization and analysis of this unique device from experiments and simulation, including carrier transport, parasitics, noise, self-heating, variability and reliability, which can provide useful information for the nanowire device hierarchical modeling and device/circuit co-design.

10:55 AM 2-2 **Broadband Compact Model for On-Chip mm-Wave Transformers and Baluns with Emphasis on Capacitive Coupling Effects,** *Yang Tang, Zuochang Ye, Yan Wang, Tsinghua University*

Distributed capacitive coupling effects in the transformers and baluns at millimeter-wave band are investigated in this paper and a lumped coupling branch with parameter estimation method is proposed. The accuracy near and beyond resonance frequency of the new equivalent circuit model is greatly improved. Different types of transformers and baluns with various geometries are fabricated by 0.13um RF CMOS process. The model agrees quite well with all the experiments up to 40GHz and further validated by EM simulations up to 80GHz, indicating that it captures the physical essence behind correctly.

11:20 AM 2-3 **Bottom-Up Digital System-Level Reliability Modeling,** *N. Ruiz Amador, V. Huard, E. Pion, F. Cacho, D. Croain, V. Robert, S. Engels, P. Flatresse, L. Anghel* ,STMicroelectronics, *TIMA Laboratory*

In this paper we demonstrate that it is possible by a bottom-up approach to build transistor-and gate-level models with enough accuracy to allow direct comparison with experimental degradations at system-level.

11:45 AM 2-4 **Wafer-Specific Centering of Compact Transistor Model Parameters for Advanced Technologies and Models.,** *B. De Vries, A.J. Scholten, P.F.E. Rommers*, M. Stoutjesdijk*, and D.B.M. Klaassen, NXP Central R&D Research, *NXP Central R&D Foundation Technology*

For older technologies and compact models it is often possible to directly calculate a compact model parameter set based on a limited amount of process-control module measurements. For advanced technologies and surface-potential-based compact models this is no longer the case. Here, we present a novel method to restore this capability.

Session 3 - Clock Synthesis and CDRs

Monday Morning, September 19
Fir Ballroom

Chair: William Walker, Fujitsu Laboratories of America
Co-Chair: Shunichi Kaeriyama, Renesas Electronics Corporation

This session covers low-skew multi-phase clock generation, a PLL synthesized from a standard cell library, and digital techniques for clock and data recovery.

10:00 AM **Introduction**

10:05 AM 3-1 **Area Efficient Phase Calibration of a 1.6 GHz Multiphase DLL,** *Ankur Agrawal, Pavan Kumar Hanumolu*, Gu-Yeon Wei**, IBM Research, *Oregon State University, **Harvard University*

This paper describes a digital calibration scheme that corrects for phase spacing errors in a multiphase clock generating delay-locked loop (DLL). The calibration scheme employs sub-sampling using a frequency-offset clock with respect to the DLL reference clock, to measure phase-offsets. The phase-correction circuit uses one digital-to-analog converter across eight variable-delay buffers to reduce the area consumption by 62%. The test-chip, designed in a 130nm CMOS process, demonstrates a 8-phase 1.6 GHz DLL with a worst-case phase error of 450fs.

10:30 AM 3-2 **Digital Clock and Data Recovery Circuit Design: Challenges and Tradeoffs,** *Mrunmay Talegaonkar, Rajesh Inti, and Pavan Kumar Hanumolu, Oregon State University*

Digital clock and recovery circuits (CDRs) have recently emerged as an alternative to their more

classical analog counterparts. This paper seeks to elucidate the design challenges and trade-offs involved in the design of digital CDRs. The jitter performance metrics such as jitter generation, jitter transfer, and jitter tolerance are related to digital CDR parameters and design guidelines are provided. The impact of digital phase detector non-linearity and quantization error, the digitally-controlled oscillator frequency quantization error, and loop latency on a digital CDR performance is analyzed and demonstrated using accurate behavioral simulations.

11:20 AM 3-3 **An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS,** *Y. Park, D. Wentzloff, University of Michigan*

This paper presents an all-digital PLL (ADPLL) in which all functional blocks have been synthesized from standard digital cells and automatically placed and routed (P&R). A calibration scheme is proposed to account for the systematic mismatch resulting from P&R. The ADPLL is fabricated in 65nm CMOS and occupies 0.042mm2. The period jitter is 3.2psrms (36pspp) at 2.5GHz, and the power consumption is 9.1mW to 14.6mW over a 1.5 to 2.7GHz frequency range.

11:45 AM 3-4 **An Open-Loop 10GHz 8-Phase Clock Generator in 65nm CMOS,** *X. Yang, J. Liu, University of Texas at Dallas*

An open-loop 10GHz 8-phase clock generator is presented. It is composed of delay units and phase interpolators with built-in phase compensation for delay variation. A delay unit design with level-shifted active inductor load enables the circuit to achieve 10GHz speed with 0.19mW/GHz/phase power efficiency in 65nm CMOS.

Session 4 – Wireless Transceivers in CMOS

Monday Morning, September 19
Pine Ballroom

Chair: Julian Tham, Broadcom
Co-Chair: Ramesh Harjani, University of Minnesota

Wireless transceiver designs for software defined radio, GPS, wireless headphones and sensors nodes are presented. Implementations range from 40nm to 180nm CMOS technology nodes.

10:00 AM **Introduction**

10:05 AM 4-1 **SAW-less Software-Defined Radio Transceivers in 40nm CMOS (INVITED),** *Jan Craninckx, Jonathan Borremans, Mark Ingels, IMEC*

The introduction of several new cellular and connectivity radio standards has attracted the wireless industry to the concept of software-defined radio systems, preferably implemented in advanced nanometer CMOS technology. A first generation of transceivers, using several advances in new circuits and architectures, combined with extensive digital compensation techniques, are indeed able to operate over the complete range of both RF frequencies and baseband bandwidths and as such act like an SDR. However, a real SDR must go further than this. Interoperability and coexistence scenarios, combined with the need to eliminate external fixed-frequency acoustic RF filters, lead to much more stringent requirements on linearity and noise. Therefore, this paper will also present a novel second generation of 40nm CMOS transceivers that enable this. On the TX side, it is crucial to achieve -160dBc/Hz noise level for all possible combinations of RF frequency, baseband bandwidth, and RX-TX duplex spacing. In the receiver, extremely linear circuits are presented, that are able to handle blockers of around 0dBm input level.

10:55 AM 4-2 **A Dual-Channel GPS/Compass/Galileo/GLONASS Reconfigurable GNSS Receiver in 65nm CMOS,** *Nan QI, Yang Xu, Baoyong Chi, Yang Xu, Xiaobao Yu, Xing Zhang, Zhihua Wang, Tsinghua University*

A fully-integrated dual-channel reconfigurable GNSS receiver supporting GPS/Compass/Galileo/GLONASS in 65nm CMOS is presented. The receiver has two independent channels to support simultaneous reception. One frequency synthesizer is shared by two channels to avoid LO crosstalk. The receiver achieves 2.2dB noise figure, 50dB IRR on average, while consuming minimum 31mW power.

11:20 AM 4-3 **Complete SOC Transceiver in 0.18um CMOS using Q-enhanced Filtering, Sub-sampling and Injection Locking,** *R. Mason, J. Fortier*, C. DeVries**, SMSC, *Hittite Microwave Corporation, **Research in Motion*

Portable wireless headphones have not been widely accepted. The main reasons for this are that power consumption is too high and interference management is poor. A workable wireless headphone is presented. The transceiver is fabricated in 0.18µm CMOS and consumes peak RX/TX currents of 10.2mA and 22mA respectively.

11:45 AM 4-4 **A Wireless Sensor Node for Condition Monitoring Powered by a Vibration Energy Harvester,** *J. Jang, D.F. Berdy, J. Lee, D. Peroulis, B. Jung, Purdue University*

A complete duty-cycle controlled, FDMA and TDMA compatible wireless condition monitoring sensor node with 85.5 µW measured average power consumption is presented with a high level of integration. It is experimentally demonstrated to operate autonomously from the power provided by a piezoelectric vibration energy harvester.

Session 5 – Technology and Circuit Drivers for Ultra-Scale CMOS

Monday Morning, September 19
Cedar Ballroom

Chair: Rajiv Joshi, IBM TJ Watson Research Center
Co-Chair: Kingsuk Maitra, GlobalFoundries

This session of invited papers covers key technology and circuit drivers such as process variability, interconnect delays, tower management, memory functionality, and reliability for marching towards 15nm CMOS.

10:00 AM **Introduction**

10:05 AM 5-1 **Design and Technology Interaction Beyond 32nm (INVITED),** *M. Clinton, C. Bittlestone, V. Menezes, V. Le, G. Girishankar, Texas Instruments*

Abstract-This paper will discuss the challenges that continued technology scaling present to circuit designers and how the close interaction between the development of technology, design automation (EDA) tools and the circuit designer can overcome these challenges and enable designs that deliver the benefits customers expect from continued technology scaling

10:55 AM 5-2 **Statistical Advantages of Intrinsic Channel Fully Depleted SOI MOSFETs over Bulk MOSFETs (INVITED),** *Toshiro Hiramoto, Anil Kumar, Tomoko Mizutani, Jun Nishimura, Takuya Saraya, University of Tokyo*

Statistical characteristics of intrinsic channel FD SOI MOSFETs and conventional bulk MOSFETs are compared. It is experimentally shown that not only Vth variability but DIBL and current onset voltage (COV) variability is well suppressed in FD SOI MOSFETs. Moreover, Vth change due to random telegraph noise (RTN) is also smaller in FD SOI MOSFETs. It terms out that the absence of random dopant fluctuation (RDF) is responsible for the suppressed variability.

11:20 AM 5-3 **28nm Metal-gate High-K CMOS SoC Technology for High-Performance Mobile Applications (INVITED),**

Session 6 – 3D and Photonic Interconnect

Monday Afternoon, September 19
Oak Ballroom

Chair: Arif Rahman, Altera
Co-Chair: Mike Li, Altera

This session covers the design, implementation, modeling and test of advanced interconnect

technologies including 3D integrated circuits and photonics.

1:30 PM **Introduction**

1:35 PM 6-1 **Three Dimensional Integration – Considerations for Memory Applications (INVITED),** *S.S. Iyer, T. Kirihata, and J.E. Barth, IBM Systems and Technology Group*

This paper reviews the technology and design considerations for the implementation of 3 Dimensional integration of memory in a high performance logic environment.

2:25 PM 6-2 **DRAM-on-logic Stack — Calibrated Thermal and Mechanical Models Integrated into PathFinding Flow (INVITED),** *D. Milojevic, H. Oprins, J. Ryckaert, P. Marchal, G. Van der Plas, IMEC*

In this paper, we present thermal and mechanical characterization of a DRAM-on-logic stack. Our experimental data indicates that a holistic optimization of design and technology is needed to achieve working 3D stacks. Particularly, the stack organization and TSV/µbump layout must be fine-tuned together with the 3D technology for managing mechanical and thermal challenges. In order to support system designers, we propose hereto a dedicated thermal and mechanical model, integrated into the design flow. We also indicate the data required from foundries and OSATs to achieve good fidelity with measurement results.

3:15 PM **BREAK**

3:30 PM 6-3 **Test Challenges for 3D Integration (INVITED),**

4:20 PM 6-4 **CDM-ESD Induced Damage in Components using Stacked-Die Packaging,** *N. Olson, N. Jack, V. Shukla, E. Rosenbaum, University of Illinois at Urbana-Champaign*

CDM-ESD robustness of stacked-die packages is investigated and compared with single-die packages. The peak discharge current is not increased significantly by die stacking. The inter-die signal interfaces are shown to be well protected against CDM by placing just a small ESD protection clamp at the receiver, if certain package integration guidelines are followed.

4:45 PM 6-5 **Silicon Photonics for On-Chip Interconnections (INVITED),** *A. Mickelson, University of Colorado at Boulder*

The state of the art of silicon photonics for on-chip interconnections is reviewed from both historical and technological perspectives. Attention is placed on motivating why silicon photonics is the replacement for copper interconnection that offers the best possibility for future improvement in performance and reduction in power consumption. The broadcast interconnection effort being carried in the author's research group is discussed in light of the requirements of many-core interconnections.

Session 7 – High Speed Wireline and Optical Transceivers

Monday Afternoon, September 19
Fir Ballroom

Chair: Elad Alon, University of California, Berkeley
Co-Chair: Ed Van Tuijl, Axiom-IC Twente

With the increasing demand for high-speed wireline and optical transceivers, this session highlights advanced techniques to improve the power and performance of these designs.

1:30 PM **Introduction**

1:35 PM 7-1 **A 19 mW/Lane SerDes Transceiver for SFI-5.1 Application,** *Siavash Fallahi*, Delong Cui*, Deyi Pi, Rose Zhu*, Greg Unruh*, Marcel Lugthart*, Afshin Momtaz*, *Broadcom Corporation*

A low-power, small-area transceiver PHY that supports SFI-5.1 is fabricated in standard 40 nm CMOS, supporting rates up to 50 Gb/s. The combined active core area of the receiver and transmitter occupies only 0.08 mm2 per lane. The RX can handle 0.65 UI plus 0.49 UI additional sinusoidal input jitter.

2:00 PM 7-2 **A Monolithic 3.125 Gbps Fiber Optic Receiver Front-end for POF Applications in 65 nm CMOS,** *Yunzhi Dong, Ken Martin*, University of Toronto, *Granite SemiCom*

This paper describes the design of an analog receiver front-end targeting multi-gigabit data communications over large-core plastic optical fibers. A receiver front-end with an integrated photo detector has been implemented in a standard TSMC 65 nm low-power bulk-silicon CMOS process. A novel hybrid current buffer based transimpedance amplifier has been proposed to drive the 14 pF photo capacitance presented by the large-area photo detector to multi-gigahertz range. A digitally controlled slow-slope equalizer has also been integrated in the receiver front-end to compensate the high-frequency losses due to the integrated photo detector. The receiver front-end consumes 50 mW dc power from a 1.2 V supply (excluding output buffer) and achieves an NRZ data rate up to 3.125 Gbps.

2:25 PM 7-3 **Addressing Link-Level Design Tradeoffs for Integrated Photonic Interconnects,** *M. Georgas, J. Leu, B. Moss, C. Sun, V. Stojanovic, Massachusetts Institute of Technology*

Integrated photonic interconnects have emerged recently as a potential solution for relieving on-chip and chip-to-chip bandwidth bottlenecks for next-generation many-core processors. To help bridge the gap between device and circuit/system designers, and aid in understanding of inherent photonic link tradeoffs, we present a set of link component models for performing interconnect design-space exploration connected to the underlying device and circuit technology. To compensate for process and thermal-induced ring resonator mismatches, we take advantage of device and circuit characteristics to propose an efficient ring tuning solution. Finally, we perform optimization of a wavelength-division-multiplexed link, demonstrating the link-level interactions between components in achieving the optimal degree of parallelism and energy-efficiency.

3:15 PM **BREAK**

3:30 PM 7-4 **A 7.4Gb/s Forwarded Clock Receiver Based on First-Harmonic Injection-Locked Oscillator Using AC Coupled Clock Multiplication Unit in 0.13um CMOS,** *Young-Ju Kim, Sang-Hye Chung,Lee-Sup Kim, KAIST*

This paper presents a forwarded clock receiver based on an injection-locked oscillator (ILO) with a simple clock multiplication unit to reduce the clock jitter and power consumption. The clock multiplication unit employs AC coupling and superposition technique to generate first-harmonic pulses. The first-harmonic injection reduces the rms and peak to peak jitter of the ILO output clock by about 0.65ps (29%) and 46.06ps (65%), respectively. The measured power efficiency of the receiver is 1.69mW/Gbps at 7.4Gb/s data rate in a 1.2V 0.13μm CMOS process.

3:55 PM 7-5 **Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS,** *Kangmin Hu, Tao Jiang, Sam Palermo*, Patrick Yin Chiang, Oregon State University, *Texas A&M University*

A testchip of 8Gb/s forwarded clock serial link receivers is presented. The receiver exploits a novel low-power super-harmonic injection-locked ring oscillator for symmetric multi-phase local clock generation and dekewing. Further power reduction is achieved by designing most the receiver circuits in the near-threshold region of 0.6V supply, with the exception of only the global clock buffer, test buffers and synthesized digital circuits at nominal 1V supply. At architectural level, 1:10 direct demultiplexing rate is chosen as a demonstration of achieving low supply operation by high-parallelism design. Fabricated in 65nm CMOS technology, two receiver prototypes are integrated in this testchip, one without and the other with front S/Hs. Including the amortized power of global clock distribution, they consume 1.3mW and 2mW respectively at 8Gb/s input data rate, which achieve the power efficiency of 0.163mW/Gb/s and 0.25mW/Gb/s. Measurement results show both receivers get BER < 10e-12 across a 20-cm FR4 PCB channel.

4:20 PM 7-6 **A 16-Gb/s Backplane Transceiver with 12-Tap Current Integrating DFE and Dynamic Adaptation of Voltage Offset and Timing Drifts in 45-nm SOI CMOS Technology,** *G. R. Gangasani, C. Hsu, J. F. Bulzacchelli*, S. Rylov*, T. Beukema*, D. Freitas, W. Kelly, M. Shannon, J. Qi, H. H. Xu, J. Natonio, T. Rasmus, J. Guo, M. Wielgos, J. Garlett, M. A. Sorna, M. Meghelli, IBM Systems and Technology Group, *IBM T. J. Watson Research Center*

This paper presents a 16-Gb/s 45-nm SOI CMOS transceiver for multi-standard backplane applications. The receiver uses a 12-tap DFE with circuit refinements for supporting higher data rates. Both the receiver and the transmitter use dynamic adaptation to combat parameter drift due to changing supply and temperature. A 3-tap FFE is included in the source-series-terminated driver. The combination of DFE and FFE permits error-free NRZ signaling at 16-Gb/s over channels exceeding 30dB loss. The 8-port core with two PLLs is fully characterized for 16GFC and consumes 385mW/link.

4:45 PM 7-7 **Power-Efficient I/O Design Considerations for High-Bandwidth Applications (INVITED),** *J. Eble, S. Best, B. Leibowitz, L. Luo, R. Palmer, J. Wilson, J. Zerbe, A. Amirkhany, N. Nguyen, Rambus Inc.*

Power-efficiency results from several generations of I/O interfaces with specific goals are presented as well as the tradeoffs made within and across those designs. Foundational work in active-power reduction at a single rate for a symmetric system, the subsequent application of that work to a burst-mode asymmetric interface, and recent research on low-overhead bursting are discussed. Dynamic voltage frequency scaling and efficiency increases enabled by system level interconnect improvements are also considered as important techniques.

Session 8 – Sensors and Biosystems

Monday Afternoon, September 19
Pine Ballroom

Chair: Farrokh Ayazi, Georgia Institute of Technology
Co-Chair: Ada Poon, Stanford University

This session presents works that push the limits and review the state of the art of general sensors, biosensors and circuits for biomedical applications.

1:30 PM **Introduction**

1:35 PM 8-1 **Thermal Diffusivity Sensing: A New Temperature Sensing Paradigm (INVITED),** *C.P.L. van Vroonhoven and K.A.A. Makinwa, Electronic Instrumentation Laboratory / DIMES, Delft University of Technology, Delft, the Netherlands*

This paper describes temperature sensors based on the well-defined thermal diffusivity of IC-grade silicon, which have low untrimmed inaccuracy (±0.2°C 3σ) and operate over a wide temperature range. Their near-linear digital output is insensitive to process spread and packaging stress, and their performance strongly benefits from process scaling.

2:00 PM 8-2 **A Self-Clocked ASIC Interface for MEMS Gyroscope with 1m˚/s/√Hz Noise Floor,** *A. Elsayed, A. Elshennawy, A. Elmallah, A. Shaban, B. George, M. Elmala, A. Ismail, A. Wassal, M. Sakr, A. Mokhtar, M. Hafez, A. Hamed, M. Saeed, M. Samir, M. Hammad, M. Elkhouly, A. Kamal, M. Rabieah*, A. Elghufaili*, S. Shaibani*, I. Hakami*, T. Alana*

An interface for MEMS gyroscope is implemented in 0.18µm HVCMOS and achieves noise floor of 1m deg/sec/sqrt(Hz) over 200Hz BW. Electromechanical sigma-delta force-feedback and self-clocking scheme based on gyro resonance are implemented. The interface includes on-chip reference generation, decimation, and temperature compensation.

2:25 PM 8-3 **A 20uW Contact Impedance Sensor for Wireless Body-Area-Network Transceiver,** *Kiseok Song, Joonsung Bae, Long Yan, Hoi-Jun Yoo, KAIST*

A low power contact impedance sensor (CIS) is presented for an energy efficient wireless body-area-network (WBAN) transceiver using a human body as a transmission medium. The proposed CIS adopts the capacitive sensing technique based on the LC resonance for detecting the parasitic capacitance between the electrodes and the human body to automatically turn on or off the transceiver. The 3'b resistive sensor, combined with a reconfigurable output driver in the transmitter, is proposed to compensate the channel quality degradation due to the contact impedance variation. It can reduce both the linearity and sensitivity requirements of the receiver front-end by 7 dB. It leads to significantly reduce the power of the LNA more than 70 % (from 2.0 mW to 0.6 mW). The proposed CIS of 1.0 mm X 1.4 mm is fabricated in 0.18 um CMOS technology, and dissipates only 20 uW from 1.0 V.

2:50 PM 8-4 **256-site Active Neural Probe and 64-channel Responsive Cortical Stimulator,** *R. Shulyzki, K. Abdelhalim, A. Bagheri, C. M. Florez, P. L. Carlen, R. Genov, University of Toronto*

The 0.35um CMOS active probe and stimulator enables responsive neural stimulation of the brain cortex. It monitors extracellular neural activity on 256 sites in the brain and generates 64 event-triggered current-mode neural stimuli. Each 0.035mm2 fully differential neural recording channel includes a 8-bit single slope ADC. Each 0.02mm2 neural stimulation channel reuses an OTA for both current sampling and current sourcing. The 13.5mW prototype is flip-chip bonded with a 64- shank Utah electrode array and validated in spatial recording of epileptic neural activity in the mouse hippocampus.

3:15 PM **BREAK**

3:30 PM 8-5 **Power Management Subsystem with Bi-directional DC to DC Converter for u-Power Biomedical Applications,** *Raymond E. Barnett, Ganesh K. Balachandran* ,Texas Instruments, *Robert Bosch Research & Technology Center*

This paper presents a power management subsystem embedded in a biomedical wireless sensor SoC. A bi-directional capacitor only DC/DC converter, optimized for loads to 60uW, allows high efficiency operation using 1 to 3V batteries. The circuit is fabricated in a 0.35um BCD technology and occupies an area of 1.125 mm2.

3:55 PM 8-6 **A Capacitor-Based AC-DC Step-Up Converter for Biomedical Implants,** *Edward Lee, Alfred Mann Foundation*

An AC-DC step-up converter architecture for generating multiple compliance voltages (CVs) in an inductive powered biomedical implant is proposed. Switches and active rectifiers are used inside the converter for charging capacitors from the AC input and delivering currents to the loads. Regulated CVs with high power efficiency are obtained by controlling the on/off times of the switches using feedback loops. For a 1MHz, 2.3V peak AC input, a power efficiency of 92.9% for a combined load power of 12.3mW on 4 CVs (□3V and □3.6V) was achieved in a 0.18μm CMOS process.

4:20 PM 8-7 **Fully Integrated Power-Efficient AC-to-DC Converter Design in Inductively-Powered Biomedical Applications (INVITED),** *Hyung-Min Lee, Maysam Ghovanloo, Georgia Institute of Technology*

Limitations for achieving high power conversion efficiency (PCE) in integrated AC-to-DC converters have been reviewed for applications such as implantable microelectronic devices. We have presented a fully integrated active voltage doubler with offset-controlled high-speed comparators, which can convert 1.72V peak AC input at 13.56MHz to 2.4V DC across a 1kΩ load, with 78% PCE.

4:45 PM 8-8 **Noise and Bandwidth Performance of Single-Molecule Biosensors (INVITED),** *J. Rosenstein, S. Sorgenfrei, K. L. Shepard, Columbia University*

Single-molecule biosensors can reveal dynamics unavailable to ensemble measurements. Common fluorescence techniques are highly specific but fundamentally limited by the number of photons that can be collected. Here, we discuss the performance of new direct electronic sensors and their potential for sensing single-molecule processes on shorter timescales.

Poster Session

Monday Evening, September 19
Cascade/Sierra Ballroom

5:00 pm – 7:00 pm

M-1 **A Discrete-Time Charge-Domain Filter with Bandwidth Calibration for LTE Application,** *Ming-Feng Huang, Industrial Technology Research Institute*

A discrete-time charge-domain filter (CDF) with bandwidth calibration was proposed for LTE

application. The CDF, based on feedback gain and delay, could suppress sinc distortion to achieve a like brick-wall filtering. The measurement showed that CDF performed a >59dB adjacent-channel rejection, >85dB stop-band attenuation, and 5-to-26 MHz reconfigurable bandwidth.

M-2 **A True Single SoC for UHF Mobile RFID Reader,** *J. Kim, S. Yun, W. Oh, M. Kil, S. Cho, PHYCHIPS Inc.*

A true single SoC for UHF Mobile RFID Reader has been implemented in a 0.18μm embedded flash CMOS technology. The SoC includes 900MHz RF transceiver, PA,MODEM, MCU, memory and peripherals with fully compliant ISO/IEC 18000-6C and EPC Global Class1 Gen2 reader protocol.

M-3 **An 80% Peak Efficiency, 410mW, Single Supply Rail Powered Class-I Linear Audio Amplifier,** *Z. Peng, S. Yang, Y. Feng, Z. Hong, B. Liu*, Fudan University, *Analog Devices*

A high efficiency high linearity Class-I audio amplifier is presented. Efficiency is improved by adopting a self-generated adaptive supply. The employed gain compression technique uses only one positive supply to maintain good linearity, and achieve above 20% better efficiency over a conventional Class-AB design.

M-4 **Band-gap Circuit Design Challenges in High-performance 32-nm Technology,** *J. Buller, J. Fletcher, S. Meyers, M. Robinson*, F. Tamayo, A. Prakash, D. Cabler, Advanced Micro Devices, *Vidatronic*

32-nm complementary metal oxide semiconductor (CMOS) silicon-on-insulator (SOI) with metal gate high-k (MGHK) offers high performance and low power for microprocessors. However, these advanced technologies come with challenges for analog design. Many of the stressor performance elements can adversely impact analog circuit behavior. For example, band-gap circuits, used ubiquitously in voltage references, are one such challenging component. We investigated both design and process methods that resulted in robust band-gap voltage and temperature response characteristics without impacting performance elements for microprocessor frequency.

M-5 **Low Power and Error Resilient PN Code Acquisition Filter via Statistical Error Compensation,** *E. Kim, D. Baker, S. Narayanan, D. Jones, N. Shanbhag, University of Illinois at Urbana Champaign*

We present a 256-tap PN code acquisition filter in an 180nm CMOS process employing statistical system-level error compensation. Under voltage overscaling (VOS), near constant detection probability Pdet above 90% with 5.8x reduction in energy is achieved at a supply voltage 27% below the point of first failure (PoFF) with an error rate pe of 0.868. This is an improvement of 5.8x in energy-efficiency over conventional error free designs and 3.79x in energy-efficiency and 2170x in error tolerance over existing error tolerant designs.

M-6 **0.4V SRAM with Bit Line Swing Suppression Charge Share Hierarchical Bit Line Scheme,** *S. Moriwaki*, A. Kawasumi*, T. Suzuki*, T. Sakurai**, S. Miyano,*Semiconductor Technology Academic Reserch Center(STARC), **The University of Tokyo*

128kbit SRAM with charge share hierarchical bit line scheme has been fabricated in 65nm foundry technology. By transferring the data between local bit lines and global bit lines with charge sharing, the variation of bit line swing which causes wasted power consumption in low voltage operation has been suppressed. 3.3μw/MHz of power consumption at 0.4V is achieved.

M-7 **An Output Structure for a Bi-Modal 6.4-Gbps GDDR5 and 2.4-Gbps DDR3 Compatible Memory Interface,** *Navin K. Mishra, Manish Jain, Phuong Le*, Sanku Mukherjee*, Arul Sendhil, Amir Amirkhany*, Rambus Chip Technologies, *Rambus Inc.*

A bi-modal x32 memory interface supports 6.4-Gbps GDDR5 signaling as well as 2.4-Gbps DDR3 signaling with a 1.5V IO supply. The interface incorporates a novel driver and pre-driver structure that supports one-tap equalization and presents very small capacitive loading to the pins. The entire interface, including both data and request channels achieves 11.6mW/Gbps and

27.7mW/Gbps energy efficiencies in GDDR5 and DDR3 modes respectively, and communicates successfully with 1.6-Gbps DDR3 and 6.0-Gbps GDDR5 DRAMs.

M-8 **A CMOS Image Sensor with on-chip Motion Detection and Object Localization,** *B. Zhao, X. Zhang, S. Chen, Nanyang Technological Univeristy*

This paper presents a CMOS image sensor with on-chip moving objects detection and localization. The sensor generates motion events by frame differencing. An on-chip localization unit processes the events on the fly and localizes moving objects in the scene. The sensor can switched to ROI mode and shoot a zoomed picture of the object. It has been fabricated using UMC 0.18 um CMOS process, power consumption was measured to only 0.4 mW at 100 FPS.

M-9 **Ultra Low-FOM High-Precision Delta-Sigma Modulators with Fully-Clocked SO and Zero Static Power Quantizers,** *Jian Xu, Xiaobo Wu, Menglian Zhao, Rui Fan, Hanqing Wang, Xiaofen Ma, Bill Liu*, Zhejiang University, *Analog Devices*

Two high-precision MBSO-based Delta-Sigma modulators with ultra low FOM (< 45fJ/conv.-step) are implemented in 0.18μm CMOS. To save 50% power, both modulators adopt novel fully-clocked SOs with new bias circuits. Modulator-I for bio-medical applications uses high density MOSCAPs and innovative area-efficient static power-less quantizer to achieve 85dB peak-SNDR over 10kHz BW and only 13μW at 1.0V supply. Modulator-II for audio applications employs another novel static power-less quantizer and duty cycle shift DWA to achieve 92dB peak-SNDR over 25kHz BW and only 58μW at 0.9V supply.

M-10 **A New CMOS Image Sensor Readout Structure for 3D Integrated Imagers,** *Shang-Fu Yeh+, Jin-Yi Lin+, Chih-Cheng Hsieh+, Ka-Yi Yeh* and Chung-Chi Jim Li* +Department of Electrical Engineering, National Tsing Hua, Taiwan *Industrial Technology Research Institute*

This paper presents a new CMOS image sensor (CIS) structure and ADC design for three-dimensional (3D) integrated imagers. The proposed CIS structure achieves a high spatial resolution without degrading the frame rate. A prototype chip shows that the array is expandable by modular sub-array design and is expected to achieve 100fps at multi-mega imaging for high-speed HDTV camera applications.

M-11 **All-Digital 3-50 GHz Ultra-Wideband Pulse Generator for Short-Range Wireless Interconnect in 40nm CMOS,** *C. Hu, Marvell Technology P. Chiang, Oregon State University*

A reconfigurable, 3-50GHz all-digital impulse generator for short-distance wireless communications is designed in 40nm-CMOS. Digital back-gate biasing is used for raised-cosine envelope pulse-shaping to achieve better spectral-mask efficiency. Pulse duration, duty-cycle, and operating frequency are digitally programmable, in order to satisfy multi-band standards compatibility. An asymmetric inverter design within the Mono-Pulse-Generator (MPG) eliminates undesired glitches for the complementary clock edge. Occupying 350umx260um die area, the proposed impulse transmitter achieves a maximum data-rate of 3Gbps and an energy-efficiency of 0.5pJ/pulse for a 25GHz carrier frequency.

M-12 **A 4GS/s, 8.45 ENOB and 5.7fJ/Conversion, Digital Assisted, Sampling System in 45nm CMOS SOI,** *M.A.T. Sanduleanu, S. Reynolds, J.O. Plouchart, IBM T.J. Watson Research Center*

A 4GS/s sampling system achieved 8.45-ENOB linearity with 5.7fJ/conversion energy efficiency. The measured IIP3 and IIP2 are 17.7dBm and 40dBm respectively. The ENOB of the sampler shows no degradation up to Nyquist frequency. Realized in a 45nm SOI CMOS the active area of the sampler is only 0.2 x 0.2mm^2.

M-13 **Energy-Efficient Transceiver Circuits for Short-Range On-chip Interconnects,** *J. Postman, P. Chiang, Oregon State University*

Transceiver blocks for low-swing signaling across short on-chip wires are proposed. First, a charge-sharing transmitter enables adjustable swing signaling from a single supply voltage. Compact sense-amplifier offset correction is introduced that enables improved sensitivity without increasing energy/conversion. Finally, digital hysteresis tuning is used to implement compact decision feedback equalization. Optimized for low-energy applications and operating from Vdd =

0.2-1.0V, measurements show energy efficiencies of 4.0-136fJ/bit/mm across 1mm and 4mm wires in 65nm-CMOS.

M-14 **A novel audio playback chip using digitally driven speaker architecture with 80%@-10dBFS power efficiency, 5.5W@3.3V supply and 100dB SNR,** *Michitaka Yoshino, Mitsuhiro Iwaide, Daigo Kuniyoshi, Hajime Ohtani, Akira Yasuda, Jun-ichi Okamura*, Hosei University., *Trigence Semiconductor*

A novel audio playback chip using digitally driven speaker architecture based on a delta-sigma modulator and newly proposed high-order mismatch shaper with novel dither circuit is presented. It can realize 5.5W output power into 4Ω speakers with only 3.3V power supply. The power efficiency from -10dBFS to 0dBFS is higher than 80%. The efficiency at low power output can realize long battery life. This chip can realize battery powered high-fidelity and high-power audio system.

M-15 **32-nm SOI Programmable, High-bandwidth 8.0-GHz Digital PLL,** *Sanjeev K Maheshwari, Emerson Fang, Sanjeev Aggarwal, AMD, Inc.*

A digital phase-locked loop to filter clock jitter in source-synchronous serial link applications is presented. The PLL achieves bandwidth programmability from 20 to 300 MHz while allowing for a maximum input frequency of 4 GHz. An improved resolution bang-bang phase detector and a double-regulated, supply-insensitive VCO mitigate extreme noise environments.

M-16 **A 38.6nV/Hz0.5 -59.6dB THD Dual-Band Micro-Electrode Array Signal Acquisition IC,** *Jing Guo, Jiageng Huang, Jie Yuan, Jessica Ka-Yan Law, Chi-Kong Yeung*, Mansun Chan, Hong Kong University of Science and Technology, *Chinese University of Hong Kong*

This paper reports the novel design of a dual-band monolithic MEA signal acquisition IC in a 0.35um CMOS process. It achieves low noise (0.9uVrms for LFP signal, 3.9uVrms for SP signal) and good linearity (-59.4dB THD for 20mVpp signal). Other performance also compares favorably against major bio-potential acquisition benchmark designs.

M-17 **Analysis and Modeling of On-Chip Power Combiners and their losses in LINC Transmitters,**

This paper presents a compact model for LINC (linear amplification with non linear components) transmitters an their power combiners. The study focuses on the detrimental effect of the transmission line nonidealities. A mathematical description of the system that considers these nonidealities is proposed. The developed analytical expressions can be used to optimize, analyze and build pre-distortion algorithms for this family of transmitters. The efficiency and linearity are reexamined in light of the new analytical expressions of the model.

M-18 **Programmable Phase/Frequency Generator for System Debug and Diagnosis Using The IEEE 1149.1 Test Bus,** *T.-Y. Tsai, G. Roberts, McGill University*

A method of analog signal generation is presented that is suitable for digital test methodologies such as the IEEE 1149.1 test standard; it can be used to produce phase and frequency signals for system test debug and diagnosis. A 0.13um chip at 4 GHz illustrates the signaling capabilities of this generator.

M-19 **Overlapped Inductors and Its Application on a Shared RF Front-end in a MultiStandard IC,** *L. Feng, R. Sadhwani, Y. Peperovits, C. D. Hull, J. C. Jensen, Intel Corporation*

A technique to build overlapped inductors at the same location while keeping good isolation between them is presented. The key idea is to use magnetic and electric cancellation to reduce coupling. A shared LNA for WiFi and Bluetooth (BT) applications using the overlapped inductor is proposed. It enables independent gain control up to the first RF stage in a receiver so that the system integration complexity is reduced.

M-20 **A 1.0V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis,** *Peiyuan Wang, Xiang Chen, Yiran Chen, Hai (Helen) Li*, Seung Kang**, Xiaochun Zhu**, Wenqing Wu**, University of Pittsburgh, *Polytechnic Institute of New York University, **Qualcomm Inc.*

A new nonvolatile latch design is proposed based on the magnetic tunneling junction (MTJ) devices. In the standby mode, the latched data can be retained in the MTJs without consuming any power. Two types of operation errors, namely, persistent and non-persistent errors, are quantitatively analyzed by including the process variations and thermal fluctuations during the read and write operations. A design at 45nm technology node is used as the example to discuss the design tradeoffs.

M-21 **A 1V 13mW Frequency-Translating Delta-Sigma ADC with 55dB SNDR for a 4MHz Band at 225MHz,** *P. M. Chopp, A. A. Hamoui, McGill University*

A frequency-translating delta-sigma ADC is fabricated in 1V 65nm CMOS. It uses single-path mixing inside its feedback loop to down-convert a 4MHz band from 225MHz (IF1) to 25MHz (IF2), achieving 55dB SNDR. Low power (13mW) is realized by sampling below IF1, and by noise-shaping at IF2.

M-22 **CMOS Color Sensor with Modulated Photodiode Depletion Region Depth,** *D. Ho, G. Gulak, R. Genov, University of Toronto*

A digital photo sensor is presented for multi-color fluorescent imaging. By electronically modulating the photo sensing region depth, the sensor reports intensity at discrete wavelengths. A 0.35um standard CMOS prototype integrates a spectrally-sensitive photodiode and a light-to-frequency analog-to-digital converter on the same die.

Session 10 – RF Building Blocks

Tuesday Morning, September 20
Oak Ballroom

Chair: Alberto Valdes-Garcia, IBM TJ Watson Research Center
Co-Chair: Andrea Mazzanti, Universita di Pavia

How to deal with non-linearity? This session presents recent advances in linearization techniques for PAs, a wide-band T/R switch, and exploiting non-linearity for frequency multiplication.

9:00 AM **Introduction**

9:05 AM 10-1 **A Fully Integrated Highly Linear Efficient Power Amplifier in 0.25µm BiCMOS Technology for Wireless Applications,** *H. Hedayati, M. Mobarak, G. Varin*, P. Meunier*, P. Gamand*, E. Sánchez-Sinencio, K. Entesari, Texas A&M University, *NXP Semiconductors*

A highly linear, efficient power amplifier in 0.25µm BiCMOS technology is presented. The linearity is improved by adding an auxiliary amplifier to the main bipolar junction transistor (BJT). The efficiency enhancement is achieved using a switchable biasing and output matching network. The experimental results show a gain of 13 dB and an output PdB of 21 dBm with a 32% PAE. The IM3 and IM5 terms are -41 dBc and -44 dBc at 21 dBm average output power.

9:30 AM 10-2 **A 1.9/2.4GHz Dual Band CMOS Power Amplifier with Integrated AM-PM Distortion Canceller,** *K. Onizuka, H. Isihara, M. Hosoya, S. Saigusa, O. Watanabe, S. Otaka, Toshiba Corporation*

A transformer-based dual band watt-level linear CMOS power amplifier is demonstrated for upcoming SDRs. Proposed AM-PM canceller improves ACLR of WCDMA uplink signal by 2.6dB at 28.0dBm output power. The test chip demonstrates peak output powers of 28.3dBm at 1.95GHz and 23.7dBm at 2.4GHz satisfying WCDMA and IEEE802.11g spectrum masks.

9:55 AM 10-3 **Managing Linearity in Radio Front-Ends (INVITED),** *Ranjit Gharpurey, University of Texas at Austin*

Front-end linearity plays a crucial role in determining the overall performance of a radio receiver. Non-linearity can impact performance in several ways, including degradation in sensitivity, reduction in gain and the appearance of spurious energy within the frequency band of interest from out-of-band sources.

In this paper, an overview of techniques for enhancing front-end linearity is presented. Circuit and device-level techniques, as well as architectures for linearization are described.

10:45 AM **BREAK**

11:05 AM 10-4 **A Transformer-Based Broadband I/O Matching-Balun-T/R Switch Front-end Combo Scheme in Standard CMOS,** *Yanjie Wang, Hua Wang, Chris Hull, Shmuel Ravid, Intel Corporation*

A transformer-based broadband front-end combo scheme (I/O matching, balun, and T/R switch) is proposed with high isolation and linearity performance. An implementation example is prototyped in a standard 90nm CMOS process covering a 1dB-bandwidth of 2GHz from 5GHz to 7GHz based on the total insertion loss. In transmitting (TX) mode, the complete front-end combo achieves 2.77dB insertion loss, +45.65dBm IIP3, and -42dB antenna-receiver isolation. In receiving (RX) mode, the front-end combo demonstrates an insertion loss of 2.62dB and +44.18dBm IIP3 with -42dB transmitter-antenna isolation. The front-end combo occupies a core area of 0.5mm2 including on-chip balun, which is conducive to broadband transceiver SOC integration.

11:30 AM 10-5 **A Low Conversion Loss Passive Frequency Doubler,** *Muhammad Adnan, Ehsan Afshari, Cornell University*

We propose a passive frequency multiplication technique that can achieve low conversion loss even for small input powers. Using this, a 20GHz doubler is designed in a 65nm CMOS process. The doubler is tested from 14GHz-25GHz and achieves conversion loss of 3.5dB with input power of 2.7dBm at 20GHz.

Session 11 – Over-Sampling Converters

Tuesday Morning, September 20
Fir Ballroom

Chair: Ron Kapusta, Analog Devices
Co-Chair: Pavan Hanumolu, Oregon State University

Over-sampling data converters using both discrete- and continuous-time look filters are presented. These converters cover signal bandwidths from 20 KHz up to 28 MHz and achieve excellent figure of merit.

9:00 AM **Introduction**

9:05 AM 11-1 **An 18μW 79dB-DR 20KHz-BW MASH ΔΣ Modulator Utilizing Self-Biased Amplifiers for Biomedical Applications,** *Le Wang, Luke Theogarajan*, Qualcomm Coorporation, *University of California Santa Barbara*

This paper presents a micro power, area-efficient 4th-order MASH delta-sigma modulator based on a novel self-biased amplifiers for neural sensing applications. A high-gain self-biased CMOS amplifier is proposed to achieve low power operation. Floating correlated double sampling technique is devised to enhance the amplifer's gain-linearity and hence the modulator's SFDR and SNDR performance. Fabricated in a 0.13 μm CMOS process, the prototype achieves 71 dB peak SNDR and 79 dB peak DR over 20 KHz neural signal bandwidth, while occupying only 0.06 mm2 silicon area. By optimizing the power budgets for different amplifiers, the MASH modulator consumes only 18 μW from 1.5 V supply. The proposed circuit techniques can be applied to other operational transconductance amplifier-based circuits for low power, high speed, and area-efficient design.

9:30 AM 11-2 **A 75dB SNDR, 10MHz Conversion Bandwidth Stage-Shared 2-2 MASH ΔΣ Modulator dissipating 9mW,** *Ramin Zanbaghi, Saurabh Saxena, Gabor C. Temes, and Terri S. Fiez, Oregon State University*

This paper presents a new stage-sharing technique in a discrete-time 2-2 MASH ΔΣ ADC to reduce the modulator power consumption. The proposed technique shares all active blocks of the modulator second stage with its first stage. The 2-2 MASH modulator utilizes second-order Chain of Integrators with Weighted Feed-forward Summation (CIFF) and Cascade of Integrators with Distributed Feedback Branches (CIFB) architectures for the first and second stages, respectively. Using the proposed technique, the second integrator and the adder op-amps of the modulator first stage are shared with

the first and second integrator op-amps of the second stage. Measurement results show that the modulator designed in a 0.13um CMOS technology achieves 75-dB SNDR over a 5MHz signal bandwidth with a clock frequency of 130MHz, while dissipating less than 9mW analog power.

9:55 AM 11-3 **A 1-1-1-1 MASH Delta-Sigma Modulator Using Dynamic Comparator-Based OTAs,** *K. Yamamoto, A. Chan Carusone, University of Toronto*

A 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs is presented. The proposed OTA asynchronously alternates between input comparison and current pulse injection. The 65-nm LP CMOS prototype achieves a FoM of 276 fJ/conv-step with 70.4 dB SNDR over a 2.5-MHz bandwidth while dissipating 3.73 mW from a 1.2-V supply.

10:20 AM 11-4 **A Double-Sampled Low-Distortion Cascade ΔΣ Modulator with an Adder/Integrator for WLAN Application,** *S. Lee, P. K. Hanumolu, G. C. Temes, J. Chae*, M. Aniya**, S. Takeuchi**, K. Hamashita**, Oregon State University, *Maxlinear, **Asahi Kasei Microdevices Corporation*

A cascade switched-capacitor ΔΣ analog-to-digital converter, suitable for WLANs, is presented. It uses a double sampling scheme with single set of DAC capacitors, and an improved low-distortion architecture with an embedded-adder integrator. The proposed architecture eliminates one active stage, and reduces the output swings in the loop-filter and hence the non-linearity. It was fabricated with a 0.18um CMOS process. The prototype chip achieves 75.5 dB DR, 74 dB SNR, 73.8 dB SNDR, -88.1 dB THD, and 90.2 dB SFDR over a 10 MHz signal band with an FoM of 0.27 pJ/conv-step.

10:45 AM **BREAK**

11:05 AM 11-5 **A 77dB SNDR, 4MHz MASH ΔΣ Modulator with a Second-Stage Multi-rate VCO-Based Quantizer,** *Samira Zali Asl, Saurabh Saxena, Pavan Kumar Hanumolu, Kartikeya Mayaram, Terri S. Fiez, Oregon State University*

A VCO-based MASH delta-sigma ADC consisting of a first-order switched-capacitor integrator with a 4-bit quantizer operating at 100MHz is followed by a second-stage VCO-based ADC operating at 1.2GHz. In a 130nm CMOS process, the prototype has a measured SNDR of 77dB with 4MHz signal bandwidth. The resulting FoM is 298fJ/conv.

11:30 AM 11-6 **A 16MHz BW 75dB DR CT Delta Sigma ADC Compensated for More than One Cycle Excess Loop Delay,** *Vikas Singh, Nagendra Krishnapura, Shanthi Pavan, Baradwaj Vigraham, Nimit Nigania, Debasish Behera, Indian Institute of Technology*

An 800MS/s CT Delta Sigma ADC with 16MHz/32MHz bandwidths consumes 47.6mW from 1.8V and occupies 1mm2 in a 0.18 μm CMOS process. The DR/SNR/SNDR for the two bandwidths are 75/67/65 dB and 64/57/57 dB respectively. Excess loop delay (ELD) of more than one cycle is compensated using a fast path outside the flash ADC. This and a low latency flash ADC and delay free DAC calibration result in the highest reported sampling rate in this process.

11:55 AM 11-7 **A 3.6GS/s, 15mW, 50dB SNDR, 28MHz Bandwidth RF Sigma-Delta ADC with a FoM of 1pJ/bit in 130nm CMOS,** *A. Ashry, H. Aboushady, LIP6 Laboratory*

A 4th order RF LC Sigma-Delta ADC clocked at 3.6GHz and centered at 900MHz is presented. The simplicity of the ADC architecture results in a significant performance enhancement and power consumption reduction. The ADC, suitable for Software Defined Radio applications, is implemented in a standard 130nm CMOS technology. It achieves a 52dB SFDR and a 50dB SNDR in a 28MHz BW and consumes only 15mW from a 1.2V supply. The Figure of Merit of the ADC is 1.0pJ/bit, which is to date the best reported FoM for an RF ADC. An efficient algorithm for the tuning and calibration of the Sigma-Delta LC-based loop filter is also presented in this paper.

Session 12 – Single Chip Architectures for Sensing and Signal Processing

Tuesday Morning, September 20
Pine Ballroom

Chair: Manoj Sachdev, University of Waterloo
Co-Chair: Ohsang Kwon, Samsung

Architectures for single-chip ICs utilizing neural networks and 2D signal processing for computational and energy challenges. Smart temperature sensing techniques for on-chip power efficiency and reliability.

9:00 AM **Introduction**

9:05 AM 12-1 **A 45nm CMOS Neuromorphic Chip with a Scalable Architecture for Learning in Networks of Spiking Neurons,** *Jae-sun Seo, Bernard Brezzo, Yong Liu, Benjamin D. Parker, Steven K. Esser*, Robert K. Montoye, Bipin Rajendran, José A. Tierno, Leland Chang, Dharmendra S. Modha*, and Daniel J. Friedman, IBM T. J. Watson Research Center, *IBM Research - Almaden*

We present a scalable integrated circuit platform for networks of spiking neurons. Through tight integration of memory (synapses) and computation (neurons), a 45nm reconfigurable chip comprising 256 neurons and 64K binary synapses with on-chip learning is demonstrated. Near-threshold, event-driven operation at 0.53V maximizes power efficiency for real-time pattern classification tasks.

9:30 AM 12-2 **A Digital Neurosynaptic Core Using Embedded Crossbar Memory with 45pJ per Spike in 45nm,** *Paul Merolla*, John Arthur*, Filipp Akopyan*, Nabil Imam**, Rajit Manohar**, Dharmendra Modha*, *IBM Research - Almaden, **Cornell University*

We fabricated a key building block of a modular neuromorphic architecture, a neurosynaptic core, with 256 digital integrate-and-fire neurons and a 1024 by 256 bit SRAM crossbar memory for synapses using IBM's 45-nm SOI process. Our fully digital implementation is able to leverage favorable CMOS scaling trends, while ensuring one-to-one correspondence between hardware and software. The core is fully configurable in terms of neuron parameters, axon types, and synapse states and is thus amenable to a wide range of applications.

9:55 AM 12-3 **Smart Integrated Temperature Sensor - Mixed-Signal Circuits and Systems in 32-nm and Beyond (INVITED),** *Y. William Li, H. Lakdawala, Intel Corporation*

Integrating smart temperature sensors into digital platforms facilitates information to be processed and transmitted, and open up new applications. Furthermore, temperature sensors are crucial components in computing platforms to manage power-efficiency trade-offs reliably under a thermal budget. This paper presents a holistic perspective about smart temperature sensor design from system- to device-level including manufacturing concerns. Through smart sensor design evolutions, we identify some scaling paths and circuit techniques to surmount analog/mixed-signal design challenges in 32-nm and beyond. We close with opportunities to design smarter temperature sensors.

10:45 AM **BREAK**

10:05 AM 12-4 **ReSSP: A 5.877 TOPS/W Reconfigurable Smart-Camera Stream Processor,** *Wei-Kai Chan, Yu-Hsiang Tseng, Pei-Kuei Tsung, Tzu-Der Chuang, Yi-Min Tsai, Wei-Yin Chen, Liang-Gee Chen, Shao-Yi Chien, National Taiwan University*

A 5.877 TOPS/W Reconfigurable Smart-camera Stream Processor is implemented in 90nm CMOS technology. A re-configurable hardware architecture with heterogeneous stream processing and subword-level parallelism is implemented to accelerate the vision processing for smart-camera applications. The area efficiency reaches 111.329 GOPS/mm2. The power efficiency and area efficiency are 4.5x to 33.0x and 3.8x to 74.2x better than the state-of-the-art works, respectively.

11:30 AM 12-5 **3.6-GHz 0.2-mW/ch/GHz 65-nm Cross-Correlator for Synthetic Aperture Radiometry,** *E. Ryman*, A. Emrich*, S. Andersson*, J. Riesbeck*, L. Svensson**, P. Larsson-Edefors**, *Omnisys Instruments AB, **Chalmers University of Technology*

A high-speed low-power cross-correlator ASIC has been implemented in a 65-nm CMOS process for the purpose of synthetic aperture radiometry from geostationary orbiting earth observation satellites. Experimental evaluation demonstrates that the chip has a top performance of 3.6 GHz at which it dissipates 790 mW.

Session 14 – VCOs, Quadrature VCOs, PLLs and All Digital PLLs

Tuesday Afternoon, September 20

Oak Ballroom

Chair: Rick Booth, Panasonic PWRL
Co-Chair: Earl McCune, Consultant

Signal generation is one of the fundamental building blocks in a wireless system. This session covers advances in VCO implementation, phase locked loops, and the emerging topics of all digital PLLs.

2:00 PM **Introduction**

2:05 PM 14-1 **A Dither-less All Digital PLL for Cellular Transmitters (INVITED),** *L. Vercesi, L. Fanori*, F. De Bernardinis, A. Liscidini*, R. Castello*, Marvell Italia Srl.,* University of Pavia*

Frequency synthesizer for cellular transmitters demands low phase-noise both in-band and out-of-band.. The paper describes the first dither-less ADPLL capable to satisfy both these requirements. These results are achieved exploiting a highly linear 2-dimension Vernier TDC and a very fine frequency resolution DCO. Both building blocks heavily rely on digital calibration techniques to precisely and efficiently implement two-point modulation and spur cancellation in the presence of many implementation impairments

2:55 PM 14-2 **A 0.5-V, 440-uW Frequency Synthesizer For Implantable Medical Devices,** *Wu-Hsin Chen, Wing-Fai Loke, Gabriel J. Thompson, Byunghoo Jung, Purdue University*

This paper presents an ultra-low-power, low-voltage frequency synthesizer designed for medical implantable devices. Several design techniques are adopted to address the issues in ultra-low voltage design. Implemented in a 130-nm CMOS technology, the 0.5-V medical band frequency synthesizer consumes 440uW with a phase noise of -91.5dBc/Hz at 1-MHz frequency offset.

3:20 PM 14-3 **A 4-GHz All Digital Fractional-N PLL with Low-Power TDC and Big Phase-Error Compensation,** *J-Y Lee, M.Park, M.Mhin, S-D Kim, M-Y Park, H-K Yu*

This paper presents an all-digital fractional-N PLL with a low-power TDC operating at the retimed reference clock. Two retimed reference clocks are employed to reduce the power of the proposed TDC estimating the fractional phase error between the reference clock and CKV clock. The application of the retimed reference clocks to TDC does not only reduce dynamic power in TDC delay inverter chain, but also simplify □r estimation including a new Tv calculation algorithm. Also, a phase-error compensation block is proposed for compensating for the big phase-error change due to the timing skew of all high-speed counter output bits. And a loop settling scanner is invented to shift DCO operation mode and additionally enhance PLL channel switching time for frequency hopping application. The proposed all-digital PLL represents - 36dBc integrated phase noise (1kHz - 20MHz), 778fs rms jitter, 9.6mW power consumption. The channel switching time of the ADPLL is measured as 630ns.

3:45 PM **BREAK**

4:00 PM 14-4 **A Quadrature LO Generator Using Bidirectionally-Coupled Oscillators for 60-GHz Applications,** *M. Hekmat, D. K. Su, B. A. Wooley, Stanford University*

A multiphase reference signal generation technique employing bidirectional coupling solves the frequency ambiguity and off-resonance operation issues in conventional coupled oscillators. Quadrature signals generated at twice the frequency of the loop drive a 40-GHz single-sideband transmitter that achieves a sideband suppression of 45dB in 90nm CMOS.

4:25 PM 14-5 **A 0.6V Quadrature VCO With Optimized Capacitive Coupling for Phase Noise Reduction,** *Feng Zhao, Fa Foster Dai, Auburn University*

This paper presents a 0.6V quadrature voltage-controlled oscillator (QVCO) with a novel capacitive coupling technique, which is employed not only for quadrature signal coupling, but also for noise reduction. As a result, the proposed QVCO can even achieve 3 to 5dB lower phase noise than a single-phase VCO of the same kind. Optimized capacitive coupling combined with inductive enhance-swing technique enables low-power consumption and low phase noise simultaneously. The QVCO achieves a measured phase noise of -132.3dBc/Hz @ 3MHz offset with a center frequency of 5.6GHz and consumes 4.2mW from a 0.6V supply. This performance corresponds to a Figure-of-Merit (FoM) of

191.5dB. The QVCO RFIC is implemented in a 0.13 μm CMOS technology with core area of 0.6x0.8mm2.

4:50 PM 14-6 **A Combined VCO and Divide-by-Two for Low-Voltage Low-Power 1.6 GHz Quadrature Signal Generation,** *Shen Wang, Dong Sam Ha, Beomsup Kim* and Vipul Chawla*, Virginia Tech, *Qualcomm*

We present a transformer-based VCO stacked with a divide-by-two for low-power quadrature signal generation. The VCO adopts Amstrong VCO configuration to alleviate small headroom and noise coupling encountered. Start-up condition and phase noise performance are analyzed. The LO fabricated in 65 nm CMOS dissipates only 2.6mW under 1V supply.

Session 15 – Phase-Locked Loop and Analog Techniques

Tuesday Afternoon, September 20
Fir Ballroom

Chair: Wei-Zen Chen, NCTU
Co-Chair: Kenneth Szajda, LSI Corporation

This session presents noise suppression techniques for PLL, a nested feedback frequency synthesizer, a high performance VCO using FBAR, and high dynamic range analog techniques.

2:00 PM **Introduction**

2:05 PM 15-1 **A 2.2GHz PLL using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise Suppression,** *Chun-wei Hsu, Karthik Tripurari, Shih-An Yu*, Peter R. Kinget, Columbia University, *Max Linear, Inc.*

Tri-state digital phase-frequency detectors (PFDs) are widely used for the large capture and locking range that they enable, but suffer from relatively large in-band phase noise. Subsampling phase detectors have recently been demonstrated to offer very low in-band noise but with only a very small capture range. We show how a PFD and a sub-sampling phase detector can be combined to maintain the phase-frequency detection capabilities while simultaneously obtaining in-band noise suppression. A 2.2GHz PLL is demonstrated in a 65nm CMOS process with an on-chip loop filter area of 0.04mm^2. The measured in-band phase noise improves from -110dBc/Hz to -122dBc/Hz when the auxiliary sub-sampling phase detector is active.

2:30 PM 15-2 **A Fractional-N Frequency Synthesizer using high-OSR Delta-Sigma Modulator and Nested-PLL,** *Pyoungwon Park, Dongmin Park, SeongHwan Cho, KAIST*

A nested-PLL(NPLL) architecture for low-noise wide-bandwidth fractional-N frequency synthesizer is presented. In order to reduce the quantization noise of the fractional-N PLL, delta-sigma modulator(DSM) is clocked at nine times of the reference frequency. A band pass filter, implemented in form of a PLL, is added to reduce the noise folding. Prototype implemented in 0.13um CMOS process achieves 26dB quantization noise suppression while consuming 9.6mW and occupying 0.46mm2

2:55 PM 15-3 **A Sub-100μW 2GHz Differential Colpitts CMOS/FBAR VCO,** *Jianlei Shi, Brian P. Otis,University of Washington*

We present a 2GHz FBAR-based differential Colpitts CMOS VCO with gm-boosting. The oscillator works with wide Vdd range(0.51V-1.5V). Under 0.6V nominal supply, the VCO consumes 126 uW and achieves -149 dBc/Hz phase noise at 1MHz offset,showing a FOM of -224dB. The minimum power consumption is 67uW with 0.51V Vdd.

3:20 PM 15-4 **A 60mW 1.15mA/channel Class-G Stereo Headphone Driver with 111dB DR and 120dB PSRR,** *Sherif Galal, Hui Zheng, Khaled Abdelfattah, Vinay Chandrasekhar, Iuri Mehr, Alex Jianzhong Chen, John Platenak, Nir Matalon, Todd L. Brooks*

A 60mW 111dB DR Class-G Stereo Headphone Driver is described. The driver utilizes higher-order loop filter to achieve PSRR of 120dB at the GSM TDMA rate of 217Hz. A driver architecture that combines Class-G and a split Class-AB/B amplifier reduces the quiescent current to 1.15mA/channel. A dual-voltage charge-pump with a single flying capacitor enables Class-G operation by adjusting the

supply rails as a function of the input signal. The driver supports battery range of 2.65V-4.5V and occupies an area of 2.3mm2 in 0.18µm CMOS technology.

3:45 PM **BREAK**

4:00 PM 15-5 **A Multi-GHz Area-Efficient Comparator with Dynamic Offset Cancellation,** *L. Kong, Y. Lu, E. Alon, University of California, Berkeley*

This paper proposes a dynamic impedance modulation technique to significantly improve the speed of comparators utilizing dynamic-offset-cancellation (DOC). Measurements show that proposed technique achieve 6X lower input-referred offset and 9X better power-supply-noise-rejection than a StrongArm comparator with only 20% speed penalty at identical core area (98um2) while dissipating 455uW.

4:25 PM 15-6 **Zero-Pole Modulation and Demodulation for Noise Reduction in Charge Amplifiers,** *N. Jaffari, K. Vleugels, B. Wooley, Stanford University*

A novel method of noise reduction, referred to as zero-pole modulation and demodulation, is proposed for charge amplifiers in photo-detection and sensor systems. The experimental charge amplifier achieves a noise reduction of 40% compared to a basic charge amplifier. The input-referred noise of the experimental charge amplifier is 100 ENC.

Session 16 – Embedded Memory Trends

Tuesday Afternoon, September 20
Pine Ballroom

Chair: Koji Nii, Renesas Electronics Corporation
Co-Chair: Chris Kim, University of Minnesota

Embedded memory topics ranging from low voltage SRAMs and emerging non-volatile memories to unclonable ID generation and fast ROMs in advanced technology nodes are presented.

2:00 PM **Introduction**

2:05 PM 16-1 **Device-Conscious Circuit Designs for 0.5-V High-Speed Memory-Rich Nanoscale CMOS LSIs (INVITED),** *A.Kotabe, K.Itoh, R.Takemura, R.Tsuchiya*, M.Horiguchi**, *Hitachi, Ltd., **Renesas Electronics Corporation*

Repair techniques and nanoscale FD-SOI MOSTs, sub-0.5-V logic circuits, a 0.5-V 1-Gb SRAM/DRAM, and compensations especially for process variations are discussed. Based on the discussion, it is concluded that a 0.5-V memory-rich CMOS LSI is possible while reducing the power to one-tenth that of a conventional 1-V CMOS LSI.

2:55 PM 16-2 **Dynamic Stability in Minimum Operating Voltage Vmin for Single-port and Dual-port SRAMs,** *Y. Tsukamoto, T. Kida, T. Yamaki, Y. Ishii, K. Nii, K. Tanaka, S. Tanaka, Y. Kihara, Renesas Electronics Corporation*

We discuss dynamic stability for single-port SRAM by examining Vmin difference between longer and shorter WL pulse width. Regarding dual-port SRAM, the Vmin degradation induced by WL pulse skew between ports in asynchronous operation is studied. The validity of our simulation results are verified by measured data for SRAM modules in 28nm generation.

3:20 PM 16-3 **Characterization of SRAM Sense Amplifier Input Offset for Yield Prediction in 28nm CMOS,** *Mohamed H. Abu-Rahma, Ying Chen, Wing Sy, Wee Ling Ong, Leon Yeow Ting, Sei Seung Yoon, Michael Han, Esin Terzioglu, Qualcomm Incorporated*

A process control monitor for SRAM sense amplifier (SA) offset is implemented in 28nm LP CMOS technology. The all-digital design of the monitor makes it adequate for low voltage testing, high speed data collection, and ease of migration to newer technologies. Detailed measurement results are provided for SA types at different conditions. Statistical yield estimation using the measured sense amplifier offset shows good correlation with measured yield for a 512Kb SRAM.

3:45 PM **BREAK**

4:00 PM 16-4 **Design Challenges for Prototypical and Emerging Memory Concepts Relying on Resistance Switching (INVITED),** *Ch. Muller, D. Deleruyelle, O. Ginez, J-M. Portal, M. Bocquet, IM2NP, Aix-Marseille University*

Integration of functional materials in memory architectures leads to emerging concepts with disruptive performances as compared to conventional charge storage technologies. Beside floating gate solutions such as EEPROM and Flash, these alternative devices involve voltage or current-controlled switching mechanisms between two distinct resistance states. The origin of the resistance change straightforwardly depends upon the nature and fundamental physical properties of func-tional materials integrated in the memory cell. After a general overview of non volatile memories, this paper is focused on prototypical and emerging memory cells and on their ability to withstand a downscaling of their critical dimensions. In addi-tion, despite different maturity levels, a peculiar attention is turned toward common guidelines helpful for designing em-bedded or distributed resistive switching memory circuits.

4:50 PM 16-5 **A 28 nm 50% Power Reduced 2T mask ROM with 0.72 ns Read Access Time Using Column Source Bias,** *Y. Umemoto, K. Nii, J. Ishikawa, K. Okamoto, K. Mori, K. Yanagisawa, Renesas Electronics Corporation*

We propose a new 2T mask ROM with dynamic column source bias control technique, which allows for high-speed operation, low-power consumption and reduction in cross-talk noise. The fabricated 128-kb ROM macro using 28-nm HK+MG technology realizes 0.72ns access time at 0.85V and a half power consumption of conventional ROM macro.

5:15 PM 16-6 **Improved Circuits for Microchip Identification using SRAM Mismatch,** *Multiple authors same affilliations: Srivatsan Chellappa, Aritra Dey , Lawrence T. Clark , Arizona State University*

In this paper we present a new, more robust hardware technique for generating secret keys and unique serial numbers using SRAM cells' inherent mismatch due to process variations in the constituent transistors. It is experimentally demonstrated and analyzed on a 90 nm test chip.

Poster Session

Tuesday Evening, September 20
Cascade/Sierra Ballroom

5:00 pm – 7:00 pm

T-1 **A Low-Power and Low-Noise 21~29 GHz Ultra-Wideband Receiver Front-End in 0.18 um CMOS Technology,** *S.L. Huang, Y.S. Lin, J.H. Lee, National Chi Nan University*

This paper presents the design and analysis of a 21~29 GHz CMOS receiver front-end in a standard 0.18 um CMOS process for ultra-wideband (UWB) automotive radar systems. The circuit comprises a low-noise amplifier (LNA), a double-balanced Gilbert-cell mixer, and two Marchand baluns. Over the 21~29 GHz automotive radar band, the receiver front-end exhibited excellent NF of 4.6±0.5 dB and conversion gain of 23.7±1.4 dB. The dc power dissipation was only 39.2 mW.

T-2 **A 2GHz Digital PLL, with Temperature Lock Range of -40°C to 125°C, in 45nm CMOS,** *B. Chattopadhyay, A. S. Kamath, S. Evani, K. Subburaj, Texas Instruments Inc.*

A 45nm, 0.09mm2, 0.5-50MHz input, 2GHz output, ring-oscillator Digital PLL, achieves -90dBC/Hz at 1MHz offset, and a temperature lock range of -40C to 125C. Outputs of any two adjacent current elements of the current-mode DAC in the DCO can be progressively brought out for separate Sigma-Delta (SD) operation. This enables the DPLL to track temperature over a large range, even as the SD step size and range are kept small to minimize jitter.

T-3 **Indirect Phase Noise Sensing for Self-Healing Voltage Controlled Oscillators,**

The push for higher performance analog/RF circuits in scaled CMOS necessitates self-healing via post-manufacturing tuning. A major challenge with self-healing is the efficient design of on-

chip sensors. We propose indirect sensing that exploits the correlations between the performance of interest and those that can be measured using easy-to-integrate sensors.

T-4 **An At-speed Self-testable Technique for the High Speed Domino Adder,** *Yu-Shun Wang, Min-Han Hsieh, Chia-Ming Liu, Chi-Wei Liu, James C.-M. Li, and Charlie Chung-Ping Chen, Graduate Institute of Electronics Engineering, National Taiwan University*

An at-speed self-testable technique is proposed for the high speed domino adder. We apply pseudo-exhaustive testing so that all testable faults in the 64-bit adder are detected by just 23K patterns. The adder latency is accurately measured by the programmable-skew clock generated from delay-locked loop (DLL). The proposed technique is validated on a 6.4GHz 64- bit domino adder with 181ps latency in 90nm CMOS technology. This on-chip technique is very useful for at-speed testing and speed binning of high performance CPU.

T-5 **A 95dB SNDR Audio ΔΣ Modulator in 65nm CMOS,** *L.Liu, D.Li,Y.Ye, L.Chen, Z.Wang, Tsinghua University*

A DT single loop 3rd order 5-bit ΔΣ modulator is implemented in 65nm CMOS. The modulator achieves 95dB SNDR with 24 kHz bandwidth and consumes only 371μW from 1V supply. SNDR keeps at 90.2dB with 133μW under 0.6V. The core area is 0.41mm2.

T-6 **A Fully Integrated CMOS Nanoscale Biosensor Microarray,** *Lei Zhang, Xiangqing He, Yan Wang, Zhiping Yu, Institute of Microelectronics, Tsinghua University*

This paper presents a fully integrated CMOS microarray for biosensor applications. A 64-pixel working electrode array with optimized reference and counter electrode structure is proposed to improve symmetry, and the feature sizes of electrodes have been scaled down to 600nm. The circuit utilizes the decoding scheme of memories to simplify the pixel design while shares potentiostat opamp and current amplifers, which allows the miniaturization of electrodes and enables large-scale integration of the microarray. The demo is fabricated in 0.18μm CMOS technology, and experimental results successfully demonstrated the biosensing detections on the nanoscale microarray. The circuit provides a current gain of 19.9dB, 3dB bandwidth of 15kHz, dynamic range of 141dB, sensing sensitivity of 37.6pA, and a driving capability of 0.46mA, respectively.

T-7 **A Passive UHF Tag for RFID-based Train Axle Temperature Measurement System,** *Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He, Institute of Microelectronics, Tsinghua University*

A fully integrated passive UHF RFID tag with embedded temperature sensor, compatible with the ISO/IEC 18000 type 6C protocol, is developed in a standard 0.18μm CMOS process, which is designed to measure the axle temperature of a running train. The consumption of RF/analog front-end circuits is 1.556μA@1.0V, and power dissipation of digital part is 5μA@1.0V. The CMOS temperature sensor exhibits a conversion time under 2 ms, less than 7 μW power dissipation, resolution of 0.31℃/LSB and error of +2.3/-1.1 ℃ with a 1.8 V power supply for range from -35 ℃ to 105 ℃. Measured sensitivity of tag is -5dBm at room temperature.

T-8 **A 48-mW, 12-bit, 150MS/s Pipelined ADC with Digital Calibration in 65nm CMOS,** *B. Peng, G.-Z. Huang, H. Li, P.-Y. Wan, P.-F. Lin,Beijing University of Technology, University of Science and Technology of China*

Digital calibrated pipelined ADC with peak SNDR=67dB,peak SFDR=81dB at 150MS/s sampling rate in 65nm CMOS process.

T-9 **Statistical VTH Shift Variation Self-Convergence Scheme Using Near Threshold VWL Injection for Local Electron Injected Asymmetric Pass Gate Transistor SRAM,** *K. Miyaji, Y. Shinozuka, S. Miyano*, K. Takeuchi, University of Tokyo, *STARC*

Statistical VTH shift variation in asymmetric pass gate transistor by local electron injection is studied. VD effect is self-compensated by ID effect. Near threshold VWL self-convergence injection is proposed to achieve self-convergence in VTH shift variation by enhancing ID effect.

The fabricated SRAM macro shows excellent operation margin.

T-10 **A Fully-integrated Optical Duobinary Transceiver in a 130nm SOI CMOS Technology,** *J. Buckwalter, J. Kim, X. Zheng*, G. Li*, K. Raj*, A. Krishnamoorthy*, UCSD, *Oracle Laboratories*

A 5-Gb/s, fully-integrated optical duobinary transceiver is demonstrated in a 130-nm silicon-on-insulator CMOS technology. Duobinary modulation is proposed to mitigate opto-electronic bandwidth limitations for photonic ring modulators. The circuit demonstrates an NRZ data eye of 500 uW amplitude and consumes 115 mW for analog and digital portions of the transmitter.

T-11 **Electrically-Driven Retargeting for Nanoscale Layouts,** *S. Banerjee*, K. B. Agarwal**, S. R. Nassif**, *IBM Research East Fishkill NY, **IBM Research Austin*

Scaling into the nanometer regime with limited lithographic capabilities leads to printability issues during manufacturing, which are due to lithographically poor target layout shapes. In this paper, we propose to perform electrically-aware modifications of the physical design to improve layout printability with minimum design perturbation. Results on sample 32nm layouts demonstrate that we can obtain required control over delay variability and lithographic yield using this method.

T-12 **A Partial Tree Vector Quantizer Dynamic Element Matching Technique for Audio Δ-Σ Converters,** *E. Hardy, H. Ihs, C. Dufaza, S. Meillère*, R. Bouchakour*, Primachip SAS, *IM2NP*

Multi-bit Delta-Sigma modulators are widely used in performing accurate, low-power, and low cost ADCs but their internal feedback DAC exhibits non-linearity. Unwanted tones and noise are generated in the band of interest. We propose in this paper a new vector-based Dynamic Element Matching scheme to avoid this effect.

T-13 **5 Gbps BPSK CMOS Transmitter with On-Chip Antenna Using Gaussian Monocycle Pulses,** *S. Kubota, N. Sasaki, M. Hafiz, A. Toya, T. Kikkawa, Hiroshima University*

A CMOS transmitter with on-chip dipole antenna using 65 nm CMOS technology was developed. The transmitter generated BPSK GMP whose center frequency was 10 GHz. GMP signals were transmitted and received by the on-chip dipole antennas. 5 Gb/s BPSK differential GMP was generated by PRBS of 27 with 1.51 pJ/bit.

T-14 **Amorphous Silicon Current Steering Digital to Analog Converter,** *A. Dey, D R. Allee, Flexible Display Center at Arizona State University*

A 6-bit current steering D/A converter (DAC) is built using only n-channel amorphous silicon (a-Si:H) thin film transistors (TFT) and capacitors. The circuit is built on silicon using a low temperature process, compatible with flexible plastic substrates. The measurements show reasonably good characteristics, achieving a DNL of less than ±1.2 LSB and INL of less than ±1.8 LSB.

T-15 **A 65nm CMOS Self-Terminated Open-Drain IDAC Line Driver Suitable for Fast Ethernet Applications,** *Joseph Aziz, Ark-Chew Wong*, Andrew Chen**, Derek Tam, Broadcom Corp., *Semtech Corp., **Lincoln Labs.*

A self-terminated line driver suitable for fast Ethernet operates in class AB mode and combines digital signal processing with low-power analog circuits. It dissipates 108mW, 48% less than an existing state-of-the-art design. It occupies 0.22mm2 in a 65nm standard CMOS technology and operates from a 2.5V supply.

T-16 **A High-PSR LDO using Feedforward Supply-Noise Cancellation Technique,** *B. Yang, B. Drost, Sachin Rao, P. K. Hanumolu, Oregon State University*

A feed-forward noise cancellation (FFNC) technique to improve the power supply noise rejection (PSR) of a low dropout regulator (LDO) is presented. The proposed FFNC operates in conjunction with a conventional LDO and extends the noise rejection bandwidth by nearly an order of magnitude. Fabricated in 0.18um CMOS, at 10mA load current, the prototype achieves a PSR of -50dB and -25dB at 1MHz and 10MHz supply noise frequencies, respectively. Compared to a conventional LDO, this represents an improvement of at least 30dB at 1MHz and 15dB at

10MHz. The prototype uses only 20pF load capacitance and occupies an active area of 0.04 mm^2.

T-17 **A Time-domain Latch Interpolation Technique for Low Power Flash ADCs,** *Jong-In Kim, Wan Kim, Barosaim Sung, Seung-Tak Ryu, KAIST*

A Time-domain latch interpolation technique is presented for low power flash analog-to-digital converter (ADC). The proposed technique reduces the number of first stage latches by half, and reduces power consumption and hardware complexity. A prototype 6bit 1GS/s flash ADC was designed for concept proof in a 90nm CMOS process.

T-18 **Low-Power Block-Level Instantaneous Comparison 7T SRAM for Dual Modular Redundancy,** *Shunsuke Okumura*, Yohei Nakata*, Koji Yanagida*, Yuki Kagiyama*, Shusuke Yoshimoto*, Hiroshi Kawaguchi*, Masahiko Yoshimoto*,**, *Kobe University, **JST, CREST*

This paper proposes a 7T SRAM that realizes a block-level instantaneous comparison feature. The data size that can be instantaneously compared is scalable. The proposed SRAM can compare 8-kb data in 130.0ns, and reduces power consumption in data comparison by 92.3%, compared to that of a parallel CRC circuit.

T-19 **A 40 nm 144 mW VLSI Processor for Realtime 60 kWord Continuous Speech Recognition,** *Multiple authors same affilliations : G.He, T.Sugahara, T.Fujinaga, Y.Miyamoto, H.Noguchi, S.Izumi, H.Kawaguchi, M.Yoshimoto, Kobe University*

We developed a low-power VLSI chip for 60-kWord real-time continuous speech recognition. We proposed several schemes to reduce the memory bandwidth and the operating clock frequency.We fabricated a VLSI test chip in 40 nm CMOS technology and measured the performance. Results show that the chip described in this paper can perform 60-kWord continuous real-time speech recognition at 126.5 MHz with power consumption of 144 mW and with little accuracy degradationn.

T-20 **A Non-Coherent Versatile DPSK Receiver for High Channel-Density Neural Prosthesis,** *Le Zheng, Kuanfu Chen, Wentai Liu, University of California, Santa Cruz*

A non-coherent versatile DPSK receiver for high channel-density neural prosthesis is presented. Detailed analyses on the non-idealities in realistic DPSK demodulation require a more adaptable DPSK receiver to ensure robust data recovery. New features such as tunable threshold voltage, area-efficient switched-capacitor array and flexible digital control are incorporated into the design. At a coil separation of 16mm, the receiver achieves a bit error rate of 2e-7 at a data rate of 2Mbps with a power consumption of 5.4mW.

T-21 **Performance, Metastability and Soft-Error Robustness Tradeoffs for Flip-Flops in 40nm CMOS,** *D. Rennie, D. Li, M. Sachdev, B. Bhuva*, S. Jagannathan*, S-J. Wen**, R. Wong**, University of Waterloo, *Vanderbilt University, **Cisco Systems Inc.*

In this paper the design tradeoffs for flip-flops between performance, soft-error robustness and metastability are analyzed. SPICE simulations are used to characterize flip-flop performance and metastability. 40nm flip-flops are fabricated and in radiation testing Quatro flip-flops showed improved SER and metastability compared with both a reference flip-flop and DICE flip-flop.

T-22 **A 5-GS/s 4-Bit Flash ADC with Triode-Load Bias Voltage Trimming Offset Calibration in 65-nm CMOS,** Junjie Yao, Guangzhou Runxin Information Tech. Co. Ltd., China, and Jin Liu, The University of Texas at Dallas, TX

A 5-GS/s 4-bit ADC is implemented in 65-nm MCOS. Offset calibration is achieved by digitally adjusting the bias voltages of the triode loads in the preamplifier without introducing additional capacitive loading in the analog path and degrading the high-speed performance. The ADC consumes 34.3 mW from a 1.2-V supply at 5 GS/s, and occupies 0.0828mm^2 active area. The ADC achieves 3.93 ENOB with a 2.5-GHz ERBW and a 0.45-pJ/convstep FOM at 5 GS/s.

Session 18 – mm Wave Circuits and Systems

Wednesday Morning, September 21
Oak Ballroom

Chair: Ehsan Afshari, Cornell University
Co-Chair: John Rogers, Carleton University

There is growing interest in mm-wave frequency range for communication, sensing, and imaging. The papers in this session present advances in CMOS implementation of such systems.

9:00 AM **Introduction**

9:05 AM 18-1 **Silicon RF Circuit Technologies Enabling mm-Wave Wireless Systems (INVITED),** *J. Long, Y. Zhao, Y. Jin, W. Wu, G. Gentile, M. Spirito, Delft University of Technology*

Silicon SoCs capable of millimeter-wave (mm-wave) frequency operation now offer a combination of performance, functionality, integration scale and cost unrivaled by other IC technologies. The components, design techniques and circuits that are propelling deep submicron silicon technologies in mm-wave system front-ends are surveyed in this paper. Examples relevant to Gbit/s rate wireless communication are highlighted, with emphasis on innovations drawn from the recent literature.

9:55 AM 18-2 **A 76-81GHz Transmitter with 10dBm Output Power at 125C for Automotive Radar in 65nm Bulk CMOS,** *K. To, V. Trivedi, Freescale Semiconductor Inc.*

A high power and wide tuning range CMOS-only transmitter, composed of a VCO and a power amplifier, operating from -40C to 125C for automotive radar is presented. The transmitter has 10dBm output power at 125C and >10GHz tuning range to cover PVT variations, with power consumption of 420mW. The 77GHz phase noise is -87dBc/Hz at 1MHz offset.

10:20 AM 18-3 **A 2.9-dB Noise Figure, Q-Band Millimeter-Wave CMOS SOI LNA,** *M. Parlak, J.F. Buckwalter, University of California, San Diego*

This paper discusses a two-stage low noise amplifier(LNA) implemented in a 45nm CMOS SOI process that operates between 43 and 53 GHz. The LNA stages are based on a cascode amplifier with simultaneous noise and input power matching. The LNA exhibits a minimum noise figure (NF) of 2.9 dB at 47 GHz and measured gain of 18.5 dB at 49 GHz. The output P1dB compression power is 3 dBm and saturation output power is 7 dBm to reach a peak efficiency of 22%. The measured OIP3 is 14 dBm. The LNA occupies an area of 0.35mm^2 with pads and consumes 19 mA from 1.2 V supply. The results present the lowest noise figure for a silicon-based millimeter-wave LNA.

10:45 AM **BREAK**

11:05 AM 18-4 **A High Gain 107 GHz Amplifier in 130 nm CMOS,** *O. Momeni, E. Afshari, Cornell University*

A systematic method to design high gain amplifiers at frequencies close to the fmax of the transistors is introduced. Next, in a 130 nm CMOS process, we design and implement a 107 GHz amplifier with a gain of 12.5 dB, PAE of 4.4%, and saturated output power of >2.3 dBm.

11:30 AM 18-5 **Double-Balanced 130-180 GHz Passive and Balanced 145-165 GHz Active Mixers in 45 nm CMOS,** *O. Inac, A. Fung*, G.M. Rebeiz, Univeristy of California, San Diego, *NASA Jet Propulsion Laboratory*

This paper presents wideband passive and active mixers in the 100-200 GHz range. The mixers are built using a 45nm CMOS SOI process with an ft of 220 GHz when referenced to the top metal layer. The passive double-balanced mixer results in a conversion loss of 12-13 dB from 130-180 GHz (including balun, transmission line and GSG pad losses) and achieves optimal performance with 3 dBm of LO power (referenced to the GSG LO pads). The active mixer achieves a conversion loss of 4.5 dB with a 3-dB bandwidth of 145-165 GHz, and consumes only 10 mW of DC power from a 1.5 V supply. The application areas are in wideband Gbps communications, imaging arrays with large IF bandwidths, and mm-wave spectrometers. To our knowledge, this work represents the first demonstration of high performance CMOS mixers in the 130-180 GHz frequency range.

11:55 AM 18-6 **60GHz Low-Loss Compact Phase Shifters Using A Transformer-Based Hybrid in 65nm CMOS,** *M. Tabesh, A. Arbabian, A. Niknejad, University of California, Berkeley*

Two compact, low-loss, passive reflective type 60GHz phase shifters are presented in standard 65nm CMOS using lumped-element baluns to implement the hybrid. The first architecture achieves 180 degrees phase shift with an average loss of 6.6dB and area of 0.031mm2. The second phase shifter demonstrates the best reported average loss of 4.5dB with an area of 0.048mm2 while having 150 degrees of phase shift. These are the smallest reported 60GHz phase shifters in silicon.

Session 19 – Nyquist A/D

Wednesday Morning, September 21
Fir Ballroom

Chair: Erick Naviasky, Cadence
Co-Chair: George LaRue, Washington State University

This year we have 4 Nyquist A/D's starting with a nW SAF for biomedical applications. Then we have a comparator based 2 step A/D and finish with 2 time-interleaved High-speed converters.

9:00 AM **Introduction**

9:05 AM 19-1 **A 0.5V 1KS/s 2.5nW 8.52-ENOB 6.8fJ/Conversion-Step SAR ADC for Biomedical Applications,** *Tsung-Che Lu, Lan-Da Van, Chi-Sheng Lin*, Chun-Ming Huang*, National Chiao Tung University, *National Chip Implementation Center*

A SAR ADC with leakage reduction bootstrapped switch (LRBS) and low-power approach for biomedical applications is presented. LRBS is employed to alleviate the leakage caused by the low-power approach for increasing SNDR. The 0.18μm CMOS prototype achieves 6.8fJ/conversion-step and 2.5nW under a 0.5V supply at 1KS/s with a Nyquist input.

9:30 AM 19-2 **A 0.7V 810μW 10b 30MS/s Comparator-Based Two-Step Pipelined ADC,** *Ho-Young Lee, David Gubbins*, Bumha Lee**, Un-Ku Moon, Oregon State University, *Linear Technology, **National Semiconductor*

This paper presents a 10b 30MS/s comparator-based two-step pipelined ADC that uses a comparator instead of an opamp to reach low-voltage and low-power operation with a rail-to-rail input. The prototype ADC, fabricated in a 0.13μm CMOS process, consumes 810μW at 0.7V supply and achieves 121fJ FOM at 10MHz input frequency.

9:55 AM 19-3 **A 450 MS/s 10-bit Time-Interleaved Zero-Crossing Based ADC,** *Jack Chu, Hae-Seung Lee, Massachusetts Institute of Technology*

A 450-MS/s 10-bit time-interleaved zero-crossing based pipelined ADC is described. The prototype ADC, fabricated in a 90-nm CMOS process, occupies 1.3 mm2. A reference pre-charging technique is applied to reduce the voltage ripples on the reference voltages. Gain, offset, and timing calibration is applied to achieve an 8.7 ENOB with a 211 MHz input signal and dissipates 34 mW from a 1.2V supply for a FOM of 182 fJ/step.

10:20 AM 19-4 **A 40-mW 7-bit 2.2-GS/s Time-Interleaved Subranging ADC for Low-Power Gigabit Wireless Communications in 65-nm CMOS,** *I-Ning Ku, Zhiwei Xu, Yen-Cheng Kuan, Yen-Hsiang Wang, Mau-Chung Frank Chang, University of California, Los Angeles*

A compact, low-power time-Interleaved ADC is presented. Novel time-splitting subranging architecture is invented to significantly boost the speed of individual ADC channels. In addition, a low-power and fast-settling distributed resistor array for reference voltages is proposed to mitigate mismatches within channels.

10:45 AM **BREAK**

Session 20 – Enhanced Simulation Techniques

Wednesday Morning, September 21
Pine Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting
Co-Chair: Frank Liu, IBM Austin Research Lab

This session presents the latest advancements in fast timing simulation algorithms, statis tical modeling, parasitic extractors, as well as simulation techniques for special power-gating structures.

9:00 AM **Introduction**

9:05 AM 20-1 **High-Dimensional Statistical Modeling and Analysis of Custom Integrated Circuits (INVITED),** *Trent McConaghy, Solido Design Automation Inc.*

Custom circuit designers have long favored manual equation-based approaches in early design stages, because it gives excellent insight and control over the design. However, this flow is threatened: as modern process nodes advance, process variation affects circuit performance more strongly, hurting the accuracy of existing equations. Because designers are typically not statistical modeling experts, it is difficult to adapt the equations to incorporate statistical variations. This paper presents a fast, deterministic technique to help designers revise equations to account for statistical variation. Specifically, the technique extracts compact equations of performance as a function of process variables, even for cases when there are thousands of possible variables and the equations are highly nonlinear. In fact, it provides a whole set of equations that trade off simplicity versus accuracy compared to SPICE. The technique is validated on a broad range of custom integrated circuit modeling problems.

9:55 AM 20-2 **Fast and Accurate Simulation of Mixed-Signal Systems in SystemVerilog with Data Supplementation,** *Myeong-Jae Park, Hanseok Kim, Minbok Lee, Jaeha Kim, Seoul National University*

This paper presents a methodology for simulating behaviors and performances of complex mixed-signal systems with an event-driven HDL simulator. Prototype models for a PLL and a high-speed I/O system demonstrate 50-times and 80-times faster simulation speeds, respectively, with the same or better accuracy compared with the conventional Verilog models.

10:20 AM 20-3 **Enhanced Sensitivity Computation for BEM Based Capacitance Extraction Using the Schur Complement Technique,** *Y. Bi, S. de Graaf, N.P. van der Meijs, Delft University of Technology*

We present a useful extension for an existing algorithm of capacitance sensitivity computation w.r.t. multiple geometric variations. The extension achieves an even better accuracy at a modest increase of computational cost compared to the existing algorithm. With such an extension, the enhanced algorithm can provide different solutions for different requirements of accuracy and efficiency. This algorithm provides a flexible tool for BEM-based extractors subject to process variations.

10:45 AM **BREAK**

11:05 AM 20-4 **Power Gating Implementation for Noise Mitigation with Body-Tied Triple-Well Structure,** *Y. Takai, M. Hashimoto, T. Onoye, Osaka University*

This paper investigates power-gating implementations that mitigate power supply noise. We focus on the body connection of power-gated circuits, and examine the amount of power supply noise induced by power-on rush current and the contribution of a power-gated circuit as a decoupling capacitance during the sleep mode. To figure out the best implementation, we designed and fabricated a test chip in 65nm process. Experimental results with measurement and simulation reveal that the power-gated circuit with body-tied structure in triple-well is the best implementation from the following three points; power supply noise due to rush current, the contribution of decoupling capacitance during the sleep mode and the leakage reduction thanks to power gating.

11:30 AM 20-5 **Exploration Of On-Chip Switched-Capacitor DC-DC Converter For Multicore Processors Using A Distributed Power Delivery Network,** *P. Zhou, D. Jiao, C. H. Kim, S. S. Sapatnekar, University of Minnesota*

We explore the design of on-chip switched-capacitor DC-DC converters for chip-multiprocessors using an accurate power grid simulator. Results show that distributed design of switched-capacitor converters can achieve largely improved IR noise and supply voltage compared to lumped design. We also demonstrate the usage of switched-capacitor converters for multi-domain power supply.

Session 21 – Power Management

Wednesday Morning, September 21
Cedar Ballroom

Chair: Jerry Zheng, Iwatt
Co-Chair: William McIntyre

Effective power management requires innovative techniques to optimize system cost and efficiency. This session includes advancements in power management for emerging applications and nanometer CMOS.

9:00 AM **Introduction**

9:05 AM 21-1 **A 90nm Data Flow Processor Demonstrating Fine Grained DVS for Energy Efficient Operation from 0.25V to 1.2V,** *Y. Shakhsheer, S. Khanna, K. Craig, S. Arrabi, J. Lach, and B. H. Calhoun, University of Virginia*

We present a 90nm data flow processor that executes DSP algorithms using fine grained DVS at the component level with rapid VDD switching and VDD dithering for near-ideal quadratic dynamic energy scaling from 0.25V-1.2V. Measurements show energy savings up to 50% and 46% compared to single-VDD and multi-VDD alternatives.

9:30 AM 21-2 **An Integrated Four-Phase Buck Converter Delivering 1A/mm2 with 700ps Controller Delay and Network-on-Chip Load in 45-nm SOI,** *N. Sturcken, M. Petracca, S. Warren, L. P. Carloni, A. V. Peterchev*, K. L. Shepard, Columbia University, *Duke University*

We present a four-phase integrated buck converter in 45nm SOI technology. The controller uses unlatched pulse-width modulation (PWM) with nonlinear gain to provide both stable small-signal dynamics and fast response (~700ps) to large input and output transients. This fast control approach reduces the required output capacitance by 5X in comparison to a controller with latched PWM at similar operating point. The converter switches at 80MHz and delivers 1A/mm2 at 83% efficiency and 0.66 conversion ratio.

9:55 AM 21-3 **A Wide-Range DC/DC Converter with 2nd Order Digital Compensation and Direct Battery Connection in 40nm CMOS,** *Justin Shi, Ying-Chih Hsu, Eric Soenen, Alan Roth, Justin Gaither*

This paper presents a digital DC-DC converter with 2nd order compensation and direct battery connect capability in 40nm CMOS. A combination of circuit and process technology is used to achieve an input range up to 5.5V with peak efficiencies of 95%. It also outlines an approach to optimize a control loop based on a sigma-delta ADC and higher order digital filter, which is demonstrated on a prototype achieving step response times under load below 38µs/V.

10:20 AM 21-4 **An 80% Peak Efficiency, 0.84mW Sleep Power Consumption, Fully-Integrated DC-DC Converter with Buck/LDO Mode Control,** *X. Gong, J. Ni*, Z. Hong, B. Liu*, Fudan University, *Analog Devices*

A fully-integrated step-down DC-DC converter with LDO mode to reduce the sleep power consumption and improve efficiency at light loads is presented. It reaches 80% at 90mA load, and efficiency at 10mA load increases by 22.6%. Furthermore, the sleep power consumption is reduced from 10mW without hybrid mode to 0.84mW.

10:45 AM **BREAK**

11:05 AM 21-5 **Perturbation On-time (POT) Control and Inhibit Time Control (ITC) in Suppression of THD of Power Factor Correction (PFC) Design,** *Jen-Chieh Tsai, Chi-Lin Chen, Yi-Ting Chen, Chia-Lung Ni, Chun-Yen Chen, Ke-Horng Chen, Chih-Jen Chen*, Heng-Lin Pan*, National Chiao Tung University,*

**Industrial Technology Research Institute*

The paper presented the perturbation on-time (POT) control technique to suppress the total harmonic distortion (THD) to improve the performance of the power factor correction (PFC) in the AC-DC converter. Simultaneously, it can improve the efficiency through the proposed inhibit time control (ITC) mechanism at low AC input voltage. The test circuit fabricated in TSMC 800V UHV process can show the highly-integrated PFC controller. Experimental results demonstrate low THD of 8%, which results in high PF of 99%. Besides, high efficiency of 95% can be ensured at the output power of 90W.

11:30 AM
21-6 **A Reconfigurable 2x / 2.5x / 3x / 4x SC DC-DC Regulator for Enhancing Area and Power Efficiencies in Transcutaneous Power Transmission,** *X. Zhang, H. Lee, University of Texas at Dallas*

A reconfigurable 2x / 2.5x / 3x / 4x switched-capacitor DC-DC regulator for transcutaneous power transmission is presented in this paper. The proposed power stage enables the regulator to maintain high power efficiencies under different input voltages caused by coupling variations. A fixed on-time regulation scheme is developed to minimize the switching power loss and to achieve small output ripple voltages of the regulator. Implemented in a standard 0.35-um n-well CMOS process, the proposed regulator delivers a maximum output current of 10 mA and achieves the peak power efficiency of 82%. When the input voltage varies by 1.6 V, the power efficiency of the proposed regulator can be improved by 40% compared to that of the fixed-ratio 4x counterpart. The output ripple reaches 0.5% of the output voltage.

11:55 AM
21-7 **A Zero Cross-Regulation (Zero-CR) Single-Inductor Bipolar-Output (SIBO) Converter with an Active-Energy-Correlation Control for Driving Cholesteric-LCD,** *Yu-Huei Lee, Ming-Yan Fan, Wei-Chung Chen, Ke-Horng Chen, Sheng-Fa Liu*, Pao-Hsien Chiu*, Sandy Chen*, Chun-Yu Shen*, Ming-Ta Hsieh*, Huai-An Li*, National Chiao Tung University, *Chunghwa Picture Tubes, Ltd.*

A zero cross-regulation (zero-CR) single-inductor bipolar-output (SIBO) converter with an adaptive-energy correlation (AEC) control is proposed as a compact power management solution for driving cholesteric-LCD (Ch-LCD). The SIBO converter can provide a pair of positive and negative output voltages with only one external inductor for achieving the polarity reversion operation in Ch-LCD to obtain high-quality displays. The proposed AEC control decides energy distribution for bipolar outputs without any cross regulation through the embedded prediction function. The chip fabricated by 0.25 μm CMOS process demonstrates zero cross-regulation at bipolar outputs with 90 % peak power conversion efficiency.