SHORT COURSE:
45nm CMOS Technology

Sunday, December 12, 9:00 a.m. - 5:30 p.m.
Continental Ballroom 1-4

Course Organizer: *Clement Wann, IBM*

The continued scaling of CMOS technology will necessitate tremendous innovation in device structures, materials and processes. Driven by aggressive technology roadmap requirements and diverse application-driven requirements, the 45nm technology node will require substantial technology development and innovation in device structure, front-end and back-end materials and processes, and lithography technology. In particular, the challenges facing 45nm CMOS technology development are substantial, with several critical manufacturing and technology solutions still unknown or in early development. This short course will analyze the requirements of 45nm CMOS technology, and will evaluate the status of the various requisite device and process technologies, including device structure, channel materials and architecture, gate stack technology and processes, contact and junction technology, lithography technology, and backend interconnect and dielectric technology. Though five lectures, the current status, development trends, and outlooks for the various components of 45nm CMOS technology will be evaluated.

The first lecture will discuss device architectural requirements for 45nm CMOS technology. Roadmap requirements will be used to drive evaluation of various conventional and non-conventional approached to achieving 45nm CMOS performance targets, based on both high-performance and low-power application needs. The second lecture will focus on several critical front-end process modules and their implications on technology scaling to 45nm and beyond. Channel engineering and contact and junction scaling will be discussed in relation to their current status and outlook for the future. The third lecture will focus on gate-stack related issues. In this lecture, the status of high-k dielectric and metal gate electrode development will be analyzed in terms of current status, problems that remain to be solved and technology outlook. The fourth lecture will describe lithography technology for the 45nm CMOS technology node. In this lecture, the status of 193nm immersion lithography as well as alternate technologies such as 157nm and EUV lithography will be reviewed. This talk will also introduce several implementation and design / manufacturability issues, including data preparation, design rules, proximity correction, etc. Status of photoresists and manufacturability issues will also be discussed. The final lecture will focus on backend process technology for the 45nm node. The status of copper and low-k dielectrics will be reviewed, as will the associated process technologies for planarization and etching. Finally, reliability and integration issues will be reviewed. Thus, through this series of lectures, a comprehensive overview of the status and outlook for 45nm CMOS technology will be provided.

Introduction

Instructor: Clement Wann, IBM, Hopewell Junction, NY

45nm Device Architecture and Roadmap

Instructor: Mark Rodder, Texas Instruments, Dallas, TX

Introduction
- Application requirements
- Scaling issues
- Roadmap and factors of uncertainty

Trends and challenges
- Power
- Performance
- Density / scaling

Potential Device architectures
- Scaling of “conventional” architectures
- Insertion of new materials
- Novel device structures

What will 45 nm CMOS be?
- Device architecture for low standby power applications
- Device architecture for high performance applications

Channel, Source/Drain, and Contact Engineering

Instructor: Mehmet Ozturk, North Carolina State University, Raleigh, NC

Introduction
Scaling the Planar MOSFET - Where is the limit?
Junction Scaling Limits- Series Resistance: Accumulation, Spreading, bulk and contact
- Limitations of conventional junction processes
- Potential solutions - Deposited SiGe Junctions, Dual Metal Contacts, Schottky junctions Channel Doping Limits
- Mobility
- Junction Leakage
- Threshold control

Life beyond the planar MOSFET - Channel Engineering for 45 nm and beyond
- Transport-Enhanced MOSFETs
- Strained Silicon Channels - Conventional Approaches
- Local Strain
- Ge as a channel material - pros and cons

Fully Depleted MOSFETs
- Ultra-thin body fully depleted MOSFETs
- Strained Si and SiGe on Insulator MOSFETs
- FINFETs

Junction and contact challenges of MOSFETs with alternative channel structures
- Fundamental Challenges - work function, scalability, and local strain
- Manufacturing Challenges – dimensional control, stability, compatibility with advanced materials

Potential Manufacturing Processes

Advanced Gate Stacks: High-K Dielectrics and Metal Gates

Motivation for use of high-k dielectric materials
Material requirements for high-k gate dielectrics
Overview of deposition techniques and processes
- ALD, MOCVD, PVD
- Metal oxides and silicates
- Nitridation and Interface preparation

High-k + polysilicon - the good, the bad and the ugly news
- VT control
- Device degradation

Motivation for metal gates
Performance of metal gate stacks
- Current Status
- Mobility issues
- VT instabilities
- Reliability

Conclusions and future outlook

Lithography Technology for 45nm CMOS

Instructor: Timothy Brunner, IBM, NY

Introduction
- Lithography as information flow
- Rayleigh scaling equations
- Lithography trends - wavelength, NA, K1, DoF, Tool Cost, Throughput

Advanced data preparation methods
- WYSIWYG is dead
- Sub-resolution Assist Features
- Phase shape and trim shape generation
- Optical Proximity Correction
- Design for Manufacturability

193nm immersion litho for 45nm
- Fundamentals of immersion
- Immersion exposure tools
- Immersion resist processes
- Alternatives - 157nm, EUV?

Resist processing trends
- Chemically amplified resist processes
- Reflectivity control - BARCs, TARCs, etc.
- Multi-layer approaches

Manufacturability issues
- CD specifications and process control
- Overlay error
- Defect control
- Throughput and economics

Conclusions

SUNDAY

BEOL Technology for the 45nm Technology Node

Instructor: John Sudijono, Chartered Semiconductor, Singapore

Introduction
Overview of low k Dielectrics and development status
- Porous low k (=2.2-2.5) dielectrics
- Ultra Porous low k (< 2.0) dielectrics

Metallization
- Cu Barrier and Seed: Materials and processes
- Cu Plating approaches
- Cu encapsulation

CMP and Wet Clean Processes
- Low down-Force polishing
- New chemical polishing approaches
- Supercritical cleaning technology

Etching and Ashing
- Etch challenges with selectivity and Profile control
- Ashing with benign chemistries for ultra porous low k

Integration and Reliability Issues and Challenges
- Novel integration approaches
- Reliability requirements and challenges

Conclusions

SHORT COURSE: Devices for Next Generation Digital Consumer Circuits and Systems

Sunday, December 12, 9:00 a.m. - 5:30 p.m.
Continental Ballroom 6-9

Course Organizer: Akira Matsuzawa, Tokyo Institute of Technology

In recent years sales of digital consumer electronic integrated circuits (used in digital TVs, DVD players, digital cameras, flat panel displays, digital audio systems, etc.) have increased to the point that they have become a significant share of the total semiconductor market. Looking forward, these systems show tremendous potential for continued growth. Digital consumer electronics will therefore extend its impact on corporate technology roadmaps and will become a new technology driver for semiconductor devices with product-specific needs, such as already occurs for personal computer and internet technologies. This short course will give insight into features of next generation digital consumer circuits and systems and and will evaluate the consequences of digital consumer electronics on device specifications from the perspective of both design and technology. Five technology flavors - system on chip (SoC), mixed signal technology, memories, imaging device, and packaging technology - will be reviewed from this perspective. Within the individual lectures, the technical outlook of the various technologies will be evaluated, based on their relationships with digital consumer electronic products and the associated device and technology requirements and trends.

The first lecture will discuss several aspects of SoC for digital consumer systems, including technology requirements and design issues. In particular, major SoC architectures such as embedded processors, media processors, and reconfigurable circuits will be discussed in depth. The second lecture will reveal the role of mixed

signal technology in digital consumer systems and discuss the current and future requirements and technology trends. The implications of digital consumer system requirements on device matching, RF circuit applications, and low-voltage operation, among others, will be discussed. The third lecture will provide an overview of memory devices for digital consumer systems. Nonvolatile memory, which has become increasingly important with the proliferation of digital consumer electronics, will be discussed in detail. Embedded memory and multi-chip packaging technology will also be discussed in this talk. The fourth lecture will provide an overview of imaging devices. The importance of these devices has increased rapidly due to the tremendous success of digital cameras. Basic characteristics, development history, current topics, and future trend of CCD and CMOS sensor devices will be reviewed. Finally, in the fifth lecture, packaging technologies for digital consumer electronics, including systems in package (SiP) will be reviewed. Requirements of digital consumer systems in relation to packaging will be discussed, including system modeling/partitioning and EDA technology. Cost-performance tradeoffs between SoC and SiP will be addressed, thus providing a broad overview of the implications of digital consumer systems on microelectronics technology from the level of devices through to design and packaging.

Introduction

Instructor: Akira Matsuzawa, Tokyo Institute of Technology, Tokyo, Japan

SoC Design

Instructor: Katsuhiko Ueda, Matsushita Electric Industrial, Japan

Digital consumer electronics and SoC
- Overview of digital consumer electronics market
- Role of SoC in digital consumer products
- Examples of SoC for digital consumer use – DTV, DVD, and 3rd generation cellular phone

Requirements for SoC design
- Concurrent system design
- Performance and cost
- Low power consumption
- Short-turnaround-time development
- Software issues

Design technologies for SoC
- Embedded processors
- Media processors
- IP development
- Mixed signal technology
- Embedded memory technology
- Low power technology
- Electronic Design Automation

Future technology trends
- SiP technology
- Design for manufacturability
- Reconfigurable logic

Mixed Signal Technology

Instructor: Maarten Vertregt, Philips, Netherlands

Introduction
- System life cycle, system trends
- System hierarchy (application, function, building block, circuit, technology)
- Digital consumer electronics impacts on mixed signal technology.
- Differentiating features - digital/analog

Circuit abstraction: Design methodology and design system with EDA tools.

Technology trends
- Technology scaling
- Diversity of demands

Silicon device requirements
- Device matching
- Power supply requirements
- RF CMOS technology
- Low voltage operation and use of scaled CMOS
- Energy efficiency

Memory Devices

Instructor: Paolo Cappelletti, ST Microelectronics, France

Memory evolution for next generation digital systems
- Application convergence
- Memory needs for portable consumer appliances
- Working memory (RAM)
- Code storage (NVM and XIP)
- Mass storage (NVM, high density, low cost)
- Power consumption and foot print constraints
- Memory market trends

NVM technologies
- Floating-gate memory
- Discrete traps memory
- Emerging technologies

System integration
- Embedded memory
- Multi-chip package technology

Imaging Devices

Instructor: Yoshiaki Hagiwara, Sony Corporation, Japan

Imaging Devices for Digital Consumer Systems
- Digital Information consumer products that utilize imaging devices
- Requirements for imaging devices
- Classification of image sensors

CCD Technology
- Basic device characteristics
- History of development
- Current topics and future

CMOS Sensor Technology
- Basic device characteristics
- History of development
- Current topics and future

Circuits and Module Technology
- Role of circuits and module technology
- Technology roadmap
- Impact on device and process technology

Packaging Technology

Instructor: David B. Tuckerman, Tessera, San Jose, CA

Digital consumer systems and packaging technology
- Packaging hierarchy (chip-level through system-level)
- Requirements and constraints on chip package technologies

Classification and comparison of chip packaging technologies
- Single-chip packages
- Leadframe based (SOP, QFP, QFN)
- Substrate based (BGA, FBGA, LGA)
- Wafer level
- Multi-chip packages
- System-in-package (SiP)
- Embedded passives

EDA tools for packaging technology
- Layout and Electrical analysis
- Thermal and Stress analysis

System-level integration and miniaturization
- Partitioning considerations
- Case studies

Technology roadmap

Plenary Session

Monday, December 13, 9:00 a.m.
Continental Ballroom

Welcome and Awards

General Chair: Jeff Welser, IBM Almaden Research

Invited Papers

Technical Program Chair: Jon Candelaria, Motorola

1.1 IEDM – A View as a Participant and a Customer, Louis Parrillo, Parrillo Consulting, LLC

On this fiftieth anniversary, we will discuss some of the inner workings of the IEDM that have enabled its success. We will also discuss the conference's impact on the industry. A historical perspective, from the early 1970's, as well as a future viewpoint will be presented on both topics.

Continually refining the IEDM to be pioneering, impartial, international, educational and (sometimes) entertaining has been deliberate and planned, and is a result of the people, the processes and the structure of the meeting.

Breakthroughs and advances in an extremely broad set of technologies have first appeared at IEDM. They have fueled the industry's progress and the world's interest in this meeting. Such topics include the early use of ion implantation and plasma etching, advances in Silicon and Compound Semiconductor technologies, Bipolar, NMOS, CMOS, HBT's, treatments of short-channel-device behavior, scaling of unipolar and bipolar devices, hot-carrier device degradation, DRAM, SRAM, NVRAM, new device structures, elucidation of device behaviors and their limitations, innovative new modules, fabrication techniques, new forms of sensors, MEMs, displays, modeling and other key technologies.

Emerging new applications including robotics, bioelectronics, the pervasive use of sensors, and nanotechnology, as well as the continued evolution of today's product applications will drive future technologies. The technical challenges continue to grow and become exacerbated by economic challenges. Looking forward, we will discuss some ways in which IEDM may evolve to continue to inform, guide and serve its customers.

1.2 Future Semiconductor Manufacturing – Challenges and Opportunities, Hiroshi, Iwai, Tokyo Institute of Technology

Although the progress of semiconductor devices has been the driving force of the development of our intelligent society for more that 30 years, there is a big concern for the manufacturing of the future devices because of expected skyrocketing cost and insufficient performance improvement. In this talk, the following topics will be presented to predict the future of semiconductor devices and their production; 45nm (and below) manufacturing challenges, implications of wafer size growth (300 mm impact on the economics of scaling? 450 mm and beyond?), ASIC vs. custom IC foundries, expected impact of new Asian foundry regions (for example China), etc.

1.3 Emerging Technologies on Silicon, Michel Brillouet, Deputy Director, CEA/LETI

Moore's Law and its mapping into the ITRS have been the most powerful drivers of the progress in microelectronics in the last decades. This paper will discuss possible future directions while approaching the 'end-of-the-roadmap'. Looking at some of the expected fundamental and practical limits of the different building blocks for an information processing system, namely the processing unit, memories, interfaces and communication, and the interconnection of these elements, we will discuss long term evolutionary paths as well as some more disruptive approaches. Furthermore an enhanced progress is expected from a synergetic development of the building blocks and of the system architecture, with some exploratory paths departing from the present way of thinking, e.g. through bio-inspired architectures.

Session 2: Displays, Sensors and MEMS – MEMS Technologies and Applications

Monday, December 13, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairs: Darrin Young, Case Western Reserve University
Jo DeBoeck, IMEC

1:30 p.m.
Introduction

1:35 p.m.
2.1 High-Speed MEMS-based Gas Chromatography, M. Agah, G. R. Lambertus, R. D. Sacks, and K. D. Wise, University of Michigan, Ann Arbor, MI

2:00 p.m.
2.2 A Reliable and Compact Polymer Based Package for Capacitive RF-MEMS Switches, Y. Oya, A. Okubora, Sony Corp., Kanagawa, Japan and M. Van Spengen, P. Soussan, S. Stoukatch, X. Rottenberg, E. Beyne, P. De Moor, I. De Wolf, and K. Baert, IMEC, Heverlee, Belgium

2:25 p.m.
2.3 A Fully Integrated CMOS and High Voltage Compatible RF MEMS Technology, L. Guan, J. K. O. Sin, H. Liu*, and Z. Xiong, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong and *Cornell University, Ithaca, NY

2:50 p.m.
2.4 Post Fabrication Laser Trimming of Micromechanical Filters Via an Effective Spring Constant Algorithm (ESCA), M. A. Abdelmoneum, M. U. Demirci, S-S Li, C. T.-C.Nguyen, University of Michigan, Ann Arbor, MI

3:15 p.m.
2.5 A Trench-Sidewall Single-wafer-MEMS Technology and its Typical Application in High-Performance Accelerometers, X. Li, B. Cheng, Y. Wang, L. Gu, J. Dong, H. Yang, X. Ge, M. Liu, Chinese Academy of Sciences, Shanhai, China

3:40 p.m.
2.6 An Electrothermally-Actuated, Dual-Mode Micromirror for Large Bi-Directional Scanning, A. Jain, S. Todd, H. Xie, University of Florida, Gainesville, FL

4:05 p.m.
2.7 Novel Ferroelectrics-Based Micro-Acoustic Devices and Their Ultrasonic Applications, Y-P Zhu, T-L Ren, Y. Yang, L-T Liu, Z-J Li, Tsinghua University, Beijing, China

Session 3: Integrated Circuits and Manufacturing – DRAM

Monday, December 13, 1:30 p.m.
Continental Ballroom 4

Co-Chairs: Luan Tran, Micron Technology
Harald Seidl, Infineon

1:30 p.m.
Introduction

1:35 p.m.
3.1 Highly Scalable Sub-50nm Vertical Double Gate Trench DRAM Cell, T. Schloesser, D. Manger, R. Weis, S. Slesazeck, F. Lau, S. Tegen, M. Sesterhenn, K. Muemmler, J. Nuetzel, D. Temmler, B. Kowalski, U. Scheler , M. Stavrev, D. Koehler, Infineon Technologies, Dresden, Germany

2:00 p.m.
3.2 Enhanced Data Retention of Damascene-finFET DRAM with Local Channel Implantation and <100> Fin Surface Orientation Engineering, J-M Yoon, C. Lee, M-S Yi, C-H Lee, J.C. Park, T.Y. Kim, H.S. Kang, S.K. Sung, E.S. Cho, H.J. Cho, Y.J. Ahn, D. Park and K. Kim, Samsung Electronics, Kyoungi-Do, Korea

2:25 p.m.
3.3 Lattice Strain Design in W/WN/Poly-Si Gate DRAM for Improving Data Retention Time, K. Okonogi, K. Ohyu, A. Toda* and H. Kobayashi, Elpida Memory, Inc and *NEC Corporation, Kanagawa, Japan

2:50 p.m.
3.4 Mechanically Enhanced Storage Node for Virtually Unlimited Height (MESH) Capacitor Aiming at Sub 70nm DRAMs, D.H. Kim, J.Y. Kim, M. Huh, Y.S. Hwang, J.M. Park, D.H. Han, D.I. Kim, M.H. Cho, B.H. Lee, H.K. Hwang, J.W. Song, N.J. Kang, G.W. Ha, S.S. Song, M.S. Shim, S.E. Kim, J.M. Kwon, B.J. Park, H.J. Oh, H.J. Kim, D.S. Woo, M.Y. Jeong, Y.I. Kim, Y.S. Lee, H.J. Kim JC. Shin, J.W. Seo, S.S. Jeong, K.H. Yoon, T. H. Ahn, J.B. Lee, Y.W. Hyung, S.J Park, H.S. Kim, Y.T. Choi, G.Y. Jin, Y.G. Park, K. Kim, Samsung Electronic, K Youngi-do, Korea

3:15 p.m.
3.5 A Highly Manufacturable Deep Trench Based DRAM Cell Layout with a Planar Array Device in a 70nm Techonogy, J. Amon, A. Kieslich, L. Heineck, T. Schuster J. Faul, J. Luetzen, C. Fan** , C.-C. Huang**, B. Fischer*, G. Enders*, S.Kudelka, U. Schroeder, K.-H. Kuesters , G. Lange*, J. Alsmeier*, Infineon Technologies AG, Dresden, Germany and *Munich, Germany and **Nanya Technology Corp., Taiwan, ROC

Session 4: Process Technology – Fully-Silicided (FUSI) Gates

Monday, December 13, 1:30 p.m.
Continental Ballroom 5

Co-Chairs: Jakub Kedzierski, IBM TJ Watson Research Center
Gyoyoung Jin, Samsung Electronics

1:30 p.m.
Introduction

1:35 p.m.
4.1 Advanced Gate Stacks with Fully Silicided (FUSI) Gates and High-k Dielectrics: Enhanced Performance at Reduced Gate Leakage, E.P. Gusev, C. Cabral, Jr., B.P. Linder, Y.H. Kim, K. Maitra, E. Cartier, H. Nayfeh*, N. Bojarczuk, A. Callegari, R. Carruthers, M.M. Frank, S. Fang*, S. Guha, M. Gribelyuk, P. Jamison, R. Jammy, M. Ieong, P. Kozlowski, V. Ku*, D. Lacey, D. LaTulipe, V. Narayanan, H. Ng*, P. Nguyen*, J. Newbury, V. Paruchuri, R. Rengarajan*, G. Shahidi, A. Steegen*, M. Steen, S. Zafar and Y. Zhang, IBM SRDC, Yorktown Heights, NY and * IBM Microelectronic Division, Hopewell Junction, NY

2:00 p.m.
4.2 Partial Silicides Technology for Tunable Work Function Electrodes on High-k Gate Dielectrics Fermi Level Pinning Controlled $PtSi_x$ for $HfO_x(N)$ pMOSFET, T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita*, M. Ohno, H. Ota*, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake and A. Toriumi*#, ASET, Tsukuba, Japan and *AIST, Tsukuba, Japan and #University of Tokyo, Tokyo, Japan

2:25 p.m.
4.3 Work Function Tuning Through Dopant Scanning and Related Effects Ni Fully Silicided Gate for Sub-45nm Nodes CMOS, D. Aime, B. Froment, F. Cacho, V. Carron*, S. Descombes, Y. Morand, N. Emonet, F. Wacquant, T. Farjot*, S. Jullian**, C. Laviron, M. Juhel, R. Pantel, R. Molins, D. Delille, A. Halimaoui, D. Bensahel, STMicroelectronics, Grenoble, France and *CEA-LETI, **Philips Semiconductor, Crolles France and **Centre des Materiaux Pierre-Marie Fourt, Evry, France

2:50 p.m.
4.4 Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique for 45nm-node LSTP and LOP Devices, K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki, NEC Corporation, Kanagawa, Japan

3:15 p.m.
4.5 Proposal of New HfSiON CMOS Fabrication Process (HAMDAMA) for Low Standby Power Device, T. Aoyama, T. Maeda, K. Torii, K. Yamashita, Y. Kobayashi, S. Kamiyama, T. Miura, H. Kitajima and T. Arikado, Selete, Tsukuba, Japan

3:40 p.m.
4.6 Diffusion-less Junctions and Super Halo Profiles for PMOS Transistors Formed by SPER and FUSI Gate in 45 nm Physical Gate Length Devices, S. Severi*#, K. G. Anil*, J. B. Pawlak**, R. Duffy**, K. Henson*, R. Lindsay^, A. Lauwers*, A. Veloso*, J.-F. de Marneffe*, J. Ramos*, B. Sijmus*, K. Devriendt*, R. A. Camillo-Castillo*, P. Eyben*, W. Vandervost*, M. Jurczak*, S. Biesemans* and K. De Meyer*#, *IMEC, Leuven, Belgium, #KU Leuven, Arenberg, Belgium, **Philips Research Leuven, Heverlee, Belgium and ^Infineon, Munich, Germany

Session 5: CMOS and Interconnect Reliability – NBTI Effect in Conventional and High-k Dielectrics

Monday, December 13, 1:30 p.m.
Continental Ballroom 6

Co-Chairs: Muhammad Ashraful Alam, Purdue University
Samuel Pan, TSMC

1:30 p.m.
Introduction

1:35 p.m.
5.1 Mechanism of Negative Bias Temperature Instability in CMOS Devices: Degradation, Recovery and Impact of Nitrogen (Invited), S. Mahapatra, M.A. Alam*, P. Bharath Kumar, T. R. Dalei and D. Saha, Indian Institute of Technology, Bombay, India, * Purdue University, West Lafayette, IN

2:00 p.m.
5.2 "On-the-fly" Characterization of NBTI in Ultra-Thin Gate-Oxide PMOSFETs, M. Denais , A. Bravaix**, V. Huard*, C. Parthasarathy, G. Ribes, F. Perrier*, Y. Rey-Tauriac and N.Revil, STMicroelectronics, Crolles, France, *Philips Semiconductors, Crolles, France, **UMR CNRS, Toulon, France

2:25 p.m.
5.3 A Geometrical Unification of the Theories of MBTI and HCI Time Exponents and Its Implications for Ultra-Scaled Planar and Surround Gate MOSFETs, H. Kufluoglu, M. Alam, Purdue University, West Lafayette, IN

2:50 p.m.
5.4 Influence of Nitrogen in Ultra-thin SiON on Negative Bias Temperature Instability under AC Stress, Y. Mitani, Toshiba Corporation, Yokohama, Japan

3:15 p.m.
5.5 Negative Bias Temperature Instabilities in HfSiON/TaN-based pMOSFETs, M. Houssa, M. Aoulaiche, S. Van Elshocht, S. De Gendt, G. Groeseneken, and M.Heyns, IMEC, Leuven, Belgium

3:40 p.m.
5.6 HCI and BTI Characteristics of ALD HfSiO(N) Gate Dielectrics as the Compositions and the Post Treatment Conditions, J.P. Kim, Y.-S. Kim, H.J. Lim, J.H. Lee, S. J. Doh, H.-S. Jung, S.-K. Han, M.-J. Kim, J.-H. Lee, N.-I. Lee, H.-K. Kang, K.-P. Suh, and Y.-S. Chung, Samsung Electronics Co., Kyunggi-Do, Korea

4:05 p.m.
5.7 Physical Model of BTI, TDDB and SILC in HfO_2-Based High-k Gate Dielectrics, K. Torii, K. Shiraishi*, S. Miyazaki**, K. Yamabe*, M. Boero*, T. Chikyow***, K. Yamada***, H. Kitajima, and T. Arikado, Semiconductor Leading Edge Technologies, Ibaraki, Japan, University of Tsukuba, Ibaraki, Japan, **Hiroshima University, Hiroshima, Japan, ***National Institute for Materials Science, Ibaraki, Japan

Session 6: Modeling and Simulation – Tranpsort in Nanoscale Silicon-Based FETs – I

Monday, December 13, 1:30 p.m.
Continental Ballroom 7-9

Co-Chairs: Mark Stettler, Intel
Enrico Sangiorgi, University of Bologna

1:30 p.m.
Introduction

1:35 p.m.
6.1 Simulation Study of Ge n-channel 7.5 nm DGFETs of Arbitrary Crystallographic Alignment, S. E. Laux, IBM, Yorktown Heights, NY

2:00 p.m.
6.2 Bandstructure Effects in Ballistic Nanoscale MOSFETs, A. Rahman, G. Klimeck and M. Lundstrom, Purdue University, West Lafayette, IN

2:25 p.m.
6.3 Relevance of Remote Scattering in Gate to Channel Mobility of Thin-Oxide CMOS Devices, P.M. Solomon and M. Yang, IBM, Yorktown Heights, NY

2:50 p.m.
6.4 Quantum Mechanical Calculation of Hole Mobility in Silicon Inversion Layers Under Arbitrary Stress, E. Wang, P. Matagne, L. Shifren, B. Obradovic, R. Kotlyar, S. Cea, J. He, Z. Ma, R. Nagisetty, S. Tyagi, M. Stettler and M.D.Giles, Intel Corporation, Hillsboro, OR and *Santa Clara, CA

3:15 p.m.
6.5 Impact of Surface Roughness on Silicon & Germanium Ultra-Thin-Body MOSFETs, T. Low, M.F. Li, W.J. Fan*, N.S. Tyam*, Y.-C. Yeo, C. Zhu, A. Chin***, L. Chan** and D.L. Kwong****, National University of Singapore, Singapore, *Nanyang Technological University, Singapore, **Chartered Semiconductor Manufacturing, Singapore, ***National Chiao Tung University, Taiwan, ROC, ****University of Texas, Austin, TX

Session 7: CMOS Devices – Strained Silicon I

Monday, December 13, 1:30 p.m.
Imperial Ballroom A

Co-Chairs: Kelin Kuhn, Intel
Manoj Mehrotra, Texas Instruments

1:30 p.m.
Introduction

1:35 p.m.
7.1 Selectively Formed High Mobility Strained Ge PMOSFETs for High Performance CMOS, H. Shang, J. Chu, S. Bedell, E. P. Gusev, P. Jamison, Y. Zhang, J. Ott, M. Copel, D. Sadana, K. Guarini and M. Ieong, IBM T.J. Watson Research Center, Yorktown Heights, NY

2:00 p.m.
7.2 Low Power Device Technology with SiGe Channel, HfSiON, and Poly-Si Gate, H.C.-H. Wang, S.-J. Chen, M.-F. Wang, P.-Y. Tsai, C.-W. Tsai, T.-W. Wang, S.M. Ting, T.-H. Hou, P.-S. Lim, H.-J. Lin, Y. Jin, H.-J. Tao, S.-C. Chen, C.H. Diaz, M.-S. Liang, and C. Hu, TSMC, Taiwan, ROC

2:25 p.m.
7.3 Performance Comparison and Channel Length Scaling of Strained Si FETs on SiGe-on-Insulator (SGOI), J. Cai, K. Rim, A. Bryant, K. Jenkins, C. Ouyang, D. Singh, Z. Ren*, K. Lee, H. Yin*, J. Hergenrother, T. Kanarsky*, A. Kumar, X. Wang*, S. Bedell, A. Reznicek, H. Hovel, D. Sadana, D. Uriarte*, R. Mitchell*, J. Ott, D. Mocuta*, P. O'Neil*, A. Mocuta*, E. Leobandung*, R. Miller, W. Haensch and M. Ieong*, IBM SRDC, Yorktown Heights, NY, *IBM Microelectronics Division, Hopewell Junction, NY

2:50 p.m.
7.4 Impact of Parasitic Resistance and Silicon Layer Thickness Scaling for Strained-Silicon MOSFETs on Relaxed $Si_{1-x}Ge_x$ Virtual Substrate, H. Kawasaki, K. Ohuchi, A. Oishi, O. Fujii, H. Tsujii, T. Ishida, K. Kasai, Y. Okayama, K. Kojima, K. Adachi, N. Aoki, T. Kanemura, D. Hagishima*, M. Fujiwara, S. Inaba, K. Ishimaru, N. Nagashima** and H. Ishiuchi, Toshiba Corporation Semiconductor Company, Kanagawa, Japan, *Toshiba Corporation, Yokohama, Japan, **Sony Corporation, Japan

3:15 p.m.
7.5 High Electron and Hole Mobility Enhancements in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator, I. Äberg, C. Ní Chléirigh, O.O. Olubuyide, and J.L. Hoyt, MIT, Cambridge, MA

3:40 p.m.
7.6 Performance Enhancement of Partially- and Fully-Depleted Strained-SOI MOSFETs and Characterization of Strained-Si Device Parameters, T. Numata, T. Irisawa, T. Tezuka, J. Koga, N. Hirashita, K. Usuda, E. Toyoda*, Y. Miyamura**, A. Tanabe, N. Sugiyama, and S. Takagi***, MIRAI-ASET, Kanagawa, Japan, *Toshiba Ceramics, **Komatsu Electronic Metals, ***MIRAI-AIST, Japan

4:05 p.m.
7.7 3D GOI CMOSFETs with Novel IrO_2(Hf) Dual Gates and High-k Dielectric on 1P6M-0.18µm-CMOS, D. S. Yu, A. Chin, C. C. Laio, M. W. Ma, W. J. Chen*, C. Zhu**, M.-F. Li**, and D. L. Kwong***, National Chiao Tung University, Hsinchu, Taiwan, ROC, *National Yun-Lin Polytechnic Inst., Huwai, Taiwan, ROC, **National University of Singapore, Singapore, ***The University of Texas, Austin, TX

Session 8: Solid State Devices – Room Temperature Single Electronics and Tunneling Devices

Monday, December 13, 1:30 p.m.
Imperial Ballroom B

Co-Chairs: Zoran Krivokapic, AMD
Adrian Ionescu, EPFL

1:30 p.m.
Introduction

1:35 p.m.
8.1 Room-Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching, M. Saitoh, H. Harata, and T. Hiramoto, University of Tokyo, Tokyo, Japan

2:00 p.m.
8.2 Transistor in a Test Tube - Harnessing Molecular Biology to the Self-Assembly of Molecular Scale Electronics (Invited), U. Sivan, Technion-Israel Institute of Technology, Haifa, Israel

2:25 p.m.
8.3 The Tunneling Field Effect Transistor (TFET) as an Add-on for Ultra-Low-Voltage Analog and Digital Processes, Th. Nirschl, P.-F. Wang*, C. Weber*, J. Sedlmeir*, R. Heinrich*, R. Kakoschke*, K. Schrufer#, J. Holz*, C. Pacha*, T. Schulz*, M. Ostermayr*, A. Olbrich*, G. Georgakos*, E. Ruderer*, W. Hansch, D. Schmitt-Landsiedel, Technical Univ., Munich, Germany, *Infineon Technologies, Munich, Germany

2:50 p.m.
8.4 Room-Temperature Single-Electron Transfer and Detection with Silicon Nanodevices, K. Nishiguchi, A. Fujiwara, Y. Ono, H. Inokawa, and Y. Takahashi, NTT Corporation, Kanagawa, Japan

3:15 p.m.
8.5 80nm Self-Aligned Complementary I-MOS Using Double Sidewall Spacer and Elevated Drain Structure and Its Applicability to Amplifiers with High Linearity, W.Y. Choi, J.Y. Song, B.Y. Choi, J.D. Lee, Y.J. Park, and B.-G. Park, Seoul National University, Seoul, Korea

Session 9: CMOS Devices – Strained Silicon II

Tuesday, December 14, 9:00 a.m.
Grand Ballroom A

Co-Chairs: Qi Xiang, AMD
Howard C.-H. Wang, TSMC

9:00 a.m.
Introduction

9:05 a.m.
9.1 Technology Booster Using Strain-Enhancing Laminated SiN (SELS) for 65nm Node HP MPUs, K. Goto, S. Satoh, H. Ohta, S. Fukuda, T. Yamamoto, T. Mori, Y. Tagawa, M. Sakuma, T. Saiki, H. Morioka, N.Tamura, N. Horiguchi, M. Kojima, T. Sugii, and K. Hashimoto, Fujitsu Limited, Tokyo, Japan

9:30 a.m.
9.2 A Novel Strain Enhanced CMOS Architecture Using Selectively Deposited High Tensile And High Compressive Silicon Nitride Films, S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, Fujitsu, Ltd., Tokyo, Japan

9:55 a.m.
9.3 Mobility Improvement for 45nm Node by Combination of Optimized Stress Control and Channel Orientation Design, T. Komoda, A. Oishi, T. Sanuki, K. Kasai, H. Yoshimura, K. Ohno*, M. Iwai, M. Saito*, F. Matsuoka, N. Nagashima* and T. Noguchi, Toshiba Corporation, Kanagawa, Japan, *Sony Corporation, Yokohama, Japan

10:20 a.m.
9.4 Key Differences of Uniaxial Process (vs. Substrate Biaxial) Stressed Si and Ge Channel MOSFETs, S.E. Thompson, University of Florida, Gainesville, FL

10:45 a.m.
9.5 In-Plane Mobility Anisotropy and Universality Under Uni-Axial Strains in n- and p-MOS Inversion Layers on (100), (110), and (111)Si, H. Irie, K. Kita, K. Kyuno, and A. Toriumi, The University of Tokyo, Tokyo, Japan

11:10 a.m.
9.6 Experimental Study of Biaxial and Uniaxial Strain Effects on Carrier Mobility in Bulk and Ultrathin-body SOI MOSFETs, K. Uchida, R. Zednik, C.-H. Lu, H. Jagannathan, J. McVittie, P.C. McIntyre, and Y. Nishi, Stanford University, Stanford, CA

11:35 a.m.
9.7 Package-Strain-Enhanced Device and Circuit Performance, S. Maikap, M. H. Liao, F. Yuan, M. H. Lee*, C.-F. Huang, S. T. Chang** and C. W. Liu, National Taiwan University, Taiwan, ROC, *ERSO/ITRI, Taiwan, ROC, **Chung Yuan Christian University, Taiwan, ROC

Session 10: Solid State Devices – SiGe HBTs

Tuesday, December 14, 9:00 a.m.
Continental Ballroom 1-3

Co-Chairs: Klaus Aufinger, Infineon
Greg Freeman, IBM

9:00 a.m.
Introduction

9:05 a.m.
10.1 Integration of High-Performance SiGe:C HBTs with Thin-Film SOI CMOS, H. Rücker, B. Heinemann, R. Barth, D. Bolze, J. Drews, O. Fursenko, T. Grabolla, U. Haak, W. Höppner, D. Knoll, M.Marschmeyer, N. Mohapatra, H. H. Richter, P. Schley, D. Schmidt, B. Tillack, G. Weidner, D. Wolansky, H.-E. Wulf, and Y. Yamamoto, IHP, Frankfurt, Germany

9:30 a.m.
10.2 Metal Emitter SiGe:C HBTs, J.J.T.M. Donkers, T. Vanhoucke, P. Agarwal, R.J.E. Hueting, P. Meunier-Beillard, M.N. Vijayaraghavan, P.H.C. Magnée, M.A. Verheijen*, R. de Kort* and J.W. Slotboom*, Philips Research Leuven, Leuven, Belgium, *Philips Research Laboratories, Eindhoven, The Netherlands

9:55 a.m.
10.3 SiGe HBT Technology with Gate Delay Below 3.3 ps, M. Khater, J. -S. Rieh, T. Adam, A. Chinthakindi, J. Johnson*, R. Krishnasamy*, M. Meghelli**, F. Pagette, D. Sanderson, C. Schnabel, K. T. Schonenberg, P. Smith, K. Stein, A. Stricker*, D. Ahlgren, and G. Freeman, IBM Microelectronics, Hopewell Junction, NY, *IBM Microelectronics, Essex Junction, VT, **IBM T.J. Watson Research Center, Yorktown Heights, NY

10:20 a.m.
10.4 A Low-Parasitic Collector Construction for High-Speed SiGe:C HBTs, B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, T. Grabolla, U. Haak, W. Höppner, D. Knoll, B. Kuck, R. Kurps, K. Köepke, S. Marschmeyer, H. H. Richter, H. Rüecker, P. Schley, D. Schmidt, W. Winkler, D. Wolansky, H.-E. Wulf, and Y. Yamamoto, IHP, Frankfurt, Germany

10:45 a.m.
10.5 3.3 ps SiGe Bipolar Technology, J. Böck, H. Schäefer, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, T. Boettner, R. Stengl, W. Perndl, T. F. Meister, Infineon Technologies, Munich, Germany

Session 11: Integrated Circuits and Manufacturing – SRAM and SOI-Based Memories

Tuesday, December 14, 9:00 a.m.
Continental Ballroom 4

Co-Chairs: Ted Houston, Texas Instruments
Jean-Pierre Colinge, University of California

9:00 a.m.
Introduction

9:05 a.m.
11.1 Aggressively Scaled (0.197 μm^2) 6T-SRAM Cell for the 32 nm Node and Beyond, D. M. Fried*, J. M. Hergenrother, A. W. Topol, L. Chang, L. Sekaric, J. W. Sleight*, S. McNab, J. Newbury, S. Steen, G. Gibson, Y. Zhang, N. Fuller, J. Bucchignano, C. Lavoie, C. Cabral, D. Canaperi, O. Dokumaci*, D. Frank, E. Duch, I. Babich, K. Wong*, T. Dalton, R. Nunes, D. Medeiros, R. Viswanathan, M. Ketchen, M. Ieong*, W. Haensch and K.W. Guarini, IBM SRDC, Yorktown Heights, NY, *IBM Microelectronics Division, Hopewell Junction, NY

9:30 a.m.
11.2 Highly Area Efficient and Cost Effective Double Stacked S3(Stacked Single-crystal Si) Peripheral CMOS SSTFT and SRAM Cell Technology for 512M Bit Density SRAM, S.-M. Jung, H. Lim, W. Cho, H. Cho, C. Yeo, Y. Kang, D. Bae, J. Na, K. Kwak, B. Choi, S. Kim, J. Jeong, Y. Chang, J. Jang, J. Kim and K. Kim, Samsung Electronics, Kyungki-do, Korea

9:55 a.m.
11.3 A 0.314μm^2 6T-SRAM Cell Build With Tall Triple-Gate Devices for 45nm Node Applications Using 0.75NA 193nm Lithography, A. Nackaerts, M. Ercken, S. Demunck, A. Lauwers, C. Baerts, H. Bender, W. Boulaert, N. Collaert, B. Degroote, C. Delvaux, J.F. de Marneffe, A. Dixit, K. De Meyer, E. Hendrickx, N. Heylen, P. Jaenen, D. Laidler, S. Locorotondo, M. Maenhoudt, I. Pollentier, K. Ronse, R. Rooyackers, J. Van Aels, G. Vandenberge, W. Vandervorst, T. Vandewyer, S. Vanhaelemeersch, M. Van Hove, J. Van Olman, S. Verhaegen, J. Versluijs, C. Vrancken, V. Wiaux, M. Jurczak and S. Biesemans, IMEC, and KU Leuven Heverlee, Belgium

10:20 a.m.
11.4 Fully Planar 0.562μm^2 T-RAM Cell in a 130nm SOI CMOS Logic Technology for High-Density High-Performance SRAMs, F. Nemati, H.-J. Cho, S. Robins, R. Gupta, M. Tarabbia, K. Yang, D. Hayes, and V. Gopalakrishnan, T-RAM, Inc., San Jose, CA

10:45 a.m.
11.5 A Capacitor-less DRAM Cell on 75nm Gate Length, 16nm Thin Fully Depleted SOI Device for High Density Embedded Memories, R. Ranica, A. Villaret, C. Fenouillet-Beranger*, P. Malinge, P. Mazoyer, P. Masson**, D. Delille, C. Charbuillet, P. Candelier, and T. Skotnicki, STMicroelectronics, Crolles Cedex, France, #Philips Semiconductors, Crolles, France, *CEA LETI, Grenoble, France, **L2MP UMR-CNRS, Marseille, France

11:10 a.m.
11.6 Fully-Depleted FBC (Floating Body Cell) with Enlarged Signal Window and Excellent Logic Process Compatibility, T. Shino, T. Higashi, N. Kusunoki, K. Fujita, T. Ohsawa, N. Aoki, H. Tanimoto, Y. Minami, T. Yamada, M. Morikado, H. Nakajima, K. Inoh, T. Hamamoto, and A. Nitayama, Toshiba Corporation, Kanagawa, Japan

Session 12: Process Technology – Metal Gate Engineering and Integration

Tuesday, December 14, 9:00 a.m.
Continental Ballroom 5

Co-Chairs: Kyoichi Suguro, Toshiba Corp.
Simon Deleonibus, CEA-LETI

9:00 a.m.
Introduction

9:05 a.m.
12.1 Challenges for the Integration of Metal Gate Electrodes (Invited), J.K. Schaeffer, C. Capasso, L.R.C. Fonseca, S. Samavedam, D.C. Gilmer, Y. Liang, S. Kalpat, B. Adetutu, H.-H. Tseng, Y. Shiho, A. Demkov, R. Hegde, W.J. Taylor, R. Gregory, J. Jiang, E. Luckowski, M.V. Raymond, K. Moore, D. Triyoso, D. Roan, B.E. White, Jr. and P.J. Tobin, Freescale Semiconductor, Inc., Austin, TX

9:30 a.m.
12.2 Poly-Gate REplacement Through Contact Hole (PRETCH): A New Method for High-K/Metal Gate and Multi-Oxide Implementation on Chip, S. Harrison, A. Cros*, P. Coronel*, F. Leverd*, A. Beverina*, R. Cerutti*, R. Wacquez*, J. Bustos*, D. Delille**, B. Tavel**, D. Barge**, J. Bienacel*, MP. Samson*, F. Martin***, S. Maitrejean***, D.Munteanu, and T. Skotnicki*, L2MP, Marseille, France, *STMicroelectronics, Crolles, France, **Philips Semiconductors, Crolles, France, ***CEA-LETI, Grenoble, France

9:55 a.m.
12.3 Evaluation of Fermi Level Pinning in Low, Midgap and High Work Function Metal Gate Electrodes on ALD and MOCVD HfO_2 Under High Temperature Exposure, R. Jha, J. Lee, B. Chen, H. Lazar, J. Gurganus, N. Biswas, P. Majhi*, G.A. Brown* and V. Misra, North Carolina State University, Raleigh, NC, *International Sematech, Austin, TX

10:20 a.m.
12.4 Substituted Aluminum Metal Gate on High-K Dielectric for Low Work-Function and Fermi-Level Pinning Free, C.S. Park, B.J. Cho, L.J. Tang*, D.-L.Wong**, The National University of Singapore, Singapore, *Institute of Microelectronics, Singapore, **The University of Texas, Austin, TX

10:45 a.m.
12.5 A Novel Methodology on Tuning Work Function of Metal Gate Using Stacking Bi-Metal Layers, I. S. Jeon, J. Lee*, P. Zhao, P. Sivasubramani, T. Oh*, H. J. Kim**, M. J. Kim, B. E. Gnade, J. Kim, R. M. Wallace, University of Texas, Dallas, TX, *Kookmin University, Seoul, Korea, **Seoul National University, Seoul, Korea

11:10 a.m.
12.6 Germanium p- & n-MOSFETs Fabricated with Novel Surface Passivation (plasma PH_3 and thin AlN) and HfO_2/TaN Gate Stack, S. J. Whang, S. J. Lee, F. Gao, N. Wu, C. X. Zhu, L.J. Tang*, L.S. Pan** and D.L. Kwong***, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore, **Institute of Materials Research and Engineering, Singapore, ***University of Texas, Austin, TX

Session 13: Process Technology – Advanced Interconnect Technologies

Tuesday, December 14, 9:00 a.m.
Continental Ballroom 6

Co-Chairs: Dirk Gravesteijn, Philips
Simon Jang, TSMC

9:00 a.m.
Introduction

9:05 a.m.
13.1 Challenges in Cu/Low K Integration (Invited), M.-S. Liang, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC

9:30 a.m.
13.2 Demonstration of an Extendable and Industrial 300mm BEOL Integration for 65nm Technology Node, O. Hinsinger, R. Fox*, E. Sabouret, C. Goldberg* , C. Verove, W. Besling**, P. Christie**, P. Brun***, E. Josse, C. Monget, O. Belmont, J. Van Hassel**,B.G. Sharma*, J.-P. Jacquemin**, P. Vannier, A. Humbert**, D. Bunel**, E. Mastromatteo**, D. Reber*, A. Farcy, J. Mueller*, C. Cregut and T. Berger, STMicroelectronics, Crolles, France, *Freescale Semiconductor, Crolles, France, **Philips Semiconductor, Crolles, France, ***CEA, Crolles, France

9:55 a.m.
13.3 Successful Dual Damascene Integration of Extreme Low k Materials (k < 2.0) Using a Novel Gap Fill Based Integration Scheme, S. Nitta, S. Purushothaman, S. Smith, M. Krishnan, D. Canaperi, T. Dalton, W. Volksen*, R. D. Miller*, B. Herbst, C.-K. Hu, E. Liniger, J. Lloyd, M. Lane, D. L. Rath and M. Colburn, IBM, Yorktown Heights, NY, *IBM Almaden Research Center, San Jose, CA

10:20 a.m.
13.4 Integration of ALD TaN Barriers in Porous Low-k Interconnect for the 45nm Node and Beyond; Solution to Relax Electron Scattering Effect, W.F.A. Besling, V. Arnal*, J.F. Guillaumond*, C. Guedj**, M. Broekaart, L.L. Chapelon*, A. Farcy*, L. Arnaud**, and J.Torres*, Philips Semiconductors Crolles R&D, Crolles France, *STMicroelectronics, Crolles, France, **CEA LETI, Grenoble, France

10:45 a.m.
13.5 Challenge of Low-k Materials for 130, 90, 65 nm Node Interconnect Technology and Beyond (Invited), H. Miyajima, K. Watanabe, K. Fujita, N. Yamada, H. Masuda, S. Nakao, S. Ito, K. Tabuchi*, T. Shimayama*, K. Akiyama,T. Hachiya, K. Higashi, N. Nakamura, A. Kajita, N. Matsunaga, M. Inohara, K. Honda, Y. Enomoto* and R. Kanamura*, Toshiba Corporation, Kanagawa, Japan, *Sony Corporation, Atsugi, Japan

11:10 a.m.
13.6 A Novel Solution for Porous Low-k Dual Damascene Post Etch Stripping/Clean with Supercritical CO_2 Technology for 65nm and Beyond Applications, C. Y. Wang, W. J. Wu, C. M. Yang, W. H. Tseng, H. C. Chen, T. I. Bao, H. Lo, J. Wang, C. H. Yu, and M.S. Liang, TSMC, Taiwan, ROC

11:35 a.m.
13.7 Direct Plating of Cu on ALD TaN for 45nm-Node Cu BEOL Metallization, C. H. Shih, H. W. Su, C. J. Lin, T. Ko, C.H. Chen, J.J. Huang, C. H. Peng, C. H. Hsieh, M.H. Tsai, W. S. Shue, C.H. Yu and M. S. Liang, TSMC, Taiwan, ROC

Session 14: Quantum Electronics and Compound Semiconductors – The New Spectrum of Optoelectronic Devices

Tuesday, December 14, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairs: Asif Khan, University of South Carolina
Rajeev Ram, Massachusetts Institute of Technology

9:00 a.m.
Introduction

9:05 a.m.
14.1 {113} Defect-Engineered Silicon Light-Emitting Diodes, G. Z. Pan, R. P. Ostroumov, Y. G. Lian, K. N. Tu and K. L. Wang, University of California, Los Angeles, CA

9:30 a.m.
14.2 255 nm Interconnected Micro-Pixel Deep Ultraviolet Light Emitting Diodes, M.A. Khan, S. Wu, W.-H. Sun, A. Chitnis, V. Adivarahan, M. Shatalov, and J. Yang, University of South Carolina, Columbia, SC

9:55 a.m.
14.3 High-Responsivity, High-Speed, and High-Saturation-Power Performances of Evanescently Coupled Photodiodes with Partially p-Doped Photo-Absorption Layer, J.-W. Shi, Y.-S. Wu, F.-H. Huang, and Y.-J. Chan, National Central University, Taiwan, ROC

10:20 a.m.
14.4 Novel Infrared Phototransistors for Atmospheric CO_2 Profiling at 2 μm Wavelength, T.F. Refaat, M.N. Abedin*, O.V. Sulima**, U.N. Singh* and S. Ismail*, Science and Technology Corporation, Hampton, VA, *NASA Langley Research Center, Hampton, VA, **University of Delaware, Newark, DE

10:45 a.m.
14.5 Photonic Crystals: Fundamentals and Applications (Invited), C. Lopez, Instituto de Ciencia de Materiales, Madrid, Spain

Session 15: Displays, Sensors and MEMS – Organic TFTs and Devices on Flexible Substrates

Tuesday, December 14, 9:00 a.m.
Imperial Ballroom A

Co-Chairs: Kyuha Chung, Samsung Electronics
Akintunde Akinwande, Massachusetts Institute of Technology

9:00 a.m
Introduction

9:05 a.m.
15.1 A Large-Area, Flexible, and Lightweight Sheet Image Scanner Integrated with Organic Field-Effect Transistors and Organic Photodiodes, T. Someya, S. Iba, Y. Kato, T. Sekitani, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai, University of Tokyo, Tokyo, Japan

9:30 a.m.
15.2 Low-Voltage Flexible Organic Circuits with Molecular Gate Dielectrics, H. Klauk, M. Halik, F. Eder, G. Schmid, C. Dehm, U. Zschieschang*, D. Rohde**, R. Brederlow***, S. Briole***, S. Maisch+, and F. Effenberger+, Infineon Technologies, Erlangen, Germany, *Freiberg University of Mining and Technology, Germany, **Technical University Dresden, Germany, ***Infineon Technologies, Munich, Germany, +University Stuttgart, Germany

9:55 a.m.
15.3 TES Thienyl Pentacene Solution-Processed OTFTs with 1 cm^2/V-s Mobility, C.-C. Kuo, M.M. Payne*, J.E. Anthony*, and T.N. Jackson, Pennsylvania State University, University Park, PA, *University of Kentucky, Lexington, KY

10:20 a.m.
15.4 An Organic Semiconductor Based Process for Photodetecting Applications, I. Kymissis, C.G. Sodini, A. I. Akinwande and V. Bulovic, MIT, Cambridge, MA

10:45 a.m.
15.5 Process Control of Threshold Voltage in Organic FETs, A. Wang, I. Kymissis, V. Bulovic, and A.I. Akinwande, MIT, Cambridge, MA

11:10 a.m.
15.6 OLED Pixel Array on a Dome, R. Bhattacharya, S. Wagner, Y.-J. Tung*, J. Esler* and M. Hack*, Princeton University, Princeton, NJ, *University Display Corporation, Ewing, NJ

Session 16: Modeling and Simulation – Reliability

Tuesday, December 14, 9:00 a.m.
Imperial Ballroom B

Co-Chairs: Yoshinari Kamakura, Osaka University
Herve Jaouen, STMicroelectronics

9:00 a.m.
Introduction

9:05 a.m.
16.1 Inversion Mobility and Gate Leakage in High-k/Metal Gate MOSFETs, R. Kotlyar, M.D. Giles, P. Matagne, B. Obradovic, L. Shifren, M. Stettler, and X. Wang, Intel Corporation, Hillsboro, OR

9:30 a.m.
16.2 Analysis on Data Retention Time of Nano-Scale DRAM and its Prediction by Indirectly Probing the Tail Cell Leakage Current, W.-S. Lee, S.-H. Lee, C.-S. Lee, K.-H. Lee, H.-J. Kim, J.-Y. Kim, W. Yang, Y.-K. Park, and J.-T. Kong, Samsung, Gyeonggi-Do, Korea

9:55 a.m.
16.3 Modeling of Retention Time Distribution of DRAM Cell Using a Monte-Carlo Method, S. Jin, J.-H. Yi, J.H. Choi*, D.G. Kang*, Y.J. Park, and H.S. Min, Seoul National University, Seoul, Korea, *Hynix Semiconductor, Inc., Kyoungki-do, Korea

10:20 a.m.
16.4 A Comprehensive Trapped Charge Profiling Technique for SONOS Flash EEPROMs, P.R. Nair, P.B. Kumar, R. Sharma, S. Mahapatra and S. Kamohara*, Indian Institute of Technology, Bombay, India, *Renesas Technologies, Tokyo, Japan

10:45 a.m.
16.5 Experimental Extraction of Impact-Ionization Coefficient at Large Operating Temperatures, S. Reggiani, E. Gnani, M. Rudan, G. Baccarani, C. Corvasce*, D. Barlini*, M. Ciappa*, W. Fichtner*, M. Denison**, N. Jensen**, G. Groos***, and M. Stecher**, University of Bologna, Bologna, Italy, *ETH Zentrum, Zurich, Switzerland, **Infineon Technologies AG, Munich, Germany, ***University of the Federal Armed Forces Munich, Neubiberg, Germany

11:10 a.m.
16.6 Electro-Thermal Comparison and Performance Optimization of Thin-Body SOI and GOI MOSFETs, E. Pop, C.O. Chui, S. Sinha, R. Dutton, and K. Goodson, Stanford University, Stanford, CA

11:35 a.m.
16.7 Power Optimization of Future Transistors and a Resulting Global Comparison Standard, P. Kapur, R. S. Shenoy, A.K. Chao, Y. Nishi and K.C. Saraswat, Stanford University, Stanford, CA

TUESDAY

Luncheon Session

Tuesday, December 14, 12:20 p.m.
Grand Ballroom B

Luncheon Presentation: "Our Energy Challenge"
Richard Smalley, Rice University

Somehow within the next few decades we must find a new energy source that can provide at least 10 terawatts (TW) of clean power on sustainable basis, and do this cheaply. To do this with nuclear fission would require 10,000 breeder reactors. In order for the billions of people in the developing world to achieve and sustain a modern lifestyle, we really need 50 TW. Assuming we don't get it all from "clean coal" or nuclear fission, where is that 10-50 TW of new power going to come from? How will we transport this energy, store it, and transform it? Who will make the necessary scientific and engineering breakthroughs? Can it be cheap enough to bring 10 billion people to a reasonable standard of living? Can it be done soon enough to avoid the hard economic times, terrorism, war and human suffering that will otherwise occur as we fight over the dwindling oil and gas reserves on the planet? Energy may very well be the single most critical challenge facing humanity in this century.

Professor Smalley received his B.S. degree in 1965 from the University of Michigan. He received his Ph.D. from Princeton in 1973, with an intervening four-year period in industry as a research chemist with Shell.

During a postdoctoral period with Lennard Wharton and Donald Levy at the University of Chicago, he pioneered what has become one of the most powerful techniques in chemical physics; supersonic beam laser spectroscopy.

After coming to Rice University in 1976 Dr. Smalley was named to the Gene and Norman Hackerman Chair in Chemistry in 1982. He was a founder of the Rice Quantum Institute in 1979, and served as the Chairman from 1986 to 1996. In 1990 he became a Professor in the Department of Physics and was appointed University Professor in 2002. He was the founding director of the Center for Nanoscale Science and Technology at Rice from 1996 to 2002, and is now Director of the new Carbon Nanotechnology Laboratory at Rice.

Dr. Smalley is the recipient of numerous awards—1990 National Academy of Sciences; 1991 American Academy of Arts and Sciences; 1991 Irving Langmuir Prize in Chemical Physics; 1992 International Prize for New Materials; 1992 E.O. Lawrence Award of the U.S. Department of Energy; 1992 Robert A. Welch Award in Chemistry; 1993 William H. Nichols Medal of the American Chemical Society; 1993 John Scott Award of the City of Philadelphia; 1994 Europhysics Prize; 1994 Harrison Howe Award; 1995 Madison Marshall Award; 1996 Franklin Medal; 1996 Nobel Prize in Chemistry; 1997 Distinguished Public Service Medal from the US Department of the Navy; 2002 Glenn T. Seaborg Medal; 2003 Lifetime Achievement Award of Small Times Magazine. He received two honorary degrees in 2004—Honorary Doctorate from the University of Richmond and Doctor Scientiarum Honoris Causa from Technion Israel Institute of Technology.

Dr. Smalley is widely known for the discovery and characterization of C60 Buckminsterfullerene a/k/a "buckyball"), a soccerball-shaped molecule, which together with other fullerenes such as C70, now constitutes the third elemental form of carbon (after graphite and diamond). His current research is on buckytubes, elongated fullerenes that are essentially a new high tech polymer, following on from nylon, polypropylene, and Kevlar. But unlike any of these previous wonder polymers, these new buckytubes conduct electricity. They are likely to find applications in nearly every technology where electrons flow. In February of 2000, this research led to the start up of a new company, Carbon Nanotechnologies, Inc. which is now developing large scale production and applications of these miraculous buckytubes.

Awards Presentation

2004 IEEE Cledo Brunetti Award

2004 IEEE Andrew S. Grove Award

2004 IEEE Daniel E. Noble Award

Session 17: CMOS Devices – Aggressively Scaled Planar MOSFETs

Tuesday, December 14, 2:15 p.m.
Grand Ballroom A

Co-Chairs: Satoshi Inaba, Toshiba
Charles Dachs, Philips Research

2:15 p.m.
Introduction

2:20 p.m.
17.1 Circuit Techniques for Subthreshold Leakage Avoidance, Control, and Tolerance (Invited), S. Borkar, Intel Corporation, Hillsboro, OR

2:45 p.m.
17.2 A Conventional 45nm CMOS Node Low-Cost Platform for General Purpose and Low Power Applications, F. Boeuf, F. Arnaud, B. Tavel*, B. Duriez*, M. Bidaud*, P. Gouraud, C. Chaton**, P. Morin, J. Todeschini*, M. Jurdit**, L. Pain**, V. De-Jonghe, M.T. Basso, D. Sotta*, F. Wacquant, J. Rosa, R. El-Farhane*, S. Jullian, N. Bicais-Lepinay, H. Bernard, J. Bustos, S. Manakli, M. Gaillardin, J. Grant*** and T. Skotnicki, STMicroelectronics, Crolles, France, *Philips Semiconductor, Crolles France, **CEA-LETI, Grenoble, France, ***Freescale Semiconductor, Crolles, France

3:10 p.m.
17.3 Transport Properties of Sub-10-nm Planar-Bulk-CMOS Devices, H. Wakabayashi, T. Ezaki, M. Hane, T. Ikezawa, T. Sakamoto, H. Kawaura, S. Yamagami, N. Ikarashi, K. Takeuchi, T. Yamamoto, and T. Mogami, NEC Corporation, Kanagawa, Japan

3:35 p.m.
17.4 Direct Evaluation of Gate Line Edge Roughness Impact on Extension Profiles in Sub-50nm N-MOSFETs, H. Fukutome, Y. Momiyama, T. Kubo, Y. Tagawa, T. Aoyama and H. Arimoto, Fujitsu, Tokyo, Japan

4:00 p.m.
17.5 Double SiGe:C Diffusion Barrier Channel 40nm CMOS With Improved Short Channel Performances, F. Ducroquet, T. Ernst, J.-M. Hartmann, O. Weber, F. Andrieu, P. Holliger, F. Laugier, P. Rivallin, G. Guégan, V. Carron, L. Brévard, C. Tabone, D. Bouchu, A. Toffoli, J. Cluzel and S. Deleonibus, CEA/DRT-LETI, Grenoble, France

4:25 p.m.
17p6 Record RF Performance of Standard 90 nm CMOS Technology, L.F. Tiemeijer, R.J. Havens, R. de Kort, A. Scholten, R. van Langevelde, D.B.M. Klaassen, G.T. Sasse*, Y. Bouttement**, C. Petot**, S. Bardy**, D.Gloria+, P. Scheer+, S. Boret+, B. Van Haaren+, C. Clement+, J-F. Larchanche+, I-S. Lim^, A. Zlotnicka^, and A. Duvallet#, Philips Research, Eindhoven, The Netherlands, **Philips Semiconductors, Caen, France, **University of Twente, The Netherlands, +STMicroelectronics, Crolles, France, ^Freescale Semiconductor, Inc., Tempe, AZ, #Freescale Semiconductor, Inc., Austin, TX

Session 18: Solid State Devices – Power, RF and Passives Technology

Tuesday, December 14, 2:15 p.m.
Continental Ballroom 1-3

Co-Chairs: Yutaka Hoshino, Renesas Technology
Bruce White, Freescale Semiconductor

2:15 p.m.
Introduction

2:20 p.m.
18.1 High-Voltage Extension (V_{br}≥800 V) for Smart-Power SOI-Technologies, T. Rotter and M. Stoisiek, University of Erlangen-Nuernberg, Erlangen, Germany

2:45 p.m.
18.2 Membrane High Voltage Devices "A Milestone Concept in Power ICs", F. Udrea, T. Trajkovic, and G. A. J. Amaratunga, Cambridge Semiconductor, Cambridge, United Kingdom

3:10 p.m.
18.3 RF Power Potential of 90 nm CMOS: Device Options, Performance, and Reliability, J. Scholvin, D.R. Greenberg* and J. A. del Alamo, MIT, Cambridge, MA, *IBM Research, Hopewell Junction, NY

3:35 p.m.
18.4 Lateral IMPATT Diodes in Standard CMOS Technology, T. Al-Attar, M.D. Mulligan and T.H. Lee, Stanford University, Stanford, CA

4:00 p.m.
18.5 New Low-Cost Thermally Stable Process to Reduce Silicon Substrate Losses: A Way to Extreme Frequencies for High Volume Si Technologies, C. Detcheverry, W.D. van Noort, R.J. Havens*, Philips Research Leuven, Leuven, Belgium, *Philips Research Laboratories, Eindhoven, The Netherlands

4:25 p.m.
18.6 Novel Differential Inductor Design for High Self-Resonance Frequency, P. Findley, G.A. Rezvani, J. Tao, RF Micro Devices, San Jose, CA

TUESDAY

Session 19: CMOS and Interconnect Relibility – Process Induced and Electrical Degradation in Flash Memories and CMOS Circuits

Tuesday, December 14, 2:15 p.m.
Continental Ballroom 4

Co-Chairs: David Esseni, University of Udine
William Tonti, IBM

2:15 p.m.
Introduction

2:20 p.m.
19.1 Ionizing Radiation Effects on MOSFET Thin and Ultra-Thin Gate Oxides (Invited), A. Paccagnella, A. Cester and G. Cellere, DEI, Universita di Padova, Padova, Italy

2:45 p.m.
19.2 Low Leakage Reliability Characterization Methodology for Advanced CMOS with Gate Oxide in the 1nm Range, S.S. Chung, S.J. Feng, Y.S. Hsieh*, A. Liu*, W.M. Lin*, D.F. Chen*, J.H. Ho*, K.T. Huang*, C.K. Yang*, O. Cheng*, Y.C. Sheng*, D.Y. Wu*, W.T. Shiau*, S.C. Chien*, K. Liao*, and S.W. Sun*, National Chiao Tung University, Taiwan, ROC, *United Microelectronics Corporation, Taiwan, ROC

3:10 p.m.
19.3 Implant Damage and Gate-Oxide-Edge Effects on Product Reliability, Y.-H. Lee, R. Nachman, S. Hu, N. Mielke, J. Liu, Intel Corporation, Santa Clara, CA

3:35 p.m.
19.4 Charge Trapping Effects in HfSiON Dielectrics on the Ring Oscillator Circuit and the Single Stage Inverter Operation, C.Y. Kang, R. Choi*, J.H. Sim*, C. Young*, B.H. Lee*, G. Bersuker*, and J.C. Lee, University of Texas at Austin, Austin, TX, *International SEMATECH, Austin, TX

4:00 p.m.
19.5 What We Have Learned About Flash Memory Reliability in the Last Ten Years (Invited), P. Cappelletti, R. Bez, A. Modelli, A. Visconti, STMicroelectronics, Agrate Brianza, Italy

4:25 p.m.
19.6 High-Energy Oxide Traps and Anomalous Soft-Programming in Flash Memories, D. Ielmini, A. S. Spinelli, A. L. Lacaita, M. Robustelli, L. Chiavarone* and A. Visconti*, Politechnico di Milano, Milan, Italy, *STMicroelectronics, Agrate Brianza, Italy

Session 20: Process Technology – High-k I: Hafnium Silicate Dielectrics

Tuesday, December 14, 2:15 p.m.
Continental Ballroom 5

Co-Chairs: Victor Wang, Freescale Semiconductor
Hirohito Watanabe, NEC

2:15 p.m.
Introduction

2:20 p.m.
20.1 Careful Examination on the Asymmetric Vfb Shift Problem for Poly-Si/HfSiON Gate Stack and its Solution by the Hf Concentration Control in the Dielectric Near the Poly-Si Interface With Small EOT Expense, M. Koyama, Y. Kamimuta, T. Ino, A. Kaneko, S. Inumiya, K. Eguchi, M. Takayanagi and A. Nishiyama, Toshiba Corporation, Kanagawa, Japan

2:45 p.m.
20.2 The Effects of TaN Thickness and Strained Substrate on the Performance and PBTI Characteristics of Poly-Si/TaN/HfSiON MOSFETs, H. -J. Cho, H. L. Lee, S. G. Park, H. B. Park, T. S. Jeon, B. J. Jin, S. B. Kang, S.G. Lee, Y. P. Kim, I. S. Jung, J. W. Lee, I. D. Bae, J. H. Choi, Y. S. Jeong, Y. G. Shin, U. I. Chung, and J. T. Moon, Samsung Electronics, Gyeonngi-Do, Korea

3:10 p.m.
20.3 Impact of Hf Concentration on Performance and Reliability for HfSiON-CMOSFET, T. Watanabe, M. Takayanagi, K. Kojima, K. Sekine, H. Yamasaki, K. Eguchi, K. Ishimaru, and H. Ishiuchi, Toshiba Corporation, Kanagawa, Japan

3:35 p.m.
20.4 Characteristics of ALD $HfSiO_x$ Using New Si Precursors for Gate Dielectric Applications, Y.-K. Kim, H.-J. Lim, H.-S. Jung, J.-H. Lee, J.E. Park, S.K. Han, J.H. Lee, J.P. Kim, S.-J. Doh, N.I. Lee, H.K. Kang, Y. Chung, H.Y. Kim*, N.K. Lee*, S. Ramanathan*, and T. Seidel*, J. Zimmerman**, V. Balema**, M. Boleslawski** and G. Irvine**, Samsung Electronics, Kyunggi-Do, Korea, *GENUS, Inc., Sunnyvale, CA, **SIGMA-ALDRICH, Sheboygan Falls, WI

4:00 p.m.
20.5 Implementation of HfSiON Gate Dielectric for Sub-60nm DRAM Dual Gate Oxide with Recess Channel Array Transistors (RCAI) and Tungsten Gate, S.G. Park, B.J. Jin, H.L. Lee, H.B. Park, T.S. Jeon, H.-J. Cho, S.Y. Kim, S.I. Jang S.B. Kang, Y.G. Shin, U-I. Chung and J.T. Moon, Samsung Electronics, Kyungki-Do, Korea

Session 21: Emerging Technologies – Nano-Computing Devices

Tuesday, December 14, 2:15 p.m.
Continental Ballroom 6

Chair: Clark Nguyen, DARPA

2:15 p.m.
Introduction

2:20 p.m.
21.1 Single-Crystal Metallic Nanowires and Metal/Semiconductor Nanowire Heterostructures, C. Lieber, Harvard University, Cambridge, MA

2:45 p.m.
21.2 Carbon Nanotube Electronics and Optoelectronics, P. Avouris, A. Afzali, J. Appenzeller, J. Chen, M. Freitag, C. Klinke, Y.-M. Lin and J.C. Tsang, IBM TJ Watson Research Center, Yorktown Heights, NY

3:10 p.m.
21.3 Self-Assembled Monolayer Molecular Devices, W. Wang, T. Lee, I. Kretzschmar, D. Routenberg and M. Reed, Yale University, New Haven, CT

3:35 p.m.
21.4 Quantum Dots as Spin Qubits, L. Kouwenhoven, Delft University of Technology, Delft, The Netherlands

4:00 p.m.
21.5 Spintronics: Semiconductors, Molecules and Quantum Information, D. Awschalom, University of California, Santa Barbara, CA

4:25 p.m.
21.6 Nanomechanical Systems, M. Roukes, Caltech, Pasadena, CA

Session 22: Quantum Electronics and Compound Semiconductors – Superscaled, Ultrafast HBTs

Tuesday, December 14, 2:15 p.m.
Continental Ballroom 7-9

Co-Chairs: David Chow, HRL
Mohammed Zaknoune, CNRS IEMN

2:15 p.m.
Introduction

2:20 p.m.
22.1 Polymer Based Technologies for Microwave and Millimeterwave Applications (Invited), K. Grenier, D. Dubuc, L. Mazenq, J-P. Busquère*, B. Ducarouge, F. Bouchriha, A. Rennane, V. Lubecke**, P. Pons, P. Ancey*, and R. Plana, LAAS-CNRS, Toulouse, France, *STMicroelectronics, Crolles, France, **University of Hawaii at Manoa, Honolulu, HI

2:45 p.m.
22.2 0.25 µm Emitter InP HBTs with f_T = 550 GHz and BVceo>2V, W. Hafez and M. Feng, University of Illinois at Urbana-Champaign, Urbana, IL

3:10 p.m.
22.3 First Demonstration of Sub-0.25µm-Width Emitter InP-DHBTs with 370GHz f_T and 430GHz f_{max}, T. Hussain, Y. Royter, M. Montes, D. Hitko, M. Madhav, I. Milosavljevic, R. Rajavel, M. Sokolich, HRL Laboratories LLC, Malibu, CA

3:35 p.m.
22.4 Ultra High-Speed 0.25µm Emitter InP-InGaAs SHBTs with f_{max} of 687 GHz, D. Yu, K. Choi, K. Lee, B. Kim, H. Zhu*, K. Vargason*, J.M. Kuo*, and Y.C. Kao*, Pohang University of Science and Technology, Gyeongbuk, Korea, *Intelligent Epitaxy Technology Inc., Richardson, TX

4:00 p.m.
22.5 Flip-Chip Mounted 26 V GaInP/GaAs Power HBTs, P. Kurpas, A. Maaßdorf, M. Neuner, W. Doser*, P. Heymann, B. Janke, F. Schnieder, T. Bergunde, T. Graßhoff, H. Blanck*, Ph. Auxemery**, W. Heinrich, and J. Wuerfl, Ferdinand-Braun-Institut fuer Hoechstfrequenztechnik (FBH), Berlin, Germany, *United Monolithic Semiconductors GmbH, Ulm, Germany, **United Monolithic Semiconductors SAS, Orsay, France

Session 23: Integrated Circuits and Manufacturing – Non-Volatile Memory Technology; MRAM, RRAM and FeRAM

Tuesday, December 14, 2:15 p.m.
Imperial Room A

Co-Chairs: Iwao Kunishima, Toshiba
Atsushi Hori, Matsushita

2:15 p.m.
Introduction

2:20 p.m.
23.1 Status and Outlook of Emerging Nonvolatile Memory Technologies, G. Müeller, T. Happ, M. Kund, G.Y. Lee, N. Nagel, and R. Sezi, Infineon Technologies, Munich, Germany

2:45 p.m.
23.2 Design and Process Integration for High-Density, High-Speed, and Low-Power $6F^2$ Cross Point Type MRAM Cell, Y. Asao, T. Kajiyama, Y. Fukuzumi, M. Amano, H. Aikawa, T. Ueda, T. Kishi, S. Ikegawa, K. Tsuchida, Y. Iwata, K. Shimura*, Y. Kato*, S. Miura*, N. Ishiwata*, H. Hada*, S. Tahara*, and H. Yoda, Toshiba Corporation, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

3:10 p.m.
23.3 High Density and Low Power Design of MRAM, C. C. Hung, M. J. Kao, Y. H. Chen, Y. H. Wang, H. H. Hsu, C. M. Chen, Y. J. Lee, W. C. Chen, W. C. Lin*, K. H. Shen, J. H. Wei, L. C. Wang, K. L. Chen, S. Chao**, D. Tang*, M.-J. Tsai, ERSO ITRI, Hsinchu, Taiwan, ROC, *TSMC, Hsinchu, Taiwan, ROC, **National Tsing Hua University, Hsinchu, Taiwan, ROC

3:35 p.m.
23.4 A 0.13µm MRAM with 0.26x0.44μm^2 MTJ Optimized on Universal MR-RA Relation for 1.2V High Speed Operation Beyond 143MHz, S. Ueno, T. Eimori, T. Kuroiwa*, H. Furuta, J. Tsuchimoto, S. Maejima, S. Iida, H. Ohshita, S. Hasegawa, S. Hirano, T. Yamaguchi, H. Kurisu, A. Yutani, N. Hashikawa, H. Maeda, Y. Ogawa, K. Kawabata, Y. Okumura, T. Tsuji, J. Ohtani, T. Tanizaki, Y. Yamaguchi, T. Ohishi, H. Hidaka, T. Takenaga*, S. Beysen*, H. Kobayashi*, T. Oomori*, T. Koga and Y. Ohji, Renesas Technology Corporation, Hyogo, Japan, *Mitsubishi Electric Corporation, Hyogo, Japan

4:00 p.m.
23.5 Improvement of Robustness Against Write Disturbance by Novel Cell Design for High Density MRAM, T. Kai, M. Yoshikawa, M. Nakayama, Y. Fukuzumi, T. Nagase, E. Kitagawa, T. Ueda, T. Kishi, S. Ikegawa, Y. Asao, K. Tsuchida, H. Yoda, N. Ishiwata*, H. Hada* and S. Tahara*, Toshiba Corporation, Kanagawa, Japan, *NEC Corporation, Kawasaki, Japan

4:25 p.m.
23.6 Highly Scalable Non-volatile Resistive Memory Using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses, I. G. Baek, M. S. Lee, S. O. Park, H. S. Kim, U.-I. Chung, S. Seo, M. J. Lee, D. H. Seo, D.-S. Suh, J. C. Park, I. K. Yoo, and J. T. Moon, Samsung Electronics Co., Ltd., Kyeonggi-Do, Korea

4:50 p.m.
23.7 Fully Logic Compatible (1.6V Vcc, 2 Additional FRAM Masks) Highly Reliable Sub 10F2 Embedded FRAM with Advanced Direct Via Technology and Robust 100nm Thick MOCVDPZT Technology, J.H. Park, H.J. Joo, S. K. Kang, Y. M. Kang, H.S. Rhie, B.J. Koo, S. Y. Lee, B.J. Bae, J.E. Lim, H. S. Jeong and K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

Session 24: Modeling and Simulation – Transport in Nanoscale Silicon-Based FETs-II

Tuesday, December 14, 2:15 p.m.
Imperial Ballroom B

Co-Chairs: Leonard Register, University of Texas
Tatsiua Ezaki, NEC

2:15 p.m.
Introduction

2:20 p.m.
24.1 Scaling Study of Si and Strained Si n-MOSFETs with Different High-k Gate Stacks, L. Yang, J. R. Watling, F. Adam-Lema, A. Asenov and J. R. Barker, University of Glasgow, Glasgow, United Kingdom

2:45 p.m.
24.2 Exploring the Limit of Strain-Induced Performance Gain in p- and n-SSDOI-MOSFETs (Invited), F. M. Bufler, Institut fur Integrierte Systeme, Zurich, Switzerland

3:10 p.m.
24.3 A Monte-Carlo Study of the Role of Scattering in Deca-nanometer MOSFETs, P. Palestri, D. Esseni, S. Eminente*, C. Fiegna +, E. Sangiorgi* and L. Selmi, University of Udine, Italy, *ARCES Center, Bologna, Italy, +University of Ferrara, Italy

3:35 p.m.
24.4 Enhanced Ballisticity in nano-MOSFETs along the ITRS Roadmap: A Monte Carlo Study, S. Eminente*, D. Esseni**, P. Palestri**, C. Fiegna^, L. Selmi^, and E. Sangiorgi+, *ARCES, Bologna, Italy, **University of Udine, Udine, Italy, ^University of Ferrara, Ferrara, Italy, +University of Bologna, Bologna, Italy

4:00 p.m.
24.5 Pragmatic Design of Nanoscale Multi-Gate CMOS, J. G. Fossum, L.-Q. Wang, J.-W. Yang, S.-H. Kim, and V. P. Trivedi, University of Florida, Gainesville, FL

4:25 p.m.
24.6 3D Quantum Modeling and Simulation of Multi-Gate Nanowire MOSFETs, M. Bescond, K. Néhari, J.L. Autran, N. Cavassilas, D. Munteanu, and M. Lannoo, L2MP-UMR CNRS, Marseille, France

TUESDAY

Session 25: 2004 IEDM Evening Panel Discussion

Tuesday, December 14, 8:00 p.m.
Continental Ballroom 4-5

What will End CMOS Scaling – Money or Physics?

CMOS scaling limits have been projected and then been defeated several times in the past 20 years. Many of the theoretical physics limits turn out to be materials or process limits, and have been addressed with ever more capital intensive manufacturing equipment and development efforts. However, the success of Moore's law is based on achieving, "smaller, cheaper, faster" all at the same time and it is clear that this is extremely challenging going forward.

Lithography costs per level are increasing as fast as dimensions are shrinking. Sub-wavelength patterning, while physically possible, is so costly that only the highest volume applications can take advantage of it. The cost reduction from 300mm wafers is offset by increased development costs for device and equipment manufacturers alike. Transistors leakage has increased by several orders of magnitude, adding extra cost for the design of complex power management circuitry. Interconnect delays should have been mitigated with low-k dielectrics and copper, but no "cure" has been found for the porosity challenge and resistivity is growing exponentially in small wires and contacts.

Is the cost-to-scale exceeding Moore's law potential benefit?

To debate this topic we have invited a distinguished panel from industry leaders who face the challenges of budgets and physics everyday. They come from around the world and represent a cross section of IDM, foundry and academic perspectives.

Moderator: Hans Stork, Texas Instruments

Panel Members:

Mark Bohr, Intel	Shang-Ti Chiang, TSMC
Gilbert DeClerck, IMEC	Marc Durcan, Micron
Masao Fukuma, NEC	Yuan Taur, UCSD

SESSION 26: 2004 IEDM Evening Panel Discussion

Tuesday, December 14 8:00 p.m.
Continental Ballroom 6-9

Nanoelectronics – Now or Never?

Traditional 'top-down' microelectronics has become nanoelectronics with device dimensions comparable to those being explored in the new field of 'bottom-up' nano- and molecular electronics. We use the terms, top-down and bottom-up, in a very general sense. Top-down refers to a way of thinking and building that begins at the macro (continuum) scale and pushes to the nanoscale. Bottom-up refers to a way of thinking and building that begins at the atomistic level and builds up to the nanoscale. The top-down approach has already delivered silicon MOSFETs with channel lengths of ~ 5nm, but scaling down device dimensions with commensurate increase in device and system performance is increasingly challenging. Bottom-up technology has demonstrated molecular switches, nanotube and nanowire FET's, NDR and single electron devices, and ultra-dense memory prototypes. Is bottom-up nanotechnology ready to address the industry's challenges, or is it still long-term research with essentially unpredictable outcomes? This panel will debate the

question of what the intersection of top-down and bottom-up electronics will mean to semiconductor technology of the future.

A panel of experts will provide their perspectives and engage the audience in a debate on the likely role of unconventional nano- and molecular electronics in future electronic systems. Specific questions to be addressed include:

— How far will the top-down approach take us and what will ultimately limit it?

— Has device scaling slowed or stopped?

— Is nanoelectronics here? Has silicon microelectronics become silicon nanoelectronics?

— How does/can bottom-up nanoelectronics address the challenges of CMOS scaling?

— What new information processing paradigms will bottom-up nanoelectronics enable?

— How can bottom-up nanoelectronics complement and extend Si CMOS?

— What can bottom-up nanoelectronics do that Si CMOS can't?

— What have been the major successes (scientific and technological) of three decades of research in nano- and molecular electronics? What are the Grand Challenges now?

— The nanotechnology field has often been accused of suffering from an excess of hype. Is this so? If so, why? Is there something real here?

— What is or should be the goal of research in bottom-up nanoelectronics?

Moderator: Mark Lundstrom, Purdue University

Panel Members:

Joerg Appenzeller, IBM	Charles Leiber, Harvard
Robert Chau, Intel	Jim Meindl, Georgia Tech
Andre DeHon, Caltech	Mark Reed, Yale
Jim Heath, Caltech	Jim Tour, Rice
Mark Horowitz, Stanford	Victor Zhirnov, SRC

Session 27: CMOS Devices – Novel SOI and Multi-Channel MOSFETs

Wednesday, December 15, 9:00 a.m.
Grand Ballroom A

Co-Chairs: Yuan Taur, University of California San Diego
Toshiro Hiramoto, University of Tokyo

9:00 a.m.
Introduction

9:05 a.m.
27.1 Sub 30 nm Multi-Bridge-Channel MOSFET(MBCFET) with Metal Gate Electrode for Ultra High Performance Application, E.-J. Yoon, S.-Y. Lee, S.-M. Kim, M.-S. Kim, S.H. Kim, L. Ming, S. Suk, K. Yeo, C. Oh, J.-D. Choe, D. Choi, D.-W. Kim, D. Park and K. Kim, Samsung Electronics, Kyoungi-Do, Korea

9:30 a.m.
27.2 Silicon on Thin BOX: A New Paradigm of The CMOSFET for Low-Power and High-Performance Application Featuring Wide-Range Back-Bias Control, R. Tsuchiya, M. Horiuchi, S. Kimura, M. Yamaoka, T. Kawahara, S. Maegawa*, T. Ipposhi*, Y. Ohji*, and H. Matsuoka, Hitachi, Ltd., Tokyo, Japan, *Renesas Technology Corporation, Hyogo, Japan

9:55 a.m.
27.3 SON (Silicon-On-Nothing) Technological CMOS Platform: Highly Performant Devices and SRAM Cells, S. Monfray, D. Chanemougame, S.Borel^, A.Talbot, F. Leverd, N. Planes, D. Delille*, D. Dutartre, R. Palla, Y. Morand, S. Descombes, M-P. Samson, N.Vulliet, T. Sparks, A.Vandooren**, T. Skotnicki, STMicroelectronics, Crolles, France^, *CEA LETI, Grenoble, France, **Freescale Semiconductor, Crolles, France

10:20 a.m.
27.4 A Novel Multi-channel Field Effect Transistor (McFET) on Bulk Si for High Performance Sub-80nm Application, S.M. Kim, E.J. Yoon, H.J. Jo, M. Li, C.W. Oh, S.Y. Lee, K.H. Yeo, M.S. Kim, S.H. Kim, D.U. Choe, J.D. Choe, S.D. Suk, D.-W. Kim, D. Park, and K. Kim, Samsung Electronics, Gyeonggi-Do, Korea

10:45 a.m.
27.5 Molybdenum-Gate HfO_2 CMOS FinFET Technology, D. Ha, H. Takeuchi, Y.-K. Choi*, T.-J. King, W.P. Bai**, D.-L. Kwong**, A. Agarwal***, and M. Ameen***, University of California, Berkeley, CA, *KAIST, Korea, **University of Texas, Austin, TX, ***Axcelis Technologies, Inc., Beverly, MA

11:10 a.m.
27.6 Large Scale Integration and Reliability Consideration of Triple Gate Transistors, J. A. Choi, K. Lee, Y. S. Jin, Y. J. Lee, S. Y. Lee, G. U. Lee, S. H. Lee, M. C. Sun, D. C. Kim, Y. M. Lee, S. G. Bae, J. H. Yang, S. Maeda, N. I. Lee, H. K. Kang and K. P. Suh, Samsung Electronics Co., Ltd., Kyoungi-Do, Korea

Session 28: Integrated Circuits and Manufacturing – Advanced Logic and Platform Technologies

Wednesday, December 15, 9:00 a.m.
Grand Ballroom B

Co-Chairs: Tahir Ghani, Intel
Mike Mendicino, Freescale

9:00 a.m.
Introduction

9:05 a.m.
28.1 SoC Integration in Deep Submicron CMOS (Invited), P. Rickert and B. Haroun, Texas Instruments, Richardson, TX

9:30 a.m.
28.2 A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell, P. Bai, C. Auth, S. Balakrishnan, M. Bost, R. Brain, V. Chikarmane, R. Heussner, M. Hussein, J. Hwang, D. Ingerly, R. James, J. Jeong, C. Kenyon, E. Lee, S-H. Lee, M. Liu, Z. Ma, T. Marieb, A. Murthy, R. Nagisetty, S. Natarajan, J. Neirynck, A. Ott, C. Parker, J. Sebastian, R. Shaheed, S. Sivakumar, J. Steigerwald, S. Tyagi, P.-H. Wang, C. Weber, B. Woolery, A. Yeoh, K. Zhang and M. Bohr, Intel Corporation, Hillsboro, OR

9:55 a.m.
28.3 High Performance and Low Power Transistors Integrated in 65nm Bulk CMOS Technology, Z. Luo, A. Steegen, M. Eller^, R. Mann, C. Baiocco, P. Nguyen, L. Kim+, M. Hoinkis, V. Ku, V. Klee^, F. Jamin, P. Wrschka, P. Shafer, W. Lin+, S. Fang, W. Tan+, D. Park, R. Mo, J. Lian^, D. Vietzke^, C. Coppock, A. Vayshenker, T. Hook, V. Chan, K. Kim^, A. Cowley, S. Kim^, E. Kaltalioglu^, B. Zhang+, S. Marokkey^, Y. Lin, K. Lee*, H. Zhu, M. Weybright, R. Rengarajan, J. Ku#, T. Schiml^, J. Sudijono+, I. Yang and C. Wann, IBM SRDC, Hopewell Junction, NY, *IBM Research, Yorktown Heights, NY, +Chartered Semiconductor Manufacturing, ^Infineon Technologies AG, #Samsung Electronics Co., Ltd.

10:20 a.m.
28.4 A 65 nm CMOS Technology for Mobile and Digital Signal Processing Applications, A. Chatterjee, J. Yoon, S. Zhao, S. Tang, K. Sadra, S. Crank, H. Mogul, R. Aggarwal, B. Chatterjee, S. Lytle, C.T. Lin, K.D. Lee, J. Kim, Q.Z. Hong, T. Kim, M. Quevedo-Lopez, G. Zhang, C. Meek, H. Mair, M. Mehrotra, L. Adam, D. Mosher, J.Y. Yang, D. Crenshaw, B. Williams, and J. Jacobs, M. Jain, J. Rosal, T. Houston, J. Wu, N.S. Nagaraj, D. Scott, S. Ashburn and A. Tsao, Texas Instruments, Dallas, TX

10:45 a.m.
28.5 A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain, A. Blosse, K. Ramkumar, P. Gopalan, C.T. Hsu, S. Narayanan, R. Gettle, R. Kapre, and S. Sharifzadeh, Cypress Semiconductor, San Jose, CA

WEDNESDAY

11:10 a.m.
28.6 Customer Oriented Technologies for Innovative Leading Edge Foundry Manufacturing (Invited), S. Yang, J. Chen, S. Chen, Z. Chen, A. Fan, B. He, Q. Jiang, E. Kuang, Y-F Lin, Y. Liu, J. Ning, C-H Pai, P.Sun, D.Tang, H-M Wu, G-Q Xing, J. Xu, X. Yu, J. Zhang, W. Zheng, C. Zhi, Semiconductor Manufacturing International Corporation, Shanghai, China

11:35 a.m.
28p7 On-Chip Transmission Line for Long Global Interconnects, H. Ito, J. Inoue, S. Gomi, H. Sugita, K. Okada, and K. Masu, Tokyo Institute of Technology, Kanagawa, Japan

Session 29: Solid State Devices – Next Generation Devices

Wednesday, December 15, 9:00 a.m.
Continental Ballroom 1-3

Co-Chairs: Hyungcheol Shin, Seoul National University
Steve S. Chung, National Chiao Tung University

9:00 a.m.
Introduction

9:05 a.m.
29.1 Carbon Nanotubes for Interconnect Applications (Invited), F. Kreupl, A.P. Graham, M. Liebau, G.S. Duesberg, R. Seidel, and E. Unger, Infineon Technologies AG, Munich, Germany

9:30 a.m.
29.2 Novel Carbon Nanotube FET Design with Tunable Polarity, Y.-M. Lin, J. Appenzeller, and P. Avouris, IBM T.J. Watson Research Center, Yorktown Heights, NY

9:55 a.m.
29.3 High Frequency S Parameters Characterization of Back-gate Carbon Nanotube Field-Effect Transistors, X. Huo, M. Zhang, P.C. H. Chan, Q. Liang, and Z. K. Tang, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong

10:20 a.m.
29.4 Self-Aligned Carbon Nanotube Transistors with Novel Chemical Doping, J. Chen, C. Klinke, A. Afzali, K. Chan, and P. Avouris, IBM T.J. Watson Research Center, Atlanta, GA

10:45 a.m.
29.5 Performance Comparison Between Carbon Nanotube and Copper Interconnects for GSI, A. Naeemi, R. Sarvari, and J.D. Meindl, Georgia Institute of Technology, Atlanta, CA

11:10 a.m.
29.6 Performance Analysis and Design Optimization of Near Ballistic Carbon Nanotube Field-Effect Transistors, J. Guo, A. Javey*, H. Dai*, and M. Lundstrom, Purdue University, West Lafayette, IN, *Stanford University, Stanford, CA

11:35 a.m.
29.7 Modulation of Drain Current by Redox-Active Molecules Incorporated in Si MOSFETs, S. Gowda, G. Mathur, Q. Li, S. Surthi, Q. Zhao, J. Lindsey, and V. Misra, North Carolina State University, Raleigh, NC

Session 30: CMOS and Interconnect Reliability Gate Dielectric Reliability – Breakdown and Device Degradation Mechanism

Wednesday, December 15, 9:00 a.m.
Continental Ballroom 4

Co-Chairs: Koji Eriguchi, Matsushita Electric
Paul Nicollian, Texas Instruments

9:00 a.m.
Introduction

9:05 a.m.
30.1 Implications of Progressive Wear-Out for Lifetime Extrapolation of Ultra-Thin (EOT~1nm) SiON Films, B. Kaczer, R. Degraeve, R. O'Connor*, Ph. Roussel, and G. Groeseneken, IMEC, Leuven, Belgium and *Dublin City Univ., Dublin Ireland

9:30 a.m.
30.2 New Insight into Gate Dielectric Breakdown Induced MOSFET Degradation by Novel Percolation Path Resistance Measurements, K.L. Pey, V.L. Lo, C.H. Tung*, W. Chandra, L.J. Tang, and R. Ranjan, Nanyang Technological University, Singapore, *Institute of Microelectronics, Singapore

9:55 a.m.
30.3 Model for Dielectric Breakdown Mechanism of $HfAlO_x/SiO_2$ Stacked Gate Dielectrics Dominated by the Generated Subordinate Carrier Injection, K. Okada, W. Mizubayashi*, N. Yasuda, H. Satake, H. Ota*, M. Kadoshima, K. Tominaga, A. Ogawa, K. Iwamoto, T. Horikawa*, T. Nabatame, and A. Toriumi, *ASET-MIRAI, Tsukuba, Japan, *MIRAI-ASRC, Tsukuba, Japan

10:20 a.m.
30.4 A Comprehensive Model for Breakdown Mechanism in HfO_2 High-k Gate Stacks, R. Ranjan, K.L. Pey, C.H. Tung*, L.J. Tang, G. Groeseneken**, L.K. Bera* and S. De Gendt**, NTU, Singapore, *IME, Singapore, **IMEC, Leuven, Belgium

10:45 a.m.
30.5 Charge Trapping in Aggressively Scaled Metal Gate/High-k Stacks, E.P. Gusev, V. Narayanan, S. Zafar, C. Cabral, Jr., E. Cartier, N. Bojarczuk, A. Callegari, R. Carruthers, M. Chudzik, C. D'Emic, E. Duch, P. Jamison, P. Kozlowski, D. LaTulipe, K. Maitra, R. McFeely, J. Newbury, V. Paruchuri, and M. Steen, IBM SRDC, Yorktown Heights, NY

11:10 a.m.
30.6 Negative U Traps in HfO_2 Gate Dielectrics and Frequency Dependence of Dynamic BTI in MOSFETs, C. Shen, M.F. Li, X.P. Wang, H.Y. Yu, Y.P. Feng, A.T.-L. Lim, Y.C. Yeo, D.S.H. Chan, and D.L. Kwong*, National University of Singapore, Singapore, #University of Texas, Austin, TX

11:35 a.m.
30.7 Characterization and Modeling of Hysteresis Phenomena in High K Dielectrics, C. Leroux, J. Mitard, G. Ghibaudo^, X. Garros, G. Reimbold, B. Guillaumot*, and F. Martin, CEA-LETI, Grenoble, France, *STMicroelectronics, Crolles, France, ^IMEP, Grenoble, France

Session 31: Modeling and Simulation – Compact Modeling

Wednesday, December 15, 9:00 a.m.
Continental Ballroom 5

Co-Chairs: Reinout Woltjer, Philips Research Laboratories Eindhoven
Jin Shyong Jan, UMC

9:00 a.m.
Introduction

9:05 a.m.
31.1 A New Dynamic Cell-Based Performance Metric for Novel CMOS Device Architectures, P. Christie, A. Heringa, G. Doornbos, A. Kumar, V. H. Nguyen, R. K. M. Ng, and M. Garg*, Philips Research, Leuven, Belgium, *Philips Research Laboratories, Eindhoven, The Netherlands

9:30 a.m.
31.2 Predictive Compact Modeling of NQS Effects and Thermal Noise in 90nm Mixed-Signal/RF CMOS Technology, W.-K. Shih, S. Mudanai, R. Rios, P. Packan, D. Becher, R. Basco, and C. Hung, Intel Corporation, Santa Clara, CA

9:55 a.m.
31.3 Capacitance Modeling of Laterally Non-Uniform MOS Devices, A.C.T. Aarts, R. van der Hout, J.C.J. Paasschens, A.J. Scholten, M. Willemsen, and D.B.M. Klaassen, Philips Research, Eindhoven, The Netherlands

10:20 a.m.
31.4 An Efficient Surface Potential Solution Algorithm for Compact MOSFET Models, R. Rios, S. Mudanai, W.-K. Shih, and P. Packan, Intel Corporation, Hillsboro, OR

10:45 a.m.
31.5 Modeling of RTS Noise in MOSFETs Under Steady-State and Large-Signal Excitation, J.S. Kolhatkar, E. Hoekstra, C. Salm, A.P. van der Wel, E.A.M. Klumperink, J. Schmitz, and H. Wallinga, University of Twente, Enschede, The Netherlands

11:10 p.m.
31.6 A Compact QM-Based Mobility Model for Nanoscale Ultra-Thin-Body CMOS Devices, V. P. Trivedi, J. G. Fossum, and F. Gámiz*, University of Florida, Gainesville, FL, *Universidad de Granada, Granada, Spain

Session 32: Displays, Sensors and MEMS – Thin Film Transistors

Wednesday, December 15, 9:00 a.m.
Continental Ballroom 6

Co-Chairs: Piero Migliorato, University of Cambridge
Bedrich Hostika, Fraunhofer IMS

9:00 a.m.
Introduction

9:05 a.m.
32.1 A Novel Transparent Air-Stable Printable n-Type Semiconductor Technology Using ZnO Nanoparticles, S.K. Volkman, S.E. Molesa, J.B. Lee, B.A. Mattis, A. de la Fuente Vornbrock, T. Bakhishev, and V. Subramanian, University of California, Berkeley, CA

9:30 a.m.
32.2 Single-Grain TFTs on Location-Controlled Crystal Grains Formed by Excimer Laser Crystallization of Si Thin Films, H. Kumomi, C. Shin*, G. Nakagawa*, and T. Asano*, Canon, Inc., Kanagawa, Japan, *Kyushu Institute of Technology, Fukuoka, Japan

9:55 a.m.
32.3 High Performance and High Reliability Polysilicon Thin-Film Transistors with Multiple Nano-Wire Channel, Y.-C. Wu, C.-Y. Chang, T.-C. Chang*, P.-T. Liu**, C.-S. Chen, C.-H. Tu, H.-W. Zan, Y.-H. Tai, S. M. Sze**, National Chiao Tung University, Taiwan, ROC, *National Sun Yat-Sen University, Taiwan, ROC, **National Nano Device Laboratories, Taiwan, ROC

10:20 a.m.
32.4 A Novel Methodology for Extracting Effective Density-of-States in Poly-Si Thin-Film Transistors, H.-C. Lin, K.-L. Yeh, M.-H. Lee, Y.-C. Su, T. -Y Huang, S.-W Shen*, and H.-Y. Lin**, National Chao Tung University, Taiwan, ROC, *National Nano Device Labs., Hsinchu, Taiwan, ROC, **Toppoly Optoelectronics Corporation, Taiwan, ROC

10:45 a.m.
32.5 Analytical Photo Leak Current Model of Low Temperature CW Laser Lateral Crystallization (CLC) Poly-Si TFTs, K. Suzuki, F. Takeuchi, Y. Ebiko, M. Chida, and N. Sasaki, Fujitsu Laboratories, Ltd., Kanagawa, Japan

11:10 a.m.
32.6 Impact of Transistor-to-Grain Size Statistics on Large-Grain Polysilicon TFT Characteristics, C. F. Cheng, M. C. Poon, C. W. Kok, and M. Chan, Hong Kong University of Science and Technology, Hong Kong

Session 33: Quantum Electronics and Compound Semiconductors – GaN-Based Power Devices

Wednesday, December 15, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairs: Ranbir Singh, Genesic Semiconductor
Robert Sadler, Northrop Grumman

9:00 a.m.
Introduction

9:05 a.m.
33.1 Recent Advances in III-V Nitride Electronic Devices (Invited), D. Pavlidis, The University of Michigan, Ann Arbor, MI

9:30 a.m.
33.2 A 100W High-Gain AlGaN/GaN HEMT Power Amplifier on a Conductive N-SiC Substrate for Wireless Base Station Applications, M. Kanamura, T. Kikkawa, and K. Joshin, Fujitsu Laboratories, Ltd., Kanagawa, Japan

9:55 a.m.
33.3 350V/150A AlGaN/GaN Power HFET on Silicon Substrate with Source-via Grounding (SVG) Structure, M. Hikita, M. Yanagihara, K. Nakazawa, H. Ueno, Y. Hirose, T. Ueda, Y. Uemoto, T. Tanaka, D. Ueda, and T. Egawa*, Matsushita Electric Industrial Co., Ltd., Nagaokakyo, Kyoto, Japan, *Nagoya Institute of Technology, Nagoya, Japan

10:20 a.m.
33.4 GaN Double Heterojunction Field Effect Transistor For Microwave and Millimeterwave Power Applications, M. Micovic, P. Hashimoto, M. Hu, I. Milosavljevic, J. Duvall, P.J. Willadsen, A. Kurdoghlian, P.W. Deelman, J.-S. Moon, A.Schmitz, M.J. Delaney, HRL Laboratories LLC, Malibu, CA

10:45 a.m.
33.5 $Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N/GaN$ Composite-Channel HEMTs with Enhanced Linearity, J. Liu, Y. Zhou, R. Chu, Y. Cai, K.J. Chen, and K.M. Lau, Hong Kong University of Science and Technology, Hong Kong

11:10 a.m.
33.6 Edge Trapping Mechanism of Current Collapse in III-N FETs, N. Braga, R. Mickevicius, R. Gaska*, M. S. Shur**, M. Asif Khan***, and G. Simin***, Integrated Systems Engineering Inc., San Jose, CA, *Sensor Electronic Technology, Inc., Columbia, SC, **Rensselaer Polytechnic Institute, Troy, NY, ***University of South Carolina, Columbia, SC

Session 34: Process Technology – High-k II: Interfaces and Materials Properties

Wednesday, December 15, 9:00 a.m.
Imperial Ballroom A

Co-Chairs: Glen Wilk, ASM
Martin Gutsche, Infineon

9:00 a.m.
Introduction

9:05 a.m.
34.1 Improved Short Channel Device Characteristics with Stress Relieved Pre-Oxide (SRPO) And a Novel Tantalum Carbon Alloy Metal Gate/HfO_2 Stack, H.-H. Tseng, C. C. Capasso, J. K. Schaeffer, E. A. Hebert, P.J. Tobin, D. C. Gilmer, D. Triyoso, M. E. Ramón, S. Kalpat, E. Luckowski, W. J. Taylor, Y. Jeon, O. Adetutu, R. I. Hegde, R. Noble, M. Jahanbani, and B. E. White, Freescale Semiconductor, Inc., Austin, TX

9:30 a.m.
34.2 Interface Engineering for Enhanced Electron Mobilities in W/HfO_2 Gate Stacks, A. Callegari, E. Cartier, P. Jamison* , S. Zafar, E. Gusev, V. Narayanan, C. D'Emic, D. Lacey, F. McFeely, R. Jammy, M. Gribelyuk*, J. Shepard*, W. Andreoni**, A. Curioni**, C. Pignedoli**, IBM, Yorktown Heights, NY, *IBM, Hopewell Junction, NY, **IBM Research GmbH, Rueschlikon, Switzerland

9:55 a.m.
34.3 Impact of Oxygen Vacancies on High-k Gate Dielectric Engineering, H. Takeuchi, H.Y. Wong, D. Ha, and T.-J. King, University of California, Berkeley, CA

10:20 a.m.
34.4 Depletion-Free Poly-Si Gate High-k CMOSFETs, W.S. Kim, S. Kamiyama, T. Aoyama, H. Itoh, T. Maeda, T. Kawahara, K. Torii, H. Kitajima, and T. Arikado, Semiconductor Leading Edge Technologies, Inc., Ibaraki, Japan

10:45 a.m.
34.5 Improved Electrical and Material Characteristics of Hafnium Titanate Multi-metal Oxide n-MOSFETs with Ultra-thin EOT (~8Ä) Gate Dielectric Application, S.J. Rhee, C.S. Kang, C.H. Choi, C.Y. Kang, S. Krishnan, M. Zhang, M.S. Akbar, and J.C. Lee, The University of Texas, Austin, TX

11:10 a.m.
34.6 A Robust Alternative for the DRAM Capacitor of 50nm Generation, K.H. Lee, S.-J. Chung, J.Y. Kim, K.-C. Kim, J.-S. Lim, K. Cho, J. Lee, H.J. Lim, C.-Y. Yoo, S.-T. Kim, U.-I. Chung, and J.-T. Moon, Samsung Electronics, Gyeonggi-Do, Korea

Session 35: CMOS Devices – Advanced Gate-Stack Devices

Wednesday, December 15, 1:30 p.m.
Grand Ballroom A

Co-Chairs: Serge Biesemans, IMEC
David Burnett, Freescale

1:30 p.m.
Introduction

1:35 p.m.
35.1 Gate Stack Optimization for 65nm CMOS Low Power and High Performance platform, B. Duriez, B. Tavel, F. Boeuf*, M.T. Basso*, Y. Laplanche*, C. Ortolland, D. Reber**, F. Wacquant*, P. Morin*, D. Lenoble*, R. Palla*, M. Bidaud, D. Barge, C. Dachs, H. Brut*, D. Roy*, M. Marin*, N. Cagnat*, R. Difrenza*, K. Rochereau, M. Denais*, P. Stolk, M. Woo**, and F. Arnaud*, Philips Semiconductors and *STMicroelectronics and **Freescale Semiconductor, Crolles, France

2:00 p.m.
35.2 45nm nMOSFET with Metal Gate on Thin SiON Driving 1150μA/μm and Off-state of 10nA/μm, K. Henson, R.J.P. Lander*, M. Demand, C.J.J. Dachs*, B. Kaczer, W. Deweerd, T. Schram, Z. Tokei, J.C. Hooker*, F.N. Cubaynes*, S. Beckx, W. Boullart, B. Coenegrachts**, J. Vertommen**, O. Richard, H. Bender, W. Vandervorst, M. Kaiser^, J-L. Everaert, M. Jurczak, S. Biesemans, IMEC and *Philips Research Leuven and **Lam Research, Leuven, Belgium and ^Philips Research, Endhoven, The Netherlands

2:25 p.m.
35.3 Work Function Engineering by FUSI and Its Impact on the Performance and Reliability of Oxynitride and Hf-silicate Based MOSFETs, A. Veloso, K. G. Anil, L. Witters, S. Brus, S. Kubicek, J.-F. de Marneffe, B. Sijmus, K. Devriendt, A. Lauwers, T. Kauerauf, M. Jurczak, and S. Biesemans, IMEC, Leuven, Belgium

2:50 p.m.
35.4 Intrinsic Characteristics of High-k Devices and Implications of Transient Charging Effects (Invited), B.H. Lee, C.D. Young, R. Choi, J.H. Sim, G. Bersuker, C.Y. Kang, R. Harris, G.A. Brown, K. Matthews, S.C. Song, N. Moumen, J. Barnett, P. Lysaght, K.S. Choi, H.C. Wen, C. Huffman, H. Alshareef, P. Majhi, S. Gopalan, J. Peterson, P. Kirsh, H.-J. Li, J. Gutt, M. Gardner, and H.R. Huff, P. Zeitzoff, R. Murto, L. Larson, C. Ramiller, International SEMATECH, Austin, TX

3:15 p.m.
35.5 Ultra-fast Measurements of the Inversion Charge in MOSFETs and Impact on Measured Mobility in High-k MOSFETs, D. V. Singh, P. Solomon, E.P. Gusev, G. Singco and Z. Ren, IBM T.J. Watson Research Center, Yorktown Heights, NY

3:40 p.m.
35.6 Experimental Determination of Mobility Scattering Mechanisms in Si/HfO_2/TiN and SiGe:C/HfO_2/TiN Surface Channel n- and p-MOSFETs, O. Weber, F. Andrieu, M. Cassa, T. Ernst, J. Mitard**, F. Ducroquet, J.-F. Damlencourt, J.-M. Hartmann, D. Lafond, A.-M. Papon, L. Militaru*, L. Thevenod, K. Romanjek^, C. Leroux, F. Martin, B. Guillaumot**, G. Ghibaudo^, S. Deleonibus, CEA-LETI, Grenoble, France and *LPM-INSA, Villeurbanne Cedex, France and **STMicroelectronics, Crolles Cedex, France and ^IMEP-ENSERG, Grenoble Cedex, France

Session 36: Integrated Circuits and Manufacturing – Floating-Gate and Discrete Traps Non-Volatile Memory

Wednesday, December 15, 1:30 p.m.
Grand Ballroom B

Co-Chairs: Roberto Bez, STMicroelectronics
Takashi Kobayashi, Hitachi, Ltd.

1:35 p.m.
36.1 8Gb MLC (Multi-Level Cell) NAND Flash Memory, J.-H. Park, S.-H. Hur, J. Lee, J.-T.Park, J.-S. Sel, J.-W. Kim, S.-B.Song, J.-Y. Lee, J.-H. Lee, S.-J. Son, Y.-S. Kim, M.-C. Park, S.-J. Chai, J.-D. Choi, U-I. Chung, J.-T. Moon, K. Kim and Kin, Samsung Electronics Co., Gyunggi-Do, Korea

2:00 p.m.
36.2 Impact of Few Electron Phenomena on Floating-Gate Memory Reliability, G. Molas, D. Deleruyelle, B. De Salvo, G. Ghibaudo*, M. Gely, S. Jacob, D. Lafond and S. Deleonibus, CEA-LETI, Grenoble, France and *IMEP-CNRS/INPG, Grenoble, France

2:25 p.m.
36.3 A Novel 2-bits/cell Nitride Storage Flash Memory with Greater than 1M P/E-Cycle Endurance, Y.-H. Shih, H.-T. Lue, K.Y. Hsieh, R. Liu, and C.-Y. Lu, Macronix International Co., Ltd., Taiwan, ROC

2:50 p.m.
36.4 Impact of SiON on Embedded Nonvolatile MNOS Memory, T. Ishimaru, N. Matsuzaki, Y. Okuyama, T. Mine, K. Watanabe, J. Yugami*, H. Kume, F. Ito*, Y. Kawashima*, T. Sakai*, Y. Kanamaru*, Y. Ishii*, M. Mizuno*, T. Hashimoto*, K. Okuyama*, K. Kuroda*, and K. Kubota*, Hitachi, Ltd., Tokyo, Japan and *Renesas Technology Corp., Tokyo, Japan

3:15 p.m.
36.5 High-K HfAlO Charge Trapping Layer in SONOS-type Nonvolatile Memory Device for High Speed Operation, Y.N. Tan, W.K. Chim, W.K. Choi, J.M. Sig, N.T. Hau and B.J. Cho, National University of Singapore, Singapore

3:40 p.m.
36.6 Damascene Gate FinFET SONOS Memory Implemented on Bulk Silicon Wafer, C.W. Oh, S.D. Suk, Y.K. Lee, S.K. Sung, J.D. Choe, S.Y. Lee, D.U. Choi, K.H.Yeo, M.S. Kim, S.M. Kim, M. Li, S.H. Kim, E.-J. Yoon, D.-W. Kim, D. Park, and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

4:05 p.m.
36.7 Impact of Stoichiometry Control in Double Junction Memory on Future Scaling, R. Ohba, Y. Mitani, N. Sugiyama and S. Fujita, Toshiba Corporation, Kanagawa, Japan

Session 37: Solid State Devices – Emerging Memories

Wednesday, December 15, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairs: Frans Widdershoven, Philips Research
Mitsu Koyanagi, Tohoku University

1:30 p.m.
Introduction

1:35 p.m.
37.1 Spinronic Materials and Devices: Past, Present and Future (Invited), S. Parkin, IBM Almaden Research Center, San Jose, CA

2:00 p.m.
37.2 Highly Manufacturable High Density Phase Change Memory of 64Mb and Beyond, S.J. Ahn, Y.J. Song, C.W. Jeong, J.M. Shin, Y. Fai, Y.N. Hwang, S.H. Lee, K.C. Ryoo, S.Y. Lee, J.H. Park, H. Horii*, Y.H. Ha*, J.H. Yi*, B.J. Kuh*, G.H. Koh, G.T. Jeong, H.S. Jeong, and K. Kim, Samsung Electronics, Kyunggi-Do, Korea

2:25 p.m.
37.3 Electrothermal and Phase-Change Dynamics in Chalcogenide-Based Memories, A.L. Lacaita, A. Redaelli, D. Ielmini, F. Pellizzer*, A. Pirovano*, A. Benvenuti* and R. Bez*, DEI - Politecnico di Milano, Milan, Italy and *STMicroelectronics, Milan, Italy

2:50 p.m.
37.4 Long-Retention Ferroelectric-Gate FET with a $(HfO_2)x(Al_2O_3)_{1-x}$ Buffer-Insulating Layer for 1T FeRAM, S. Sakai, M. Takahashi and R. Ilangovan, National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan

3:15 p.m.
37.5 Scalability Study on a Capacitorless 1T-DRAM: From Single-gate PD-SOI to Double-gate FinDRAM (Invited), T. Tanaka, E. Yoshida, and T. Miyashita, Fujitsu Laboratories, Ltd., Tokyo, Japan

3:40 p.m.
37.6 A New Vertically Stacked Poly-Si MOSFET for 533MHz High Speed 64Mbit SRAM, T. Kikuchi, S. Moriya, H. Matsuoka, K. Nakazato*, A. Nishida**, H. Chakihara**, M. Matsuoka**, and M. Moniwa**, Hitachi, Ltd., Tokyo, Japan and *Hitachi Cambridge Laboratory, Cambridge, UK and **Renesas Technology Corp., Tokyo, Japan

4:05 p.m.
37.7 Integration of Manufacturable 65nm-node HfSiON Transistors Optimized with Low-Thermal-Budget CMOS Process, A. Mineji, Y. Tamura, T. Watanabe, H. Ozaki, F. Ootsuka, T. Aoyama, S. Shibata, K. Tsujita, N. Ohashi, M. Yasuhira, and T. Arikado, Selete, Ibaraki, Japan

Session 38: CMOS and Interconnect Reliability – ESD, Soft-Errors and Back-End Reliability Issues for Nanoscale CMOS Technologies

Wednesday, December 15, 1:30 p.m.
Continental Ballroom 4

Co-Chairs: Kaustav Banerjee, University of California Santa Barbara Rich Blish, AMD

1:30 p.m.
Introduction

1:35 p.m.
38.1 ESD and Latchup Reliability for Nanometer CMOS Technologies (Invited), C. Duvvury and G. Boselli, Texas Instruments, Dallas, TX

2:00 p.m.
38.2 Transient-Induced Latchup in CMOS Technology: Physical Mechanism and Device Simulation, M.D. Ker and S.F. Hsu, National Chiao-Tung University, Hsinchu, Taiwan

2:25 p.m.
38.3 Comprehensive Study of Soft Errors in Advanced CMOS Circuits with 90/130nm Technology, Y. Tosaka, H. Ehara*, M. Igeta*, T. Uemura, H. Oka, N. Matsuoka**, and K. Hatanaka**, Fujitsu Laboratories, Ltd., Tokyo, Japan and *Fujitsu Ltd., Tokyo, Japan and **Osaka University, Osaka, Japan

2:50 p.m.
38.4 Investigation of Soft Error Rate Including Multi-Bit Upsets in Advanced SRAM Using Neutron Irradiation Test and 3D Mixed-Mode Device Simulation, Y. Kawakami, M. Hane, H. Nakamura*, T. Yamada*, and K. Kumagai*, NEC Corporation, Kanagawa, Japan and *NEC Electronics Corp., Kanagawa, Japan

3:15 p.m.
38.5 Enhanced Dielectric-Constant Reliability of Low-k Porous Organosilicate Glass (k=2.3) for 45-nm-Generation Cu Interconnects, D. Ryuzaki, H. Sakurai*, K. Abe*, K. Takeda, and H. Fukuda, Hitachi, Ltd., Tokyo, Japan and *Hitachi Chemical Co., Ltd., Ibaraki, Japan

3:40 p.m.
38.6 Thermally Robust Cu Interconnects with Cu-Ag Alloy for Sub 45nm Node, A. Isobayashi, Y. Enomoto, H. Yamada*, S. Takahashi and S. Kadomura, Sony Corporation, Kanagawa, Japan and *Sony Computer Entertainment, Inc.

4:05 p.m.
38.7 Effect of Mechanical Strength and Residual Stress of Dielectric Capping Layer on Electromigration Performance in Cu/Low-k Interconnects, K.-W Lee, H.J. Shin, Y.J. Wee, T.K. Kim, J.H. Kim, S.M. Choi, B.S. Suh, S.J. Lee, K.-K. Park, S.J. Lee, J.W. Hwang, S.W. Nam, Y.J. Moon, J.E. Ku, H.J. Lee, M.Y. Kim, I.H. Oh, J.Y. Maeng, A.T. Kim, I.R. Kim, J.E. Lee, S.M. Lee, W.-H. Choi, S.J. Park, N.I. Lee, H.-K. Kang and G.P. Suh, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea

Session 39: Modeling and Simulation – Process Modeling

Wednesday, December 15, 1:30 p.m.
Continental Ballroom 5

Co-Chairs: Conor Rafferty, Noble Device Technologies
Gerhard Hobler, TU Vienna

1:30 p.m.
Introduction

1:35 p.m.
39.1 Front End Stress Modeling for Advanced Logic Technologies (Invited), S.M. Cea, M. Armstrong, C. Auth, T. Ghani, M.D. Giles, T. Hoffmann, R. Kotlyar, P. Matagne, K. Mistry, R. Nagisetty, B. Obradovic, R. Shaheed, L. Shifren, M. Stettler, S. Tyagi, X. Wang, C. Weber, K. Zawadzki, Intel Corporation, Hillsboro, OR

2:00 p.m.
39.2 On the Modeling of Transient Diffusion and Activation of Boron During Post-Implantation Annealing, P. Pichler, C. J. Ortiz, B. Colombeau*, N.E.B. Cowern*, E. Lampin**, A. Claverie#, F. Cristiano#, W. Lerch^, S. Paul^, Fraunhofer-IISB, Erlangen, Germany and *University of Surrey, Guildford, UK and **IEMN/ISEN, Villeneuve d'Ascq, France and #CEMES/LAAS CNRS, Toulouse, France and ^Mattson Thermal Products, GmbH, Dornstadt, Germany

2:25 p.m.
39.3 Electrical Deactivation and Diffusion of Boron in Preamorphized Ultrashallow Junctions: Interstitial Transport and F Co-Implant Control, B. Colombeau, A. J. Smith, N. E. B. Cowern, W. Lerch*, S. Paul*, B. J. Pawlak**, F. Cristiano#, X. Hebras#, University of Surrey, Guildford, UK,*Mattson Thermal Products GmbH, Dornst and **Philips Innovative Technology Solutions, Leuven, Belgium and #LAAS-CNRS, Toulouse, France

2:50 p.m.
39.4 Simulation of High-Temperature Millisecond Annealing Based on Atomistic Modeling of Boron Diffusion/Activation in Silicon, M. Hane, T. Ikezawa*, T. Matsuda**, and S. Shishiguchi**, NEC Corporation, Kanagawa, Japan and *NEC Informatec Systems, Ltd. And **NEC Electronics Corporation

3:15 p.m.
39.5 Transient Behavior of Phosphorus Dose Loss and Modeling of Dopant Segregation at the Si/SiO_2 Interface, J.R. Tsai, L.W. Ho, S.H. Lin, T.C. Chang*, M.D. Shieh*, H.C. Lin**, C.P. Lin, W.S. Feng, and R.D. Chang, Chang Gung University, Taiwan, ROC and *Nanya Technology Corp., Taiwan, ROC and **National Nano Device Lab, Taiwan, ROC

3:40 p.m.
39.6 Experimental and Simulation Study of Boron Segregation and Diffusion during Gate Oxidation and Spike Annealing, A. Ghetti, A. Benvenuti, G. Molteni, S. Alberici, V. Soncini, A. Pavan, STMicroelectronics, Agrate Brianza, Italy

Session 40: Displays, Sensors and MEMS – Image Sensors and Bio Sensors

Wednesday, December 15, 1:30 p.m.
Continental Ballroom 6

Co-Chairs: Homayoon Haddad, Agilent
Roland Thewes, Infineon Technologies

1:30 p.m.
Introduction

1:35 p.m.
40.1 Device Technologies for High Quality and Smaller Pixel in CCD and CMOS Image Sensors, H. Abe, Sony, Kanagawa, Japan

2:00 p.m.
40.2 Dark Current Reduction in Very-Large Area CCD Imagers for Professional DSC Applications, I. Peters, A. Kleimann, F. Polderdijk, W. Klaassens, R. Frost*, and J.T. Bosiers, DALSA Professional Imaging, Eindhoven, The Netherlands and *DALSA Semiconductors, Quebec, Canada

2:25 p.m.
40.3 Crosstalk Improvement Technology Applicable to 0.14µm CMOS Image Sensor, C.H. Tseng, S.W. Wuu, H.-C.Chien, D.-N. Yaung,T.-H. Hsu, J.S. Lin, H.-J. Hsu, C.Y. Yu, C.H. Lo, C.S. Wang, TSMC, Taiwan, ROC

2:50 p.m.
40.4 MOSFETs and High-Speed Photodetectors on GeOI Substrates Fabricated Using Melt Growth, Y. Liu, K. Gopalakrishnan, P. Griffin, K. Ma, M. Deal, J. Plummer, Stanford University, Stanford, CA

3:15 p.m.
40.5 A Highly Manufacturable Nano-Metallic Particle Based DNA Micro-Array, J. Li, C. Xu, Y. Wang, Z. Lu*, and M. Chan, Hong Kong University of Science and Technology, Hong Kong and *Southeast University, Nanjing, China PR

3:40 p.m.
40.6 Label-Free Detection of DNA Hybridization with Au/SiO_2/Si Diodes and Poly-Si TFTs, P. Estrela, A.G. Stewart, P. Migliorato, and H. Maeda*, University of Cambridge, Cambridge, UK and *TPRC Seiko Epson, Nagano-ken, Japan

4:05 p.m.
40.7 Three-Dimensional Multichannel Si Microprobe Electrode Array Chip for Analysis of the Nervous System, T. Kawano, A. Ishihara*, T. Harimoto*, H. Takao, K. Sawada, S. Usui**, and M. Ishida, Toyohashi University of Technology, Toyohashi, Japan and *Chukyo University, Toyota, Japan and **RIKEN BSI, Saitama, Japan

Session 41: Quantum Electronics and Compound Semiconductors – HEMTs: Physics and New Technologies

Wednesday, December 15, 1:30 p.m.
Continental Ballroom 7-9

Co-Chairs: Tetsuya Suemitsu, NTT Photonics Laboratories
Giovanni Verzellesi, Universita' di Modena e Reggio Emilia

1:30 p.m.
Introduction

1:35 p.m.
41.1 Thermal, Electrical and Environmental Reliability of InP HEMTs and GaAs PHEMTs (Invited), J. A. del Alamo and A. A. Villanueva, MIT, Cambridge, MA

2:00 p.m.
41.2 100nm InAlAs/InGaAs Double-Gate HEMT Using Transferred Substrate, N. Wichmann, I. Duszynski, S. Bollaert, J. Mateos*, X. Wallart, A. Cappy, IEMN-DHS, Velleneuve d'Ascq, France and *Universidad de Salamanca, Salamanca, Spain

2:25 p.m.
41.3 Suppression of Kink Phenomenon In Ultra-High-Speed Strained InAs-Inserted E-Mode HEMTS with a New Y-Shaped Gate Structure, D.H. Kim, T.W. Kim, H.H. Noh, J.H. Lee, W.Feng*, X. Xie*, Q. Du*, J. Jiang*, J.-I. Song and K.S. Seo, Seoul National University, Seoul, Korea and *MBET Pte Ltd., Singapore

2:50 p.m.
41.4 Growth and Characterization of AlGaN/AlN/GaN HEMTs on 100-mm-Diameter Epitaxial AlN/Sapphire Templates, M. Miyoshi, A. Imanishi, H. Ishikawa, T. Egawa, K. Asai*, M. Mouri*, T. Shibata*, M. Tanaka*, and O. Oda*, Nagoya Institute of Technology, Nagoya, Japan and *NGK Insulators, Ltd., Nagoya, Japan

3:15 p.m.
41.5 Polarization Engineering of InAlN/GaN HFET and the Effect on DC and RF Performance, O. Katz, D. Mistele, B. Meyler, G. Bahir, and J. Salzman, Technion, Haifa, Israel

3:40 p.m.
41.6 Universal Signature of Ballistic Transport in Nanoscale Field Effect Transistors, A. Schliemann, L. Worschech, A. Forchel, G. Curatola*, and G. Iannaccone*, Universitat Wurzburg, Wurzburg, Germany and *Universita degli Studi di Pisa, Pisa, Italy

Session 42: Process Technology – Advances in Sourse Drain Engineering

Wednesday, December 15, 1:30 p.m.
Imperial Ballroom

Co-Chairs: Kevin Jones, University of Florida
Franck Arnaud, STMicroelectronics

1:30 p.m.
Introduction

1:35 p.m.
42.1 Front-End-of-Line (FEOL) Optimization for High-Performance, High-Reliable Strained-Si MOSFETs; from Virtual Substrate to Gate Oxidation, J.-W. Lee, S.-G. Lee, Y.-P. Kim, C.-S. Kim, H.-J. Cho, S.-B. Kim, I.-S. Jung, D.-H. Lee, D.-C. Kim, T.-S. Jeon, S.-G. Park, H.-B. Park, Y.-H. Son, Y.-E. Lee, G.-J. Jin, H.-L. Lee, B.-Y. Koo, J-B Kang, Y-G Shin, U-I Chung, J-T Moon, Samsung Electronics Co., Gyeonggi-Do, Korea

2:00 p.m.
42.2 Highly Controllable Cyclic Selective Epitaxial Growth (CySEG) for 65nm CMOS Technology and Beyond, S.H. Lee, D.S. Shin, H.S. Rhee, T. Ueno, H. Lee, M.H. Park, N.-I. Lee, H.-K. Kang, and K.-P. Suh, Samsung Electronics Co.,Ltd, Kyunggi-Do, Korea

2:25 p.m.
42.3 A Systematic Study of Trade-offs in Engineering a Locally Strained pMOSFET, F. Nouri, P. Verheyen*, L. Washington, V. Moroz**, I. De Wolf*, M. Kawaguchi, S. Biesemans*, R. Schreutelkamp, Y. Kim, M.Shen, X. Xu**, R. Rooyackers*, M. Jurczak*, G. Eneman*, K. De Meyer*, L. Smith*, D. Pramanik*, H. Forstner, and G. Higashi, Applied Materials, Inc., Sunnyvale, CA and *IMEC, Leuven, Belgium and **Synopsys, Mountain View, CA and KU Leuven, Leuven, Belgium

2:50 p.m.
42.4 Drastic Suppression of Thermally Induced Leakage of NiSi Silicided Shallow Junctions by Pre-SALICIDE Fluorine Implantation, M. Tsuchiaki, K. Ohuchi* and A. Nishiyama, Toshiba Corporation, Kanagawa, Japan and *Toshiba Semiconductor Company, Yokohama, Japan

3:15 p.m.
42.5 A Highly Manufacturable Low-k ALD-SiBN Process for 60nm NAND Flash Devices and Beyond, J.G. Kim, J.-Y. Ahn, H.-S. Kim, J.-W. Lim, C.-H. Kim*, H. Shu*, K. Hasebe*, S.-H. Hur, H.-S. Kim, Y.-G. Shin, U-I. Chung, and J.-T. Moon, Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea and *Tokyo Electron Ltd. Yamanashi, Japan