WELCOME FROM THE GENERAL CHAIR

On behalf of the entire IEDM committee, I would like to welcome you to the 2010 IEEE International Electron Devices Meeting to be held December 6-8, 2010 in San Francisco. The IEDM continues to be the world's premier venue for presenting the latest breakthroughs and the broadest and best technical information in electronic device technologies. This year we have a strong collection of both contributed and invited papers that will be presented by industrial and academic leaders and students from around the world. Short summaries of each paper are available on the IEDM web site, which we encourage everyone to visit – http://www.ieee.org/conference/iedm. This year, we will continue to distribute an abbreviated digest at the meeting, along with electronic versions of the complete abstracts, to more effectively leverage modern electronic content distribution capabilities. The full digest will be available on the IEEE Xplore website and the DVD package offered by the IEEE Electron Devices Society after the conference.

Meikei Ieong
General Chair

In addition to the many regular paper sessions - and the always informative and entertaining IEDM Luncheon on Tuesday - we will again feature several special sessions.

On Sunday December 5, 2010, two short courses will be offered: "15nm CMOS Technology" and "Reliability and yield of advanced integrated technologies". These courses have been organized and will be presented by internationally known leading researchers active in their respective areas of technology. The topics have broad appeal to IEDM participants with material suitable for newcomers as well as experts in the field.

The Plenary Session on Monday morning will feature three invited talks: Kinam Kim from SAIT will give a talk entitled "Future memory (tentative)", Prof. Arunjai Mittal from Infineon will present a talk entitled "Microelectronics: Enabling Energy Savings through Innovation and Technology". The final talk of the session will be provided by Luke P. Lee from University of Carlifornia, Berkeley, who will give a talk entitled "Bionanoscience for Global Healthcare Technology".

Kazunari Ishimaru
Technical Program Chair

The Luncheon on Tuesday will be given by James Clifford, Senior Vice President of Qualcomm.

On Tuesday night, we will again feature our popular and interactive Panel sessions. The first panel is entitled "Power crunch - threat or opportunity?" and will be organized by Ralf Brederlow from Texas Instruments. The second panel is entitled "Heterogeneous device integration as enabler of functional diversification for More Than Moore". This panel will be organized by Adrian Ionescue of EPFL.

Recognizing the increasing importance of device and circuit interaction, we will to continue to offer a special session, on Tuesday afternoon, entitled "Challenges for non-conventional devices and 3D LSIs".

The Emerging Technology special session this year features breakthroughs in "Next Generation Power Devices and Technology ", and will include six talks from leading experts in this exciting area looking from a broad variety of perspectives including materials, devices, technology, and applications.

On behalf of the IEDM, Kazunari Ishimaru, the Technical Program Chair, Veena Misra, the Technical Program Vice-Chair, and I want to express our sincere appreciation to all of the IEDM authors and to each of the members of the IEDM committee. The authors really make the IEDM what it is; a forum for the presentation of the leading work in our field. The IEDM committee members did an outstanding job in planning and organizing the 2010 conference.

Veena Misra
Technical Program Vice-Chair

The IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution which has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at this conference and on their website – http://www.ieee.org

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2010 IEEE International Electron Devices Meeting.

Meikei Ieong
General Chair

Conference Highlights

SHORT COURSES
Sunday, December 5, 9:00 a.m. - 5:30 p.m.
Continental Ballrooms 1-4
Continental Ballrooms 6-9

PLENARY SESSION
Monday, December 6, 9:00 a.m. - 12:00 p.m.
Grand Ballroom B

PLENARY SESSION AWARD PRESENTATIONS

2009 Roger A. Haken
Best Student Paper Award:

To: Perrine Batude of CEA, LETI, MINATEC

"For the paper entitled, "Advances in 3D CMOS Sequential Integration"

EDS Celebrated Member

To: Herbert Kroemer

"For fundamental contributions to the field of electron devices for the benefit of humanity"

2010 EDS J.J. Ebers Award

To: Mark E. Law

"For contributions to widely used silicon integrated circuit process modeling"

2010 EDS Distinguished Service Award

To: Marvin H. White

"To recognize and honor outstanding service to the Electron Devices Society."

2010 EDS Education Award

To: To Be Announced

"To honor an individual(s) who has made distinguished contributions to education within the field of interest of the Electron Devices Society"

2010 IEEE/EDS Fellows
(Only includes those who requested to be recognized at the IEDM)

To: Joerg Appenzeller
Amitava Chatterjee
Long-Sheng Fan
Yogesh Gianchandani
Dimitros Ioannou
Takamaro Kikkawa
Richard Lai
Patrick Lenahan
Chang Liu
Kaizad Mistry
Kwok Ng
Yasuhisa Omura
Thomas Skotnicki
Nobukazu Teranishi
Shumpei Yamazaki

RECEPTION
Monday, December 6, 6:30 p.m. – 8:00 p.m.
Grand Ballroom B

IEDM LUNCHEON
Tuesday, December 7
12:20 p.m. - 2:00 p.m.
Grand Ballroom B

2010 IEEE Cledo Brunetti Award

To: Ghavam G. Shahidi, IBM T.J. Watson Research Center

"For contributions to and leadership in the development of silicon-on-insulator CMOS technology."

2010 IEEE Andrew S. Grove Award

To: Bijan Davari, IBM T.J Watson Research Center

"For contributions to high performance deep-submicron CMOS technology."

2010 IEEE Daniel E. Noble Award

To: Shinichi Abe, Toyota Motor Corporation, Shoichi Sasaki, Keio University, Takehisa Yaegashi, Cordia Corporation Ltd.

"For pioneering contributions to the development and market penetration of hybrid electric vehicles (HEVs) through the establishment of innovative architectures and control technologies."

2010 IEEE Frederik Philips Award

To: John E. Kelly III, IBM

"For leadership in the development and commercialization of silicon technology and for forging industry-university partnerships for semiconductor research and development."

2010 IEEE David Sarnoff Award

To: Mark J.W. Rodwell, University of California, Santa Barbara

"For development of millimeter-wave and sub-millimeter-wave InP bipolar transistors and integrated circuits."

2010 IEEE Kiyo Tomiyasu Award

To: Tsu-Jae King Liu, University of California at Berkeley

"For contributions to nanoscale MOS transistors, memory devices, and MEMs devices."

LUNCHEON PRESENTATION

Luncheon Presentation: *"Evolution and Directions for Mobile Wireless Devices", James Clifford, Qualcomm CDMA Technologies*

PANEL SESSION

Tuesday, December 7
8:00 p.m. - 10:00 p.m.
Continental Ballroom 4
Continental Ballroom 6

SPECIAL SESSION

Tuesday, December 7
2:15 p.m. – 5:00 p.m.
Grand Ballroom A

GENERAL INFORMATION

Hilton San Francisco Union Square
333 O'Farrell Street
San Francisco, CA 94102
415-771-1400
December 6-8, 2010

REGISTRATION INFORMATION

	Advance (Postmarked by November 16th)	After (November 16th or at Conference)
Technical Session		
IEEE Member	$450.00	$490.00
Non-member	$590.00	$630.00
Students:		
Member	$100.00	$100.00
Non-Member	$150.00	$150.00

Short Courses (Due to limited space, it is recommended that you register in advance for the Short Courses)

Member	$450.00	$450.00
Non-member	$525.00	$525.00
Student Member	$125.00	$125.00
Student Non-Member	$175.00	$175.00

Payment of the Technical Session registration fee entitles the registrant to one copy of the technical digest on a USB, one ticket for the Monday evening Wine and Cheese Reception and entrance to all technical sessions. Technical Session registration does not include entrance to the Short Courses or the Tuesday luncheon. TO QUALIFY FOR THE MEMBER REGISTRATION FEE, REGISTRANT MUST BE A MEMBER OF IEEE PRIOR TO THE CONFERENCE.

Payment of the Short Course registration fee entitles the registrant to entrance to one short course, one copy of the course workbook and one copy of the CD-ROM of the short course workbook. Short Course registration does not include entrance to the Technical Sessions.

For Advance Registration, go to www.ieee-iedm.org and click on "Register", NO LATER THAN NOVEMBER 16, 2010 to qualify for the early registration price. Due to limited space, it is recommended that you register in advance to attend the Short Courses.

Confirmations will be sent out to all conference registrants.

REGISTRATION FORM AND PAYMENT SHOULD BE SENT TO:

IEDM
19803 Laurel Valley Place
Montgomery Village, MD 20886 USA
Tel: 301-527-0900 ext. 2
Fax: 301-527-0994

Checks MUST BE MADE PAYABLE TO 2010 IEDM, IN U.S. DOLLARS AND DRAWN ON A U.S. BANK. International registrants should not send wire transfers. If International participants cannot send a check prior to the conference, mail the registration form without payment prior to the conference. Bring payment with you and pay the registration fee onsite.

Your registration materials will be held for you at the conference. Your cancelled check is your receipt.

CANCELLATION POLICY: You are encouraged to register in advance for your own convenience. Due to printing and hotel commitments, refunds requested after November 15 cannot be guaranteed. A $30.00 processing fee will be withheld from ALL refunds.

REGISTRATION CENTER: The Conference Registration Center, located in the East Lounge of the Hilton San Francisco Union Square will be open as follows:

SHORT COURSE REGISTRANTS ONLY

Saturday, December 4	5:00 p.m.- 7:00 p.m.
Sunday, December 5	8:00 a.m.- 11:00 a.m.

TECHNICAL SESSION REGISTRANTS

Sunday, December 5	11:00 a.m. - 5:00 p.m.
Monday, December 6	8:00 a.m. - 5:00 p.m.
Tuesday, December 7	8:30 a.m. - 5:00 p.m.
Wednesday, December 8	8:30 a.m. - 3:00 p.m.

HOTEL RESERVATIONS: A block of rooms at the Hilton San Francisco Union Square has been reserved for IEDM participants. Special IEDM room rates are as follows:

Single/Double: $199
Plus a 14.05% city tax.

To make a reservation, go to www.ieee-iedm.org and click on "General Information", then click on "Hotel Information", NO LATER THAN NOVEMBER 6th to qualify for a room under our special rates. An advance deposit or credit card guarantee is necessary to hold your room, if arrival is scheduled after 6:00 p.m.

SHORT COURSES: The IEDM sponsors two short courses on Sunday, December 5, from 9 a.m. to 5:30 p.m. The courses are: "15nm CMOS Technology" and "Reliability and Yield Advanced Integrated Technologies" These courses will be presented by experts in the fields. Lectures will start with introductory material for the general audience and progress towards description of the latest developments.

For Advance Registration, go to www.ieee-iedm.org and click on "Register." The registration fee is $450 for IEEE members and $525 for non IEEE members. Registration entitles the registrant to one copy of the short course workbook, one copy of the short course CD-Rom, refreshments and lunch. Attendance is limited, so advanced registration is recommended.

EVENING DISCUSSIONS: On Tuesday evening, December 7, beginning at 8:00 p.m., the IEDM will offer two evening Panel Discussions on timely issues.

"Heterogeneous Device Integration as Enabler of Functional Diversification for More than Moore"
"Power Crunch – Threat or Opportunity"

TO PERMIT SPONTANEOUS AND CANDID DISCUSSION, NO VERBATIM RECORDING BY TAPE OR CAMERA WILL BE PERMITTED IN ANY PANEL DISCUSSION.

SPEAKER PREPARATION ROOM: The IEDM will sponsor a Speaker Preparation Room for speakers to preview their presentations. Speakers must preview their presentations one day in advance. There will be no previewing of presentations the day of the presentation.

The Speaker Ready Room will be open for speaker use:

Saturday, December 4	5:00 p.m. – 7:00 p.m.
Sunday, December 5	8:00 a.m. – 5:00 p.m.
Monday, December 6	8:00 a.m. – 5:00 p.m.
Tuesday, December 7	8:00 a.m. – 5:00 p.m.
Wednesday, December 8	8:00 a.m. – 12:00 p.m.

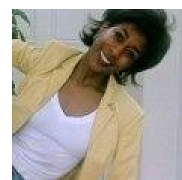
IEDM LUNCHEON: The IEDM luncheon featuring an address by James Clifford, Senior Vice President and General Manager of Operations of Qualcomm CDMA Technologies on "Evolution and Directions for Mobile Wireless Devices:, will be held on Tuesday, December 7, at 12:20 p.m. in Grand Ballroom B. Luncheon tickets are available through Advance Registration or on-site at a cost of $55.00 to conference attendees only.

WINE AND CHEESE RECEPTION: A Wine and Cheese Reception for conference participants and their guests will be held on Monday, December 6 from 6:30 p.m. to 8:00 p.m. in Grand Ballroom B. ONE ADMISSION TO THE RECEPTION IS INCLUDED IN THE REGISTRATION FEE.

TECHNICAL DIGEST and CD-ROM: Extra copies of the Technical Digest/USB can be purchased by conference registrants through Advance Registration. A LIMITED number of Digests will be for sale after 2:00 p.m. on Tuesday, December 7 at the On-Site Registration Desk of the Conference. The unit cost of the USB, if ordered through Advance Registration or purchased on-site is $125.00. Digests will be available after the conference by mail from IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855. Customer Service Department 732-981-0060 or toll free: 800-678-4333, email is customer-service@ieee.org. One copy of the technical digest/USB is included in the registration fee.

GRADUATES OF THE LAST DECADE (GOLD): Your Career and Networking with IEEE Electron Devices Society AdCom Members – by Ravi M. Todi, EDS GOLD Representative

Come join us on Sunday evening, December 5, 2010, at the Hilton San Francisco Union Square Hotel for the EDS Graduates of the Last Decade (GOLD) event. This free career development strategy session is especially designed for graduate students and young professionals. The program includes a seminar on career development strategies for succeeding in today's globally-competitive world; a panel discussion focusing on career path selection with expert panelists from academia, research, and manufacturing; and a golden opportunity for you to network with EDS Officers and Administrative Committee (AdCom) members. The 2010 Early Career Award winner will also be presented at this event. It's a great opportunity to network and develop some key skills to be competitive in today's global environment.



Sheila Thorne, Worldwide IT Specialist Profession Leader, IBM
Do as I Say, Not as I Did — Lessons in Career Management

There are books and lectures on how to be successful. There are lots of hints and tips on how to get ahead. This session takes a different approach: what not to do. A great refresher for those in mid-career; a good primer for those just starting out.

Sheila Thorne is a mechanical engineer by training and an IT specialist by experience. She has over 28 years of IBM experience in diverse areas and has designed cash gates for ATMs, implemented networks, developed applications and facilitated strategy & requirements sessions. Sheila has taught and developed methodology classes and is a member of the National Speakers Association, a Senior Member of IEEE and an Open Group Master Certified IT Specialist

For additional details on this EDS sponsored GOLD event, please contact EDS GOLD representative, Dr. Ravi Todi at rtodi@ieee.org

MEMBERSHIP PROMOTION FOR NON-IEEE MEMBERS: Special Offers for non-IEEE Members!
Credit Voucher Offer: If you register and pay for the conference as a non-IEEE member, you will receive a Credit Voucher in your registration packet, worth US$25.00 towards one year of IEEE membership and Free EDS membership (total value US$37.00). This offer is also valid for members of other scientific/technical societies and non-member students.

Credit Vouchers are only valid at the conference and must be redeemed at the EDS Membership Booth, located in the conference registration area.

MEMBERSHIP PROMOTION FOR CURRENT IEEE MEMBERS: Attention IEEE Members!
Your IEDM conference registration includes membership in the IEEE Electron Devices Society (EDS). As an EDS member you will receive the following basic membership benefits:

- On-line access to the following publications at www.ieeexplore.ieee.org:
  - **New!** ***IEEE Journal of Photovoltaics*** *(Coming in 2011)*
  - *IEEE Electron Device Letters* (All issues available from 1980 to current)
  - *IEEE Trans. on Electron Devices* (All issues available from 1954 to current)
  - *IEEE IEDM Proceedings* (All digests available from 1955 to current)
  - *IEEE/OSA Journal of Lightwave Technology*
  - *Electron Devices Society Newsletter*
- Free Copy-Editing Service of manuscripts submitted to IEEE Transactions on Electron Devices or IEEE Electron Device Letters
- QuestEDS – An EDS member benefit service where members can submit questions on-line concerning the EDS field of interest and can view the answers provided by experts in the field.
- Electron Devices Member Roster (www.ieee.org/society/eds/roster)

The IEEE Membership Desk will be open during the following hours:

Monday, December 6	9:00 a.m. - 5:00 p.m.
Tuesday, December 7	9:00 a.m. - 5:00 p.m.
Wednesday, December 8	9:00 a.m. - 3:00 p.m.

MESSAGE CENTER: An IEDM Message Board will be in operation in the Registration Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator (415-771-1400) for the IEDM Conference Message Desk. Please check the message board periodically.

ROGER A. HAKEN BEST STUDENT PAPER: The 2009 Roger A. Haken Best Student Paper Award will be presented on Monday, December 6, at the Plenary Session to Perrine Batude of CEA, LETI, MINATEC for the paper entitled, "Advances in 3D CMOS Sequential Integration".

One paper presented by a student at the 2010 IEDM will be selected for the 2010 Best Student Paper Award. To be eligible, the paper must be based on the student's own work and have been identified as a student paper at the time of submission. Presentation of the award will be made at the 2011 IEDM.

BADGES: Badges are required for admittance to all sessions and the Wine and Cheese Reception. Please wear your badge at all times while attending the conference, so that you will not be delayed entry to a session.

PRESS ROOM: Beginning on Monday, the Press Room will be in operation during registration hours.

AIRPORT TRANSPORTATION: The SFO Airporter and taxi service is available from the San Francisco International Airport to the Hilton San Francisco Union Square Hotel. The following estimated rates are subject to change:

SFO Airporter - $15 one way/ $30 round Trip
Taxi - $30 one way

RECRUITING: In keeping with the long standing tradition of fostering a low key, research oriented atmosphere for the IEDM, the Conference Committee and the Electron Devices Society of the IEEE discourage overt and highly visible recruiting activities in association with the IEDM. IEEE policy #9.l8 prohibits recruiting at IEEE-sponsored conferences, consequently, recruiters and recruitment advertisements will not be permitted in IEDM hotel space or meeting facilities and all unauthorized material will be removed from the premises.

PLEASE DIRECT CONFERENCE INQUIRIES TO:

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IEDM
19803 Laurel Valley Place
Montgomery Village, MD 20886 USA
Tel: 301-527-0900 ext. 2
Fax: 301-527-0994
Email: phyllism@widerkehr.com

Seated from left to right: Zsolt Tokei, Characterization, Reliability, and Yield Chair, Tzu-Ning Fang, Memory Technology Chair, Kazunari Ishimaru, Technical Program Chair, Meikei Ieong, General Chair, Veena Misra, Technical Program Vice Chair, Albert Chin, Asian Arrangements Co-Chair, Howard C.-H. Wang, Short Course Chair, Suman Datta, Quantum, Power, and Compound Semiconductor Devices Chair

Standing from left to right: Polly Mahoney, Assistant Conference Manager, Stefan De Gendt, European Arrangements Co-Chair, Norikatsu Takaura, Asian Arrangements Co- Chair, Tahir Ghani, Emerging Technologies Chair, Masami Hane, Publications Chair, Karlheinz Bock, Displays, Sensors and MEMS Chair, Werner Weber, Short Course Vice Chair, Giovanni Ghione, European Arrangements Co-Chair, John Suehle, Publicity Chair, Patrick Fay, Publicity Vice Chair, Kentaro Shibahara, Process Technology Chair, Seok-Hee Lee, CMOS Devices and Technology Chair, Ganesh Samudra, Modeling and Simulation Chair, Phyllis Mahoney, Conference Manager

SHORT COURSE

15nm CMOS Technology

Sunday, December 5
9:00 a.m. – 5:30 p.m.

Course Organizer: *Kelin J. Kuhn, Intel Corporation*

The 15nm technology node faces extraordinary challenges in scaling, transistor architecture, lithography technique, and back-end integration, as well as increasing pressure for co-optimization of process and circuit design. Evolution in the trends of CMOS development are occurring, with potential significant changes in transistor architecture (will 15nm be the first non-planar generation?), gate construction (are future innovations in dielectric and metal materials possible?), patterning (will 15nm be the EUV intercept generation?), backend materials selection (is a lower k architecture possible?) and design/process interaction (will variation be the ultimate limiter?). To help guide us through these challenges, this short course brings the leading technologists from industry to provide insight and likely solutions for 15 nm CMOS technologies.

The first lecture by ST Microelectronics Fellow, Thomas Skotnicki, begins with an overview of the ITRS roadmap, and then discusses specific scaling challenges for voltage, power, density, performance; as well as reviewing SOC requirements. Next, Mukesh Khare of IBM Research will share his thoughts on the 15nm transistor architecture challenges, including electrostatics, variation, parasitic elements, leakage, and mobility enhancement; as well as reviewing key technologies such as high-k metal gate. The third talk by Intel Fellow, Sam Sivakumar, covers lithographic challenges for the 15nm node, reviewing both the knobs available for lithographic improvement and the available alternatives for the 15nm generation. The fourth talk is by Yoshihiro Hayashi of Renesas and reviews the challenges of back-end integration toward the 15nm node including assembly/BE interactions, and discusses connectivity and functionality in the BEOL. The final talk by Texas Instruments Fellow, Clive Bittlestone, covers the increasing challenges of device/circuit interaction, with discussion on the impact of various scaling and transistor architecture choices on product implementation.

Introduction and Overview
Instructor: Kelin J. Kuhn, Intel Corporation

CMOS Technologies – Trends, Scaling and Issues
Instructor: Thomas Skotnicki, ST Microelectronics, Fellow and Director of Advanced Devices

ITRS overview
Voltage scaling (for logic/for SRAM)
Power scaling (low power/leakage)
Density scaling (Gate length/pitch, variability)
Performance scaling (mobility/electrostatics)
SOC requirements and prerogatives
Perspective

15nm Device Challenges and Solutions
Mukesh Khare, IBM Research

Conventional and Fully Depleted (inc. MultiGate) device
Electrostatics: Gate Length Scaling
Intrinsic Device Variability
Transistor Parasitics
Device Leakage
Gate Dielectric: High-K Metal Gate
Mobility Enhancement

Lithography for 15nm Technology Node
Instructor: Sam Sivakumar, Intel Corporation

Introduction

The Knobs for Feature Size Scaling
Bigger Lenses
Shorter wavelengths
Trying harder
Lithography choices for the next generation
The technical considerations
The economic considerations
The co-optimization imperative

BEOL Technology toward the 15nm Technology Node
Instructor: Yoshihiro Hayashi, Renesas Electronics Corporation
Introduction
BEOL Impact on LSI performances
Scalability in BEOL
Low-k and Etch Stop Options
Cu Pitch Scaling, Line Resistance challenges
EM / TDDB Reliability
Connectivity in BEOL
Assembly/BE interactions
Chip-to-chip interconnections
Functionality in BEOL
BEOL memories and RF options

Device / Circuit Interactions at 15nm Technology Node
Instructor: Clive Bittlestone, Texas Instruments
Scaling roadmap and resulting circuit challenges
Device architecture choices and impact on circuits/designs
Interconnect Cap and RC issues and product impact at 15nm node
Variation effects at 15nm node, Vccmin implications
Design for manufacturing issues at the 15nm node

SHORT COURSE

Reliability and Yield of Advanced Integrated Technologies

Sunday, December 5
9:00 a.m. – 5:30 p.m.

Course Organizer: Guido Groeseneken, IMEC

With the continuous downscaling of CMOS technologies, reliability is more and more becoming a major bottleneck. First of all the electric fields and current and power densities have increased continuously and are now reaching the maximum values that can be allowed for reliable operation. At the same time an impressive effort is taking place introducing new materials and novel device architectures to maintain the effective performance scaling. New materials like high k dielectrics and metal gates for both logic and memory technologies have already been introduced, while Ge or III-V materials for high mobility devices and novel device concepts such as Multiple gate FET's are under investigation. These new materials and devices often have unknown reliability behavior and/or introduce new failure mechanisms, whereas their speed of introduction exceeds the capabilities to explore their reliability performance in great detail. Finally, the market is continuously demanding higher reliability levels, with single digit failure rates in FIT units (1 FIT= 1 failure per 10^9 operating hours) for present technologies.

In the past, the technological reliability margins were always sufficiently high, while in the technologies under development reliability may no longer be guaranteed at the technology level. This fact may enforce designers to develop methodologies to design reliability systems with unreliable components or technologies.

In this course the basics and the recent developments in the most important front-end (device related) and backend (interconnect related) failure mechanisms will be discussed. The first lecture will discuss the fundamental physical understanding of two FEOL crucial reliability mechanisms: Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature instability (BTI) and the impact of high k dielectrics on these mechanisms. The second lecture will discuss how the decreasing features of the Cu and low-k interconnects affects BEOL reliability: electro-migration, stress induced voiding and TDDB of low k dielectrics. The third lecture addresses the impact of scaling and novel device architectures on the problem of Electrostatic Discharge Protection in advanced CMOS technologies. The fourth lecture addresses reliable VLSI designs using devices with reliability problems and process variations. The final lecture elaborates on yield, yield models and design for manufacturability. It presents a comprehensive study of the primary sources of variability and their effects on active devices, interconnect and ultimately product performance and yield, and develops a robust Design for Manufacturability (DFM) methodology.

Introduction and Overview
Instructor: Guido Groeseneken, IMEC

FEOL Reliability: BTI and TDDB in High k/Metal Gate, FinFET and Ge-based Technologies
Instructor : Ben Kaczer, IMEC

- Basic understanding of Time-Dependent Dielectric Breakdown (TDDB)
- Basic understanding of Bias Temperature instability (BTI)
- Impact of geometrical scaling and of high k dielectrics
- Accelerated reliability testing and reliability projection
- Reliability of scaled devices and circuits

BEOL Reliability: Metal Migration, Stress Voiding, via and Low-k Dielectric Reliability
Instructor: Shinichi Ogawa, National Institute of Advanced Industrial Science and Technology

- Cu damascene process technology reliability issues
- Impact on electromigration and stress-induced voiding
- Time-dependent dielectric breakdown (TDDB) in scaled Cu/Low-k interconnects
- Impact of process options: clean, dry etch, barrier sputtering, CMP, etc.
- Technological measures to improve reliability

Electrostatic Discharge Aspects of FinFETs and other Most Advanced CMOS Technologies
Instructor: Christian Russ, Infineon

- Overview of ESD performance of industrial IC technologies
- ESD operation and characterization of scaled FETs, gg-nMOS, SCR, diodes etc.
- ESD performance for SOI and bulk FinFET technologies and devices
- Role of strained silicon and High K dielectrics on ESD properties.
- Measures for improving ESD performance in advanced CMOS technologies

Reliability-Aware Design
Instructor: Ashraf M. Alam, Purdue University

- Impact of process variability on VLSI design
- Reliability as time-dependent variability
- Design of reliable circuits with unreliable components
- Case studies and examples

Yield, Yield Models and Design for Manufacturability
Instructor: Andrzej J. Strojwas, PDF Solutions, Inc.

- Role of random defects, systematic layout effects, parametric yield losses
- Yield models capable of predicting all significant yield loss components
- Methods for statistical process characterization, performance verification and optimization techniques
- Design for Manufacturability (DFM) methodology based on statistical optimization approaches
- Lithographic limitations in future technology nodes and the related design methodology
- Design fabric with a limited number of printability friendly patterns that enable the co-optimization of circuit, process and design for advanced CMOS

Plenary Session

Monday, December 6, 9:00 a.m.
Grand Ballroom B

Welcome and Awards

General Chair: Meikei Ieong, TSMC

Invited Papers

Technical Program Chair: Kazunari Ishimaru, Toshiba America Electronic Components, Inc.

1.1 From The Future Si Technology Perspective : Challenges and Opportunities – Kinam Kim, Samsung Advanced Institute of Technology

Recently, mobile device market is booming due to the introduction of smart phone, table PC and e-books with more advanced computing capability and connectivity. These devices require extremely low power consumption and multifunctional chips, but maintain high performance to process and mass storage to store vast amount of heterogeneous data. Current silicon technology reaches to 30 nm technology node. As silicon technology enters into below 20 nm node, new structures and materials together with new lithography will be introduced in order to continuously provide the advantages of dimensional scaling. Silicon technology will be successfully extended to beyond 10nm by employing various possible technical approaches. Also, a creative and intelligent use of silicon will benefit our society, and diverse new applications will be another growth engines for silicon industry from 2010s such as biosensor, medical imaging device, solar cell, GaN on Si LED and power device, etc. In this keynote, I would like to present several silicon based nano-electronics topics on research direction to become the first mover in these times of innovation and changes.

1.2 Energy Efficiency Enabled by Power Electronics – Arunjai Mittal, Infineon Technologies AG

Today, the biggest potential for energy saving lies in the way we use the available energy. State-of-the-art power semiconductors and electronic circuit topologies help reduce losses along the entire electrical energy chain – from energy generation to energy distribution and to consumption. E.g., converters driven by Insulated Gate Bipolar Transistors (IGBT) enable excellent grid coupling of electrical energy generated by wind or solar power plants. In motor drives, energy saving in the range of 25% to 40% can be achieved with the use of variable speed drive (VSD) technology. Lighting applications, consuming ~20% of the available electrical energy, offer energy saving potential too. The use of new microelectronic concepts, in addition to LED lighting will play a major role here. Super-junction MOSFET technology combined with silicon carbide based components and new digital power management based circuitry will help improve efficiency of power supplies above the 90% mark. Intelligent combination of energy generation sources, efficient distribution, monitoring and control of the flow of the electrical energy, will result in the development of a “Smart Grid”, once again helping us to use energy most efficiently to full-fill the growing demands on energy consumption globally.

1.3 Bionanoscience for Global Healthcare Technology - Luke P. Lee, University of California, Berkeley

It is critical time to solve the problems of current qualitative biology and medicine, as well as low-cost healthcare system. In this talk, I will discuss satellite nanoscopes, which can create molecular optogenetics for remote optical control of gene regulations and molecular imaging of living cells for understanding signaling pathways and cellular dynamics. I will also share my vision for precision cell biology and personalized medicine via Cellular BASICs* (Biologic Application Specific Integrated Circuits). Using these well-established cellular BASICs platform and nanoplasmonic optical antennae, we are developing Optofluidic Application Specific Integrated System (OASIS) for label-free bioassays and nucleic acid diagnostics. In summary, I will discuss the critical role of 21st precision nanobiology for nanomedicine and low-cost healthcare systems.

Session 2: Process Technology - Advanced 3D Integration
Monday, December 6, 1:30 p.m.
Grand Ballroom A
Co-Chairs: James J.-Q. Lu, Rensselaer Polytechnic Institute
Tanemasa Asano, Kyushu University

1:30 p.m.
Introduction

1:35 p.m.
2.1 High Density 3D Integration Using CMOS Foundry Technologies for 28 nm Node and Beyond, J.C. Lin, W.C. Chiou, K.F Yang, H.B. Chang, Y.C. Lin, E.B. Liao, J.P. Hung, Y.L. Lin, P.H. Tsai, Y.C. Shih, T.J. Wu, W.J. Wu, F.W. Tsai, Y.H. Huang, T.Y. Wang, C.L. Yu, C.H. Chang, M.F. Chen, S.Y. Hou , C. H. Tung, S.P. Jeng, C.H. Yu, TSMC

The key technology challenges as well as solutions in the development and fabrication of high-density three dimensional (3D) chip integration structures have been investigated. Key 3D IC enabling technologies, such as through silicon via (TSV), wiring and redistribution layer (RDL), wafer thinning and handling, micro-bump (m-bump) processes and joining, that form the building blocks for 3D IC technology were developed based on well developed Si foundry technologies. Test vehicles (TVs) have been designed and fabricated to develop and optimize the processes, structures, as well as to evaluate the performance, reliability and yield of the 3D integration scheme.

2:00 p.m.
2.2 Comprehensive Analysis of the Impact of Single and Arrays of Through Silicon Vias Induced Stress on High-k / Metal Gate CMOS Performances, A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos^, N. Minas, S. Domae*, D. Perry**, M. Choi, A. Redolfi, C. Okoro, Y. Yang***, J. Van Olmen, S. Thangaraju, D. Sabuncuoglu Tezcan, P. Soussan, J.H. Cho***, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, IMEC, * Panasonic, **Qualcomm, ***Samsung, ^Newcastle University

For the first time a comprehensive study is given for the stress induced by single- and arrays of TSVs and its impact on both analog and digital FEOL devices and circuits. This work provides a complete experimental assessment and quantifies the stress distribution and its effect on front end devices.

2:25 p.m.
2.3 Wafer Thinning, Bonding, and Interconnects Induced Local Strain/Stress in 3D-LSIs with Fine-Pitch High-Density Microbumps and Through-Si Vias, M. Murugesan, H. Kino, H. Nohira*, T. Tanaka, and M. Koyanagi, Tohoku University, *Tokyo City University

Locally induced stress by wafer thinning, bonding and interconnects in thinned Si substrate of 3D-LSI has been investigated. Mechanical strain/stress and crystal defects were produced in extremely thin wafers (thickness ~10 μm) of 3D-LSIs not only during wafer thinning, but also after wafer bonding using fine-pitch, high-density microbumps and curing. A local tensile strain of ~1.8 GPa was induced by 4x4 μm^2 square sized Si microbumps in 10 μm-thick Si wafers after bonding and curing. The maximum local stress of -500 MPa introduced using Si underbumps caused a 10% change in the drain current of pMOS transistor. The induced stress by CuSn interconnects penetrates deeper for larger bump size and wider for smaller bump pitch.

2:50 p.m.
2.4 Reliability and Structural Design of a Wafer-Level 3D Integration Scheme with W TSVs Based on Cu-Oxide Hybrid Wafer Bonding, K. N. Chen*, T. M. Shaw, C. Cabral, Jr., and G. Zuo, National Chiao Tung University*, IBM TJ Watson Research Center

We demonstrate a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding. Hybrid Cu-oxide hybrid bonding shows excellent bond quality and reliability. Excellent performances of initial reliability and quality evaluations for Cu-oxide hybrid bonding are key milestones in proving manufacturability of 3D integration technology.

3:15 p.m.
2.5 Ultra-Thin Chip Technology for System-in-Foil Applications, E. A. Angelopoulos, M. Zimmermann, W. Appel, S. Endler, S. Ferwana, C. Harendt, T. Hoang, A. Prümm, J. N. Burghartz, IMS CHIPS
We present a new additive ultra-thin chip fabrication process down to chip thickness of 6 µm with control better than ±0.2 µm, surface topography <20 nm and excellent mechanical flexibility. Chip thickness is defined through buried cavities underneath chip areas. Chip-to-wafer attachment is via vertical anchors within the cavities.

3:40 p.m.
2.6 Engineered Substrates and 3D Integration Technology Based on Direct Bonding for Future More Moore and More than Moore Integrated Devices (Invited), L. Clavelier, C. Deguet, L. Di Cioccio, E. Augendre, A. Brugere, P. Gueguen, Y Le Tiec, H. Moriceau, M. Rabarot, T. Signamarcheix, J. Widiez, O. Faynot, F. Andrieu, O. Weber, C. Le Royer, P. Batude, L. Hutin, J.F. Damlencourt, S. Deleonibus, CEA/LETI Minatec

This paper deals with new generations of substrates and 3Dintegration techniques, based on direct bonding techniques, enabling future devices in the More Moore and in the More than Moore areas.

Session 3: CMOS Devices and Technology – Ultra-Thin Body Transistors and Device Variability
Monday, December 6, 1:30 p.m.
Grand Ballroom B
Co-Chairs: *Michael Wu, TSMC*
Ken Rim, IBM

1:30 p.m.
Introduction

1:35 p.m.
3.1 Extremely-Thin-Body InGaAs-On-Insulator MOSFETs on Si Fabricated by Direct Wafer Bonding, M. Yokoyama, R. Iida, S. H. Kim, N. Taoka,Y. Urabe*, T. Yasuda*, H. Takagi*, H. Yamada**, N. Fukuhara**, M. Hata**, M. Sugiyama, Y. Nakano, M. Takenaka, S. Takagi, University of Tokyo, *National Institute of Advanced Industrial Sceince and Technology, **Sumitomo Chemical Co., Ltd.

We have developed the extremely-thin-body 3.5- and 9-nm-thick III-V-OI <i>n</i>MOSFETs using highly doped accumulation channels with Al^2O^3 ultrathin BOX, for the first time. The double-gate operation is found to improve I_{on}/I_{off} and <i>S</i> factor even for the InGaAs-OI MOSFETs with the highly doping concentration N_D of 1 X $10^{19}cm^{-3}$.

2:00 p.m.
3.2 Planar Fully Depleted SOI Technology: A Powerful Architecture for the 20nm Node and Beyond (Invited), O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, T. Ernst and S. Deleonibus, CEA/LETI MINATEC

Recent device developments and achievements have demonstrated that planar undoped channel Fully depleted SOI devices are becoming a serious alternative to Bulk technologies for 20nm node and below. We have proven this planar option to be easier to integrate than the non planar devices like FinFET. This paper gives an overview of the main advantages provided by this technology, as well as the key challenges that need to be addressed. Electrostatic integrity, drivability, within wafer variability and scalability are addressed through silicon data (down to 18nm gate length) and TCAD analyses. Solutions to the Multiple V_T challenges and non logic devices (ESD, I/Os) are also reported.

2:25 p.m.
3.3 Anomalous Electron Mobility in Extremely-Thin SOI (ETSOI) Diffusion Layers with SOI Thickness of Less Than 10 nm and High Doping Concentration of Greater Than $1x10^{18}cm^{-3}$, Naotoshi Kadotani,Tsunaki Takahashi, Kunro Chen,Tetsuo Kodera, Shunri Oda, Ken Uchida, Tokyo Institute of Technology

This paper is the first to report carrier transport in heavily doped ETSOI diffusion layers. We found that electron mobility in heavily doped ETSOI diffusion layer is totally different from electron mobility in heavily doped bulk Si. In other words, electron mobility is enhanced in thinner ETSOI diffusion layers (T_{soi}>5nm), whereas electron mobility is degraded as dopant concentration increases when T_{soi} is 2nm.

2:50 p.m.
3.4 Work-function Engineering in Gate First Technology for Multi-V_T Dual-Gate FDSOI CMOS on UTBOX, O. Weber, F. Andrieu, J. Mazurier, M. Cassé, X. Garros, C. Leroux, F. Martin, P. Perreau, C. Fenouillet-Béranger, S. Barnola, R. Gassilloud, O. Thomas, J-P. Noel, O. Rozeau, M-A. Jaud, T. Poiroux, D. Lafond, A. Toffoli, F. Allain, C. Tabone, L. Tosti, L. Brévard, P. Lehnen #, U. Weber#, P.K. Baumann#, O. Boissiere#, W. Schwarzenbach+, K. Bourdelle+, B-Y Nguyen+, F. Bœuf*, T. Skotnicki*, and O. Faynot, CEA-LETI Minatec, *STMicroelectronics, #AIXTRON AG, +SOITEC

For the first time, we demonstrate low-V_T (V_{Tlin} ~± 0.32) nMOS and pMOS adjusted in a gate first FDSOI technology by work-function engineering of TiN/TaAlN metal gates. Especially, for low-VT pMOS, various Chemical-Vapor-Deposited TaAlN stacks with optimized Al concentration have been studied to finely tune the work-function above midgap while maintaining good reliability and mobility. Short channel performance of 500µA/µm ION and 245µA/µm IEFF at 2nA/µm I_{OFF} and V_{DD}=0.9V is reported on pMOS with a TaAlN gate. In addition, it is found that the combination of these two metal gates with either n- or p-doped ground planes below the Ultra-Thin Buried Oxide (BOX) can offer 4 different V_T from 0.32V to 0.6V for both nMOS and pMOS.

3:15 p.m.
3.5 Impact of DIBL Variability on SRAM Static Noise Margin Analyzed by DMA SRAM TEG, X. Song, M. Suzuki, T. Saraya, A. Nishida*, T. Tsunomura*, S. Kamohara*, K. Takeuchi*, S. Inaba*, T. Mogami*, T. Hiramoto, University of Tokyo, *MIRAI-Selete

The static noise margin (SNM) as well as V_{th}, g_m, body factor, and drain-induced-barrier-lowering (DIBL) in individual transistors in SRAM cells are directly measured by 16k bit device-matrix-array (DMA) SRAM TEG. It is found that, besides V_{th} variability, DIBL variability degrades SRAM stability and its V_{dd} dependence while the variability of gm and body factor has only a small effect.

3:40 p.m.
3.6 An Anomalous Correlation Between Gate Leakage Current and Threshold Voltage Fluctuation in Advanced MOSFETs, Z. Liu, P. Chang*, X. Yu*, J. Deng*, S.-J. Han, G. Shahidi, W. Haensch, K. Rim*, IBM TJ Watson Research Center, *IBM SRDC

An anomalous correlation of gate leakage and threshold voltage fluctuation in aggressively scaled MOSFETs is first revealed and analyzed by statistical technique and a new physical model is proposed. For a range of V_t, gate leakage at fixed gate and drain bias increases with V_t before it decreases at higher V_t. The behavior can be accurately modeled by a trade-off between two mechanisms (two reversed functions): V_t roll-off effect and gate leakage current density dependence on surface potential.

Session 4: Characterization, Reliability, and Yield – Front End of Line (FEOL) Reliability
Monday, December 6, 1:30 p.m.
Continental Ballroom 1-3
Co-Chairs: *Andreas Kerber, GF*
Sangwoo Pae, Intel Corporation

1:30 p.m.
Introduction

1:35 p.m.
4.1 6Å EOT $Si_{0.45}Ge_{0.55}$ pMOSFET with Optimized Reliability (V_{DD}=1V): Meeting the NBTI Lifetime Target at Ultra-Thin EOT, J. Franco, B. Kaczer, G. Eneman, J. Mitard, A. Stesmans*, V. Afanas'ev*, T.

Kauerauf, Ph.J. Roussel, M. Toledano-Luque, M. Cho, R. Degraeve, T. Grasser**, L.-Å. Ragnarsson, L. Witters, J. Tseng, S. Takeoka, W.-E. Wang, T. Y. Hoffmann, G. Groeseneken, IMEC, *KU Leuven, **TU Wien

A 6Å EOT $Si_{0.45}Ge_{0.55}$ pFET with 10 year lifetime at operating conditions (V_{DD}=1V) is demonstrated. Gate stack optimization with a high Ge fraction, a thick SiGe quantum well and a thin Si cap alleviates NBTI for ultra-thin EOT devices which implement interfacial layer scavenging. A thin Si cap has a beneficial impact on both the recoverable and the permanent component of NBTI degradation.

2:00 p.m.

4.2 An On-Chip Monitor for Statistically Significant Circuit Aging Characterization, J. Keane, W. Zhang, C. H. Kim, University of Minnesota

We implemented an on-chip system that facilitates statistical aging characterization in an array of ROSCs. Microsecond measurements and Δf resolution ranging down to 0.07% are achieved. Results show the fresh frequency and stress-induced shift are uncorrelated, both the μ and σ of that shift increase with stress, and σ/μ decreases.

2:25 p.m.

4.3 Product Drift from NBTI: Guardbanding, Circuit and Statistical Effects, A.T. Krishnan, F. Cano, C. Chancellor, V. Reddy, Z. Qi, P. Jain, J. Carulli, J. Masin, S. Zuhoski, S. Krishnan, J. Ondrusek, Texas Instruments

Circuits employing advanced performance and power management techniques (clock gating, half-cycle paths) are shown to be much moressensitive to NBTI. A stochastic guard banding model accounting for time-dependent variance, reordering effects and granularity of data is demonstrated.

2:50 p.m.

4.4 Recent Advances in Understanding the Bias Temperature Instability (Invited), T. Grasser, B. Kaczer#, W. Goes, H. Reisinger**, Th. Aichinger*, Ph. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco#, Ph. Roussel#, M. Nelheibel**, TU Wien, *KAI, **Infineon, #IMEC

3:15 p.m.

4.5 Modeling the Breakdown Statistics of Gate Dielectric Stacks Including Percolation and Progressive Breakdown, J. Sune, E.Y. Wu*, and S. Tous, Universitat Autònoma Barcelona, *IBM Microelectronics

Experiments reveal that the breakdown-related failure of high-K stack dielectrics is affected both by percolation effects and by progressive breakdown effects. A complete model for the stack failure distribution based on the cell-that includes both phenomena on equal grounds is presented and successfully applied to deal with experimental data in the presence of multiple BD events in competition.

3:40 p.m.

4.6 PBTI Mechanisms in La Containing Hf-based Oxides Assessed by Vary Fast IV Measurements, X. Garros, L. Brunet, M. Rafik*, J. Coignus, E. Vincent*, A . Bravaix**, F. Boulanger, CEA-LETI, *STMicroelectronics, **IM2NP

The paper insvestigates PBTI in La-doped Hf-based oxides for the 28nm node by an ultra fast measurement technique and by electrical modeling. Main characteristics of PBTI degradations are established and comparison with standard measurements is also provided. PBTI traps spectroscopy is finally presented.

4:05 p.m.

4.7 Abnormal Slow Recovery Characteristic of La-Doped $HfSiO_x$ N-MOSFET Bias-Temperature Instability, G.A. Du, D.S. Ang, C. J. Gu, C.M. Ng*, Nanyang Technological University, *GLOBALFOUNDRIES

We report, for the first time, an abnormal slow recovery characteristic of La-doped $HfSiO_x$ n-MOSFETs subjected to bias-temperature stress. Results show that La introduces a new degradation mechanism having much higher activation energy and slower recovery than the conventional BTI mechanism. In the high temperature regime, the new mechanism contributes significantly to n-MOSFET degradation.

Session 5: Memory Technology – Flash Memory
Monday, December 6, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: Hang-Ting Lue, Macronix
Yoshiaki Fukuzumi, Toshiba Corporation

1:30 p.m.
Introduction

1:35 p.m.
5.1 A Highly Manufacturable Integration Technology for 27nm Multi-Level NAND Flash Memory, C.-H. Lee, S.-K. Sung, S.-H. Lee, S. Park, D.-H. Jang, J. Lee, S. Choi, E. Ahn, S. Kwon, H.-C. Baek, S.-S. Cho, J. Lim, J. Shin, J. Kim, K. Shin, K. Min, B. Yong Choi, S. J. Hwang, M.l Kim, T.-H. Kim, M. Park, Y. Rah, J. Choi, K. Kim, J.-H. Choi, T.-S. Jung, Samsung Electronics Co., Ltd.

A highly manufacturable multi-level NAND flash memory with a 27nm design rule has been successfully developed for the first time. Its unit cell size is 0.00375um^2 which is the smallest ever reported. Self Aligned Double Patterning is used to improve Vth distribution. By using advanced channel doping technique, the channel junction leakage is minimized and the Vpass window is improved. The optimized doping structure and cell operation scheme are evaluated. And MLC and 3bit operation are successfully demonstrated with flash cells of 32Gb density with reasonable reliability.

2:00 p.m.
5.2 25nm 64Gb MLC NAND Technology and Scaling Challenges (Invited), K. Prall, K. Parat*, Micron Technology, *Intel Corporation

This paper describes the Intel-Micron 25nm NAND technology including the key process advances, scaling challenges, and cell electrical results. This technology is used for the manufacturing of a worlds leading edge 64Gb MLC NAND memory.

2:25 p.m.
5.3 Ultimate Scalability of TaN Metal Floating gate with Incorporation of High-k Blocking Dielectrics for Flash Memory Applications, S. Jayanti, X. Yang, R. Suri, V. Misra, North Carolina State University

We have investigated Hf based high-k layers as interpoly dielectric and TaN as metal FG for NAND Flash memory applications. Scalability of TaN FG down to 1nm thickness has been explored. We have demonstrated an excellent memory performance with window as large as 16V when combined with engineered IPD layers.

2:50 p.m.
5.4 Highly-Scaled 3.6-nm ENT Trapping Layer MONOS Device with Good Retention and Endurance, C.Y. Tsai, T.H. Lee, H. Wang*, A. Chin, National Chiao-Tung University, *Nanyang Technological Universtiy

Novel MONOS CTF, with record thinnest 3.6 nm ENT trapping layer, has a large 3.1 V 10-year extrapolated retention at 125°C and excellent 10^6 endurance at a fast 100 µs and 16 V Program/Erase. This is achieved using ion-implanted higher k trapping layer with better trapping efficiency and deeper work-function.

3:15 p.m.
5.5 A Novel BE-SONOS NAND Flash Using Non-cut Trapping Layer with Superb Reliability, C.-C. Hsieh, H.-T. Lue, K.-P. Chang, Y.-H. Hsiao, T.-H. Hsu, C.-P. Chen, Y.J. Chen, K. F. Chen, C. Lo, T. T. Han, M.S. Chen, W. P. Lu, S. Y. Wang, J. H. Liao, S. P. Hong, F. H. Hsu, T. Yang, K.-C. Chen, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd.

This work presents superb chip-level reliability of BE-SONOS charge trapping NAND Flash fabricated in both 75nm and 38nm half-pitches. Contrary to the common perception of charge lateral migration in nitride, excellent data retention was obtained by not cutting the SiN. High (100K) cycling endurance was demonstrated.

3:40 p.m.
5.6 Study of Fast Initial Charge Loss and it's Impact on the Programmed States Vt Distribution of Charge-Trapping NAND Flash, C.-P. Chen, H.-T. Lue, C.-C. Hsieh, K.-P. Chang, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd.

We report for the first time a fast initial charge loss (within 1 sec) in charge-trapping NAND devices. The impacts of fast initial charge loss are: (1) it produces a programmed state Vt offset, and (2) it broadens the Vt distribution thus threatens the MLC capability. We also propose a refill method to suppress this effect, and have successfully demonstrated tight Vt distributions in a BE-SONOS NAND test chip.

4:05 p.m.
5.7 Universal Guiding Principle for the Fabrication of Highly Scalable MONOS-Type Memories - Atomistic Recipes Based on Designing Interface Oxygen Chemical Potential-, K. Yamaguchi, A. Otake, K. Kamiya*, Y. Shigeta*, K.Shiraishi, University of Tsukuba, *University of Hyogo

We have proposed a universal guiding principle for fabricating future MONOS memories by designing SiO_2/SiN interfaces. We have proposed skilful and realistic recipes for suppressing formation of undesirable O-related defects in SiN layers by lowering the O chemical potential by inserting thin a Si layer into SiO_2 near SiO_2/SiN interfaces.

Session 6: Quantum Power and Compound Semiconductor Devices – Next Generation Digital Devices
Monday, December 6, 1:30 p.m.
Continental Ballroom 5
Co-Chairs: Mantu Hudait, Virginia Tech
Sungjoo Lee, National University of Singapore

1:30 p.m.
Introduction

1:35 p.m.
6.1 Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications, M. Radosavljevic, G. Dewey, J.M. Fastenau*, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu*, D. Lubyshev*, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, R. Chau, Intel Corporation, *IQE, Inc.

Non-planar, multi-gate InGaAs quantum well field effect transistors (QWFETs) with high-K gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation of 5nm are reported and show more enhancement-mode threshold voltage and significantly improved electrostatics with reducing transistor gate length due to stronger gate control of the channel compared to planar high-K InGaAs QWFETs.

2:00 p.m.
6.2 Self-aligned III-V MOSFETS Heterointegrated on a 200 mm Si Substrate Using an Industry Standard Process Flow, R.J.W. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W.Y. Loh, J. Oh, C.E. Smith, P. Kirsch, P. Majhi, R. Jammy, SEMATECH

We present the first demonstration of self-aligned IIII-V MOSFETs hetero-integrated on a 200 mm Si substrate and fabricated with state-of-art industry standard Si processing tools. We present statistically significant data demonstrating that III-V on Si devices can be processed on a Si line with controlled contamination, uniformity and yield while demonstrating good device performance (L_g = 500 nm, Ion = 471 uA/µm @ 1V Vcc g_m,ext = 1005 µS/um).

2:25 p.m.
6.3 Advanced Composite High-k Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors, A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ranirez, P. Schiffer, T.N. Jackson, S.E.

Mohney, J.B. Boos*, B.R. Bennett*, I. Geppert**, M. Eizenberg**, S. Datta, The Pennsylvania State University, *Naval Research Lab, **Technion - Israel Institute of Technology Universtiy

This paper demonstrates integration of composite high-k gate stack (3.3 nm Al_2O_3-1.0 nm GaSb) with mixed anion $InAs_{0.8}Sb_{0.2}$ quantum-well field effect transistor (QWFET). The composite gate stack achieves; (i) EOT of 4.2 nm with $<10^{-7}$A/cm^2 gate leakage (ii) low D_{it} interface ($\sim 1x10^{12}$/cm^2/eV) (iii) high drift μ of 3,900-5,060 cm^2/V-s at NS of $5x10^{11}$-$3x10^{12}$/cm^2. The $InAs_{0.8}Sb_{0.2}$ MOS-QWFETs with composite gate stack exhibit extrinsic (intrinsic) g_m of 334 (502) μS/μm and drive current of 380 μA/μm at V_{DS} = 0.5V for Lg=1 μm.

2:50 p.m.
6.4 Development of High-k Dielectric for Antimonides and a Sub 350ºC III-V pMOSFET Outperforming Ge, A. Nainani, T. Irisawa, Z. Yuan, Y.Sun*, T. Krishnamohan, M. Reason**, B.R. Bennett**, J.B. Boos**, M. Ancona**, Y. Nishi, K.C. Saraswat, Stanford University, *Stanford Linear Accelerator Center, **Naval Research Lab

We report development of InxGa1-xSb pMOSFETs with SS of 120mV/$_{decade}$, I_{ON}/I_{OFF}>104 & Gm,max of 140/90mS/mm, using self-aligned gate-first process. ALD Al_2O_3 with Dit of $3x10^{11}$/cm^{2}eV^{-1} and strain engineering has enabled surface(buried) channel pMOSFETs with peak μ_h of 620(910)cm^2/Vs and having over 50(100)% mobility gain on Germanium over entire sheet-charge range.

3:15 p.m.
6.5 Correlation between Channel Mobility Improvements and Negative V_{th} Shifts in III-V MISFETs: Dipole Fluctuation as New Scattering Mechanism, Y. Urabe, N. Miyata, H. Ishii, T. Itatani, T. Maeda, T. Yasuda, H. Yamada*, N. Fukuhara*, M. Hata*, M. Yokoyama**, N. Taoka**, M. Takenaka**, S. Takagi**, AIST, *Sumitomo Chemical, **The University of Tokyo

Channel mobility improvements for the InGaAs MISFETs on (111)A and (100) are associated with the dipole ordering at the Al_2O_3/InGaAs interface. For the InP MISFETs, the effects of the interface dipoles are minor, due to the contribution of Coulomb scattering and interface POx layer.

3:40 p.m.
6.6 Band-Engineered Ge-on-Si Lasers (Invited), J. Liu, X. Sun*, R. Camacho-Aguilera*, Y. Cai*, Lionel C. Kimerling, J. Michel, Dartmouth College, *MIT

We report room temperature, optically-pumped Ge-on-Si lasers with direct gap emission at 1590-1610 nm as a result of band-engineering that compensates the energy difference between direct and indirect band gaps. Room temperature direct gap electroluminescence has also been demonstrated using Ge/Si heterojunction diodes, indicating the feasibility of electrically pumped lasers.

4:05 p.m.
6.7 High Mobility Strained Germanium Quantum Well Field Effect Transistor as the P-Channel Device Option for Low Power (Vcc=0.5V) III-V CMOS Architecture, R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, Intel Corporation

We demonstrate a high mobility strained germanium p-channel QWFET for low power CMOS architecture with scaled TOXE = 14.5Å and hole mobility of 770 cm^2/V*s at n_s =$5x10^{12}$ cm^{-2}, which is 4x higher than state-of-the-art strained silicon. This suggests the Ge QWFET is a viable p-channel option for III-V CMOS.

Session 7: Displays, Sensors, and MEMS – MEMS Resonators
Monday, December 6, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Farrokh Ayazi, Georgia Tech
Christofer Hierold, ETH Zurich

1:30 p.m.

Introduction

1:35 p.m.
7.1 High-Q Torsional Mode Si Triangular Beam Resonators Encapsulated using SiGe Thin Film, Y. Naito, P. Helin*, K. Nakamura, J. De Coster*, B. Guo*, L. Haspeslagh*, K. Onishi, H.A.C. Tilmans*, Panasonic Corporation, *IMEC

This paper presents a SOI-based 20 MHz MEMS torsional resonator, wafer-level packaged using SiGe thin films, displaying a high quality factor (220,000), low motional resistance (12 kΩ) for low DC bias (1 V), which is advantageous to realize a low power consuming oscillator. The quality factor remains above 100,000 over the temperature range of -40 to +140 degree C.

2:00 p.m.
7.2 Fully Micromechanical Piezo-Thermal Oscillators, A. Rahafrooz, S. Pourkamali, Universtiy of Denver

This work presents micromechanical resonant devices capable of self-sustained oscillation without the need for supporting electronic circuitry. These oscillators with simple to fabricate fully silicon structures and frequencies as high as 6.6MHz, power consumption as low as a few mili-Watts, and output voltage amplitude as high as 825mV are demonstrated.

2:25 p.m.
7.3 Q-Boosted AlN Array-Composite Resonator with Q>10,000, L.-W. Hung, C.T.-C. Nguyen, University of California, Berkeley

Quality factors (Q's) greater than 10,000 and higher than reported for any other sputtered AlN d31-piezoelectric micromechanical resonator have been demonstrated for the first time using an energy sharing mechanical circuit that mechanically couples an electrode-equipped AlN resonator with several electrode-less ones.

2:50 p.m.
7.4 Self-Polarized Capacitive Silicon Micromechanical Resonators via Charge Trapping, A.K. Samarao, F. Ayazi, Georgia Institute of Technology

This work presents charge trapping on the silicon resonator as a viable passive turn-ON mechanism for capacitive silicon micromechanical resonators. At a polarization voltage (Vp) of 0 V on a 20 µm thick capacitive silicon bulk acoustic resonator (SiBAR), an insertion loss (I.L.) of 30.7 dB and a Q of 59,000 has been measured in vacuum at a resonance frequency of 104.81 MHz.

3:15 p.m.
7.5 Sub-100ppb/ºC Temperature Stability in Thermally Actuated High Frequency Silicon Resonators via Degenerate Phosphorous Doping and Bias Current Optimization, A.Hajjam, A. Rahafrooz, S. Pourkamali, University of Denver

In this work, we study temperature drift behavior of thermally actuated high frequency single crystalline silicon resonators and demonstrate temperature compensation of such via a combination of N-type degenerate doping and optimization of the operating bias current. Temperature compensation results for several resonators with different frequencies ranging from 3MHz to 60MHz are presented showing TCF as low -0.05ppm/ºC.

3:40 p.m.
7.6 Resonant-Body Fin-FETs with nW Power Consumption, S.T. Bartsch, D. Grogg, A. Lovera, D. Tsamados, S. Ayöz, A.M. Ionescu, EPFL

Experimental results are reported for the first time on resonant-body Fin FETs with two independent lateral gates that are operated from weak to strong inversion at resonance frequencies from 25 MHz to 70MHZ with hight quality factors of the order of 3000, enabling unique trade-off between power consumption and gain.

Session 8: Modeling and Simulation – High-Frequency and Multi-Gate Device Modeling

Monday, December 6, 1:30 p.m.
Continental Ballroom 7-9
Co-Chairs: *Shinji Odanaka, Osaka University*
Gert-Jan Smit, NXP Semiconductors

1:30 p.m.
Introduction

1:35 p.m.
8.1 Compact Modeling and Analysis of Coupling Noise Induced by Through-Silicon Vias in 3-D ICs, C. Xu, R. Suaya*, K. Banerjee, University of California, Santa Barbara, *Mentor Graphics Corporation

This work presents compact models for both cases of without and with the high conductivity buried layer in dual-well bulk CMOS, which can be employed for keep away radius estimation. A comparative analysis of the coupling noise due to TSV in both dual-well bulk CMOS and PD-SOI is presented.

2:00 p.m.
8.2 Large Signal Substrate Modeling in RF SOI Technologies, S. Parthasarathy, B. Swaminathan, A. Sundaram, R.A. Groves, R.L. Wolf, F.G. Anderson, IBM SRDC

A modeling methodology has been demonstrated for SOI substrates for use in RF front end circuits. It has been shown that the use of a varactor to model the BOX capacitor improves the harmonic distortion predictions from simulations for circuits in RF/Analog applications.

2:25 p.m.
8.3 A Surface-Potential Based Model for GaN HEMTs in RF Power Amplifier Applications, D.L. John, F. Allerstam, T. Roedle, S.K. Murad, G.D.J. Smit, NXP Semiconductors

In this work, we present the first surface-potential based compact model for RF GaN HEMTs, and benchmark our work against both numerical simulations and device measurements. It is expected that such an approach will be superior to other modeling techniques in terms of scalability and model performance for applications where accurate distortion modeling is of paramount importance.

2:50 p.m.
8.4 FinFET Compact Modelling for Analogue and RF Applications (Invited), A.J. Scholten, G.D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, A. Mercha*, and D.B.M. Klaassen, NXP-TSMC Research Center, *IMEC

We derive a new compact expression for the effective FinFET gate resistance and validate it on
experimental data. Moreover, a model for FinFET thermal noise is presented, which predicts measured data accurately. It is demonstrated that the observed increase of drain current noise with drain-source voltage is not due to microscopic excess noise, but to the access resistances which modify the transfer of channel thermal noise to the terminals.

3:15 p.m.
8.5 MuGFET Carrier Mobility and Velocity: Impacts of Fin Aspect Ratio, Orientation and Stress, N. Xu, X. Sun, W. Xiong*, C. R. Cleavelin, T.-J. King Liu, University of California, Berkeley, *Texas Instruments Incorporated

A detailed study of the impacts of fin aspect ratio and crystalline orientation and process-induced channel stress on the performance of multi-gate transistors is presented. It is found that CESL-induced stress provides for the greatest enhancement in carrier mobility and ballistic velocity, for n- and p-channel FinFETs and Tri-Gate FET structures. Extracted carrier velocity values in short-channel FinFETs still largely depend on carrier mobility.

3:40 p.m.
8.6 Phonon-Limited Mobility and Injection Velocity in n- and p-doped Ultrascaled Nanowire Field-Effect Transistors with Different Crystal Orientations, M. Luisier, Purdue University

In this paper the performances of Si NW FETs in the presence of electron-phonon scattering are investigated using a quantum transport solver. Two important device metrics, the low-field mobility and the injection velocity are computed and analyzed in n- and p-doped NW FETs with [100], [110], and [111] transport.

4:05p.m.
8.7 Beating the Nernst Limit of 59mV/pH with Double-Gated Nano-Scale Field-Effect Transistors and Its Applications to Ultra-Sensitive DNA Biosensors, J. Go, Pradeep R. Nair, B. Reddy Jr.*, B. Dorvel*, R. Bashir*, M.A. Alam, Purdue University, *University of Illinois at Urbana Champaigne

We have demonstrated that extraordinary high pH sensitivity (far above the Nernst limit) can be achieved with DGFET device and this sensitivity gain can be used to counteract the screening limits of DNA detection. Back gate operation shows signal amplification due to its asymmetric thickness of top/back oxide.

Session 9: Solid-State and Nanoelectronic Devices – CNT, MTJ, Devices and Nanowire Photodiodes
Monday, December 6, 1:30 p.m.
Imperial Ballroom
Co-Chairs: Ru Huang, Peking University
Fu-liang Yang, National Nano Device Laboratories

1:30 p.m.
Introduction

1:35p.m.
9.1 Wafer Scale Fabrication of Carbon Nanotube FETs with Embedded Poly-Gates, S.-J. Han, J. Chang, A.D. Franklin, A.A. Bol, R. Loesing*, D. Guo, G.S. Tulevski, W. Haensch, Z. Chen, IBM TJ Watson Research Center, *IBM SRDC

We report for the first time a wafer-scale fabrication of high performance CNFETs using an 8” production line. A novel embedded poly-Si gate structure is employed to provide excellent electrostatics in the devices and the compatibilities with CMOS processes. In addition, the first-ever measured CNFET threshold tuning through poly-Si gate doping is presented.

2:00 p.m.
9.2 Graphitic Interfacial Layer to Carbon Nanotube for Low Electrical Contact Resistance, Y. Chai, A. Hazeghi, K. Takei**, H.-Y. Chen, P.C. H. Chan*, A. Javey**, H.-S. P. Wong, Stanford University, *Hong Kong University of Science and Technology, **University of California, Berkeley

We used graphitic interfacial layer to improve the electrical contact between metal and metallic CNT. The average resistance of the CNT is lowered to 15% of the value of the same contact without the graphitic layer. Effective barrier height is reduced from 204meV to 36meV by introducing the graphitic layer.

2:25 p.m.
9.3 Resistive Switching of Carbon-Based RRAM with CNT Electrodes for Ultra-Dense Memory, Y. Chai, Y. Wu, K. Takei**, H.-Y. Chen, S. Yu, P.C.H. Chan*, A. Javey**, H.-S. P. Wong, Stanford University, *Hong Kong University of Science and Technology, **University of California, Berkeley

We successfully demonstrated carbon-based RRAM with CNT electrodes for ultra-dense memory. The use of CNT as electrode leads to the ultimately scaled cross-point area (~1 nm^2) and the use of a-C enable an all-carbon memory. Carbon-based CRS is shown for the first time, enabling cross-point memory without cell selection devices.

2:50 p.m.
9.4 Magnetic Tunnel Junction for Nonvolatile CMOS Logic (Invited), H. Ohno, Tohoku University

Magnetic tunnel junction (MTJ) is a nonvolatile memory capable of fast-read/write with high endurance together with back-end-of-the-line compatibility, offering a possibility of constructing low-power high-performance nonvolatile CMOS logic employing logic-in-memory architecture. Current status of the MTJ technology and the nonvolatile CMOS/MTJ logic circuits together with prospects are presented.

3:15 p.m.
9.5 Cost-efficient Fabrication of UV/Vis Nanowire Photodiodes Enabled by ZnO/Si Radial Heterojunction, H.-D. Um, K.-T. Park, J.-Y. Jung, S.-W. Jee, S.A. Moiz, C. H. Ahn*, H.K. Cho*, E. Lee**, D.-W. Kim**, J.-H. Lee, Hanyang University, *Sungkyunkwan University, **Ewha Womans University

Radial heterojunction nanowires using a ZnO(shell)/Si(core) coaxial structure are for the first time reported for a novel photodiode application. Strong antireflective characteristics are shown by employing a vertically aligned Si nanowire. A thin ZnO shell deposited onto a Si nanowire formed a radial junction which enabled effective separation of charge carriers. Our coaxial ZnO/Si nanowire photodetectors suggest bright prospect for enhancing a photoresponsivity while less consuming ZnO via controlling the wired nanostructure.

Session 10: CMOS Devices and Technology – CMOS Performance Enhancing and Novel Devices
Tuesday, December 7, 9:00 a.m.
Grand Ballroom A
Co-Chairs: *Michel Haond, STMicroelectronics*
Rusty Harris, Texas A&M University
9:00 a.m.
Introduction

9:05 a.m.
10.1 Novel Stress-Memorization-Technology (SMT) for High Electron Mobility Enhancement of Gate Last High-k/Metal Gate Devices, K.-Y. Lim, H.-J. Lee, C.R. Ryu, K.-I. Seo, U.H. Kwon, S.H. Kim, J.W. Choi, K.S. Oh, H.K. Jeon, C.G. Song, T.W. Kwon, J.Y. Cho , S.H. Lee, Y.S. Sohn, H.S. Yoon, K.H. Lee, J.H. Park, W.J. Kim, S.P. Sim, C.G. Koh, S.B. Kang, S.Y. Choi, C.H. Chung, Samsung Electronics Co.

Gate last high-k/metal gate compatible Source/Drain (S/D) stress-memorization-technology (SMT) is presented. Channel stress is simulated by using mask-edge dislocation model and actual stress is also measured by Raman spectroscopy. Extremely deep pre-amorphization-implant for SMT enhances short-channel electron mobility by 40~60%. More than 10% short channel drive current gain is achieved.

9:30 a.m.
10.2 CxFET: A Novel Steep Subthreshold Swing CMOS Featuring a Tunnel-Injection Bipolar Transistor and MOSFET Device Complex, D. Hisamoto, S. Saito*, A. Shima*, H.i Yoshimoto*, K. Torii*, E. Takeda, Hitachi Research Institute, *Hitachi Ltd.

MOSFET (CxFET) that enabled a steeper subthreshold swing was developed. Multiple devices were able to be successfully integrated in a single scaled MOSFET. Applying an enhanced input signal, Vg, to the tunnel junction, stimulated tunneling carrier injection, which resulted in a steep subthreshold swing.

9:55 a.m.
10.3 A Phase-Change via-Reconfigurable On-Chip Inductor, C.-Y. Wen, E. K. Chua, R. Zhao*, C.T. Chong*, J.A. Bain, T.E. Schlesinger, L. Pileggi, J. Paramesh, Carnegie Mellon University, *Data Storage Institute

This paper describes a new approach to the realization of reconfigurable CMOS-compatible RF inductors using phase-change vias. Reversible reconfiguration of a custom-fabricated inductor prototype is demonstrated by using voltage pulses to transform the phase-change switch between ON and OFF states. The RF performance shows a 110% inductance change with quality factors (OFF) (ON) of 12.4 (5.8).

10:20 a.m.
10.4 Implant-Free SiGe Quantum Well pFET: A Novel, Highly Scalable and Low Thermal Budget Device, Featuring Raised Source/Drain & High-Mobility Channel, G. Hellings, L. Witters, R. Krom, J. Mitard, A.

Hikavyy, R. Loo, A. Schulze, G. Eneman, C. Kerner, J. Franco, T. Chiarella, S. Takeoka, J. Tseng, W.Wang, W. Vandervorst, P. Absil, S. Biesemans, M. Heyns, K. De Meyer, M. Meuris, T. Hoffmann, IMEC

A novel bulk-Si based pMOSFET structure is presented featuring a high-mobility $SiGe_{0.45}$ channel and raised $SiGe_{0.25}$ source/drains. This device offers enhanced scalability with respect to standard pMOS devices, leading to 50% improved drive current. 30nm gate length devices show a high drive current 582 µA/µm at I_{OFF}=100 nA/µm, DIBL=126mV/V, SS=80mV/dec, showing superior electro- statics without halo implants. Finally, the compatibility with additional strain-boosters is demonstrated.

10:45 a.m.
10.5 High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond $1x10^{20}$ cm^{-3}, G. Thareja, J. Liang, S. Chopra*, B. Adams*, N. Patil, S.-L. Cheng, A. Nainani, E. Tasyurek, Y. Kim*, S. Moffatt*, R. Brennan**, J. McVittie, T. Kamins, K. Saraswat, Y. Nishi, Stanford University, *Applied Materials, Inc., **Solecon Laboratories

For the first time, high performance Ge nMOSFET is fabricated using laser annealing of ion-implanted antimony (Sb) dopants which provides donor activation beyond $1x10^{20}cm^{-3}$ in germanium. Record $I_{on}/I_{off} > 10^5$ is demonstrated for n+/p junctions combined with significant reduction of contact resistance to $7x10^{-7}$ Ω-cm^2. Performance projections for ITRS HP 22nm technology node are also discussed.

11:10 a.m.
10.6 High-Mobility 0.85nm-EOT $Si_{0.45}Ge_{0.55}$ pFETs: Delivering High Performance at Scaled VDD, J. Mitard, L. Witters, M. Garcia Bardon, P. Christie, J. Franco, A. Mercha, P. Magnone*, M. Alioto**, F. Crupii*, L.-Å. Ragnarsson, A. Hikavyy, B. Vincent, T. Chiarella, R. Loo, J. Tseng, S. Yamaguchi, S. Takeoka, W-E. Wang, P. Absil, T. Hoffmann, IMEC, *Università della Calabria, **Università di Siena

This work demonstrates the successful integration of 0.85nm-EOT $SiGe_{0.55}$ pFETs using a gate first approach. An in-depth analysis, ranging from capacitor-level up to circuit-level is carried out, with systematic benchmarking to a conventional Si-channel reference. Outperforming the state-of-the-art $Si_{0.55}Ge_{0.45}$ pFETs, an ION of 630µA/µm at L_{G_poly}=35nm with I_{OFF}=100nA/µm and V_{DD}=-1V has been achieved without any epi-S/D boosters. Significant improvements at lower VDD have also been confirmed through complex circuit simulations and validated by experimental results.

Session 11: Process Technology - Channel Engineering and High-k Technology
Tuesday, December 7, 9:00 a.m.
Continental Ballroom 1-3
Co-Chairs: Kaori Tai, Sony Semiconductor Kyushu Corporation
Nicolas Planes, STMicroelectronics

9:00 a.m.
Introduction

9:05 a.m.
11.1 Dual Strained Channel Co-Integration into CMOS, RO and SRAM Cells on FDSOI Down to 17nm Gate Length, L. Hutin, C. Le Royer, F. Andrieu, O. Weber, M. Cassé, J.-M. Hartmann, D. Cooper, A. Béché*, L. Brevard, L. Brunet, J. Cluzel, P. Batude, M. Vinet, O. Faynot, CEA LETI Minatec, CEA INAC

We hereby present for the first time a successful Dual Strained Channel On Insulator (DSCOI) planar co-integration of tensily strained SOI nFETs and compressively strained SiGe pFETs down to 17nm gate length with functional ring oscillators and 6T SRAM cells.

9:30 a.m.
11.2 A Solution for an Ideal Planar Multi-Gates Process for Ultimate CMOS?, S. Monfray, J.-L. Huguenin, M. Martin*, M.-P. Samson, C. Borowiak, C. Arvet, JF. Dalemcourt*, P. Perreau*, Y. Campidelli, S. Barnola*, G. Bidal, S. Denorme, Y. Campidelli, K. Benotmane*, F. Leverd, P. Gouraud, B. Le-Gratiet, C. De-Butet*, L. Pinzelli,

R. Beneyton, T. Morel, R.Wacquez*, J. Bustos, B. Icard*, L. Pain*, S. Barraud*, T. Ernst*, F. Boeuf, O. Faynot*, T. Skotnicki, STMicroelectronics, *CEA LETI Minatec

We demonstrate for the first time high-performant planar multi-gates devices with Si-conduction channel of 4nm, allowing drive current up to 1350µA/µm @I_{off}=0.4nA/µm. We also demonstrate in this paper an ideal planar self-aligned solution, based on the direct exposure of a HSQ layer through a 5nm Si-channel. This opens the way to an easy planar multi-gate process for ultimate CMOS, fully co-integrable with conventional devices.

9:55 a.m.
11.3 Diamond-Like Carbon (DLC) Liner with Highly Compressive Stress Formed on AlGaN/GaN MOS-HEMTs with In Situ Silane Surface Passivation for Performance Enhancement, X. Liu, B. Liu, E. K. F. Low, H.-C. Chin, W. Liu*, M. Yang**, L. S. Tan, Y.-C. Yeo, University of Singapore (NUS), *Institute of Materials Research and Engineering, **Data Storage Institute

We report the first demonstration of AlGaN/GaN MOS-HEMTs enhanced by DLC liner with high compressive stress. I_D,SAT enhancement (V_G = 2 V and V_D = 10 V) of up to 30 % and peak transconductance (V_D = 5 V) increase of 22 % were obtained for DLC strained devices with L_G of less than 500 nm. Positive Vth shift of ~1 V shows the potential of realizing enhancement mode AlGaN/GaN HEMTs with strain engineering.

10:20 a.m.
11.4 Physical Origin of pFET Threshold Voltage Modulation by Ge Channel Ion Implantation (GC-I/I), Y. Tsuchiya, N. Berliner*, R. Iijima, F. Monsieur**, L. Tai^, N. Loubet**, L. F. Edge*, M. Takayanagi, and V. Paruchuri*, Toshiba America Electronic Components, Inc., *IBM Research at Albany Nanotech, **STMicroelectronics, ^IBM SRDC

We show a new Ge channel ion implantation (GC-I/I) scheme for realization of low V_{TH} pFET. GC-I/I enables ~500mV V_{TH} lowering with no Tinv, GIDL and NBTI degradations. We also reveal the physical origin of the large V_{TH} modulation. Based on experimental findings, we propose simplified photo-resist masked dual low-V_{TH} CMOS flow and demonstrate low-V_{TH} pFET/nFET operations.

10:45 a.m.
11.5 Preparation of Epitaxial HfO_2 Film (EOT=0.5 nm) on Si Substrate Using Atomic-Layer Deposition of Amorphous Film and Rapid Thermal Crystallization (RTC) in an Abrupt Temperature Gradient, S. Migita, Y. Morita, W. Mizubayashi, H. Ota, National Institute of Advanced Industrial Science and Technology

We present an epitaxial growth technique of HfO_2 films on Si using atomic-layer deposition and rapid thermal crystallization (RTC). The RTC produces an abrupt temperature gradient in amorphous HfO_2 film and initiates epitaxial crystallization from Si interface. Using the RTC, 0.50 nm EOT with 1.03 A/cm^2 is achieved.

11:10 a.m.
11.6 A Novel Multi Deposition Multi Room-Temperature Annealing Technique via Ultraviolet-Ozone to Improve High-K/Metal (HfZrO/TiN) Gate Stack Integrity for a Gate-Last Process, L. Wu, W.J. Liu, K.S. Yew, D.S. Ang, T.T. Le, T.L. Duan, C.H. Hou*, X.F. Yu*, D.Y. Lee*, K.Y. Hsu*, J. Xu*, H.J. Tao*, M. Cao*, H.Y. Yu, Nanyang Technological University, *TSMC

ALD HfZrO high-K fabricated by novel multi deposition multi annealing (MDMA) technique at room temperature in UVO is systematically investigated for the first time via both physical and electrical characterization for gate last process. As compared to the reference gate stack treated by conventional rapid thermal annealing (with PVD TiN electrode), the devices receiving MDMA in UVO demonstrates: 1) more than one order of magnitude leakage reduction; 2) much improved stress induced degradation; 3) enhanced dielectrics break-down strength and TDDB. STM and XPS analysis suggest both oxygen vacancies (Vo) and grain boundaries suppression in the MDMA treated samples are likely responsible for the device improvement.

Session 12: Memory Technology – IT and Magnetic RAM
Tuesday, December 7, 9:00 a.m.
Continental Ballroom 4

Co-Chairs: Agostino Pirovano, Micron Technology
Rajeev Malik, IBM

9:00 a.m.
Introduction

9:05 a.m.
12.1 32nm High-density High-speed T-RAM Embedded Memory Technology, R. Gupta, F. Nemati, S. Robins, K. Yang, V. Gopalakrishnan, J.J. Sundarraj, R. Chopra, R. Roy, H.-J. Cho, W.P. Maszara, N.R. Mohapatra, J. Wuu, D. Weiss, S. Nakib, T-RAM Semiconductor

T-RAM technology with substantially better density-performance tradeoff than conventional 6T-SRAM and DRAM was previously reported at the 130nm technology node. Details of implementation in a 32nm HKMG SOI CMOS logic process, with read and write times of 1ns and bit fail rate under 0.5ppm are reported here for the first time.

9:30 a.m.
12.2 Ultimately Scaled 20nm Unified-RAM, D.-I. Moon, S.-J. Choi, C.-J. Kim, J.-Y. Kim, J.-S. Lee, J.-S. Oh*, Gi-Sung Lee*, Yun-Chang Park*, Dae-Won Hong*, D.-W. Lee*, Y.-S. Kim*, J.-W. Kim*, J.-W. Han, Y.-K. Choi, KAIST, *National Nanofab Center
A 20 nm all-around-gate FET is demonstrated for unified-RAM by the use of an 8 nm Si-nanowire on the bulk-substrate. High performances of non-volatile memory and 1T-DRAM are presented.

9:55 a.m.
12.3 A Novel Low-Voltage Biasing Scheme for Double Gate FBC Achieving 5s Retention and 1e16 Endurance at 85ºC, Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, W. Schwarzenbach*, O. Bonnin*, K. K.Bourdelle*, B.-Y. Nguyen*, C. Mazure*, L. Altimime, M. Jurczak, IMEC, *SOITEC

A novel low-voltage biasing scheme on ultra-thin BOX FDSOI floating body cell is experimentally demonstrated. The new biasing scheme enhances the positive feedback loop. Therefore, the required VDS can be reduced to 1.5V while 5 seconds retention time can still be achieved at 85ºC. Endurance up to 10^{16} cycles is shown.

10:20 a.m.
12.4 Memory Technology Trends and Future Challenges (Invited), S. Hong, Hynix Semiconductor, Inc.

Challenges in scaling semiconductor memory technologies are reviewed with special focus on DRAM and NAND Flash where technology scaling-down is at risk below 20nm. Some recent progress on overcoming scaling challenges of current and new memory technologies are introduced as well as some of the possible technology replacements are reviewed.

10:45 a.m.
12.5 Switching Distributions and Write Reliability of Perpendicular Spin Torque MRAM, D.C. Worledge, G. Hu, P.L. Trouilloud, D.W. Abraham, S. Brown, M.C. Gaidis, J. Nowak, E. J. O'Sullivan, R.P. Robertazzi, J. Z. Sun, and W.J. Gallagher, IBM TJ Watson Research Center

We report data from 4-kbit spin torque MRAM arrays using tunnel junctions with magnetization perpendicular to the wafer plane. We show for the first time the switching distribution of perpendicular spin torque junctions, $std(V_c)/V_c = 4.4\%$, sufficient to yield a 64 Mb chip. Furthermore we report switching probability curves down to error probabilities of $5x10^{-9}$ per pulse which do not show the anomalous switching seen in previous studies of in-plane magnetized bits.

11:10 a.m.
12.6 On-Axis Scheme and Novel MTJ Structure for Sub-30nm Gb Density STT-MRAM, S.C. Oh, J.H. Jeong, W.C. Lim, W.J. Kim, Y.H. Kim, H.J. Shin, J.E. Lee, Y.G. Shin, S. Choi and C. Chung, Samsung Electronics Co., Ltd.

Feasibility of STT-MRAM as next generation non-volatile memory has been tested for the replacement of DRAM and NOR. For competition with DRAM, STT-MRAM unit cell size should be reduced to 6 ~ $8F^2$ and switching current density is required to be less than 1 MA/cm^2. Here, we report that the cell characteristics of on-axis STT-MRAM with 6 ~ $8F^2$ are similar to those of the off-axis STT-MRAM with 12 ~ $16F^2$. In addition, we suggest a novel MTJ with the operation current density of 0.8 MA/cm^2. These results open a way to scale STT-MRAM down to sub-30 nm node using present technology. By further material engineering of ferromagnetic electrode and MTJ structure design, the usage of present technology could be extended down to sub-20 nm node.

11:35 a.m.
12.7 Fully Integrated 54nm STT-RAM with the Smallest Bit Cell Dimension for High Density Memory Application, S.-O. Chung, G.-M. Rho, S.-D. Kim, H.-J. Suh, D.-J. Kim, H.-J. Kim, S.-H. Lee, J.-H. Park, H.-M. Hwang, Y.-B. Ahn, Y.-H.Seo, D.-H. Jung, M.-S. Lee, S.-H. Cho, J.-N. Kim, G.-J. Park, G.-A. Jin, A. Drilskill-Smith*, V. Nikitin*, A. Ong*, X.Tang*, Y.-G.Kim, J.-S. Rho, S.-K.Park, S.-W. Chung, J.-G.Jeong, S.-J. Hong, Hynix Semiconductor, Inc., *Grandis, Inc.

To compete with existing memories, the emerging memory should have a comparable unit cell dimension. We demonstrated tthe 64Mbit STT-RAM technology with a $14F^2$ cell at the 54nm node. The compact cell can provide a large enough current drivability and also a stable MTJ performance.

Session 13: Emerging Technologies – Next Generation Power Devices and Technology
Tuesday, December 7, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: Tahir Ghani, Intel Corporation

9:00 a.m.
Introduction

9:05 a.m.
13.1 Current Status and Future Trends in Silicon Power Devices (Invited), Philip Hower, Sameer Pendharkar, Taylor Efland, Texas Instruments

9:30 a.m.
13.2 AlGaN/GaN Transistors for Power Electronics (Invited), Umesh Mishra, University of California, Santa Barbara

9:55 a.m.
13.3 Silicon Carbide based Power Devices (Invited), Mikael Ostling, TranSiC

10:20 a.m.
13.4 Ultra High Voltage Semiconductor Power Devices for Grid Applications (Invited), Munaf Rahimo, ABB

10:45 a.m.
13.5 Advanced SiC and GaN Power Electronics for Automotive Systems (Invited), Masakazu Kanechika, Tsutomu Uesugi, Tetsu Kachi, Toyota Central R&D Labs

11:10 a.m.
13.6 Advanced Power Devices for Many-core Processor Power Supploes (Invited), Michael Briere, Consultant

Session 14: Displays, Sensors, and MEMS – Image Sensors
Tuesday, December 7, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: *Daniel McGrath, Aptina Imaging*
Yoshiaru Kudoh, Sony Corporation

9:00 a.m.
Introduction

9:05 a.m.
14.1 A Leading-Edge 0.9um Pixel CMOS Image Sensor Technology with Backside Illumination: Future Challenges for Pixel Scaling (Invited), S.G. Wuu, C.C. Wang, B.C. Hseih, Y.L. Tu, C.H. Tseng, T.H. Hsu, R.S. Hsiao, S. Takahashi, R.J. Lin, C.S. Tsai, Y.P. Chao, K.Y. Chou, P.S. Chou, H.Y. Tu, L.Tran,

In this paper, a leading edge N65 0.9um pixel BSI technology using 300mm bulk silicon wafer is reported with process breakthroughs. Challenges to go beyond <0.9um pixel size are discussed.

9:30 a.m.
14.2 A 3x3, 5µm pitch, 3-transistor Single Photon Avalanche Diode Array with Integrated 11V Bias Generation in 90nm CMOS Technology, R.K. Henderson, E.A.G. Webster, R. Walker, J.A. Richardson*, L.A. Grant*, University of Edinburgh, *STMicroelectronics

A 3x3 prototype image sensor array of CMOS avalanche photodiodes with 3-transistor NMOS pixel circuitry is integrated in a 90nm CMOS image sensor technology. A 5um pixel pitch is obtained with <1% crosstalk, 170Hz mean dark count rate at 20C, 36% photon detection efficiency at 410nm and 107ps FWHM jitter.

9:55 a.m.
14.3 A Miniature Actively Recharged Single-Photon Detector Free of Afterpulsing Effects with 6ns Dead Time in a 0.18µm CMOS Technology, C. Niclass, M. Soga, Toyota Central Research and Development Labs, Inc.

A CMOS single-photon detector, including a highly miniaturized active recharge circuit, achieving the highest counting rate yet reported for an afterpulsing-free Geiger-mode photodiode is introduced. Thanks to its low-noise and 6-ns dead time figure, a dynamic-range of 116dB for steady-state photon counting in a single acquisition time of 20ms was achieved.

10:20 a.m.
14.4 A Low Dark Current and High Quantum Efficiency Monolithic Germanium-on-Silicon CMOS Imager Technology for Day and Night Imaging Applications, I. Aberg, B. Ackland, J.V. Beach, C. Godek, R. Johnson, C.A. King, A. Lattes, J. O'Neill, S. Pappas, T.S. Sriram, C.S. Rafferty, NoblePeak Vision Corporation

A low noise, high quantum efficiency Ge photo-diode was integrated in a 10 µm pitch video graphics array CMOS image sensor, the first large-scale integration of single crystal Ge into a silicon product. Night imaging in moonless conditions was demonstrated in this technology for the first time.

10:45 a.m.
14.5 10 µm Pixel-to-Pixel Pitch Hybrid Backside Illuminated AlGaN-on-Si Imagers for Solar Blind EUV Radiation Detection, P.E. Malinowski, J.Y. Duboz*, P. De Moor, J. John, K. Minoglou, P. Srivastava, Y. Creten, T. Torfs, J. Putzeys, F. Semond*, E. Frayssinet*, B. Giordanengo**, A. BenMoussa**, J. F. Hochedez**, R. Mertens, C. Van Hoof, IMEC, *CRHEA-CNRS, **Royal Observatory of Belgium

We present state-of-the-art 10 µm pixel pitch hybrid AlGaN-on-Si EUV imagers. 256x256 backside illuminated Focal Plane Arrays were integrated with dedicated CMOS readouts. The AlGaN active layer provides intrinsic solar blindness with 280 nm cut-off wavelength. Sensitivity was verified using synchrotron radiation down to 1 nm wavelength.

11:10 a.m.
14.6 Efficiency Enhancement and Polarization Detection Capability of Photodiode by Accumulating Local Electric Field on the Metal Electrodes, Y.-S. Lai, H.-L. Chen*, C.H. Lin**, H.M. Chang*, S.C. Tseng*, Y.M. Chi*, C.Ho, F.-L. Yang, National Nano Device Laboratories, *National Taiwan University, **National Cheng Kung University

By chiral-shape patterns over finger-type electrodes of conventional photodiode, for the first time, record high >80% external quantum efficiency (EQE) and polarization detection capability are successfully achieved simultaneously through the self-accumulated local electric field due to strong local surface plasmon resonance (LSPR). Device has expected high efficiency to absorb the incident visible energy profiting the visible applications potentially.

Session 15: Modeling and Simulation – Challenges in Advanced Device Performance and Variation Modeling
Tuesday, December 7, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: Martin Giles, Intel Corporation
Fabrizio Bonani, Politecnico Di Torino

9:00 a.m.
Introduction

9:05 a.m.
15.1 Transfer of Physically-Based Models from Process to Device Simulations: Application to Advanced Strained Si/SiGe MOSFETs, E.M. Bazizi, P.F. Fazzini, F. Cristiano, A. Pakfar*, C. Tavernier*, F. Payet*, T. Skotnicki*, C. Zechner**, N. Zographos**, D. Matveev**, N.E.B. Cowern^, N.S. Bennett^, C. Ahn^, J.C. Yoon^, CNRS-LAAS, *STMicroelectronics, **Synopsys Switzerland LLC, ^Newcastle University

Integrated process and device simulations were used to predict sub-45nm Strained-Si/$Si_{0.8}Ge_{0.2}$ device performance. Physically-based process models, generalized from Si to strained-Si and SiGe, describe dopant implantation and diffusion, including amorphization, defect interactions and evolution, as well as dopant-defect interactions. The models are used within a unique simulation tool to reproduce the
electrical characteristics of Si/SiGe devices.

9:30 a.m.
15.2 Simulation Study of the on-current Improvements in Ge and sGe versus Si and sSi nano MOSFETs, F. Conzatti, P. Toniutti, D. Esseni, P. Palestri, L. Selmi, DIEGM-UNET

A comprehensive semiclassical transport model for n/p inversion layers in strained channels is used to analyze the competitive edge of Ge/sGe n/pMOSFETs wrt their Si/sSi counterparts. Results suggest that unstrained Ge devices exhibit a too limited margin wrt sSi transistors to justify their introduction in CMOS technology.
9:55 a.m.
15.3 TCAD: Present State and Future Challenges, T. Ma, V. Moroz, R. Borges, L. Smith, Synopsys, Inc.

Since the advent of computer modeling of semiconductor processes and devices in the 1970s, Technology Computer-Aided Design (TCAD) has been an integral part of technology development over the past four decades. Today, the use of TCAD has become widespread not only for "More Moore," but also "More Than Moore" technologies. As process and device complexity continues to rise, so does the complexity in technology modeling. This paper discusses the present state and future challenges of front-end process and device modeling.

10:20 a.m.
15.4 Electrical Modulation of Ion Concentration in Dual-Gated Nanochannels, Y. Liu, R.W. Dutton, Stanford University

Coupled Poisson-Nernst-Planck and Stokes simulations demonstrate the operation principle of using electrical bias control in dual-gated nanochannels to create solution zones of depleted or accumulated ions. Such ionic modulation completely overcomes the screening limit (channel width ~60X the Debye length), revealing a novel mechanism for electrically-tunable biological sample preparation and desalination.

10:45 a.m.
15.5 Theory of Workfunction Control of Silicides by Doping for Future Si-Nano-Devices Based on Fundamental Physics of why Silicides Exist in Nature, T. Nakayama, K. Kakushima*, O. Nakatsuka**, Y.

Machida, S. Sotome, T. Matsuki^, K. Ohmori^, H. Iwai*, S. Zaima**, T. Chikyow^^, K. Shiraishi#, K. Yamada#, National Chiao Tung University, *Tokyo Institute of Technology, **Negoya University, ^Waseda University, ^^NIMS, #University of Tsukuba

We have revealed by the first-principles calculations that the workfunction of siliide is controlled by the dopant not segregated at the silicide/Si interface but in the silicide, and the control of doping sites is essential to realize desired workfunction. These findings give guidelines to design silicide-based nanocontacts in future devices.

11:10 a.m.
15.6 3D Device Simulation of Work-Function and Interface Trap Fluctuations on High-k/Metal Gate Devices, M.-H. Han, C.-Y. Yiu, C.-H. Yu, K.-F. Lee, Y. Li, National Chiao Tung University

We study the WKF and ITF using 3D device simulation on high-k/metal gate technology. Statistically, WKF and ITF are correlated by each other and should be counted simultaneously. The WKF induced sVth, based on our simulation, explains position-dependent local work-functions effect successfully which is beyond the AWF and compact methods.

11:35 a.m.
15.7 Analysis of Pocket Profile Deactivation and its Impact on Vth Variation for Laser Annealed Device using an Atomistic Kinetic Monte Carlo Approach, T. Noda, W. Vandervorst*, C. Vrancken*, C. Ortolland*, E. Rosseel*, P.P. Absil*, S. Biesemans*, T.Y. Hoffmann*, Panasonic Coporation, *IMEC

An analysis of pocket profile deactivation and its impact on Vth variation for Laser annealed device using an atomistic kinetic Monte Carlo (KMC) approach are shown. Carbon co-implant impact on pFET extension/pocket is also modeled using an atomistic KMC. KMC clarified that although B-pocket in nFET shows significant deactivation, As-pocket in pFET does not show deactivation with thermal budget scaling. The difference of pocket deactivation is one of important reason for higher Vth mismatch for nFET than for pFET.

Session 16: Solid-State and Nanoelectronic Devices – Low-Power and Steep Slope Switching Devices
Tuesday, December 7, 9:00 a.m.
Imperial Ballroom
Co-Chairs: *Steven J. Koester, University of Minnesota- Twin Cities*
Thomas Ernst, CEA-LETI

9:00 a.m.
Introduction
9:05 a.m.
16.1 Prospect of Tunneling Green Transistor for 0.1V CMOS (Invited), C. Hu, P. Patel, A. Bowonder, K. Jeon, S.H. Kim, W.Y. Loh*, C.Y. Kang*, J. Oh*, P. Majhi*, A. Javey, T.-J. King Liu, R. Jammy*, University of California, Berkeley, *International Sematech

9:30 a.m.
16.2 Performance Benchmarks for Si, III-V, TFET, and Carbon Nanotube FET -- Re-thinking the Technology Assessment Methodology for Complementary Logic Applications, L. Wei, S. Oh, H.-S.P. Wong, Stanford University

We present a new device technology assessment methodology based on energy-delay optimization which treats I_{off} and V_{dd} as “free variables”, and bounded by constraints due to device variation and circuit noise margin. We show that for each emerging device, there is a corresponding optimal set of I_{off} and V_{dd}, and an optimal energy-delay.

9:55 a.m.
16.3 Metal-Ferroelectric-Metal-Oxide-Semiconductor Field Effect Transistor with Sub-60mV/decade Subthreshold Swing and Internal Voltage Amplification, A. Rusu, G.A. Salvatore, D. Jiménez*, A.M. Ionescu, EPFL, *Universitat Autònoma de Barcelona

This work reports the first complete experimental demonstration and investigation of subthreshold swing, SS, smaller than 60mV/decade, at room temperature, due to internal voltage amplification in Field Effect Transistor with Metal-Ferroelectric-Metal-Oxide gate stack. SSmin as low as 46mV/decade and average swings, SSavg, as low as 51 to 57mV/dec, extracted over more than two decades of current are reported for the first time.

10:20 a.m.
16.4 A Predictive Contact Reliability Model for MEM Logic Switches, H. Kam, E. Alon, T.J. King Liu, University of California, Berkeley

A predictive MEM switch contact reliability model is developed and validated in this work. The results show that endurance depends not only on the contacting material but also on V_{DD}, series resistance, and load capacitance. Endurance exceeding 10^{15} on/off cycles is projected for a scaled switch technology operating at 1V.

10:45 a.m.
16.5 Polymer Solid-Electrolyte (PSE) Switch Embedded in 90nm CMOS with Forming-free and 10nsec Programming for Low Power, Nonvolatile Programmable Logic (NPL), M. Tada, T. Sakamoto, K. Okamoto, M. Miyamura, N. Banno, Y. Katoh, S. Ishida, N. Iguchi, N. Sakimura, H. Hada, NEC Corporation

A novel polymer solid-electrolyte (PSE) switch, NanoBridge, has been successfully embedded in a 90nm-node CMOS for the first time, featuring a forming-free programming and extremely high OFF/ON resistance ratio of 10^5. A fast programming of 10nsec is also achieved in 50nm, 1k-bit-cell array by introducing the PSE integrated with a fully logic compatible process below 350°C.

Luncheon Session

Tuesday, December 7, 12:20 p.m.
Grand Ballroom B

Luncheon Presentation: "Evolution and Directions for Mobile Wireless Devices"
James Clifford, Senior VP and General Manager of Operations, Qualcomm CDMA Technologies

Mobile wireless applications have become a necessity in everyday life, and have become important product drivers for the semiconductor industry. The product market landscape has been driven by an insatiable demand for data speeds, device features, sleek appearances and increased battery life. This talk will outline the evolution of Qualcomm's chip sets, and will elaborate on the technology requirements. Qualcomm has become a top 10 semiconductor supplier while exercising the fabless semiconductor model through the use of collaborative relationships with supply chain partners. While a focus on continued device scaling and the use of Moore's law has been a backbone thus far the industry is struggling with the increased cost of wafer fabs and R&D. It is predicted that an expansion of the ecosystem to include increased use of external research and "More than Moore" will play an increasingly important role moving forward.

Jim Clifford is currently Senior Vice President and General Manager of Operations at QUALCOMM CDMA Technologies (QCT). In this role, Clifford is responsible for IC and Packaging Technologies, Procurement, Integrated Supply and Demand Planning, and Quality in addition to managing the overall operations functions for the QCT division.

Clifford has been at QUALCOMM since 1994, when he joined the company as a director of business development and oversaw product development in its OmniTRACS division. In 1996 he moved to QCT as director ASICs, and has focused on sourcing IC chips during the explosive growth for CDMA technology. He was promoted to vice president of operations in 1997, senior vice president in 2000, and GM of Operations in 2003.

Prior to his career at QUALCOMM, Clifford had more than 20 years of experience at Unisys in positions ranging from IC design to vice president and general manager of mainframe computer manufacturing. Clifford holds a Bachelor's of Science in Physics from San Diego State University, and is a graduate of the Executive Program for Scientists and Engineers program offered by the University of California, San Diego.

Session 17: Device Circuits
Tuesday, December 7, 2:15 p.m.
Grand Ballroom A

Chair: Kazunari Ishimaru, Toshiba Corp.

2:15 p.m.
Introduction

Recognizing the increasing importance of the inter-dependence of circuit and technology, the IEDM started a special all-invited session on the confluence of design and process technology back in 2007. Those discussed were mainly conventional CMOS. This year's theme is "Design challenges for non-conventional devices and 3D LSIs". This session brings together design experts from different areas to discuss issues in implementing non-conventional devices and 3D LSI enablement.

2:20 p.m.
17.1 ThruChip Interface (TCI) for 3D Integration of Low-Power System (Invited), T. Kuroda, Keio University

A ThruChip Interface (TCI) employs inductive coupling for 3D CMOS integration. It is implemented by digital circuits in a standard CMOS. It bears comparison with TSV in terms of data rate (>10Gb/s/ch), reliability ($BER<10^{-14}$), energy dissipation (<0.1pJ/b), but it is much less expensive. The cost/performance will be improved exponentially by thinning chip thickness.

2:45 p.m.
17.2 Thermal-Aware Design of 3D ICs with Inter-Tier Liquid Cooling (Invited), D. Atienza, Embedded Systems Laboratory, EPFL

Continuous advances in manufacturing technologies are enabling the development of more powerful and compact 3D multi-processor ICs. However, 3D stacking originates higher power and heat densities, leading to degraded performance if cooling is not handled properly at all levels. In this talk, I present a novel thermal-aware design paradigm for 3D-ICs, developed in cooperation with IBM, that includes thermal modeling as fundamental step to design 3D multi-processor ICs with inter-tier liquid cooling microchannels, in combination with the use of dynamic thermal management at system-level to tune the flow rate of the coolant in each tier to achieve thermally-balanced 3D-ICs.

3:10 p.m.
17.3 Device and Circuit Interactive Design and Optimization Beyond the Conventional Scaling Era (Invited), S. Oh, L. Wei, S. Chong, J. Luo, H.-S. P. Wong, Stanford University

When gate length scaling and strain are no long the performance booster, technology development and system design must be taken into consideration for technology development. In this paper, several issues on technology development are addressed based on the study of device/circuit interactive design and optimization. New trends for device design are expected: 1) parasitics, and 2) understanding device design and its impact on the circuit-level environment.

3:35 p.m.
17.4 May the Fourth (terminal) be with you - Circuit Design beyond FinFET (Invited), H. Koike, S. O'uchi, M. Hioki, K. Endo, T. Matsukawa, Y. Liu, M. Masahara, T. Tsutsumi, K. Sakamoto, T. Nakagawa, T. Sekigawa, AIST

Since its original proposal of XMOS transistor in early 1980s, AIST has had a long history of double-gate device research, including recent special collaborative efforts by device and circuit researchers. This paper presents the results from such activities, including XDXMOS (cross-drive XMOS), Flex Power FPGA, Flex-Pass-Gate SRAM and low-voltage opamp using Adaptive-Vt differential pair.

4:00 p.m.
17.5 Intrinsic Variability in Nano-CMOS Design and Beyond (Invited), Y. Cao, Arizona State University

Intrinsic device variability, such as dopant and geometry fluctuations, poses a fundamental challenge to CMOS scaling and IC design. Predictive modeling helps benchmark its impact on circuit performance, indicating the trend, priority and techniques of variability control. Moreover, it illustrates the vast opportunities of feedback devices in future robust design.

4:25 p.m.
17.6 Low-Power Circuit Challenges in Cellular/Molecular Interfaces (Invited), E. Yoon, University of Michigan

Challenges at the junction of electrical interfaces to living systems require system solutions integrating device technologies, smart circuit schemes and packaging innovations. Ultra-low-power, very-small, implantable biosensors for neural prostheses and cochlear microsystems will be introduced for in-vivo cellular interface, while label-free detection of DNA molecules will be reviewed for in-vitro interface.

Session 18: Process Technology – Advanced Technologies for Ge MOSFETs and New Concept Devices
Tuesday, December 7, 2:15 p.m.
Continental Ballroom 1-3
*Co-Chairs: Patrick G.Q. Lo, Institute of Microelectronics/A*STAR*
Athanasios Dimoulas, NCSR DEMOKRITOS

2: 15 p.m.
Introduction

2:20 p.m.
18.1 Ge MOSFETs Performance: Impact of Ge Interface Passivation, C.H. Lee, T. Nishimura, T. Tabata, S.K. Wang, K. Nagashio, K. Kita, A. Toriumi, University of Tokyo

We have systematically investigated Ge interface passivation methods, and the highest electron and hole mobility have been demonstrated by dramatic reduction of Dit thanks to the collaboration of self-passivation and valency passivation. This study strongly suggests us that high performance Ge CMOS is really feasible.

2:45 p.m.
18.2 Higher k Metal-Gate/High-k Ge n-MOSFETs with <1 nm EOT Using Laser Annealing, W.B. Chen, B.S. Shie, C.H. Cheng, K.C. Hsu, C.C. Chi*, A. Chin, National Chiao Tung University, *National Tsing Hua University

High performance metal-gate/high-k/Ge n-MOSFETs are reached with low 73 Ω/sq R_s, 1.1 n-factor, 0.95 nm EOT, small 106 mV/dec SS, and good 312 cm^2/Vs mobility at 0.7 MV/cm. These are achieved by using LA that leads to 57% higher gate capacitance, smaller diffusion, better n^+/p junction and 10X higher I_{on}/I_{off}.

3:10 p.m.
18.3 Prospects for MEM Logic Switch Technology (Invited), T.-J. King Liu, J. Jeon, R. Nathanael, H. Kam, V. Pott*, E. Alon, University of California, Berkeley, *Institute of Microelectronics

This paper provides an overview of recent progress in device design, materials/process integration and technology scaling toward achieving MEM switches suitable for ultra-low-power digital IC applications.

3:10 p.m.
18.4 Record Low Contact Resistivity to n-type Ge for CMOS and Memory Applications, K. Martens, A. Firrincieli, R. Rooyackers*, B. Vincent*, R. Loo*, S. Locorotondo*, E. Rosseel*, T. Vandeweyer*, G. Hellings*, B. De Jaege*, M. Meuris*, P. Favia*, H. Bender*, B. Douhard*, J. Delmotte*, W. Vandervorst, E. Simoen*, M. Jurczak*, D. Wouters, J. A. Kittl*, KU Leuven, *IMEC

Record low contact resistivity to n-Ge of rho_c < $2x10^{-6}$ Ωcm^2 was demonstrated for the first time by two different approaches: 1) introducing millisecond laser annealing in combination to NiGe snow-plow (to enhance active dopants at the interface), and 2) using doped epi-Si-passivation layers for n-Ge contacts (eliminating Fermi level pinning). This is a dramatic improvement compared to typical best values of ~10^{-4} Ωcm^2 achieved by previously reported techniques, opening the opportunity to realizing the high potential of Ge for Ge-CMOS and memory applications.

4:00 p.m.
18.5 High Mobility High on/off ratio C-V Dispersion-free Ge n-MOSFETs and their Strain Response, Y.-C. Fu, W. Hsu, Y.-T. Chen, H.-S. Lan, C.-H. Lee, H.-C. Chang, H.-Y. Lee, G.-L. Luo, C.-H. Chien, C.W. Liu, C. Hu, F.-L. Yang, National Nano Device Laboratories, *National Taiwan Univesrity,**University of California, Berkeley

The record high peak mobility of ~1050 cm^2/V-s on (001) Ge is demonstrated in NFET. The best achieved subthreshold swing is 150mV/dec and the on/off ratio is $2x10^4$. The low defective n^+/p junction produced a record high on/off ratio of $2x10^5$, an ideality factor of 1.05 and strong electroluminescence. The uniaxial <110> tensile strain on <110> channel direction gives the best mobility enhancement.

Session 19: Memory Technology – Resistive RAMs
Tuesday, December 7, 2:15 p.m.
Continental Ballroom 4
Co-Chairs: Ichiro Fujiwara, Sony Corporation
Gabriel Molas, CEA LETI MINATEC

2:15 p.m.
Introduction

2:20 p.m.
19.1 9nm Half-Pitch Functional Resistive Memory Cell with <1uA Programming Current Using Thermally Oxidized Sub-Stoichiometric WO_x Film, C. Ho, C.-L. Hsu, C.-C. Chen, J.-T. Liu, C.-S. Wu, C.-C. Huang, C. Hu*, F.-L. Yang, National Nano Device Laboratories, *University of California, Berkeley

Record 9nm half-pitch functional resistive-memory cell and the lowest reported 1uA programming-current have been achieved with oxidized sub-stoichiometric WO_x and Nano-Injection-Lithography. Unexpectedly low programming-current at 9nm-diameter has been examined in-depth, it offers potential for scaling low-power non-volatile memory. Device shows resistance ratio around 10, stability during read, and data-retention. Switching based on oxygen-ion dynamics can account for device characteristics.

2:45 p.m.
19.2 A Forming-free WOx Resistive Memory Using a Novel Self-aligned Field Enhancement Feature with Excellent Reliability and Scalability, W.C. Chien, Y.R. Chen, Y.C. Chen, A.T.H. Chuang, F.M. Lee, Y.Y. Lin, E.K. Lai, Y.H. Shih, K.Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd.

A thorough investigation of the switching mechanism for WO_x ReRAM gives clues to improve its performance and reliability. Consequently, a forming-free ReRAM device with self-aligned Field Enhancement structure is proposed. This scalable device demonstrates excellent characteristics - 50ns fast switching, 10^6 cycling endurance, large MLC window, and excellent data retention.

3:10 p.m.
19.3 Low Power Operating Bipolar TMO ReRAM for Sub 10 nm Era, M.J. Kim, I.G. Baek, Y.H. Ha, S.J. Baik, J.H. Kim, D.J. Seong, C.R. Lim, Y.G. Shin, S. Choi, C. Chung, KAIST

We report a method to acquire low operational currents from a hetero structure ReRAM (AlOx/TiOx). The AlOx layer as a tunnel barrier is critical for switching, and thus switching parameters are governed by the properties of

the AlOx layer. By tuning tunnel oxide properties along with adopting 5 nm sized Dash B, operational currents of < 10 µA have been achieved.

3:35 p.m.
19.4 High Performance Ultra-Low Energy RRAM with Good Retention and Endurance, C.H. Cheng, A. Chin*, F.S. Yeh, National Tsing Hua University, *National Chiao Tung University

High performance novel RRAM of 0.3 uW set power (0.1 µA at 3 V), 0.6 nW reset power (-0.3 nA at -1.8 V), ultra-low 6 fJ switching energy at 20 ns time, good 125°C extrapolated 10-year on/off retention of 200, and 1,000,000 cycling endurance were reached simultaneously.

4:00 p.m.
19.5 Diode-less Nano-scale ZrO_x/HfO_x RRAM Device with Excellent Switching Uniformity and Reliability for High-density Cross-point Memory Applications, J. Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju , S. Kim, S. Park, H. Hwang, Gwangju Institute of Science and Technology

Diode-less RRAM cell device with excellent switching uniformity and reliability were demonstrated. By scaling active device size down to 50nm and active film thickness down to 5nm, we can minimize extrinsic defect-related switching non-uniformity. Due to excellent switching uniformity, we can implement diode-less RRAM cell by back-to-back connection.

4:25 p.m.
19.6 Metal Oxide RRAM Switching Mechanism Based on Conductive Filament Microscopic Properties, G. Bersuker, D.C. Gilmer, D. Veksler, J. Yum, H. Park, S. Lian, L. Vandelli*, A. Padovani*, L. Larcher*, K. McKenna*, A. Shluger**, V. Iglesias#, M. Porti#, M. Nafrìa#, W. Taylor, P.D. Kirsch, R. Jammy, SEMATECH, *DISMI Università di Modena e Reggio Emilia, **University College London, #Universitat Autònoma de Barcelona

This study, which was performed on $TiN/HfO_2/TiN$ RRAM stacks, by combining electrical, physical and transport/atomistic modeling results identifies critical conductive filament features controlling RRAM operations. The forming process is found to define the filament shape, which determines the temperature profile and, consequently, switching characteristics. The findings indicate that reset/set are assisted by the electric field, thus favoring bipolar operation.

4:50 p.m.
19.7 Evidence and Solution of Over-RESET Problem for HfOx Based Resistive Memory with Sub-ns Switching Speed and High Endurance, H.Y. Lee, Y.S. Chen, P.S. Chen**, P.Y. Gu*, Y.Y. Hsu*, S.M. Wang*, W.H. Liu*, C.H. Tsai*, S.S. Sheu*, P.C. Chiang*, W. P. Lin*, C.H. Lin*, W.S. Chen*, F.T. Chen*, C. H. Lien, M.-J. Tsai*, National Tsing Hua University, *Industrial Technology Research Institute, **MingShin University of Science and Technology

The memory performances of HfO_x RRAM are greatly improved in this work. Record high switching speed down to 300 ps is achieved. A novel over-RESET phenomenon to wear the RLow is deduced. A method is proposed for the memory device to maintain the memory window and to endure switch up to 10^{10} cycles.

Session 20: Quantum Power and Compound Semiconductor Devices – Advanced Power Devices and Reliability
Tuesday, December 7, 2:15 p.m.
Continental Ballroom 5
Co-Chairs: *Jan Sonsky, NXP Semiconductors*
Sandeep Bahl, National Semiconductor
2:15 p.m.
Introduction

2:20 p.m.

20.1 Spatially-Discriminating Trap Characterization Methods for HEMTs and Their Application to RF-Stressed AlGaN/GaN HEMTs, S.A. Ringel, A.R. Arehart, A. Sasikumar, G.D. Via*, B. Winningham*, B. Poling**, E. Heller*, Ohio State University, *Sensors Directorate Wright Patterson Air Force Base, **Wyle Labs

New constant drain-current deep level optical/transient spectroscopy (CID-DLTS/DLOS) methods to quantify trap energies and concentrations in AlGaN/GaN high electron mobility transistors (HEMTs) are described. These methods are applied to RF stressed HEMTs to characterize the impact of stressing on traps and identified a significant increase in virtual gate related levels.

2:45 p.m.

20.2 RF Power Degradation of GaN High Electron Mobility Transistors, J. Joh, J.A. del Alamo, Massachusetts Institute of Technology

In GaN HEMTs, RF degradation mechanisms have yet been understood well. To fill this void, we have developed a methodology to systematically investigate RF reliability. We found that RF stress degrades the device much more severely than DC at the same stress voltage and induces a prominent increase in source resistance.

3:10 p.m.

20.3 A Comprehensive Reliability Investigation of the Voltage-, Temperature- and Device Geometry-Dependence of the Gate Degradation on State-of-the-Art GaN-on-Si HEMTs, D. Marcon, T. Kauerauf, F. Medjdoub, J. Das, M. Van Hove, P. Srivastava, K. Cheng, M. Leys, R. Mertens, S. Decoutere, G. Meneghesso*, E. Zanoni*, G. Borghs, IMEC, *University of Padova

The gate reliability of GaN HEMTs is analyzed in detail. We found that the degradation appears even below the critical voltage with a voltage- and temperature-accelerated kinetics. For the first time, the TDDB approach of CMOS technology has been comprehensively applied to this technology, finally allowing lifetime extrapolation.

3:35 p.m.

20.4 Reliability of Enhancement-Mode AlGaN/GaN HEMTs Under ON-State Gate Overdrive, C. Ma, H. Chen, C. Zhou, S. Huang, L. Yuan, J. Roberts*, K.J. Chen, Hong Kong Universityof Science and Technology, *Nitronex

We report the ON-state reliability of enhancement-mode AlGaN/GaN HEMTs treated by fluorine plasma under gate overdrive. A critical gate stress voltage is observed, beyond which the channel turn-on voltage shifts negatively. This is caused by the impact ionization of the F ions in the barrier layer by hot electron injection.

4:00 p.m.

20.5 Blocking-Voltage Boosting Technology for GaN Transistors by Widening Depletion Layer in Si Substrate, H. Umeda, A. Suzuki, Y. Anda, M. Ishida, T. Ueda, T. Tanaka, D. Ueda, Panasonic Corporation

A new Blocking Voltage Boosting technique to increase the breakdown voltages of AlGaN/GaN HFETs on Si is presented, in which heavily p-type doped channel stoppers prevents the inversion electrons from flowing as a leakage current. The blocking voltage is increased to 1340V over 1.4µm thick GaN on highly resistive Si.

4:25 p.m.

20.6 Normally-Off AlGaN/GaN-on-Si MOSFETs with TaN Floating Gates and ALD SiO_2 Tunnel Dielectrics, B. Lee, C. Kirkpatrick, X. Yang, S. Jayanti, R. Suri, J. Roberts*, V. Misra, North Carolina State University, *Nitronex, Inc.

A normally-off AlGaN/GaN MOS-HFET was demonstrated by using a combination of ALD SiO_2 tunnel dielectric and a TaN FG layer. With SiO_2/TaN/HAH stack enhancement mode operation was achieved after 15V 500ms pulse programming while gate leakage and transconductance displayed minimal degradation. The retention measurement show less than 10% charge loss after 1000s. This approach is attractive for use of AlGaN/GaN based MOS-HFETs in power applications.

4:50 p.m.

20.7 High Performance CMOS-Compatible Superjunction FINFETs for Sub-100V Applications, A. Yoo, J.C. W. Ng*, J.K.O. Sin*, W.T. Ng, University of Toronto, *Hong Kong University of Science and Technology

This paper introduces a superjunction (SJ) power FINFET to address the challenges associated with sub-100V applications. The proposed SJ-FINFET is SOI-CMOS compatible. It employs a 3D corrugated MOS channel and alternating n/p drift region pillars (the fins) to achieve a 30% reduction in specific on-resistance (Ron,sp) when compared to conventional SJ-LDMOSFETs.

5:15 p.m.

20.8 State-of-the-art Device in High Voltage Power ICs with Lowest On-State Resistance, R.Y. Su, F.J. Yang, J.L. Tsay, C.C. Cheng, R.S. Liou, H.C. Tuan, TSMC

High performance LDMOS of 600-800V Vbdss has been developed with PB (Pbody)_Extension RESURF scheme for smart power applications. This device design demonstrates the lowest specific on-state resistance against to the latest publications (40% improvement than triple RESURF, 65% improvement than double RESURF in JI LDMOSFET) and breaks 1-D silicon limit. This technology also surpasses the performance in thin SOI technology, yet it uses the bulk Si material and less manufacturing processing steps.

Session 21: Display, Sensors, and MEMS – Thin Film Transistors

Tuesday, December 7, 2:15 p.m.

Continental Ballroom 6

Co-Chairs: *Raj B. Apte, Xerox PARC*

Jerzy Kanicki, University of Michigan

2:15 p.m.

Introduction

2:20 p.m.

21.1 High Performance Single-Grain Ge TFTs without Seed Substrate, T. Chen, R. Ishihara, C.I.M Beenakker, Delft Institute of Microsystems and Nanoelectronics

We report high performance single-grain Ge TFTs by µ-Czochralski process. Electron mobilites are 3337cm2/Vs with on/off ratio of 10^8 @V_{DS}=0.1V. Hole mobilities are 1719cm^2/Vs with on/off ratio of 10^8 @V_{DS}=0.05V. The high mobility is due to improved interface property and tensile stress.

2:45 p.m.

21.2 Ultra-low power TFTs with 10 nm Stacked Gate Insulator Fabricated by Nitric Acid Oxidation of Si (NAOS) Method, T. Matsumoto, M. Yamada, H. Tsuji, K. Taniguchi, Y. Kubota*, S. Imai*, S. Terakawa, H. Kobayashi, Osaka University, *Sharp Corp.

We have succeeded in fabrication of ultra-low power poly-Si based TFTs with 10 nm gate insulators and 1 V driving voltage. An ultrathin interfacial SiO_2 layer formed in HNO_3 at 120°C decreases a gate leakage current by 2 orders of magnitude, resulting in high on/off ratio of 10^9.

3:10 p.m.

21.3 180nm Gate Length Amorphous InGaZnO Thin Film Transistor for High Density Image Sensor Applications, S. Jeon, S. Park*, I. Song, J. Park, S. Kim, S. Kim, H. Yin, E. Lee, S. Ahn,C. Kim, and U.-I. Chung, Samsung Advanced Institute of Technology

The scalability to nanometer scale of oxide TFTs suggests that the oxide TFT is a feasible approach to switch elements for high density CMOS image sensor devices. Based on the low temperature stackable nature, optical transparency, and excellent short channel device performance, a workable high density CMOS image sensor can be realized.

3:35 p.m.

21.4 Oxide TFT Rectifier Achieving 13.56-MHz Wireless Operation with DC Output up to 12 V, T. Kawamura, H. Wakana, K. Fujii, H. Ozaki, K. Watanabe, T. Yamazoe, H. Uchiyama, K. Torii, Hitachi, Ltd.

We have fabricated a rectifier by using fully-depleted amorphous In-Ga-Zn-O (a-IGZO) TFTs. It exhibited the rectification of 13.56-MHz wireless input from a commercial RFID reader/writer for the first time in oxide TFT devices. The result opens the way for wireless application of oxide TFTs.

4:00 p.m.
21.5 Very High Performance Non-Volatile Memory on Flexible Plastic Substrate, C.H. Cheng, A. Chin*, F.S. Yeh, National Tsing Hua University, *National Chiao Tung University

We report record-best performance non-volatile memory on flexible plastic substrate, with ultra-low 5 uW switching power (1.6 μA at 3 V; -0.5 nA at -2 V), excellent 10^5 cycling endurance, large on/off retention memory window >100 even at 85°C, and fast 50 ns switching for the first time.

4:25 p.m.
21.6 Submicron Low-Voltage Organic Transistors and Circuits Enabled by High-Resolution Silicon Stencil Masks, F. Ante, F. Letzkus*, J. Butschke*, U. Zschieschang, K. Kern, J.N. Burghartz*, H. Klauk, Max Planck Institute for Solid State Research, *IMS CHIPS

We demonstrate submicron top contact organic thin-film transistors with record static performance (transconductance 1 S/m, on/off ratio 10^8, subthreshold swing 100 mV/dec) and organic complementary ring oscillators with record low voltage dynamic performance (stage delay 30 µs at 3 V) enabled by high-resolution silicon stencil masks and a solvent-free, low-temperature fabrication process.

Session 22: Modeling and Simulation – Simulation of Memory Devices
Tuesday, December 7, 2:15 p.m.
Continental Ballroom 7-9
Co-Chairs: Paolo Fantini, Micron
Kenji Shiraishi, University of Tsukuba

2:15 p.m.
Introduction
2:20 p.m.
22.1 Modeling the Switching Dynamics of Programmable-Metallization-Cell (PMC) Memory and Its Application as Synapse Device for a Neuromorphic Computation System, S. Yu, H.-S.P.Wong, Stanford University

A physical model is developed and corroborated with the experimental data to investigate the switching dynamics of programmable-metallization-cell (PMC) memory. For the first time, the time-dependent switching process can be quantified and I-V characteristics can be reproduced. This model shows that PMC can exhibit the spike-timing-dependent plasticity as synapse devices.

2:45 p.m.
22.2 A Model for the RESET Operation of Electrochemical Conducting Bridge Resistive Memory (CB-ReRAM), Y.-Y. Lin, F.-M. Lee, W.-C. Chien, Y.-C. Chen, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd.

The time evolution of the RESET process for the electrochemical conducting bridge resistive memory (CB-ReRAM) is modeled. The RESET current has three origins: (i) ionic (ii) tunneling, and (iii) Ohmic. Counterintuitively the ionic (electrochemical) current is the smallest of the three. New electrode materials are proposed to improve the programming efficiency and reduce the RESET current.

3:10 p.m.
22.3 The First Principle Computer Simulation and Real Device Characteristics of Superlattice Phase-Change Memory (Invited), J. Tominaga, R. Simpson, P. Fons, A. Kolobov, National Institute of Advanced Industrial Science and Technology

We present that atomically controlled Ge-Sb-Te films enable to greatly suppress switching energy, and to increase speed faster than that using the composite films in Set and Reset. The first principle computer simulation using NVT ensemble dynamics and real device fabrication based on the model are reported.

3:35 p.m.
22.4 A Novel Floating Body Cell Memory with Laterally Engineered Bandgap using Si-Si:C Heterostructure, S.-J. Choi, D.-I. Moon, Y. Ding*, E.Y.J. Kong*, Y.-C. Yeo*, Y.-K. Choi, KAIST, *National University of Singapore

A lateral bandgap-engineered floating-body-cell (FBC) memory is demonstrated for the first time, featuring high-k, metal-gate, and epitaxial Si:C S/D. Through the comparative study with control groups, figures of merit in FBC memory are remarkably enhanced (the best sensing window of 260uA/um in all sub-100nm FBC devices) under various operating conditions.

4:00 p.m.
22.5 Investigation of the Role of H-related Defects in Al_2O_3 Blocking Layer on Charge-Trap Memory Retention by Atomistic Simulations and Device Physical Modelling, G. Molas, L. Masoero, P. Blaise, A. Padovani**, J. P. Colonna, E. Vianello^, M. Bocquet, E. Nowak, M. Gasulla, O. Cueto, H. Grampeix, F. Martin, R. Kies, P. Brianceau, M. Gély, A.M. Papon, D. Lafond, J.P. Barnes, C. Licitra, G. Ghibaudo*, L. Larcher, S. Deleonibus, B. De Salvo, CEA-LETI Minatec, *IMEP CNRS, **University of Modena, ^FBK

We use atomistic simulation, consolidated by a detailed Al_2O_3 physico-chemical material analysis, to investigate the origin of traps in Al_2O_3. It is shown that the leakage currents through Al_2O_3 layers, with different post-deposition anneals, are strictly correlated to the H content. Then, the hydrogen-based trap features estimated by quantum simulations are introduced in a TANOS device simulator. A very good agreement is obtained between model and device experimental data, allowing for a clear understanding of the role of alumina H content on the retention characteristics of charge-trap memories.

4:25 p.m.
22.6 3D Monte Carlo Simulation of the Programming Dynamics and their Statistical Variability in Nanoscale Charge-Trap Memories, S.M. Amoroso, A. Maconi, A. Mauri*, C. Monzio Compagnoni, E. Greco*, E. Camozzi*, S. Viganò*, P. Tessariol*, A. Ghetti*, A.S. Spinelli, A.L. Lacaita, Politecnico di Milano, *Numonyx

We present an investigation of the programming dynamics of nanoscale chargetrap memories (CTM), based on 3D Monte Carlo simulations. The model allows to clarify several issues affecting the program of
CTM, as the reduced slope of the ISPP transients, programming variability, and the width of the final programmed VT distribution.

4:50 p.m.
22.7 Numerical Analysis of Typical STT-MTJ Stacks for 1T-1R Memory Arrays, C. Augustine
A. Raychowdhury*, D. Somasekhar*, J. Tschanz*, K. Roy, V. De*, Intel Corporation, *Purdue University

In this paper we have presented a numerical study of four types of MTJ stacks and evaluated their relative merits and demerits for embedded memory applications. The advantage of SAF free Layers in cell writability and stability has been shown.

5:15 p.m.
22.8 Quantitative Model for TMR and Spin-Transfer Torque in MTJ Devices, D. Datta,
B. Behin-Aein, S. Salahuddin*, S. Datta, Purdue University, *University of California, Berkeley

We present the first theoretical model for MTJ devices that provides qualitative and quantitative agreement with experimental resistances, TMR, in-plane and out-of-plane torques with single set of parameters. We also predict that appropriately designed asymmetric MTJ structures can lead to significant difference in the magnitude of torques exerted on ferromagnetic contacts.

Session 23: Solid-State and Nanoelectronic Devices – Graphene Devices

Tuesday, December 7, 2:15 p.m.
Imperial Ballroom
Co-Chairs: *Zhihong Chen, Purdue University*
Eric Pop, University of Illinois Urbana-Champaign

2:15 p.m.
Introduction

2:20 p.m.
23.1 Graphene-Based Fast Electronics and Optoelectronics (Invited), Ph. Avouris, Y.-M. Lin, F. Xia, D.B. Farmer, T. Mueller, C. Dimitrakopoulos, K. Jenkins, A. Grill, IBM TJ Watson Research Center

We discuss the use of monolayer graphene as the channel of RF field-effect transistors (GFETs) and as the photoconductive element of photodetectors. GFETs with cutoff frequencies up to 100 GHz and wide wavelength range, ultrafast photodetectors, will be demonstrated. Electric field-induced bandgap opening in bilayer graphene will also be demonstrated.

2:45 p.m.
23.2 Graphene Field-Effect Transistors Based on Boron Nitride Gate Dielectrics, I.Meric, C.R. Dean, A.F. Young, J. Hone, P. Kim, K.L. Shepard, Columbia University

Graphene field-effect transistors with hexagonal boron nitride (h-BN), an insulating isomorph of graphene, as the dielectric are investigated. The devices show mobilities exceeding 10,000 cm^2/V-sec and current saturation down to 500 nm channel lengths with intrinsic transconductance above 400 mS/mm. The work demonstrates the favorable properties of using h-BN as a gate dielectric for graphene FETs.

3:10 p.m.
23.3 Understanding the Contact Characteristics in Single or Multi-Layer Graphene Devices: The Impact of Defects (Carbon Vacancies) and the Asymmetric Transportation Behavior, W.J. Liu, M. F. Li*, S.H. Xu, Q. Zhang, Y.H. Zhu, K.L. Pey, H.L. Hu, Z.X. Shen, X. Zou, J.L. Wang, J. Wei**, H.L. Zhu^, H.Y. Yu, Nanyang Technological University, *Fudan University, **A*STAR, ^Institute of Microelectronics

The Rc of Ti/SLG (or MLG) prepared by EBM and SPUTTER are studied physically and electrically. Two independent measurement methods show consistent Rc. Rc of Ti/SLG (DLG) by SPUTTER is larger than that by EBM. It is believed that sputter process can create carbon vacancies in graphene, leading to the increase of Rc, which is supported by Raman spectra. SKPM, for the first time, is used to understand the asymmetric transportation behavior in graphene devices. The p-n-p (n-p-n) junction is believed to be responsible for the asymmetric transportation in electron (hole) region due to WF difference induced p (n)- type doping in metal/graphene junctions.

3:35 p.m.
23.4 Impacts of Graphene/SiO_2 Interaction on FET Mobility and Raman Spectra in Mechanically Exfoliated Graphene Films, K. Nagashio, T. Yamashita, J. Fujita, T. Nishimura, K. Kita, A. Toriumi, University of Tokyo

Mobility of the graphene transferred on the SiO_2/Si substrate scatters and is limited to typical value of ~10,000 cm^2/Vs. Without understanding the interaction between graphene and SiO2, it is difficult to improve transport properties. This paper discusses the effects of the surface treatment of SiO_2 by O_2 plasma on graphene characteristics.

4:00 p.m.
23.5 RF Performance of Pre-Patterned Locally-Embedded-Back-Gate Graphene Device, J. Lee, H. Jeong*, J. Lee, H. Shin, J. Heo*, H. Yang*, S.-H. Lee*, J. Shin*, S. Seo*, U. Chung*, I. Yoo*, K. Kim*, Seaoul National University, *Samsung Advanced Institute of Technology

For the first time, we measured RF performance of devices with graphene grown using low temperature ICP-CVD method on 6-inch wafer. f_T increase is moderately obtained with the decrease of gate length. Despite the low gm due to underlap region, we obtained f_T =80 GHz.

4:25 p.m.
23.6 Gigahertz Ambipolar Frequency Multiplier Based on CVD Graphene, H. Wang, A. Hsu, K.K. Kim, J. Kong, T. Palacios, Massachusetts Institute of Technology

Ambipolar transport in graphene offers great flexibility for novel device and circuit applications. This paper discusses the RF performance of CVD grown graphene transistors for the first time. Then, a new graphene ambipolar frequency multiplier that can operate at 1.4 GHz with extremely high output spectrum purity is demonstrated.

Session 24: Tuesday Evening Panel Session
Tuesday, December 7, 8:00 p.m.
Continental Ballroom 4

“Heterogeneous Device Integration as Enabler of Functional Diversification for More than Moore”

Organizer: Adrian M. Ionescu, Ecole Polytechnique Fédérale de Lausanne

Aggressive scaling of CMOS technology has been the key driver of microelectronics industry for more than 40 years and the International Technology Roadmap currently foresees 22-nm CMOS in production by 2015.

However, many new challenging applications of nanoelectronics that could drastically improve our quality of life will require not only more computing power and memory at lower cost and lower power consumption but also the diversification of functionality. Non-digital functions such as radio frequency and analogue circuitry, high voltage switches, various sensors and actuators and energy harvesters are more and more demanded for communications, automotive, environmental monitoring and medical applications, requiring a mixture of technologies, each optimized to the specific function.

This requires advanced research and developments into new materials, new devices, new processes and the integration of nanoelectronics and other innovative devices into single chips using so-called heterogeneous or mixed process technologies.

The future of Nanoelectronics is foreseen as a combination of More Moore and More than Moore with the heterogeneous integration of a large variety of technologies, and their exploitation in System-On-Chip or System-In-Package, combining various discrete subsystems using different optimized process technologies.
Heterogeneous Integration becomes the glue to bring all these technologies and components together into one system and support a large diversity of applications with performance that cannot be reached otherwise.

The objectives of this panel are to provide a perspective on the status and the industry needs in terms of heterogeneous integration for various application domains.

The panel will explore some key questions such as:

- What are the most advanced technological advances in heterogeneous integration and, particularly, what is the role and potential of 3D heterogeneous integration?
- What are the requirements to System Integration Technologies for Smart Systems? What advanced Packaging Technologies demands for Smart Systems Application Environments?
- Is silicon going to be hybridized via heterogeneous integration with III-V materials? What devices and applications will take full benefits?
- What is the potential and the advantages of radio frequency MEMS and what functionalities and performance can be obtained by their heterogeneous integration with CMOS?
- What is status and advances of heterogeneous integration of optoelectronic devices and opto-electronic advanced functions?

- Can we foresee the heterogeneous integration of energy harvesters and power sources on silicon? How realistic is to talk about future battery less wireless sensor nodes or wireless personal devices?
- Is heterogeneous integration the enabler of life after CMOS or it will extend the life of CMOS as the core technology of complex systems in which functional diversification will be enabled as an extension of CMOS platforms?

Panelists（Tentative, not confirmed yet）:

Eric Beyne, IMEC, Belgium
Klaus-Dieter Lang, Fraunhofer
Shinichi Takagi, University of Tokyo
Clark T. Nguyen, UC at Berkeley
Mario Paniccia, Intel Corporation
Joseph A. Paradiso, MIT

Session 25: Tuesday Evening Panel Session

Tuesday, December 7, 8:00 p.m.
Continental Ballroom 6

"Power Crunch - Threat or Opportunity?"

Organizer: Ralf Brederlow, Texas Instruments.

While entering the sub-100nm roadmap parasitic delays, increasing variability and leakage currents threaten the trend to keep energy consumption per computational operation on a reasonable level. Increasing processing power needs for the last few process generations led to continuous improvements in materials and device parameters simply to work against laws of scaling. To keep a constant improvement in processing speed for each new generation the negative side effects of system power has to be an essential part of system optimization. Today measures to keep power at reasonable levels are mandatory for each new high performance or low power system. Stricter regulations and increasing cost of energy are expected to even accelerate this trend. This panel will discuss needs for power optimization on device, circuit (digital & memory), technology and system level. Power optimization is a 'hen and egg' problem - so discussion will show different starting points and how they influence the solution.

Panelists

Dennis Sylvester, Univ. of Michigan
David Frank or Leland Chang, IBM
Takayasu Sakurai, Univ. of Tokyo
Anantha Chandrakasan, MIT
Roberto Bez, Numonyx
Andrea Lacaita, Univ. of Milano

Session 26: Process Technology – Advanced Source/Drain and Channel Engineering
Wednesday, December 8, 9:00 a.m.
Grand Ballroom A
Co-Chairs: Dan Gealy, Micron Technology, Inc.
Robert M. Wallace, University of Texas at Dallas

9:00 a.m.
Introduction

9:05 a.m.
26.1 Low-Resistive and Homogenous NiPt-Silicide Formation using Ultra-Low Temperature Annealing with Microwave System for 22nm-node CMOS and Beyond, T. Yamaguchi, Y. Kawasaki, T. Yamashita, Y. Yamamoto, Y. Goto, J. Tsuchimoto, S. Kudo, K. Maekawa, M. Fujisawa, K. Asai, Renesas Electronics Corp.

A novel NiPt-silicide formation using microwave annealing is proposed, and superior properties of NiPt silicide in ultra-shallow junction are demonstrated for the first time. Low-resistive and homogeneous NiPtSi can be formed, and an increase of the junction leakage current due to the abnormal NiPt-silicide growth is successfully suppressed.

9:30 a.m.
26.2 Ultra-low Series Resistance W/ErSi$_2$/n$^+$-Si and W/Pd$_2$Si/p$^+$-Si S/D Electrodes for Advanced CMOS Platform, R. Kuroda, H. Tanaka, Y. Nakao, A. Teramoto, N. Miyamoto, S. Sugawa, and T. Ohmi, Tohoku University
Ultra-low series resistance S/D electrodes are developed. R_c of $8.0x10^{-10}$ Ω-cm^2 and R_{sheet} of 4.9 Ω/□ are achieved by W/ErSi$_2$/n+-Si and W/Pd$_2$Si/p+-Si metal stacked silicide structures. CMOS performance is successfully demonstrated. The developed technology is a highly promising S/D electrode platform for scaled down CMOS to maximize the current drivability.

9:55a.m.
26.3 Contact Resistance Reduction to FinFET Source/Drain Using Dielectric Dipole Mitigated Schottky Barrier Height Tuning, B.E. Coss, C. Smith*, W.-Y. Loh*, K.J. Chung, P. Majhi*, R.M. Wallace, J. Kim, R. Jammy*, University of Texas at Dallas and *SEMATECH

We demonstrate for the first time contact resistance reduction using dielectric dipole mitigated Schottky barrier height (SBH) tuning on a FinFET source/drain. Different techniques for forming a SiO2/AlO$_x$ dipole layer are investigated using diodes. FinFETs, with contacts containing a SBH tuning dipole layer, are also presented. Reduction of the SBH by 100meV from the AlO$_x$/SiO$_2$ dipole results in a 10Ω-µm^2 reduction in specific contact resistivity and a 100Ω-µm reduction in FinFET source/drain resistance ($R_{S/D}$). Contact formation without the need for silicide makes this technique very promising for emerging devices, alternative channel materials, and sub-22nm CMOSFETS.

10:20 a.m.
26.4 Atomic-Layer-Deposited LaAlO$_3$/SrTiO$_3$ all Oxide Field-Effect Transistors, L. Dong, Y.Q. Liu*, M. Xu, Y.Q. Wu, R. Colby**, E.A. Stach, R. Droopad**, R.G. Gordon*, and P. D. Ye, Purdue University, *Harvard, **Texas State University

The conducting channel can be formed at amorphous/crystalline hetero-interfaces. Insulating amorphous LaAlO$_3$ are formed on insulating crystalline SrTiO$_3$ (100) surface by simple atomic-layer deposition (ALD) of LaAlO$_3$. Well-behaved all oxide field-effect transistors (FETs) are demonstrated.

10:45 a.m.
26.5 Reliable Single Atom Doping and Discrete Dopant Effects on Transistor Performance, T. Shinada, M. Hori, Y. Ono*, K. Taira, A. Komatsubara, T. Tanii, T. Endo* and I. Ohdomari, Waseda University, *Tohoku University

For reliable deterministic single-atom doping, or single-ion implantation(SII), improvement of single-ion detection efficiency is successfully achieved by controlling channel potential using back-gate of transistor. We also fabricate transistors whose channel-dopants are introduced one-by-one using SII and find that subthreshold current becomes larger when dopants are located at drain-side than source-side.
11:10 a.m.
26.6 Self-aligned Metal Source/Drain $In_xGa_{1-x}As$ n-MOSFETs Using Ni-InGaAs Alloy, S.H. Kim*, M. Yokoyama*, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe*, N. Miyata*, T. Yasuda*, H. Yamada*, N. Fukuhara**, M. Hata**, M. Takenaka, S. Takagi, University of Tokyo, National Institute of Advanced Industrial Science & Technology, **Sumitomo Chemical Co., Ltd.

The Ni-InGaAs alloy was found to be a promising metal S/D material for high performance InGaAs n-MOSFETs, and self-aligned metal S/D InGaAs MOSFETs have been demonstrated for the first time. The Ni-InGaAs alloy S/D and the SBH engineering have realized low R_{SD} and the high electron mobility of 2006 cm^2/Vs.

Session 27: CMOS Devices and Technology – Advanced High-k Metal Gate SoC and High Performance CMOS Platforms
Wednesday, December 8, 9:00 a.m.
Grand Ballroom B
Co-Chairs: Ben Sell, Intel Corporation
Mahalingam Nandakumar, Texas Instruments

9:00 a.m.
Introduction

9:05 a.m.
27.1 High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme, C.C. Wu, D.W. Lin, A. Keshavarzi, C.H. Huang, C.T. Chan, C.H. Tseng, C.L. Chen, C.Y. Hsieh, K.Y. Wong, M.L. Cheng, T.H. Li, Y.C. Lin, L.Y. Yang, C.P. Lin, C.S. Hou, H.C. Lin, J.L. Yang, K.F. Yu, M.J. Chen, T.H. Hsieh, Y.C. Peng, C.H. Chiou, C.J. Lee, C.W. Huang, C.Y. Lu, F.K. Yang, H.K. Chen, L.W. Weng, P.C. Yen, S.H. Wang, S.W. Chang, S.W. Chuang, T.C. Gan, T.L. Wu, T.Y. Lee, W.S. Huang, Y.J. Huang, Y.W. Tseng, C.M. Wu, E. Ou-Yang, K.Y. Hsu, L.T. Lin, S.B. Wang T.M. Kwok, C.C. Su, C.H. Tsai, M.J. Huang, H.M. Lin, A.S. Chang, S.H. Liao, L.S. Chen, J.H. Chen, P.S. Lim, X.F. Yu, S.Y. Ku, Y.B. Lee, P.C. Hhieh, P.W. Wang, S.S. Lin, S.S. Lin, Y.H. Chiu, H.J. Tao, M. Cao, TSMC

A high performance 22nm bulk FinFET achieves the best-in-class Ion of 1200(N)/1100(P) uA/um for Ioff=100nA/μm at 1V. Excellent short-channel-control is demonstrated down to 20nm L_{gate}. Dual-Epitaxy and multi-stressors are essential to boost performance. Dual workfunction HK/MG is deployed in CMOS process showing promising reliability. Excellent SRAM static-noise-margin at 0.45V is shown.

9:30 a.m.
27.2 RF CMOS Technology Scaling in High-k/Metal Gate Era for RF SoC (System-on-Chip) Applications, C.-H. Jan, M. Agostinelli, H. Deshpande, M.A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala*, J. Lin, Y-L Lu, S. Mudanai, J. Park, A. Rahman, J. Rizk, W.-K. Shin, K. Soumyanath*, H. Tashiro, C. Tsai, P. VanDerVoorn, J.-Y. Yeh, P. Bai, Intel Corp.

The impact of silicon technology scaling trends and the associated technological innovations on RF CMOS device characteristics are examined. The majority of RF device performance metrics have steadily improved by the introduction of innovative transistor and interconnect technologies, including strained silicon and high-k/metal gates in the past decade.

9:55 a.m.
27.3 Cost Effective 28nm LP SoC Technology Optimized with Circuit/Device/Process Co-Design for Smart Mobile Devices (Invited), P.R. Chidambaram, C. Gan, S. Sengupta, L. Ge, M. Han, J. Wang, P. Patel, P. Kamal, F. Vang, A. Datta, K. Bellur, R. Bucki, J. Fischer, C. Matar, G. Yeap, Qualcomm, Inc.

Design strategies enabled with multiple design rule set, power gating techniques (head switches) and router compatible multi Vt transistors are the key to productize the 4G SOC in a cost effective 28nm Poly SiON flow with embedded strain.

10:20 a.m.

27.4 Context Dependent Effects on LF (1/f) Noise in Advanced CMOS Devices, P. Srinivasan, O. Olubuyide, Y. S. Choi, A. Marshall, Texas Instruments

The dependence of low frequency (1/f) noise on the proximity of adjacent features within an integrated circuit is investigated. Context layout effects of LOD (Length of gate Oxide Definition), Active to Active Spacing, and DSL (Dual Stress Liners) boundary are studied and explained using mobility and number fluctuation theory. Recommendations to reduce 1/f noise are provided.

10:45 a.m.

27.5 A 0.039um^2 High Performance eDRAM Cell Based on 32nm High-K/Metal SOI Technology, N. Butt, K. Mcstay, A. Cestero, H. Ho, W. Kong, S. Fang, R. Krishnan, B. Khan, A. Tessier, W. Davies, S. Lee, Y. Zhang, J. Johnson, S. Rombawa, R. Takalkar, A. Blauberg, K.V. Hawkins, J. Liu, S. Rosenblatt, P. Goyal, S. Gupta, J. Ervin, Z. Li, J. Barth, M. Yin. T. Weaver, J. H. Li, S. Narasimha, P. Parries, W.K. Henson, N. Robson, T. Kirahata, M. Chudzik, E. Maciejewski, P. Agnello, S. Stiffler, and S.S. Iyer, IBM SRDC

We present industry's smallest eDRAM cell and the densest embedded memory integrated into the highest performance 32nm High-K Metal Gate SOI based logic technology. With aggressive cell scaling, High-K/Metal trench lowers parasitic resistance while maximizing capacitance. Fully-integrated 32Mb product prototypes demonstrate state-of-the-art sub 1.5ns latency with excellent retention and yield characteristics. The sub 1.5ns latency and 2ns cycle time have been verified with preliminary testing whereas even better performance is expected with further characterization. In addition, the trench capacitors set the industry benchmark for the most efficient decoupling in any 32nm technology.

Session 28: Characterization, Reliability, and Yield – RTN and Memory

Wednesday, December 8, 9:00 a.m.

Continental Ballroom 1-3

Co-Chairs: *Hiroshi Miki, Hitachi America*
Yen-Hao Shih, Macronix International Co., Ltd.

9:00 a.m.

Introduction

9:05 a.m.

28.1 Hysteretic Drain-Current Behavior Due To Random Telegraph Noise in Scaled-down FETs with High-k/Metal-gate Stacks, H. Miki, N. Tega, Z. Ren*, C.P. D'Emic*, Y. Zhu*, D.J. Frank*, M.A. Guillorn*, D.-G. Park*, W. Haensch*, and K. Torii**, Hitachi America, Ltd., *IBM TJ Watson Research Center, **Hitachi, Ltd.

Hysteretic effects associated with random telegraph noise (RTN) are demonstrated to lead to enhancement of drain current at the onset of FET turn-on. Comprehensive time domain analyses revealed that it is a consequence of voltage dependence of capture and emission rates of RTN traps. Relevant trap parameters are statistically accumulated.

9:30 a.m.

28.2 Random Telegraph Noise in 45-nm CMOS: Analysis Using an On-Chip Test and Measurement System, S. Realov, K.L. Shepard, Columbia University

RTN measurements in 45-nm CMOS across device bias and geometry using an on-chip characterization system are reported. An automated methodology for extracting RTN levels, amplitude, and dwell times is developed. Complex RTN magnitude is statistically modeled. Device size and bias parameter dependencies of the developed model are examined.

9:55 a.m.

28.3 Statistical Characterization of Trap Position, Energy, Amplitude and Time Constants by RTN Measurement of Multiple Individual Traps, T. Nagumo, K. Takeuchi, T. Hase and Y. Hayashi, Renesas Electronics Corp.

Distributions of trap properties of random telegraph noise are examined by characterizing more than 70 individual traps. Most of traps are found in an energy range around 0.2 eV width. Inconsistently with conventional noise model, distribution of time constants is found to be scattered independently with trap position.

10:20 a.m.
28.4 Generic Learning of TDDB Applied to RRAM for Improved Understanding of Conduction and Switching Mechanism Through Multiple Filaments, R. Degraeve, Ph. Roussel, L. Goux, D. Wouters, J. Kittl, L. Altimime, M. Jurczak, G. Groeseneken, IMEC

This paper demonstrates the competition effect in the switching of several conductive filaments in RRAM using a small-size FUSI gate nmos transistor and sets out the theory for predicting the maximum applicable set voltage. We expand the post-BD conduction model revealing that the reset operation corresponds to a pinch-off of the filament at its narrowest point.

10:45 a.m.
28.5 Single Electron Induced RRAM Switching by Discrete Conductive Levels in Contact RTN Signals, Y.H.Tseng,W.C. Shen, C.-E. Huang, C. -H. Kuo*, Y.-D. Chih*, C.J. Lin, Y.-C. King, National Tsing Hua University, *TSMC

Single electron trapping/de-trapping behavior is firstly investigated in the contact RRAM device. Instability in HRS at 250°C and temperature-dependency of resistance levels are successfully explained by carrier hopping between empty trap states. Detail analyses on the capture and emission of RTN signals provide further verifications for the trap-induced resistive switching model.

11:10 a.m.
28.6 The Impact of Hole-Induced Electromigration on the Cycling Endurance of Phase Change Memory, M.H. Lee, R. Cheek*, C.F. Chen, Y. Zhu*, J. Bruley*, F.H. Baumann**, Y.H. Shih, E.K. Lai, M. Breitwisch*, A. Schrott*, S. Raoux, E.A. Joseph*, H.Y. Cheng, J.Y. Wu, H.L. Lung, C. Lam*, Macronix International Co., Ltd., 8IBM TJ Watson Research Center, **IBM Hopewell Junction

High current-density induced failure in PCM is investigated. The cycling endurance was dramatically affected by the polarity of the SET/RESET current, as well as both electrical characteristics and physical features after failure. These can be well explained by hole-induced electromigration in GST, a p-type semiconductor. The impact of electromigration for future scaled phase change memory is also discussed.

Session 29: Memory Technology – Phase Change Memory and 3-Dimensional Memory
Wednesday, December 8, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: Daewon Ha, Samsung Electronics Co., Ltd.
Yoshitaka Sasago, Hitachi, Ltd.

9:00 a.m.
Introduction

9:05 a.m.
29.1 N-doped GeTe as Performance Booster for Embedded Phase-Change Memories, A. Fantini, V. Sousa, L. Perniola, S. Maitrejean, J.C. Bastien, E. Gourvest, S. Braga**, N. Pashkov, A. Bastard, B. Hyot, A. Roule, A. Persico, H. Feldis, C. Jahan, J.F. Nodin, B. De Salvo, R. Annunziata*, D. Benshael*, P. Mazoyer*, F. Boulanger, CEA-LETI, MINATEC, *STMicroelectronics, **Universita degli studi di Pavia

For the first time in this paper the impact of N doping in GeTe is investigated to boost the data retention performances of Phase-Change Memories (PCM). Light N addition stabilizes the amorphous phase, without sacrifying the programming performances. The extracted 10-years fail temperature for GeTeN2% is 154°C.

9:30 a.m.
29.2 Phase Change Memory Line Concept for Embedded Memory Applications (Invited), K. Attenborough, G.A.M. Hurkx, R. Delhougne, J. Perez, M.T. Wang*, T.C. Ong*, L. Tran*, D. Roy, D.J. Gravesteijn, M.J. van Duuren, NXP-TSMC Research Center, *TSMC

We report on successful array level integration of a PCRAM memory with a narrow line of doped-Sb_2Te, embedded in fully standard 65nm CMOS. Demonstrator cells can be reversibly reprogrammed between two well-defined resistance levels and correlate well with data achieved on megabit array level.

9:55 a.m.
29.3 Temperature- and Time- Dependent Conduction Controlled by Activation Energy in PCM, D. Fugazza, D. Ielmini, G. Montemurro, A.L. Lacaita, Politechnico di Milano and IVNET

Temperature and time-dependence of the resistance in phase-change-memory is addressed. The non-Arrhenius behaviour is explained by temperature-dependent current localization in the frame of the distributed Poole-Frenkel model. Noise and drift are evidenced to originate from changes of the activation energy along the hopping path. Scaling rules for noise and drift are developed.

10:20 a.m.
29.4 Voltage Polarity Effects in GST-Based Phase Change Memory: Physical Origins and Implications, A. Padilla, G. W. Burr, K. Virwani, A. Debunne, C.T. Rettner, T. Topuria, P.M. Rice, B. Jackson, D. Dupouy, A. Kellock, R. M. Shelby, K. Gopalakrishnan, R.S. Shenoy, B.N. Kurdi, IBM Almaden Research Center
We show that bias polarity can greatly accelerate device failure in GST-based (GeSbTe) PCM devices, and trace this effect to elemental segregation, initially driven by bias across the melt but then enhanced during the crystallization process. Implications include device, pulse, and materials design for high endurance.

10:45 a.m.
29.5 Device, Circuit and System-Level Analysis of Noise in Multi-bit Phase-Change Memory, G.F. Close, U. Frey, M. Breitwisch*, H.L. Lung**, C. Lam*, C. Hagleitner, E. Eleftheriou, IBM Research, *IBM TJ Watson Research Center, **Macronix International Co., Ltd.

The impact of noise on data integrity in multi-bit PCM chips is quantified with a combination of experiments and simulations. A prototype chip with 4-M cells and device-level measurements support our system-level analysis, which shows that a raw bit error rate of $\sim 10^{-4}$ is achievable at 3-bit/cell.

11:10 a.m.
29.6 3-Dimensional $4F^2$ ReRAM Cell with CMOS Logic Compatible Process, C.-H. Wang, Y.-H. Tsai, K.-C. Lin, M.-F. Chang, Y.-C. King, and C. J. Lin, S.-S. Sheu*, Y.-S. Chen*, H.-Y. Lee*, F.T. Chen*, and M.-J. Tsai*, National Tsing Hua University, *Industrial Technology Research Institute

A new 3D BJT ReRAM with CMOS compatible process is reported. The new BJT is formed under the resistive film as a current driver. The 3D ReRAM cell is operated with a low voltage of 2V/1.5V for reset and set. By adapting the 3D BJT in ReRAM, the cell is scaled down to $4F^2$.

11:35 a.m.
29.7 Novel 3-Dimensional Dual Control-Gate with Surrounding Floating-Gate (DC-SF) NAND Flash Cell for 1Tb File Storage Application, S.J. Whang, K.H. Lee, D.G. Shin, B.Y. Kim, M.S. Kim, J.H Bin, J.H. Han, S.J. Kim, B.M. Lee, Y.K. Jung, S.Y. Cho, C.H. Shin, H.S. Yoo*, S.M. Choi*, K. Hong, S. Aritome*, S.K. Park, and S.J. Hong, Hynix Semiconductor, Inc.

A novel 3-dimensional Dual Control-gate with Surrounding Floating-gate (DC-SF) NAND flash has been successfully developed, for the first time. With this structure, high coupling ratio, low voltage cell operation, and

wide P/E window (9.2V) can be obtained. Then the 3D DC-SF NAND flash cell is the most promising candidate for 1Tb and beyond with stacked multi bit FG cell (2 ~ 4bit/cell).

Session 30: Quantum, Power, and Compound Semiconductor Devices – Ultra High Speed Transistors
Wednesday, December 8, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: Toshihide Kikkawa, Fujitsu Laboratories Ltd.
Sylvain Delage, Alcatel-Thales III-V Lab

9:00 a.m.
Introduction

9:05 a.m.
30.1 220GHz f_T and 400GHz f_{max} in 40-nm GaN DH-HEMTs with Re-grown Ohmic, K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P.J. Willadsen, C. Butler,
A. Schmitz, D. Wheeler, A. Fung*, M. Micovic, HRL Laboratories, *Jet Propulsion Laboratory

We report record RF performance in 40nm-gate GaN-HEMT technology. Through vertical scaling in an AlN/GaN/AlGaN double heterojunction HEMT structure and reduction of access resistance using MBE re-growth of n+-GaN ohmic contacts, fully-passivated 40-nm devices exhibited excellent DC and RF characteristics, demonstrating a record f_T of 220GHz and a record f_{max} of 400GHz.
9:30 a.m.
30.2 Advanced Gate Technologies for State-of-the-art f_T in AlGaN/GaN HEMTs, J. Chung, T-W Kim, and T. Palacios, MIT Microsystems Technology Laboratories

We identified, for the first time, the g_m-collapse at RF frequencies with respect to the DC g_m as one of the key causes of the lower-than-expected f_T in AlGaN/GaN HEMTs. By combining gate recess and oxygen plasma treatment to reduce the g_m-collapse, we achieved a record f_T of 225 GHz.

9:55 a.m.
30.3 100GHz Depletion-Mode Ga_2O_3/GaN Single Nanowire MOSFET by Photo-Enhanced Chemical Oxidation Method, J.-W. Yu, Y.-R. Wu, J.-J. Huang, L.-H. Peng, National Taiwan University

By taking advantages of 2DEG induced at the Ga_2O_3/GaN interface due to the discontinuity of polarization and the high-field action due to the fringing-field effect exerted by the metal gate over the inclined GaN facets, we demonstrate a high-speed operation of GaN NW transistors in the 100GHz regime.

10:20 a.m.
30.4 High-Performance Monolithically-Integrated E/D Mode InAlN/AlN/GaN HEMTs for Mixed-Signal Applications, Y. Tang, P. Saunier*, R. Wang, A. Ketterson*, X. Gao**, S. Guo**, G. Snider, D. Jena, H. Grace Xing, and P. Fay, University of Notre Dame, *TriQuint Semiconductor, **IQE RF LLC

E- and D-mode InAlN HEMT devices with 144-nm gate lengths have been fabricated together on the same wafer, and exhibit well-matched performance in terms of drain current density, transconductance, and microwave performance. Ring oscillator circuits have also been fabricated and characterized to demonstrate the integration; 15.3 ps/stage delays have been measured.

10:45 a.m.
30.5 SiGe HBT Technology with f_T/f_{max} of 300 GHz/500 GHz and 2.0 ps CML Gate Delay, B. Heinemann, R. Barth, D. Bolze, J. Drews, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, S. Marschmeyer, H. Rücker, D. Schmidt, M.A. Schubert, B. Tillack, C. Wipf, D. Wolansky, Y. Yamamoto, IHP

A SiGe HBT technology featuring f_T/ f_{max}/BV_{CEo}=300GHz/500GHz/1.6V and minimum CML ring oscillator gate delays of 2.0 ps is presented. The speed-improvement compared to previous SiGe HBT technologies originates from reduced specific collector-base capacitance and base resistance and scaling of device dimensions.

11:10 a.m.
30.6 50 nm E-mode I $_{0.7}$ Ga$_{0.3}$ As PHEMTs on 100 mm InP Substrate with f_{max} > 1 THz, D.-H. Kim, J.A. del Alamo*, P. Chen, W. Ha, M. Urteaga, B. Brar, Teledyne Scientific Company, *MIT

In this work, we demonstrate a record f_{max} in excess of 1 THz for a device with an enhancement-mode operation.

11:35 a.m.
30.7 60 nm Self-Aligned-Gate InGaAs HEMTs with Record High-Frequency Characteristics, T.-W. Kim, D.-H. Kim and J.A. del Alamo, MIT

We have developed a new Mo-based self-aligned gate technology for HEMTs that yields outstanding contact resistance, source resistance, transconductance and high frequency characteristics. A 60 nm self-aligned InGaAs HEMT exhibits a record ft of 580 GHz and f_{max} of 675 GHz at 0.6 V.

Session 31: Displays, Sensors, and MEMS – PV and Energy Harvesting
Wednesday, December 8, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: *Ken Hsieh, Macronix*
Kazuyoshi Torii, Hitachi CRL

9:00 a.m.
Introduction

9:05 a.m.
31.1 Novel 140°C Hybrid Thin Film Solar Cell/Transistor Technology with 9.6% Conversion Efficiency and 1.1 cm^2/V-s Electron Mobility for Low-Temperature Substrates, C.-H. Shen, J.-M. Shieh, H.-C. Kuo*, J.Y. Huang*, W.-H. Huang, C.-W. Hsu*, Y.-H. Lin*, H.-Y. Chiu*, H.-Y. Jhan*, B.-T. Dai, C. Hu** and F.-L. Yang, National Nano Device Laboraotories, *National Chiao Tung University, ** University of California, Berkeley

For the first time, we report a low temperature silicon thin film deposition technology using high density plasma for high performance and low cost solar cells with embedded transistor modules. For process temperature at 140°C, energy conversion efficiency of 9.6% and electron mobility of 1.1 cm^2/V-s have been achieved. Device performance with process temperature down to 90°C and 60°C has also been examined in depth. This very low process temperature technology can integrate energy harvesting with electronics on inexpensive and flexible substrates.

9:30 a.m.
31.2 Boosting Short Circuit Current with Rationally Designed Periodic Si Nanopillar Surface Texturing for Thin Film Solar Cell, S. M. Wong, H.Y. Yu, Y.L. Li, J.S. Li*, F. Wang*, M.F. Yang*, N. Singh, P.G.Q. Lo, D.L. Kwong, A*Star, *Nanyang Technological University

This work experimentally investigates the impact of the large-scale rational-designed periodic Si nanopillar (SiNP) array structural parameters (e.g. diameter/ periodicity/ height) on the reflectance and hence the absorption of the SiNP array for the first time, and the results are in consistence with our theoretical prediction. Owing to the significantly enhanced light absorption of the optimized SiNP array texturing, a short circuit current density (Jsc) of 34.3mA/cm^2 is realized on planar p-n SiNP surface textured solar cell, which is the highest to date among reported Si nanowire (SiNW)/SiNP based solar cells. This is in distinct comparison to Jsc of 18.1 mA/cm2 demonstrated on the solar cell without SiNP.

9:55 a.m.
31.3 Above-CMOS a-Si and CIGS Solar Cells for Powering Autonomous Microsystems, J. Lu
W. Liu*, C.H.M. van der Werf**, A. Y. Kovalgin, Y. Sun*, R.E.I. Schropp**, J. Schmitz, University of Twente, *Nankai University, **Debye Institute

Two types of solar cells are successfully grown on chips from two CMOS generations. The efficiency of Aamorphous-silicon (a-Si) solar cells reaches 5.2%, copper-indium-gallium-selenide (CIGS) cells 7.1%. CMOS

functionality is unaffected. The main integration issues: adhesion, surface topography, metal ion contamination, process temperature, and mechanical stress can be resolved while maintaining standard photovoltaic processing.

10:20 a.m.
31.4 Versatile Silicon Photodiode Detector Technology for Scanning Electron Microscopy with High-Efficiency Sub-5 keV Electron Detection, A. Ŝakić, L.K. Nanver, G. van Veen*, K. Kooijmans*, P. Vogelsang*, T.LM. Scholtes, W. de Boer, W. Wien, S. Milosavljevic, T. Knežević, I. Spee*, Delft University of Technology, *FEI Company, **University of Zagreb

A new technology is presented for fabricating high-performance silicon photodiode radiation detectors for Scanning Electron Microscopy (SEM). It gives an impressive enhancement of the performance of SEM systems by enabling high-efficiency low-energy electron detection down to 200 eV in flexible configurations including segmented, closely-packed photodiodes and through-wafer apertures.
10:45 a.m.
31.5 A CMOS-Compatible Piezoelectric Vibration Energy Scavenger Based on the Integration of Bulk PZT Films on Silicon, E.E. Aktakka, R.L. Peterson, K. Najafi, University of Michigan

This paper presents a CMOS-compatible piezoelectric inertial power generator. The wafer-level fabrication process integrates bulk piezoelectric ceramic on silicon by aligned low-temperature solder-bonding and thinning to 5µm to 100 µm while conserving bulk properties. The 12.1mm3 harvester generates 0.15µw from input acceleration of 0.1g at 263Hz and 10.2µw from 2g at 252Hz.

11:10 a.m.
31.6 Integration of Organic Photovoltaic and Thermoelectric Hybrid Module for Energy Harvesting Applications, T. Suzuki, K. Yoshikawa, and S. Momose, Fujitsu Laboratories, Ltd.

We propose a hybrid energy harvesting device having two operation mode, PV or TE power generator. The device was successfully fabricated using organic materials, and the electric properties of the organic PV/TE hybrid cells were reported. An example application of the fabricated flexible hybrid module was demonstrated.

Session 32: Modeling and Simulation – Simulation of Non-Silicon Materials and Devices
Wednesday, December 8, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: Umberto Ravaioli, University of Illinois
Tatsuya Kunikiyo, Renesas Electronics Corporation

9:00 a.m.
Introduction

9:05 a.m.
32.1 Low-Field Mobility and High Field Drift Velocity in Graphene Nanoribbons and Graphene Bilayers, M. Bresciani, A. Paussa, P. Palestri, D. Esseni, L. Selmi, University of Udine

A semiclassical approach is employed to simulate the mobility and the saturation velocity in graphene-nano-ribbons and graphene bilayers. Scattering with remote phonons strongly affects the mobility but it impacts the saturation velocity much less than in previous models. For given band-gap graphene-bilayer does not offer a clear advantage over nano-ribbons.

9:30 a.m.
32.2 Full Band Assessment of Phonon-limited Mobility in Graphene Nanoribbons, A. Betti, G. Fiori and G. Iannaccone, Università di Pisa

We present a detailed investigation of the electron-phonon interaction in graphene nanoribbons by means of a full band analysis, based on a tight-binding description of the electronic structure and phonon
dispersion curves. In this way we assess the intrinsic limitations to mobility posed by lateral confinement of graphene.

9:55 a.m.
32.3 Computational Study of Graphene Nanoribbon FETs for RF Applications, I. Imperiale, S. Bonsignore, A. Gnudi, E. Gnani, S. Reggiani, G. Baccarani, University of Bologna

We perform a simulation study of GNR-FETs for high-frequency analog performance and suggest optimization criteria. Besides confirming the excellent cut-off frequency potential well above 1 THz, our study highlights limitations in the maximum achievable voltage-gain due to the small band-gap.

10:20 a.m.
32.4 High On-Off Ratio Bilayer Graphene Complementary Field Effect Transistors, K. Majumdar, K.V.R.M. Murali, N. Bhat, F. Xia, Y.-M. Lin, Indian Institute of Science, *IBM SRDC, **IBM TJWatson Research Center

We propose a novel S/D engineering for dual-gated Bilayer Graphene FET using doped semiconductors (with a bandgap) as source and drain to obtain unipolar complementary transistors. A self-consistent NEGF solver has been developed and validated against experimental data, to predict I_{on}/I_{off} ~$3.2x10^4$ and subthreshold slope 110 mV/decade with excellent scalability and current saturation, for a 20nm gate length unipolar BLG FET - an important step towards bilayer graphene logic devices.

10:45 a.m.
32.5 Multi-scale Simulations of Partially Unzipped CNT Hetero-junction Tunneling Field Effect Transistor, L. Leem, A. Srivastava, S. Li, G. Iannaccone, J.S. Harris, G. Fiori, Stanford University, *Università di Pisa

We investigated the performance of partially unzipped CNT heterojunctions, by means of a multi-scaled simulation approach. GNR/CNT heterojunctions demonstrated to be good candidates for low voltage logic applications and show better performance in terms of low subthreshold slope and strongly suppressed ambipolar behavior as compared to CNT and GNR TFETs.

11:10 a.m.
32.6 GaAs: Gap State Passivation at Interfaces and Surfaces, J. Robertson, L. Lin, Cambridge University

Electronic structure calculations on surface, interface and defect configurations of GaAs describe passivation of gap states within the electron counting rule. The critical defects, As-As dimers, give gap states at GaAs-oxide interfaces because they are 4-fold not 3-fold coordinated as on surfaces. GaAs interface defects cannot easily be passivated independently.

Session 33: Process Technology – Novel Process Technologies
Wednesday, December 8, 1:30 p.m.
Grand Ballroom A
Co-Chairs: *Naoya Inoue, Renesas Electronics*
Kyoungsub Shin, Samsung Electronics

1:30 p.m.
Introduction

1:35 p.m.
33.1 Test Chip Fabrication on Extreme Ultra Violet Lithography for High Volume Manufacturing (Invited), I. Mori, H. Aoyama, SELETE

PL test site could be investigated overall lithographic performance, which is determined by the performance of exposure tool, the resist quality of printability and mask defect evaluation. Once we begin using EUVL for device fabrication, we can accelerate device development towards the 15 nm logic node.

2:00 p.m.

33.2 Experimental Demonstration of Aperiodic Patterns of Directed Self-Assembly by Block Copolymer Lithography for Random Logic Circuit Layout, L.-W. Chang, X. Bao, C. Bencher* and H.-S. Philip Wong, Stanford University, *Applied Materials

We experimentally demonstrate a new paradigm: the use of guiding templates close to the natural length scale of the block copolymer can effectively control the size, shape, and pitch of the self-assembled features for random logic circuit layouts. We also present preliminary experimental investigations of the design space and rules for forming the pre-patterned templates to acquire desirable contact hole arrangements by block copolymer lithography.

2:25 p.m.
33.3 A Novel Cylinder-Type MIM Capacitor in Porous Low-k Film (CAPL) for Embedded DRAM with Advanced CMOS Logics, K. Hijioka, N. Inoue, I. Kume, J. Kawahara, N. Furutake, H. Shirai*, T. Itoh*, T. Ogura*, K. Kazama*, Y. Yamamoto*, Y. Kasama*, H. Katsuyama*, K. Manabe, H. Yamamoto, S. Saito, T. Hase, Y. Hayashi, LSI Research Laboratory, *Renesas Electronics Corp.

A novel cylinder-type MIM capacitor in porous low-k film (CAPL), with maintaining logic performance, is proposed for embedded DRAMs. The profile analysis with diffusion-reaction model clarified that the molecular-pore-stack (MPS, k=2.5) with extreme small pores suppressed the metal contamination in the low-k during metal CVD for the MIM electrodes. The CAPL with the MPS SiOCH film was successfully integrated into a BEOL without degradation of characteristics and reliability.

2:50 p.m.
33.4 Ultra-high Density Carbon Nanotubes on Al-Cu for Advanced Vias, J. Dijon, H. Okuno, E. Quesnel, M. Fayolle*, T. Vo*, J. Pontcharra*, D. Acquaviva**, D. Bouvet**, A.M. Ionescu**, C.S. Esconjauregui^, J. Robertson^, CEA LITEN DRNM, *CEA LETI MINATEC, **Ecole Politechnique Federale Lausanne, ^Cambridge University

An integration scheme for carbon nanotube via interconnects is described able to produce nanotube densities of 2.5 10^{12} tubes/cm^2 or 8 10^{12} walls/cm^2 on metallic Al-Cu lines, an order of magnitude beyond the previous state of art, and, for first time, close to that needed for implementation

3:15 p.m.
33.5 High Reliability 32 nm Cu/ULK BEOL Based on PVD CuMn Seed, and its Extendibility, T. Nogami[1/2], T. Bolom[5], A. Simon[6], B-Y. Kim[6], C-K. Hu [2], K. Tsumura [4], A. Madan[3] , P. Flaitz[3] , C. Parks[3], P. DeHaven[3], R. Davis [3], M. Zaitz [3], B. St. Lawrence [3], R. Murphy [3], L. Tai [3], S. Molis [3], S-H. Rhee[5], T. Usui[4], C. Cabral Jr.[2] , J. Maniscalco [1], L. Clevenger[3], B. Li[3], C. Christiansen[3], F. Chen[3], T. Lee[3], J. Schmatz [1], H. Shobha[1], F. Ito[7], T. Ryan[5], S. Nguyen[1/2], D. Canaperi[1], J. Arnold[1], S. Choi[3/2], S. Cohen[2], E. Liniger[2], H-C. Chen[1], S-T. Chen[1], T. Vo[1], J. Kelly[1], O. Straten[1], C. Penny[1], G. Bonilla[2], J. Wynne[1], P. Kozlowski[1], T. Spooner[1], D. Edelstein[1/2], [1]IBM @ Albany Nano Technology Research Center, [2]IBM TJ Watson Research Center, [3]IBM Microelectronics, [4]Toshiba America Electronic Components, Inc. [5]GLOBALFOUNDRIES, Inc., [6]STMicroelectronics, Inc., [7]Renesas Electronics America

A 32 nm BEOL with PVD CuMn seedlayer and conventional PVD-TaN/Ta liner was fully characterized by fundamental, integrated, and reliability methods. CuMn was confirmed to have fundamental advantages over CuAl, such as higher electromigration (EM) reliability for the same Cu line resistance (R). Both low R and high reliability (EM, SM, and TDDB) were achieved. Improved extendibility of CuMn relative to CuAl was also supported by studies of alloy interactions with advanced liner materials Ru and Co, and by enhancement of ultra-thin TaN barrier performance.

3:40 p.m.
33.6 Advanced Flip-Chip Package Production Solution for 40nm/28nm Technology Nodes, C.S. Chen, C.S. Liu, C.H. Lee, H.Y. Tsai, H.P. Pu, K.C. Hsu, H.J. Kuo, M.D. Cheng, C.Y. Wu, S.L. Chiu, H.W. Chen, C.W. Hsiao, C. H. Tung, M.J. Lii, C.H. Yu, TSMC

The key technology challenges and solutions in the packaging and assembly for both the 40 and 28 nm technology nodes are reported. The key challenge of chip-package-interactions (CPI) due to the use of fragile extreme low-k (ELK) dielectric materials in the BEOL has been resolved by the redesigning of the BEOL structure and optimizing the materials set including both the organic substrate and lead free materials.

Session 34: CMOS Devices and Technology – Advanced FinFETs and Nanowire FETs
Wednesday, December 8, 1:30 p.m.
Grand Ballroom B
Co-Chairs: Meishoku Masahara, AIST
Geoffrey Yeap, Qualcomm, Inc.

1:30 p.m.
Introduction

1:35 p.m.
34.1 A Low Operating Power FinFET Transistor Module Featuring Scaled Gate Stack and Strain Engineering for 32/28nm SoC Technology, C.-C. Yeh, C.-S. Chang, H.-N. Lin, W.-H. Tseng, L.-S. Lai, T.-H. Perng, T.-L. Lee, C.-Y. Chang, L.-G. Yao, C.-C. Chen, T.-M. Kuan, J. J. Xu, C.-C. Ho, T.-C. Chen, S.-S. Lin, H.-J. Tao, M. Cao, C.-H. Chang, T.-C. Ko, N.-K. Chen, S.-C. Chen, C.-P. Lin, H.-C. Lin, C.-Y. Chan, H.-T. Lin, S.-T. Yang, J.-C. Sheu, C.-Y. Fu, S.-T. Hung, F. Yuan, M.-F. Shieh, C.-F. Hu, and C. Wann, TSMC

We show that FinFET, the transistor architecture of choice for high performance CPU applications, can also be extended for general purpose SoC applications by proper device optimization. We demon-strate superior, best-in-its-class performance to our knowledge, as well as multi-Vt flexibility for low-operating power applications. By high-k/metal-gate and process flow optimizations, significant Ion improvement and Ioff reduction have been achieved through EOT scaling and mobility improvement. N-FinFET and P-FinFET achieve I_{ON} of 1325 µA/um and 1000 µA/um at 1 nA/um leakage current under V_{DD} of 1 V, respectively. FinFET is promising for low operating power designs owing to its ex-cellent SCE, DIBL and swing.

2:00 p.m.
34.2 Strained SiGe and Si FinFETs for High Performance Logic with SiGe/Si Stack on SOI, I. Ok, K. Akarvardar*, S. Lin&**, M. Baykan^, C.D. Young, P.Y. Hung, M.P. Rodgers^^, S. Bennett^^, H.O. Stamper^^, D.L. Franca^^, J. Yum*, J.P. Nadeau##, C. Hobbs, P. Kirsch, P. Majhi, R. Jammy,SEMATECH, *GLOBALFOUNDRIES, **UMC, ^University of Florida, ^^CNSE, #University of Texas at Austin ##FEI
We report high performance (Ion~1 mA/µm at Ioff 100nA/µm @ 1V Vcc) short channel PFET SiGe/Si FinFETs as a result of a high SiGe mobility, low Tinv (scaled High-k) and low Rsd combined to uni-axial strain additivity. We demonstrate a dual channel scheme for high mobility CMOS FinFETs

2:25 p.m.
34.3 Understanding of Short-Channel Mobility in Tri-Gate Nanowire MOSFETs and Enhanced Stress Memorization Technique for Performance Improvement, M. Saitoh, Y. Nakabayashi, K. Ota, K. Uchida*, and T. Numata, Toshiba Corp., *Tokyo Institute of Technology

We found short-channel mobility in SOI nanowire transistors (NW Tr.) is dominated by the strain induced in the NW channel. We enhanced NW strain by stress memorization technique (SMT). In <110> NW nFETs, Ion on the same DIBL largely increases by SMT thanks to mobility increase and parasitic resistance reduction.

2:50 p.m.
34.4 Experimental Study on Carrier Transport Limiting Phenomena in 10 nm Width Nanowire CMOS Transistors, K. Tachi, M. Cassé, S. Barraud, C. Dupré, A. Hubert, N. Vulliet**, M-E. Faivre
C. Vizioz, C. Carabasse, V. Delaye, J.M. Hartmann, H. Iwai^, S. Cristoloveanu*, O. Faynot, T. Ernst, CEA LETI MINATEC, *IMEP-LAHC, **STMicroelectronics, ^Tokyo Institute of Technology

For the first time, we experimentally analyze the limiting scattering phenomena in gate-all-around nanowire CMOS transistors with aggressive dimensions and with high-k/metal gate stack by low temperature measurement down to

5 K. One-level and multiple-level stacked nanowires structures are measured and compared. Apparent mobility is degraded in short channel devices.

3:15 p.m.

34.5 Investigation of Hole Mobility in Gate-All-Around Si Nanowire p-MOSFETs with High-k/Metal-Gate: Effects of Hydrogen Thermal Annealing and Nanowire Shape, P. Hashemi J.T. Teherani, J.L. Hoyt, MIT Microsystems Technology Laboratories

A detailed study of hole mobility is presented for gate-all-around Si NW p-MOSFETs with conformal high-k/MG and various hydrogen annealing processes. Increasing hole mobility is observed with decreasing NW width down to 12 nm. A 33% hole mobility enhancement is achieved relative to universal (100) at high Ninv.

3:40 p.m.

34.6 New Observations of Suppressed Randomization in LER/LWR of Si Nanowire Transistors: Experiments and Mechanism Analysis, R. Wang, T. Yu, R. Huang, Y. Ai, S. Pu, Z. Hao, J. Zhuge, Y. Wang, Peking University

The nanowire (NW) line-edge/width roughness (LER/LWR) effects in Si nanowire transistors (SNWTs) are investigated by both experiments and theoretical analysis. New LER/LWR characteristics are first observed in SNWTs and an improved characterization method is proposed. The effects of the key fabrication process on the NW LWR are studied in detail. The mechanism of reducing the random variation is analyzed and a physical device model is also developed.

Session 35: Characterization , Reliability, and Yield – Back-end SRAM and ESD Reliability

Wednesday, December 8, 1:30 p.m.

Continental Ballroom 1-3

Co-Chairs: Elyse Rosenbaum, University of Illinois at Urbana-Champaign
Werner Simburger, Infineon

1:30 p.m.

Introduction

1:35 p.m.

35.1 Investigation on TSV Impact on 65nm CMOS Devices and Circuits, H. Chaabouni, M. Rousseau*, P. Leduc*, A. Farcy**, R. El Farhane*, A. Thuaire*, G. Haury**, A. Valentian*, G. Billiot*, M. Assous*, F. De Crecy*, J. Cluzel*, A. Toffoli*, D. Bouchu*, L. Cadix, T. Lacrevaz, P. Ancey**, N. Sillon*, B. Flechet, *CEA Léti, MINATEC, **STMicroelectronics

4µm wide copper Through Silicon Vias (TSVs) were processed on underlying 65 nm CMOS devices and circuits in order to evaluate the impact of the three-dimensionnal (3D) integration process. Electrical tests on isolated MOSFET and ring oscillators in the presence of TSV are compared to modeling results. Beside TSV mechanical impact, an electrical coupling between TSV and MOSFET is experimentally quantified and reported for the first time. This coupling induces a spike variation up to 7 µA/µm on the static NMOS drain current. However, the ring oscillators response is not impacted

2:00 p.m.

35.2 A Comprehensive Breakdown Model Describing Temperature Dependent Activation Energy of Low-k/Extreme Low-k Dielectric TDDB, M.N. Chang, R. Ranjan, Y.-H. Lee, S.Y. Lee, C.S. Wang, J.R. Shih, K. Wu, TSMC

Temperature dependent activation energy has been observed for backend LK and ELK dielectrics TDDB. We demonstrated the charge transport through the LK/ELK is dominated by Poole-Frenkel mechanism even at low E-field, and Cu-ion diffusion occurs at later stage of stressing. A comprehensive breakdown model is proposed, which describes LK/ELK temperature dependent TDDB activation energy is associated with both trap creation and ion diffusion processes.

2:25 p.m.

35.3 Direct Visualization of Anomalous-Phosphorus Diffusion in Failure-Bit Gates of SRAM-Load pMOSFETs with High-Resolution Scanning Spreading Resistance Microscopy, L. Zhang, K. Hara, A. Kinoshita, T. Hashimoto, Y. Hayase, M. Kurihara, D. Hagishima, T. Ishikawa, S. Takeno, Toshiba Corp.

In this study, we directly observed fail bits of pMOS with Vth variations in SRAM by both SSRM and a nanoprober, clarified that the failure is originated from the phosphorus anomalous diffusion into the pMOS gate bottom. We succeeded in observing the pn-junction boundary within a thin SRAM poly-Si gate with the size of less than 60 nm. The gate-phosphorus doping and STI geometry influence on pn boundary is investigated systematically. A significant improvement in process margin is achieved with controlling of the phosphorous-anomalous diffusion.

2:50 p.m.
35.4 A Quantitative Inquisition into ESD Sensitivity to Strain in Nanoscale CMOS Protection Devices, D. Sarkar, S. Thijs*, D. Linten*, C. Russ**, H. Gossner**, K. Banerjee, University of California, Santa Barbara, *IMEC, **Infineon Technologies AG

Impact of strain on different ESD protection devices is investigated. It is shown for the first time that the ESD sensitivity to strain can vary substantially depending on whether the devices stressed are bulk or SOI and on the mode in which they are stressed.

3:15 p.m.
35.5 Charged Device Model (CDM) ESD Challenges for Laterally Diffused nMOS (nLDMOS) Silicon Controlled Rectifier (SCR) Devices for High-Voltage Applications in Standard Low-Voltage CMOS Technology, A. Griffoni, S.-H. Chen, S. Thijs, D. Linten, M. Scholz, G. Groeseneken, IMEC

The turn-on behavior of high-voltage-tolerant nLDMOS SCRs is investigated during CDM ESD events. An early failure occurs because of gate-oxide damage. A device optimization is proposed, which improves the CDM ESD robustness up to 2.7x, unchanging the HBM ESD robustness.

Session 36: Displays, Sensors, and MEMS – Biosensors and MEMS
Wednesday, December 8, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: *Chris Van Hoof, IMEC*
Peter Steeneken, NXP Semiconductors

1:30 p.m.
Introduction

1:35 p.m.
36.1 CMOS Biosensor Platform (Invited), Frans Widdershoven, NXP Semiconductors.

A CMOS biosensor platform based on capacitive sensing with nanoelectrolytic capacitors integrated in a low-power 90-nm CMOS process is presented. Operation principle and sensor integration are described. Real-time observation of Brownian motion of nanoparticles is demonstrated, and a model biological assay is performed and verified with QCM.

2:00 p.m.
36.2 A Novel Smart Nanowire Biosensor with Hybrid Sensor/Memory/CMOS Technology (Invited), M-C. Chen, C.-Y. Lin, C.-F. Hsieh*, H.-Y. Chen, J.-T. Horng*, C.-M. Tsai, C.-C. Huang, and F.-L. Yang, National Nano Device Laboratories, *Chang Gung University

For the first time, a novel smart biosensor with hybrid sensor/memory /CMOS poly-Si nanowire technology has been developed. Special designed oxide-nitride-oxide composite dielectric underneath 50nm nanowire realizes an electrically Vth-adjustable sensor to compensate device variation. The detections of pH, hydrogen peroxide and DNA are demonstrated using various functionalized receptors. A substrate-ionic coupling operation of the buried-channel field-effect sensor exhibits superior pH sensitivity (Vth shift >100 mV/pH) beyond Nernst limitation. The

built-in memory of nanowire devices possess steady electrically Vth adjustment (>2 V P/E window), enable portable physiology monitoring and in-situ recording.

2:25 p.m.
36.3 Design and Fabrication of a Biomedical Lab-on-Chip System for SNP Detection in DNA, M. Op de Beeck*, W. De Malsche*+, M. Hiraoka*^ P. Fiorini*, L. Zhang*+ , J. Op De Beeck+, B. Majeed*, D. Sabuncuoglu Tezcan*, G. Desmet+, D. Ueda^, C. Van Hoof*, and I. Yamashita^, *IMEC, + Vrije Univ. Brussel, Belgium ^ Panasonic Corp. # Katholieke Univ.

A Lab-on-Chip system for SNP detection in DNA is proposed. A core component is a Si-based micro-pillar filter enabling separation of DNA segments with different length. An on-chip integrated conductive polymer actuator generates the high pressure required to sustain the fluid flow through the system.

2:50 p.m.
36.4 A Fast and Low Actuation Voltage MEMS Switch for MM-wave and Its Integration, A. Akiba, S. Mitarai, S. Morita, K. Ikeda, S. Kurth*, S. Leidich*, A. Bertz**, M. Nowack**, J. Froemel*, T. Gessner*, Sony Corp., *Fraunhofer Research Institute for Electronic Nanosystems, **Chemnitz University of Technology
A novel mm-wave MEMS SPST switch has been developed, which was driven by 5.0 V in less than 10 usec. The insertion loss and the isolation at 60 GHz were 1.2 dB and 18 dB, respectively. A Silicon interposer was also fabricated as the integration technology for the switch module.

3:15 p.m.
36.5 BiCMOS Embedded RF-MEMS Switch for above 90 GHz Applications using Backside Integration Technique, M. Kaynak, M. Wietstruck, R. Scholz, J. Drews, R. Barth, K.E. Ehwald, A. Fox, U. Haak, D. Knoll, F. Korndörfer, S. Marschmeyer, K. Schulz, C. Wipf, D. Wolansky, B. Tillack*, K. Zoschke**, T. Fischer**, S. Kim^, J. S. Kim^, W-G. Lee^, J. W. Kim^, IHP, *Technische Universität Berlin, **Fraunhofer IZM, ^National Nano Fab Center

We demonstrate a novel back-side processed, back to front self-aligned BiCMOS embedded RF-MEMS switch for the 90 to 140GHz frequency band. The insertion loss of the wafer level packaged switch is less than 0.5dB up to 140GHz, and isolation is better than 15dB in the frequency range of 90 to 140GHz.

3:40 p.m.
36.6 A New Charge-Trap-Engineered Memory Device with Silicon-Oxide-Nitride-Vacuum-Silicon (SONVAS) Structure for LTPS-TFT-Based Applications, T.-C. Liao, C.-Y. Wu, S.-K. Chen*, M.H. Yu, T.-K. Kang**, H.-C. Cheng, National Chiao Tung University, *TSMC, **Feng Chia University

For the first time, a new Silicon-Oxide-Nitride-Vacuum-Silicon (SONVAS) LTPS-TFT-based charge-trapping Memory integrated on gate-all-around field-enhanced-nanowire architecture was demonstrated. Vacuum, simply formed by in-situ encapsulation, substituted for traditional tunneling oxide. Due to the lowest-k and empty properties of vacuum, SONVAS features field enhancement in tunneling layer and immunity against defects generated in tunneling oxide during P/E cycling, resulting in much-improved P/E efficiency and reliability, respectively.