IEEE SOLID-STATE CIRCUITS SOCIETY/IEEE SAN FRANCISCO SECTION, BAY AREA COUNCIL/UNIV. OF PA.

ADVANCE PROGRAM

1954 ~ 50th Anniversary ~ 2003

2003 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 9, 10, 11, 12, 13

CONFERENCE THEME:
POWER-AWARE SYSTEMS

SAN FRANCISCO MARRIOTT HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY: 2 WORKSHOPS: Analog Telecom; Near-Limit CMOS; 7 TUTORIALS

3 SPECIAL-TOPIC EVENING SESSIONS: 3G Cell-Phone Integration; Circuits for Emerging Technologies; Highlights of DAC

50th-ANNIVERSARY EVENTS (page 91) **WEB REGISTRATION:** Hotel, Conference: 1 Short Course, 7 Tutorials, 4 Workshops

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE HIGHLIGHTS

2003 is the 50th Anniversary of ISSCC. This year, several special events are planned to celebrate the 50th anniversary including: a plenary presentation by Gordon Moore on the past present and future of integrated circuits; a historical exhibit of key milestones in solid-state circuits; a living-history video of key contributors to IC technology; a 50th-Anniversary Social Hour; and a 50th Anniversary Edition of the JSSCC / ISSCC DVD free to ISSCC registrants.

On Sunday, February 9, the day before the official opening of the Conference, ISSCC 2003 offers:

- A choice of up to 3 of a total of 7 Tutorials
- An ISSCC Workshop on Analog Telecom Access Circuits and Concepts (ATACC), which will address optical and electrical backplane transceivers.
- An SSCTC Workshop on Implications of Near-Limit CMOS on Circuits and Applications

On Sunday evening, three special-topic evening sessions addressing next-generation circuit-design challenges will be offered starting at 7:30 PM:

- How Far Can Integration Go for 3G Cellphones
- Circuits in Emerging Technologies
- Highlights of DAC (in which some of the best circuit-design-related papers from the Design-Automation Conference are presented for ISSCC attendees)

These sessions offer leading experts in the field presenting tutorial background and state-of-the-art design strategies in a workshop format, and are open to all attendees.

On Monday, February 10th, ISSCC 2003 offers three plenary papers followed by technical sessions. There will be a special 50th-Anniversary Social Hour for all attendees, from 5:15 to 6:30 in Golden-Gate Hall. Evening panels will be held on Monday and Tuesday evenings from 8:00PM to 10:00PM.

On Thursday, February 11th, ISSCC 2003 offers a choice of three events:

- An ISSCC Short Course: System-On-A-Chip Design. Three sessions of the Short Course will be offered, with staggered starting times that will be filled on a first-come, first-served basis
- An ISSCC Microprocessor-Design Workshop: Microprocessor Design in the Power-Constrained Era
- An ISSCC Workshop on Gigahertz Radio Front Ends (GIRAFE)

Use of the ISSCC web-registration site (www.isscc.org) is strongly encouraged. You will be provided with immediate confirmation on registration for tutorials, workshops and the Short Course.

CONFERENCE INFORMATION

The coordinated timing of papers given at ISSCC permits attendees to session-hop from session to session, without having to miss any important material. This Advance Program provides you with the starting time for each paper. Taking of **pictures and videos** during sessions is **not permitted**.

A printed Supplement with speakers' visuals will be sent to all registered attendees within one month of the conclusion of ISSCC 2003. A CDROM containing both the ISSCC 2003 Digest of Technical Papers and the Visuals Supplement will be mailed in late Spring to speakers and all attendees paying the member or non-member Conference-registration fee.

Conference Information: Courtesy Associates; Phone: 202-973-8667; Fax: 202-973-8722; email: isscc@courtesyassoc.com

Press Information: Kenneth C. Smith, University of Toronto Phone: 416-978-5033; Fax: 416-971-2286; email: lcfujino@cs.com

Registration: Event Solutions Unlimited, P.O. Box 32862, Baltimore, MD 21282; Phone: 410-559-2236 or 1-800-937-8728; Fax: 410-559-2217; email: isscinfo@yesevents.com

ISSCC Website: www.isscc.org

Make the most of your trip to San Francisco! Visit the San Francisco Convention & Visitors Bureau Website at www.sfvisitor.org.

ISSCC 2003 is sponsored by the IEEE Solid-State Circuits Society. Co-sponsors are the IEEE San Francisco Section and Bay Area Council, and the University of Pennsylvania.

CONTENTS

T1: Basics of Serial Backplane Transceivers

This tutorial covers basic elements of the design of multi-gigabit-per-second serial transceivers for use in backplane applications. Sources of signal impairment, such as dielectric losses, reflections at connectors, crosstalk, and package limitations will be addressed. Channel modeling and measurement techniques will also be presented. Modulation and equalization techniques to overcome the bandwidth limitations will be covered, as well as practical considerations for the integration of multiple channels onto a large digital ASIC. An overview of clock-and-data-recovery circuits will be presented, and first-order circuit designs will be discussed. Finally, all aspects of the design of a serial transceiver will be reviewed in the context of a real-world example.

Instructor: Aaron Buchwald was born in Ames, IA, in 1960. He received the BSEE degree from the University of Iowa in 1982, and the MS and Ph.D degrees in electrical engineering from the University of California, Los Angeles, in 1984 and 1993, respectively. He has worked for Hughes Aircraft in El Segundo, CA, and Siemens in Munich, Germany. He was an Assistant Professor at The Hong Kong University of Science and Technology, and since 1994 has been with Broadcom Corporation in Irvine, CA.

T2: Design For Test and Debug

This tutorial is targeted towards the impact of design for test and debug on micro-architectural and circuit implementations. It will begin with review of failure mechanisms on chip, fault modeling, and Automatic Test Pattern Generation (ATPG). Then an overview of initial chip bring-up and qualification procedures will be presented, followed by scan methodologies and specific implementations of scan for latches and flip-flops; BIST for memory structures and regular logic; BISR and redundancy techniques for memory; An overview of JTAG interface; Implementation of on-chip logic analyzers and clock compression for debugging; Current and advanced chip probing techniques and FIB repair. Included, as well, will be discussion of various other test/debug techniques.

Instructor: Shannon Morton is a Chief Engineer in SGI's high-end MIPS microprocessor design team in Boston, MA, where he is the implementation leader for the L2 cache. In 1991, he graduated from the University of Adelaide, Australia, with a BE in electrical and electronic engineering, and again in 1996, with a Ph.D in asynchronous systems. From 1997 to 2001, he was a Principal Engineer at DEC/Compaq with the Alpha Microprocessor Design Team, where he contributed to the implementation of EV7. He lead the L2 cache design for EV8, working closely with the test group on various test/debug features such as BIST/BISR for memories, JTAG interfaces, OCLA, and clock compression. His interests include signal integrity, advanced circuits and technologies, and design for productivity.

T3: Introduction to BioMEMS

BioMEMS integrates microscale sensors, actuators, microfluidics, micro-optics, and structural elements with computation, communications, and controls. This tutorial presents an introduction to BioMEMS technology and its application to bioanalytical, surgical, and therapeutic microsystems with special emphasis on opportunity directions for the circuit designer. Basic concepts in biology needed to understand biochips will also be presented.

Instructor: Dennis Polla currently serves as President and CEO of the SurroMed Institute of Nanobiotechnology in Singapore. He has previously held faculty positions at Yale University and the University of Minnesota where he served as Director of the Biomedical Engineering Institute, Professor of Electrical Engineering, and Chairman of the Department of Biomedical Engineering. Dr. Polla studied electrical engineering at MIT and completed his Ph.D in MEMS at U.C. Berkeley.

T4: MRAM Technology & Circuits

Magnetoresistive Random-Access Memory (MRAM) technology is approaching manufacturing status. It promises the density and read-and-write performance of DRAM with the nonvolatility of hard-disk drives, but without the write-fatigue problems of EEPROMs or flash memory. This tutorial describes the fundamentals of MRAM technology starting with magnetoresistance and concentrating predominantly on Giant MagnetoResistance and Tunneling Magnetoresistance. Cell designs include the Pseudo-Spin Valve (PSV) and the Magnetic Tunnel Junction (MTJ) cell. Briefly described are the unique processes used for fabricating MRAMs and how these processes result in on-chip integration with circuits. The most common chip architectures for reading and writing data are described. Emphasis is placed on the MTJ cell because it appears to be closest to production. The basic properties of the MTJ cell lead to circuit-design constraints. The voltage across the tunnel junction is limited due to the thin dielectric used. Tunneling resistance is likely to have a wide tolerance due to its exponential dependence on dielectric thickness. Circuit challenges related to sensing data from the MTJ cell are discussed. Writing MTJ cells requires currents in two orthogonal lines, and relatively tight tolerances must be maintained in order for all cells in the memory array to operate properly. Finally, some challenges for future MRAM designs are identified, and some potential solutions to these challenges are discussed.

Instructor: James Daughton is Chief Technical Officer and a board member of NVE Corporation, which he founded in 1989. NVE specializes in products combining integrated circuits with advanced magnetic materials. Before founding NVE, Dr. Daughton spent over 15 years at Honeywell, managing solid-state research and development. Before that, he spent 10 years at IBM in Yorktown Heights and Burlington, working on magnetic and semiconductor memory devices. He received his BS, MS, and Ph. D degrees in electrical engineering in 1959, 1961, and 1963, respectively, from Iowa State University. He is a fellow of the IEEE, a member of the Magnetics Society, and an adjunct professor of physics at the University of Minnesota. He has published over 65 papers and has 19 issued patents, primarily dealing with thin magnetic films and devices. In 1994, Dr. Daughton was a Distinguished Lecturer for the Magnetics Society of the IEEE.

T5: Wireless LAN: Architectures and Design

An overview of competing wireless LAN architectures in the 2.4GHz and 5.0GHz spectra is presented. RF and analog requirements will be discussed. A detailed discussion of competing modem algorithms (OFDM, QAM, QPSK, CCK, etc.) will be presented, with advantages and disadvantages identified for each. Filtering requirements and some aspects of the software protocol stack will be compared. The tutorial will end with some implementation ideas for the harder issues, and a performance analysis for each system.

Instructor: David Shoemaker is VP of Engineering at Engim, in Acton, MA. Engim is a start-up focused on high-performance communications, currently targeted at Wireless LAN. David leads efforts in RF, analog, digital, and software systems at Engim, and is currently working on a 600Mb/s access point for wireless LAN. Previously, David was CTO for the Internet Infrastructure Business Unit at Texas Instruments, focusing on high performance network processing interfaces. David received his Ph.D, SM, and SB from MIT.

T6: Highly Integrated RF and Wirelss Transceivers

This tutorial provides an introduction to the challenges associated with highly-integrated RF and wireless transceivers. Both system-level and circuit-level challenges are addressed. The focus is on transceivers for high-data-rate systems such as EDGE, WCDMA, and 802.11, which require linearity in both the TX and RX paths. Some of the topics that will be addressed are architectures such as direct-conversion RX and TX which enable elimination of external components, circuit-level issues associated with implementing these architectures, the impact of finite isolation, and manufacturability.

Instructor: Tony Montalvo received his BS in Physics from Loyola University in 1985, his MSEE from Columbia University in 1987 and his Ph. D in electrical engineering from North Carolina State University in 1995. From 1987 to 1991, he was a flash-memory designer with AMD. From 1995 to 2000 he was with Ericsson in Research Triangle Park, NC, where he was the manager of the RF and Analog IC group. Since 2000, he has been the Director of the Analog Devices Raleigh Design Center. He is also an Adjunct Professor at North Carolina State University where he was named Outstanding Teacher in 1995. He holds 14 patents and has authored or co-authored 8 papers.

T7: DSL Splitters and Drivers

This tutorial will start with a general introduction to ADSL. The signal characteristics will be described with discussion on DMT-modulation, power level, crest factor, etc. Further along in the tutorial, the architecture of an ADSL analog front end will be shown emphasizing the design for performance. Some design, architecture and integration considerations will be reviewed. Attention will be given to the hybrid function showing the impact of the echo path. Line-driver characteristics and requirements, such as linearity and power dissipation, will be handled. Because of their importance, several classes/topologies of line drivers will be highlighted, with emphasis on their power dissipation. The issues of further density increase and possible solutions will be discussed. Finally, the POTS splitter function and its restrictions will be examined while looking for the possibilities for integration. The tutorial will end with an examination of the possibilities for the further evolution of ADSL towards higher bandwidth and more flexibility.

Instructor: Elve D. J. Moons was born in 1959 in Kermt, Belgium. He graduated from the Katholieke Universiteit Leuven in 1982, where he received a degree in electronic engineering. In the same year, he joined the microelectronics design group within Alcatel Bell in Antwerp, Belgium. There, he was active in the integration of telecommunication circuits, especially in the development of several generations of subscriber-line interface circuits. In the beginning he was a designer and later became ASIC team leader. For the past few years he has been involved in the development of ADSL analog front-end components while managing the analog ASIC design team within Alcatel in Antwerp, Belgium.

W1: Analog Telecom and Circuit Concepts

(Salon 7)

Organizer/Chair: Jan Sevenhans, *Alcatel BND*
Committee:
David Allstot, *University of Washington, Seattle, WA*
Russell Apfel, *Legerity, Austin, TX*
Franz Dielacher, *Infineon Technology Austria, Villach, Austria*
Kunihiko Iizuka, *Sharp, Tenri-shi, Japan*
Tetsuro Itakura, *Toshiba, Kawasaki-shi, Japan*
John Long, *Delft University of Technology, Mekelweg, The Netherlands*
Bram Nauta, *University of Twente, Enschede, The Netherlands*
Jan Sevenhans, *Alcatel BND, Antwerp, Belgium*
Trudy Stetzler, *Texas Instruments, Stafford, TX*
Hirotaka Tamura, *Fujitsu Laboratories, Kawasaki-shi, Japan*

Photons and electrons are competing to capture the backplane transceiver market in the next few years. Optical backplanes are coming, and integrated optics are in line as the next step. But electrical interconnect in the gigahertz range is the current bread and butter technology. Broadband Telecom is pushing this technology towards its natural limits, and will continue to do so in the next few years. Voltage-mode and current-mode I/O drivers and receivers are still driving electrons back and forth over the copper connections in the rack and in the PCBs of routers and gigahertz link equipment. Probably at some point, photons will take over this job and become the messengers for terabit connections.

This Workshop will challenge the experts in electrical and optical transceivers from the electrical or fibre optical interface circuits to the digital synchronisers for data recovery and system interface building blocks. It is a full day dedicated to the strongest technologies and circuits. Electrons and photons will exercise the minds of the speakers and the experts in the audience during the eight presentations and also in the concluding panel discussion.

Lunch and breaks are included in the registration fee. The workshop begins at 8:30 AM and ends at approximately 5:30 PM. If the workshop is full, the registering attendee will not be charged, or will be reimbursed after the Conference if a check was submitted.

Workshop Program

Time	Topics
8:00	BREAKFAST
8:30	**Welcome** **Jan Sevenhans,** *Alcatel BND*
8:40	**Electrical Backplane Interconnects to 12Gb/s and Beyond** **John T. Stonick,** *Accelerant*
9:25	**Optical Backplanes-Fact or Fiction?** **D. V. Plant,** *Photonics*
10:10	COFFEE BREAK
10:25	**Integrated Electrical Backplane Transceivers** **Kimo Tam,** *Analog Devices*
11:10	**High-Data-Bandwidth Transceivers for Multi-Channel Serial Data** **Muneo Fukaishi,** *NEC*
11:55	**The Future of Electrical Backplanes: High-Speed at Low-Cost** **Gerrit den Besten,** *Philips*
12:40	LUNCH
1:40	**Electrical Interconnect for Backplanes and Short (<30m) Cables** **Takeshi Horie,** *Fujitsu*
2:25	**Transponders and Transceivers for Serial and Parallel Optical Links** **Michael Neuhaeuser,** *Infineon*
3:10	**CMOS Capabilities for Electrical Backplane Transceivers** **Andy Joy,** *Texas Instruments*
3:55	PANEL DISCUSSION
4:40	**Conclusion**

W2: Implications of Near-Limit CMOS on Circuits and Applications

(Golden Gate B2/B3)

Organizers: Tak Ning, *IBM Research*
Stan Schuster, *IBM Research*

While technologists continue to provide us with ever-faster CMOS devices, it is clear that these fast devices have properties that were not seen in CMOS just a few years ago. From the perspective of circuits and applications, these unexpected properties are mostly detrimental, resulting in increasing challenges to circuits and systems designers. From the technologists' perspective, we are approaching the limits of scaled CMOS. Scaling degrades device characteristics challenging the circuits designer.

This workshop provides an open forum for discussions of the implications of evolving CMOS, near its limits, on circuits and applications. Invited speakers will lead off discussion on issues related to:

— CMOS near its scaling limits, status and future prospects
— Power and power density, issues at the chip and system levels
— Reliability, issues such as burn-in, soft error, error correction, etc.
— Gate current, its limits and effects on circuits
— Low-power designs, their benefits and potential pitfalls

Workshop Program

Time	Topics
8:00	BREAKFAST
8:30	**Welcome and Introduction**
8:40	**Challenges Near the Limits of CMOS Scaling** **Yuan Taur,** *University of California, San Diego, CA*
9:20	**Low-Power Technologies in the Near-Limit CMOS Regime** **Kazuo Yano,** *Hitachi, Tokyo, Japan*
10:00	COFFEE BREAK
10:30	**Infant-Mortality Control by Burn-In and by Design** **Shirley Glenn,** *Intel, Hillsboro, OR*
11:10	**Transistor and BEOL Tradeoffs in Near-Limit CMOS Technology** **Rich Klein,** *Advanced Micro Devices, Sunnyvale, CA*
11:50	LUNCH
1:00	**Effects of Gate Tunneling in Near-Limit CMOS Circuits** **Hisham Massoud,** *Duke University, Durham, NC*
1:40	**Low-Power Challenges for Digital CMOS Beyond 90nm** **Shekhar Borkar,** *Intel, Hillsboro, OR*
2:20	BREAK
2:50	**Design, Process and Environmental Contributors to Delay Variation** **Kerry Bernstein,** *IBM, Burlington, VT*
3:30	**Talk title TBD** **Rob Rutenbar,** *Carnegie Mellon University, Pittsburgh, PA*
4:10	**Conclusion**

SE1: Highlights of DAC

(Salon 7)

Organizer/Chair: **Steve Molloy,** Chief Architect, *Netergy Microelectronics, Santa Clara, CA*
Session Co-Chair: **Joseph Williams,** Distinguished Member of Technical Staff, *Agere Systems, Holmdel, NJ*

This special session contains four excellent presentations from the Design Automation Conference (DAC) held in June 2002. Each year DAC covers the latest in design methodologies and EDA tool developments, with a strong level of participation from both industry and academia. The four presentations in this session cover a variety of representative topics, including design methodology, analog and digital simulation techniques, and recent advancements in model development.

As designs become more and more complex, design-time windows are also becoming shorter. This creates an interesting challenge: to achieve fully-operational first silicon for designs of incredible complexity. The first presentation describes design methodologies and CAD-tool requirements for advanced 10MGate SoC design in the context of several large design examples.

The second presentation is by a DAC Best Paper Award winner, and describes a novel technique for mixing compiled-code and interpreted-code approaches to instruction-set simulation. Compiled-code simulators traditionally have the advantage of higher speed, though this comes with many restrictions including a requirement for static program code. This presentation demonstrates high performance with fewer restrictions using a just-in-time compilation technique. The approach is described in the context of several real-world processors including the ARM7 and ST200.

Frequency synthesizers are critical components in many important system-design areas such as wireless communications. Simulation places demanding requirements on both accuracy and simulation speed. The third presentation describes new simulation techniques for fractional-N synthesizers, and their application to a variety of circuits. The proposed techniques are shown to match closely with measured results, and are widely applicable to a variety of simulation frameworks.

In the past, it has been shown that the sizing of transistor-level analog and mixed-signal integrated circuits can be formulated as a geometric program. A particularly time-consuming and computationally expensive step in this process has always been the generation of analog performance models. The final presentation of the session describes design-automation techniques for generating high-quality analog performance models, replacing what, in the past, has been a manual process. The techniques are based on a new direct-fitting approach that efficiently fits model templates to numerical data from SPICE simulations.

SE1: Highlights of DAC

Time	Topics
7:30	**Challenges in Achieving First-Silicon Success for 10MGate SoCs: A Silicon Engineering Perspective** **Aurangzeb Khan,** Corporate Vice President/General Manager, *Cadence Design Systems, Sunnyvale, CA*
8:00	**A Universal Technique for Fast and Flexible Instruction-Set Architecture Simulation** **Achim Nohl,** *Aachen University of Technology, Aachen, Germany*
8:30	**Fast and Accurate Behavioral Simulation of Fractional-N Frequency Synthesizers and other PLL/DLL Circuits** **Michael H. Perrott,** Assistant Professor, *Massachusetts Institute of Technology, Cambridge, MA*
9:00	**An Efficient Optimization-Based Technique to Generate Posynomial Performance Models for Analog Integrated Circuits** **Walter P. Daems,** *Katholieke Universiteit, Leuven, Belgium* **Georges Gielen,** *Katholieke Universiteit, Leuven, Belgium* **Willy Sansen,** *Katholieke Universiteit, Leuven, Belgium*

SE2: Circuits in Emerging Technologies

(Salon 8)

Organizer: **Werner Simbuerger,** *Infineon, Corporate Research, Munich, Germany*
Chair: **Ian Young,** *Intel, Logic Technology Development, Hillsboro, OR*

Ubiquitous access to information, anywhere, anyplace, and anytime, will require whole new kinds of information systems. This demand for novel communication systems will translate into innovation in emerging technologies, circuit-design methodologies and fabrication techniques. At the core of these approaches, heavy emphasis is placed on finding the right match between circuit techniques and fabrication-process technology.

This Special-Topic Evening Session addresses circuit techniques that are emerging for both high-performance design at microwave frequencies and for future giga-scale integrated circuits. Some of these techniques include high-speed CMOS, SiGe, GaAs and InP, double-gate FinFET, and Carbon Nanotube technologies.

Recently, CMOS has been demonstrated to be a viable technology for very-high-bit-rate broadband circuit design at over 10Gb/s in highly integrated systems.

Meanwhile, advances in device scaling and doping-profile optimization have also resulted in SiGe bipolar transistors with impressive performance, including cut-off frequencies in the range of 200GHz. This makes them an attractive choice for applications at 40Gb/s and above.

Current InP bipolar integrated-circuits support high-performance mixed-signal applications at frequencies up to 200GHz. The high cut-off frequencies and high breakdown voltages present a unique combination which addresses some major issues.

With the scaling of device dimensions being the primary factor driving improvements in integrated circuit performance and cost, new device structures, such as FinFET, and new materials will be needed to overcome the technological challenges.

Finally, nanometer-scale electronic devices will not only be much smaller, but they must also operate according to designs and quantum-mechanical principles that are quite different from those employed by present-day microelectronic devices.

The speakers will present circuits and circuit techniques in these emerging technologies. In addition, they will address potential solutions for overcoming emerging challenges.

Time	Topics
7:30	**CMOS High-Speed Broadband Techniques** **Michael Green,** Professor, *University of California, Irvine, CA*
8:00	**Design of SiGe Bipolar Circuits for 40^{+}Gb/s Applications** **Herbert Knapp,** *Infineon Technologies, Corporate Research, Munich, Germany*
8:30	**Indium-Phosphide Bipolar Integrated Circuits: 40GHz and Beyond** **Mark Rodwell,** Professor, *University of California, Santa Barbara, CA*
9:00	**The Double-Gate FinFET: Device Impact on Circuit Design** **Ingo Aller,** *IBM Entwicklung GmbH, Boeblingen, Germany*
9:15	**Carbon Nanotubes: From Synthesis to Integration** **Hongjie Dai,** Associate Professor, *Stanford University, CA*

SE3: How Far Can Integration Go For 3G Cellphones?

(Salon 9)

Organizer: **William O. Camp, Jr.,** Senior Scientist, *Sony Ericsson Mobile Communications, Research Triangle Park, NC*

Chair: **Trudy Stetzler,** Senior Member of the Technical Staff, *Texas Instruments, Stafford, TX*

This special-topic session will use a 3G Cellular Phone as an example of the integration that should be possible in the near future for such devices. The first talk discusses the trends in cellular-phone integration and the architectural tradeoffs that must be made as further integration occurs. It will be shown that the requirements on these phones are increasing with each new standard as well as by the requirement for increased functionality that is expected by the user.

The second and third talks then discuss the baseband and RF sections of a cellular phone. The challenges to increased integration in each of these sections are discussed. Architectural options and tradeoffs are reviewed, and trends in each of these areas are demonstrated.

The last talk reviews these architectural tradeoffs in light of technology advances that might be expected to occur in the near- to mid-term time frame. Technological advances that are required to permit further integration with a simultaneous increase in performance are discussed.

Time	Topics
7:30	**System Requirements and Integration Trends** **Sven Mattisson,** Expert, Analog System Design, *Ericsson, Lund, Sweden*
8:00	**Integration of Analog, Digital and Power Regulation on a Chip** **James Mielke,** Director Systems and Architecture, *Motorola, Tempe, AZ*
8:30	**Advanced RF Integration** **William Krenik,** Wireless Advanced Architectures Manager, *Texas Instruments, Dallas, TX*
9:00	**Challenges and Future Trends** **John Long,** Professor, *Delft University of Technology, Delft, The Netherlands*

SESSION 1 SALON 7-9

PLENARY SESSION –– INVITED PAPERS

Chair: **Tim Tredwell,** *Eastman Kodak Research Labs, Rochester, NY*
ISSCC Executive-Committee Chair

Associate Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Program-Committee Chair

FORMAL OPENING OF CONFERENCE **8:30 AM**

1.1 No Exponential Is Forever: But "Forever" Can Be Delayed! **8:40 AM**

Gordon E. Moore
Intel (Retired)

By any measure, the semiconductor industry has experienced fantastic growth over the last 50 years. Starting from nothing, it has now passed $200 billion in annual revenue and has become the foundation of a trillion-dollar electronics industry. This unprecedented growth is the result of the combination of a unique technology and an extremely elastic market. Over this brief history, many parameters relating to the industry have changed approximately exponentially with time. These include chip complexity, chip performance, feature size, and the numbers of transistors produced each year. This talk will explore some of these trends, and will look at the current status of silicon technology, and at challenges going forward.

ISSCC, SSCS, JSSC, & IEEE AWARD PRESENTATIONS **9:30 AM**

BREAK 10:00 AM

1.2 Perspectives on Power-Aware Electronics

10:15 AM

Takayasu Sakurai
University of Tokyo, Tokyo, Japan

In the coming ubiquitous IT society, low-power design is one of the key features at which the VLSI designer should aim. Otherwise, power increase will remain as one of the main obstacles to Moore's law growth. Unless VLSI power is lowered by orders of magnitude, we cannot enjoy the progress that scaling offers.

This talk will cover what we now have, and what we should provide in our low-power armory to allow us to cope with ever-increasing leakage loss, as well as dynamic power. The techniques to be presented range over the system, software, circuit, and device level including interconnect and I/O issues. The novel trend is to examine cooperative approaches between levels such as software-circuit cooperation and circuit-technology cooperation.

The biggest challenge that System-on-Chip designers must resolve in the future is the fact that transistors for digital and memory circuits will be more and more leaky as technology generations advance. Approaches to solving this serious problem will be described. Beyond the quest for low-power solutions lies a promising world of ubiquitous VLSI devices and products ranging from “wireless sensors and tags for everything” to “everything-you-must-do mobile terminals”.

1.3 Interfacing Electronic Systems to the External World: The New Challenge!

11:05 AM

Bruno Murari
STMicroelectronics, Cornaredo, Italy

The dramatic evolution of semiconductor technology over the last 50 years has a real industrial and social revolution that is still ongoing today. The started progress from single-transistor to ULSI circuits has been very fast. As technology proceeded according to the well-known Moore’s Law, circuit-design techniques moved more and more from analog to digital following the continuous progress made in microlithography.

While there has been a corresponding huge increase in the computing power of digital circuits, this has not been accompanied by a comparable evolution in the capability of integrated circuits to interface to the external world. For free-standing computers, speed is the key factor. In other applications such as mobile phones, the interfaces with the external world are fundamental and provide the driving force in the evolution of these products. Technologies like BiCMOS, HVCMOS and BCD, which are already available and will further evolve in the future, appear to be more suitable than pure CMOS in satisfying those needs. We are moving now to SoC (System on Chip) and in the future to SiP (System in Package) techniques that will include also micromachined and, even, photonic technologies.

In this paper, both recent and future developments in analog interfaces will be analyzed, with particular attention given to the problem of power-consumption reduction in portable devices. As well, an overview of new applications of MEMS and photonic devices will be presented.

MULTIMEDIA SIGNAL PROCESSING

Chair: **Albert Van der Werf,** *Philips Research Laboratories, Eindhoven, The Netherlands*
Associate Chair: **Hideto Hidaka,** *Mitsubishi Electric Hyogo, Japan*

2.1 A Fully-Integrated 0.13μm CMOS Mixed-Signal SoC for DVD Player Applications

1:30 PM

K. Okamoto, T. Morie, A. Yamamoto, K. Nagano, K. Sushihara, H. Nakahira, R. Horibe, K. Aida, T. Takahashi, M. Ochiai, A. Soneda, T. Kakiage, T. Iwasaki, H. Taniuchi, T. Shibata, T. Ochi, M. Takiguchi, T. Yamamoto, T. Seike, A. Matsuzawa
Matsushita Electric Industrial, Moriguchi, Japan

A mixed-signal SoC for DVD applications is designed in 0.13μm 1P 6M CMOS. One DSP, two 32b RISC CPUs, three dedicated processing units, PRML read channel with an analog front end (AFE) and several other sub-systems are integrated on the same die. The AFE contains a 5th-order G_m-C filter and over 66dB C/N. The SoC contains 24M transistors in a 64mm^2 die and consumes 1.5W at 40MS/s which corresponds to 1.5x DVD playback.

2.2 A Single-Chip MPEG2 CODEC for DVD+RW

2:00 PM

J. Geerlings[1], E. Desmicht[2], H. de Perthuis[2]
[1]Philips Semiconductors, Eindhoven, The Netherlands
[2]Philips Semiconductors, Caen, France

A single-chip MPEG2 audio/video encoder and decoder is designed for consumer digital recording systems. The chip includes a CPU core with peripherals, a PCI/XIO bus interface, data streaming units to data sources and sinks, graphics engines, video display units and video DACs. The chip contains 32M transistors in 102mm^2 and is fabricated in a 0.18μm 6M CMOS process.

2.3 A 160mW, 80nA Standby, MPEG-4 Audiovisual LSI with 16Mb Embedded DRAM and a 5GOPS Adaptive Post Filter

2:30 PM

H. Arakida[1], M. Takahashi[1], Y. Tsuboi[1], T. Nishikawa[1], H. Yamamoto[1], T. Fujiyoshi[1], Y. Kitasho[1], Y. Ueda[1], M. Watanabe[1], T. Fujita[1], T. Terazawa[2], K. Ohmori[2], M. Koana[2], H. Nakamura[3], E. Watanabe[1], H. Ando[1], T. Aikawa[1], T. Furuyama[1]
[1]Toshiba, Kawasaki, Japan
[2]Toshiba Microelectronics, Kawasaki, Japan
[3]Toshiba Information Systems, Kawasaki, Japan

A single-chip MPEG4 audiovisual LSI in a 0.13μm 5M CMOS technology with 16Mb embedded DRAM is presented. Four 16b RISC processors and dedicated hardware accelerators including a 5GOPS post filtering engine are integrated on the IC. The chip consumes 160mW at 125MHz and uses 80nA in the standby mode. This LSI handles MPEG4 CIF video encoding at 15frames/s and audio encoding simultaneously.

BREAK 3:00 PM

2.4 A 210mW Graphics LSI Implementing Full 3D Pipeline with 264Mtexels/s Texturing for Mobile Multimedia Applications

3:15 PM

R. Woo[1], S. Choi[1], J-H. Sohn[1], S-J. Song[1], Y-D. Bae[1], C-W. Yoon[1], B-G. Nam[1], J-H. Woo[1], S-E. Kim[1], I-C. Park[1], S. Shin[2], K-D. Yoo[2], J-Y. Jung[2], H-J. Yoo[1]
[1]KAIST, Daejeon, Republic of Korea
[2]Hynix Semiconductor, Icheon, Republic of Korea

A 121mm^2 graphics LSI is for portable 2D/3D graphics and MPEG4 applications. The LSI contains a RISC processor with MAC, a 3D rendering engine, 29Mb DRAM and is built in a 0.16μm pure DRAM technology. Programmable clocking allows the LSI to operate in several power modes for various applications. In lower cost mode, power consumption is under 210mW, delivering 264M texture mapped pixels per second.

2.5 Image Processor Capable of Block-Noise-Free JPEG2000 Compression with 30frames/s for Digital Camera Applications

3:45 PM

H. Yamauchi, S. Okada, K. Taketa, T. Ohyama, Y. Matsuda, T. Watanabe, S. Okada, T. Mori, Y. Matsuo, Y. Yamada, T. Ichikawa, Y. Matsushita, A. Kobayashi
Sanyo Electric, Gifu, Japan

A one-chip image processor for next-generation digital cameras and broadband PDAs multimedia mobile phones is described. It is capable of processing JPEG2000 data with 30frames/s and a 27MHz operating frequency. The process is fabricated in 0.25μm CMOS and contains 8.5M transistors in a 103mm^2 area.

2.6 A 51.2GOPS Scalable Video Recognition Processor for Intelligent Cruise Control Based on a Linear Array of 128 4-Way VLIW Processing Elements

4:15 PM

S. Kyo, T. Koga, S. Okazaki, R. Uchida, S. Yoshimoto, I. Kuroda
NEC, Kawasaki, Japan

A 51.2GOPS fully programmable and scalable video recognition processor is based on a linear connection of 128 4-way VLIW processing elements and an asynchronous data mapping mechanism. Execution is under 33ms/frame for complex weather robust road area/lane marking vehicle detection. The chip contains 21.4M transistors in 121mm^2 area fabricated in 0.18μm 7M CMOS.

2.7 A 1GOPS Reconfigurable Signal Processing IC with Embedded FPGA and 3-Port 1.2GB/s Flash Memory Subsystem

4:45 PM

M. Borgatti, L. Calì, G. De Sandre, B. Forêt, D. Iezzi, F. Lertora, G. Muzzi, M. Pasotti, M. Poles, P. Rolandi
STMicroelectronics, Agrate Brianza, Italy

A 1GOPS dynamically reconfigurable processing unit with embedded flash memory and SRAM-based FPGA for image/voice processing/recognition applications is described. Code, data and FPGA bitstreams are stored in the embedded flash memory and are independently accessible through 3 content-specific, 64b I/O ports with a peak read rate of 1.2GB/s. The system is implemented in a 0.18μm 2P 6M CMOS flash technology with a chip area of 70mm^2.

CONCLUSION 5:15 PM

OVERSAMPLED A/D CONVERTERS

Chair: **Brian Brandt,** *Maxim Integrated Products, North Chelmsford, MA*
Associate Chair: **David Johns,** *University of Toronto, Toronto, Canada*

3.1 A 1.5V 1mA 72dB Passive ΣΔ ADC for a GSM Transceiver in 0.13μm Digital CMOS

1:30 PM

F. Chen, S. Ramaswamy, B. Bakkaloglu
Texas Instruments, Dallas, Texas

A passive switched-capacitor ΣΔ ADC consisting of only switches, capacitors and a comparator, is implemented in a 0.13μm digital CMOS process. This high-speed low-voltage architecture is used in a zero-IF GSM transceiver and has a measured peak SNDR of 67dB over a bandwidth of 100kHz with a SFDR of 75dB and a dynamic range of 72dB. The ADC consumes 1mA from a 1.5V power supply at a clock rate of 104MHz.

3.2 A 114dB 68mW Chopper-Stabilized Stereo Multi-Bit Audio A/D Converter

2:00 PM

Y. Yang[1], A. Chokhawala[1], M. Alexander[2], J. Melanson[1], D. Hester[1]
[1]Cirrus Logic, Austin, TX
[2]Design Consultant, Austin, TX

A fifth-order single-loop seventeen level ΣΔ modulator with an input feedforward gain stage and second-order mismatch shaping logic achieves 114dB dynamic range and -105dB THD over the 20kHz audio band. This stereo ADC occupies 5.62mm^2 active area in a 0.35μm 2P 3M CMOS process and dissipates only 55mW power in the analog circuits.

3.3 A 1.2V Dual-Mode WCDMA/GPRS ΣΔ Modulator

2:30 PM

A. Dezzani, E. Andre
STMicroelectronics, Crolles, France

A dual-mode ΣΔ modulator is designed to meet the specifications of a WCDMA/GPRS receiver and is composed of a single-bit second-order modulator followed by a multi-bit stage that adapts performance to broadband signals. The modulator achieves 82dB and 70dB of dynamic range over bandwidths of 100kHz and 1.92MHz, respectively, and dissipates 4.3mW from a 1.2V supply. The circuit is implemented in 0.13μm CMOS technology and occupies an active area of 0.2mm^2.

BREAK 3:00 PM

3.4 A Tri-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver

3:15 PM

R. van Veldhoven
Philips Research, Eindhoven, The Netherlands

Complex continuous-time fifth-order ΣΔ modulator with 1b quantizer and switched-capacitor feedback DAC for a GSM/CDMA2000/UMTS receiver achieves a dynamic range of 92/83/74dB in 200/1228/3840kHz. Power consumption of one modulator is 3.8/4.1/4.5mW at 1.8V. Processed in 0.18μm CMOS, the 0.55mm^2 IC includes a PLL, two oscillators and a bandgap reference.

3.5 A Continuous-Time ΣΔ Modulator with 88dB Dynamic Range and 1.1MHz Signal Bandwidth

3:45 PM

S. Yan[1], E. Sánchez-Sinencio[2]
[1]University of Texas, Austin, TX
[2]Texas A&M University, College Station, TX

A baseband continuous-time multi-bit ΣΔ modulator achieves 88dB dynamic range over a 1.1MHz signal bandwidth consuming 62mW from a 3.3V supply. Excess loop delay encountered in conventional continuous-time modulators is eliminated by the proposed architecture. Clock-jitter sensitivity is considerably reduced compared with prior designs.

3.6 A 4.4mW 76dB Complex ΣΔ ADC for Bluetooth Receivers

4:15 PM

K. Philips
Philips Research, Eindhoven, The Netherlands

A ΣΔ ADC with a fifth-order continuous-time complex loop filter achieves 76dB of DNR in a 1MHz channel. The input impedance is less than 400Ω and allows operation with a current-mode RF front-end. Image rejection is over 50dB, and IM3 distortion is below -82dBc. The circuit dissipates 4.4mW and is implemented in 0.18μm CMOS.

3.7 A Dual Channel ΣΔ ADC with 40MHz Aggregate Signal Bandwidth

4:45 PM

A. Tabatabaei, K. Onodera, M. Zargari, H. Samavati, D. Su
Atheros Communications, Sunnyvale, CA

A dual-channel ΣΔ ADC has been integrated in 0.13μm CMOS technology with an oversampling ratio of 4. The ADC employs a cascade of low-pass and band-pass modulators and achieves an aggregate quadrature signal bandwidth of 40MHz at a sampling frequency of 160MS/s and 54dB dynamic range while dissipating 175mW from a 2.5V supply.

CONCLUSION 5:15 PM

CLOCK RECOVERY AND BACKPLANE TRANSCEIVERS

Chair: **Larry DeVito,** *Analog Devices, Wilmington, MA*
Associate Chair: **Stefanos Sidiropoulos,** *Aeluros, Mountain View, CA*

4.1 A 10Gb/s/ch, 50mW 120×130μm² Clock and Data Recovery Circuit

1:30 PM

S. Kaeriyama, M. Mizuno
NEC, Sagamihara, Japan

A 10Gb/s clock and data recovery circuit for SerDes macro uses half the power and a quarter the die size of prior art. In 0.15μm CMOS the CDR dissipates 50mW in an area of 120×130μm² while maintaining a 10Gb/s bandwidth per channel. Jitter tolerance is also improved and the influence of PVT variations is reduced.

4.2 A CMOS Multi-Channel 10Gb/s Transceiver

2:00 PM

H. Takauchi[1], H. Tamura[1], S. Matsubara[2], M. Kibune[1], Y. Doi[1], T. Chiba[3], H. Anbutsu[1], H. Yamaguchi[1], T. Mori[1], M. Takatsu[1], K. Gotoh[1], T. Sakai[4], T. Yamamura[4]
[1]Fujitsu Laboratories, Kawasaki, Japan
[2]Fujitsu LSI Solutions, Kawasaki, Japan
[3]Fujitsu Higashi-Nihon Digital Technology, Sapporo, Japan
[4]Fujitsu, Akiruno, Japan

A quad 10Gb/s transceiver in 0.11μm CMOS communicates electric signals over balanced copper media. The transceiver uses a single 1.2V power supply and dissipates 415mW per channel. One PLL supplies a reference clock to two transmitter channels and two receiver channels. The transceiver contains analog front ends, clock recovery units, and 312MHz parallel interfaces.

4.3 A Second-Order Semi-Digital Clock Recovery Circuit Based on Injection Locking

2:30 PM

M-J. Lee[1], W. Dally[2], J. Poulton[1], T. Greer[1], J. Edmondson[1], R. Farjad-Rad[1], H-T. Ng[1], R. Rathi[1], R. Senthinathan[1]
[1]Velio Communications, Milpitas, CA
[2]Stanford University, Stanford, CA

A 3.125Gb/s clock recovery circuit in 0.18μm CMOS comprises a multiplying delay-locked loop (MDLL), an injection-locked slave oscillator and a phase control unit. Injection locking reduces MDLL clock distortion and varies the delay of the recovered clock, while a frequency loop in the phase control unit ameliorates the trade off between phase wander and frequency tolerance. Experimental results show high frequency jitter tolerance is improved by 0.08UI.

BREAK 3:00 PM

4.4 A 2.5 - 10Gb/s CMOS Transceiver with Alternating Edge Sampling Phase Detection for Loop Characteristic Stabilization

3:15 PM

B-J. Lee[1], M-S. Hwang[1], S-H. Lee[2], D-K. Jeong[1]
[1]Seoul National University, Seoul, Republic of Korea
[2]Silicon Image, Sunnyvale, CA

A 2.5 to 10Gb/s CMOS transceiver in 0.18µm CMOS dissipates 540mW from a 1.8V supply with a BER better than 10^{-12}. CDR loop characteristics are stabilized across various jitter environments with small hardware overhead using an alternating edge sampling phase detector.

4.5 8Gb/s Differential Simultaneous Bidirectional Link With 4mV 9ps Waveform Capture Diagnostic Capability

3:45 PM

B. Casper, A. Martin, J. Jaussi, J. Kennedy, R. Mooney
Intel Labs, Circuit Research, Hillsboro, OR

Differential simultaneous bidirectional I/O circuits in 0.18µm CMOS operate up to 8Gb/s with BER better than 10^{-11} using 32b LFSR. The cell area is 0.13mm^2 and the dissipation is 120mW. On-die diagnostic measurement of individual I/O link performance is enabled with a variable offset comparator and clock phase interpolator with resolution of 4mV and 9ps.

4.6 Equalization and Clock Recovery for a 2.5 - 10Gb/s 2-PAM/4-PAM Backplane Transceiver Cell

4:15 PM

J. Zerbe[1], C. Werner[1], V. Stojanovic[1], F. Chen[1], J. Wei[1], G. Tsang[1], D. Kim[1], W. Stonecypher[1], A. Ho[1], T. Thrush[1], R. Kollipara[1], G-J. Yeh[1], M. Horowitz[2], K. Donnelly[1]
[1]Rambus, Los Altos, CA
[2]Stanford University, Stanford, CA

A backplane transceiver uses a folded 5-tap TX equalizer and 5-tap RX equalizer to counteract losses and reflections. A flexible 2-PAM/4-PAM CDR uses select transitions for receive clock recovery. BER better than 10^{-15} at 10Gb/s and power <60mW/Gb are measured values for a 16" backplane with two high speed connectors.

4.7 A 2.7Gb/s CDMA-Interconnect Transceiver Chip Set with Multi-Level Signal Data Recovery for Re-Configurable VLSI Systems

4:45 PM

Z. Xu[1], H. Shin[2], J. Kim[1], F. Chang[1], C. Chien[1]
[1]University of California, Los Angeles, CA
[2]Qualcomm, San Diego, CA

A 2.7Gb/s interconnect transceiver chip-set based on Code Division Multiple Access (CDMA) is described and implemented in 0.18µm CMOS technology to achieve real-time system re-configurability and multiple I/O communication. The transceiver chip-set, with an Alexander-type multi-level data recovery circuit, can reconfigure multiple I/O signal routes within a symbol period of 0.8ns. The chip-set dissipates 74mW and occupies 0.3mm^2 per I/O pair.

CONCLUSION 5:15 PM

WIRELESS PAN TRANSCEIVERS

Chair: **Thomas Lee,** *Stanford University, Stanford, CA*
Associate Chair: **Mary Jo Nettles,** *Mobilian, San Diego, CA*

5.1 A Dual-Mode 802.11b/Bluetooth Radio in 0.35μm CMOS

1:30 PM

H. Darabi[1], J. Chiu[1], S. Khorram[1], H. Kim[1], Z. Zhou[1], S. Jiang[1], K. Evans[2], E. Chien[1], B. Ibrahim[1], E. Geronaga[1], L. Tran[1], R. Rofougaran[1]
[1]Broadcom, El Segundo, CA
[2]SolarFlare Communications, Irvine, CA

A dual-mode CMOS 2.4GHz transceiver consumes 65mA in RX and 78mA in TX from a 3V supply. The receiver achieves a typical sensitivity of -88dBm at 11Mb/s for 802.11b, and -83dBm for Bluetooth mode. The receiver minimum IIP3 is -8dBm, and the transmitter delivers a nominal output power of 0dBm, with a power control range of 20dB in 2dB steps.

5.2 A 2.4GHz Dual-Mode 0.18μm CMOS Transceiver for Bluetooth and 802.11b

2:00 PM

T. Cho[1], D. Kang[1], S. Dow[2], C-H. Heng[1], B. Song[3]
[1]Wireless Interface Technologies, San Diego, CA
[2]Santel Networks, Newark, CA
[3]University of California, San Diego, CA

A 2.4GHz dual-mode RF transceiver IC implements transmit and receive functions for both Bluetooth with -80dB sensitivity and 802.11b Wireless LAN with -88dB sensitivity in a single chip without doubling the required silicon area. Implemented in 0.18μm CMOS process, the circuit operates at 1.8V, and die size is 16mm^2 including pads.

5.3 A 43mW Bluetooth Transceiver with -91dBm Sensitivity

2:30 PM

C. Cojocaru[1], T. Pamir[1], F. Balteanu[1], A. Namdar[1], D. Payer[2], I. Gheorghe[1], T. Lipan[1], K. Sheikh[1], J. Pingot[1], H. Paananen[3], M. Littow[2], E. Macrobbie[1], M. Cloutier[1]
[1]Skyworks Solutions, Ottawa, Ontario, Canada
[2]Conexant Systems, San Diego, CA
[3]Nokia Research Center, Tokyo, Japan

A Bluetooth transceiver has -91dBm sensitivity while drawing 24mA from a 1.8V supply. The receiver has a low-IF path with 30dB image and 9dB co-channel rejection, 80dB of AGC, digital equalization and complex PLL demodulation. The transmitter uses direct two-point modulation and draws 18mA at +6dBm output power. The DS PLL settles in 100μs. LDO regulators power the analog and digital sections.

BREAK 3:00 PM

5.4 An Experimental Coin-sized Radio for Low Power WPAN (IEEE 802.15.4) Applications at 2.4GHz

3:15 PM

P. Choi, H. Park, I. Nam, K. Kang, Y. Ku, S. Shin, S. Park, T. Kim, B. Kim, H. Choi, S. Kim, S. Park, M. Kim, S. Park, K. Lee
KAIST, Daejeon, Republic of Korea

A 2.4GHz radio for IEEE 802.15.4 WPANs using 0.18µm CMOS technology consumes 21mW and 30mW at 1.8V supply in RX and TX mode, respectively. The receiver utilizes a low-IF architecture with a poly-phase filter and transistor linearization technique. A ROM-based DSSS GMSK signal is directly up-converted using I/Q mixing. Silicon area is 8.75mm^2.

5.5 A Single-Chip CMOS Bluetooth Transceiver with 1.5MHz IF and Direct Modulation Transmitter

3:45 PM

H. Ishikuro, M. Hamada, K. Agawa, S. Kousai, H. Kobayashi, D. Nguyen, F. Hatori
Toshiba, Kawasaki, Japan

A single-chip Bluetooth transceiver in 0.18µm CMOS integrates a direct VCO modulation transmitter and 1.5MHz-IF receiver to reduce power consumption and cost. The receiver achieves a sensitivity of -77dBm and transmitting power of +4dBm.

5.6 A Low Power CMOS Bluetooth Transceiver with a Digital Offset Canceling DLL-Based GFSK Demodulator

4:15 PM

C-H. Park[1], S. Byun[2], Y. Song[2], S. Wang[2], C. Conroy[3], B. Kim[3]
[1]Stelsys Telecom, Seoul, Republic of Korea
[2]KAIST, Daejeon, Republic of Korea
[3]Berkana Wireless, San Jose, CA

A 0.18µm CMOS Bluetooth IC consumes 33mA in RX mode and 25mA in TX mode. The IC has a DLL-based GFSK demodulator with frequency offset cancellation. The receiver has -78dBm sensitivity at 0.1% BER, and the transmitter delivers a nominal 0dBm power level with 20dB control.

5.7 CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise

4:45 PM

A. Ismail, A. Abidi
University of California, Los Angeles, CA

A 1.5GHz CMOS differential VCO reduces the spectral density of up-converted flicker noise by 20dB, thereby reaching the phase noise target of -105dBc/Hz at 50kHz offset required for the PDC receive VCO. Flicker noise is suppressed by this amount across almost the entire tuning range from 1.43 to 1.64GHz, while drawing 6mA from a 2.7V supply.

CONCLUSION 5:00 PM

LOW-POWER DIGITAL TECHNIQUES

Chair: **Ron Preston,** *Intel, Shrewsbury, MA*
Associate Chair: **Masayuki Mizuno,** *NEC, Sagamihara-shi, Kanagawa, Japan*

6.1 Dynamic-Sleep Transistor and Body Bias for Active Leakage Power Control of Microprocessors

1:30 PM

J. Tschanz, S. Narendra, Y. Ye, B. Bloechel, S. Borkar, V. De
Intel, Hillsboro, OR

Sleep transistors and body bias are used to control active leakage for a 32b integer execution core implemented in a 100nm dual V_T CMOS technology. A PMOS sleep transistor degrades performance by 4% but offers 20X leakage reduction which is further improved with body bias. Time constants for leakage convergence range from 30ns to 300ns allowing 9-44% power savings for idle periods greater than 100 clock cycles.

6.2 A Shared-Well Dual-Supply-Voltage 64-bit ALU

2:00 PM

Y. Shimazaki[1], R. Zlatanovici[2], B. Nikolic[2]
[1]Hitachi, Tokyo, Japan
[2]University of California, Berkeley, CA

A shared N-well, dual-supply-voltage 64b ALU module in 0.18µm, 1.8V CMOS 1P 5M technology operates at 1.16GHz on a 9mm^2 die. For a target delay increase of 2.8%, energy savings are 25.3% using dual supplies. An 8.3% increase in delay, saves 33.3% in energy.

6.3 0.5V, 400 MHz, V_{DD}-Hopping Processor with Zero V_{TH} FD-SOI Technology

2:30 PM

H. Kawaguchi[1], T. Miyazaki[2], D. Yamada[2], D. Antono[2], S. Hattori[3], K. Kanda[2], K. Nose[4], K. Inagaki[2], T. Hiramoto[2], T. Sakurai[2]
[1]University of Tokyo, Tokyo, Japan
[2]University of Tokyo, Tokyo, Japan
[3]KDDI, Tokyo, Japan
[4]NEC, Tokyo, Japan

A 0.5V, 400MHz, 3.5mW, 16b RISC processor with a 0.25µm, dual V_{TH}, fully-depleted SOI technology is presented. Zero V_{TH} is used in logic for high speed while memories and register files adopt a higher V_{DD} and V_{TH} to suppress leakage. Experimental results show that V_{DD}-hopping is effective in leakage dominant environments.

BREAK 3:00 PM

6.4 An Autonomous Decentralized Low-Power System with Adaptive-Universal Control for a Chip Multi-Processor

3:15 PM

M. Miyazaki, G. Ono, H. Tanaka, N. Ohkubo, T. Kawahara
Hitachi, Central Research Laboratory, Tokyo, Japan

A technique for adaptive-universal control of clock frequency, supply voltage, and body bias optimizes the performance-to-power ratio of chip multiprocessors. The technique is based on a compound built-in self-test and self-instructed look-up table scheme for an autonomous and decentralized system. Applied to a 32b ALU, power is reduced by seventy times.

6.5 A 400MHz 183mW Microcontroller in Body-Tied SOI Technology

3:45 PM

H. Sato, N. Itoh, K. Yoshida, Y. Nakase, H. Makino, A. Yamada, T. Arakawa, S. Iwade, T. Ipposhi
Mitsubishi Electric, Hyogo, Japan

A low-power microcontroller is designed in 0.10μm body-tied SOI CMOS technology by reusing existing design resources developed in 0.18μm bulk CMOS. Only two new masks are needed for this work. The performance is evaluated by simulations and indicates operation at 400MHz with 183mW dissipation at 0.8V and represents a five-times improvement in power-delay product.

6.6 A 3.5GHz 32mW 150nm Multiphase Clock Generator for High-performance Microprocessors

4:15 PM

A. Alvandpour[1], R. Krishnamurthy[1], D. Eckerbert[2], S. Apperson[1], B. Bloechel[1], S. Borkar[1]
[1]Intel, Hillsboro, OR
[2]Chalmers University, Goteborg, Sweden

A 3.5GHz 8-phase all-digital clock generator is fabricated in 150nm CMOS to achieve scalable 1.7x frequency-range and 9ps end-to-end time resolution measured at 1.6V, 110°C. A closed-to-open loop control scheme enables 32mW open-loop power consumption, 300μW at clock gate-off, zero-cycle response during clock re-enable, and <4% static phase error.

6.7 A 0.3V 3.6GHz 0.3mW Frequency Divider with Differential ED-CMOS/SOI Circuit Technology

4:45 PM

T. Douseki[1], T. Shimamura[1], N. Shibata[2]
[1]NTT, Atsugi, Japan
[2]NTT Electronics, Tokyo, Japan

A differential ED-CMOS/SOI circuit combines both zero V_T CMOS/SOI and ED-MOS/SOI circuits and operates at supply voltages as low as 0.3V. An experimental frequency divider, fabricated in a 0.25μm fully-depleted SOI process, achieves a maximum operating frequency of 3.6GHz at 0.3V and 5.4GHz at 0.5V while reducing power dissipation to less than 1mW.

6.8 A 9μW 50MHz 32b Adder Using a Self-Adjusted Forward Body Bias in SoCs

5:00 PM

K. Ishibashi, T. Yamashita, Y. Arima, I. Minematsu, T. Fujimoto
STARC, Yokohama, Japan

This 32b adder in a 0.13μm CMOS process consumes 9μW at 50MHz and 0.3V and operates at 500MHz at 0.6V. Forward body biases are self-adjusted to minimize the threshold voltage and reduce PVT dependence. The power of the SoC can be reduced to 1/4 that of standard CMOS by gating the forward body bias in the IP blocks.

CONCLUSION 5:15 PM

E1: Analog IP –– Stairway to SoC Heaven?

(Salon 7)

Organizer: **Rudolf J. Koch,** *Infineon Technologies, Munich, Germany*
Moderator: **Franz Dielacher,** *Infineon Technologies, Villach, Austria*

Exploding costs in ultra-deep-submicron technologies make any redesign extremely expensive. Stringent time-to-market constraints and fast-technology evolutions are putting the analog designers under high pressure. Fast safe design and implementation of analog functions is therefore urgently needed. In the past, analog synthesis has promised these benefits, yet has failed. Is Analog IP to be the next vision doomed to failure? Can new, less-ambitious paradigms finally make analog Electronic Design Automation (EDA) for SoC a success story? Or, will SoC prove to be a short-lived vision?

Panelists:

Yousif Ammar, CEO, *XIGNAL, Unterhaching, Germany*
Georges Gielen, Professor, *Katholieke Universiteit Leuven, Leuven, Belgium*
Thomas Heydler, President/CEO, *Barcelona Design, Newark, CA*
Masao Hotta, Senior Chief Engineer & General Manager, *Hitachi, Gunma-ken, Japan*
Philippe Magarshack, Vice-President, *STMicroelectronics Central R&D Group, Crolles, France*
Jean-Francois Pollet, COO, *Dolphin Integration, Meylan, France*
Bill Redman-White, Fellow, *Philips, Semiconductor* / Professor, *Southampton University, United Kingdom*

E2: Will MEMS, Imagers, and Displays Be Key to the Growth of the IC Industry?

(Salon 8)

Organizer: **Khalil Najafi,** Professor, *Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI*
Moderator: **Kensall D. Wise,** Professor, *Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI*

This panel will discuss how the IC industry can tap into new markets driven by imagers/displays/MEMS. The panelists will tackle several questions: Will the IC industry continue to grow based only on faster/bigger digital/analog chips? Will computing and communications be the biggest growth markets for ICs, or will imagers/displays/MEMS needed in toys, healthcare, environmental sensing, etc. help expand the applications of ICs? Will there be more MEMS on IC chips? Will conventional ICs become only a small part of microsystems as MEMS/imagers/displays take away a bigger piece of the system's pie?

Panelists:

Yoshiaki Hagiwara, Principal Engineer, *Sony, Tokyo, Japan*
Christofer Hierold, Professsor, *Swiss Federal Institute of Technology, Zurich, Switzerland*
Roger Howe, Professor, *Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA*
R. Daniel McGrath, *Andover, MA*
Clark C.T. Nguyen, Program Manager, *Microsystems Technology Office, DARPA*
Ray Roop, Director, *Strategic Technology, Sensor Products Division, Motorola, Tempe, AZ*

E3: Good, Bad, Ugly –– 50 Years of Memory Evolution. What Next?

(Salon 9)

Organizer: **John Barth,** Senior Engineer, *IBM Microelectronics, Burlington, VT*
Moderator: **Sreedhar Natarajan,** Design Manager, *Mosys, Kanata, Canada*

In light of the up-coming 50th anniversary of the ISSCC, the memory sub-committee has chosen to review memory evolution over the past 50 years. This panel will address the surviving innovative memory technologies as well as the failures in memory technology. Many memory technologies have come and gone (CCD, Bubble, etc.). The panelists will isolate the good, bad and the absolutely impractical (or ugly) memory technologies in the last 50 years.

Panelists:

Howard Kalter, President, *HLK, Burlington, VT*
Dick Foss, Chairman, *Mosaid Technologies, Calabogie, Canada*
Adin Hyslop, Director of Design, *Ramtron International, Colorado Springs, CO*
Changhyun Kim, Vice President, Memory Division, *Samsung, Hwasung, Republic of Korea*
Joel Karp, Consultant, *Atherton, CA*
Roelof Salters, Research Fellow, *Philips Semiconductors, Eindhoven, The Netherlands*

DACS AND AMPS

Chair: **Ken Poulton,** *Agilent Laboratories, Palo Alto, CA*
Associate Chair: **Roy Scott Kaller,** *Standard Microsystems, Phoenix, AZ*

7.1 A 16b 400MS/s DAC with -80dBc IMD to 300MHz and -160dBm/Hz Noise Power Spectral Density

8:30 AM

W. Schofield, D. Mercer, L. St. Onge
Analog Devices, Wilmington, MA

A current-output DAC with on-board calibration engine guarantees 16b monotonicity and achieves better than -160dBm/Hz noise power spectral density. Well bootstrapping, local bias generation and constant data activity techniques are combined to achieve better than -80dBc IMD to 300MHz at 400MS/s.

7.2 A 1.5V 14b 100MS/s Self-Calibrated DAC

9:00 AM

Y. Cong, R. Geiger
Iowa State University, Ames, IA

A calibrated 14b current-steering DAC is fabricated in a 0.13µm digital CMOS process. The DAC achieves 14b static linearity with a single 1.5V supply, and the core occupies 0.1mm^2. Dynamic linearity is improved through reduction of parasitic effects. At 100MS/s, the SFDR is 82dB and 62dB at signals of 0.9MHz and 42.5MHz, respectively. Power consumption is 16.7mW.

7.3 A 4 x 40W Digital Input Class-AB Power DAC with 100dB Dynamic Range

9:30 AM

C. Meroni[1], E. Botti[1], A. Grosso[1], F. Stefani[1], M. Ghioni[2], A. Baschirotto[3]
[1]STMicroelectronics, Milan, Italy
[2]Politecnico di Milano, Milan, Italy
[3]Universitá di Lecce, Lecce, Italy

A 4 x 40W power DAC for car-radio audio systems has a 100dB dynamic range and is realized in a 0.6µm BiCMOS/DMOS technology. EMI is reduced using a multi-bit DAC with a current-mode interface, DDWA algorithm and a class-AB amplifier with 2nd-order filtering. Total output noise of 25µV_{RMS} without signal yields a 110dB SNR.

BREAK 10:00 AM

7.4 A 500MHz CMOS Anti-Alias Filter using Feedforward Opamps with Local Common-Mode Feedback

10:15 AM

J. Harrison, N. Weste
Macquarie University, Marsfield, Australia

A 500MHz op-amp-RC filter in a 0.18µm CMOS process achieves an integrator signal swing of 1.73V_{p-p} for -40dB THD and thermal noise of 18nV/√Hz. A three-stage op-amp with two feed-forward paths and common-mode feedback local to each stage is used. The op-amp features 8GHz unity-gain frequency and 40dB gain at 500MHz.

7.5 A Class-D Output Stage with Zero Dead Time

10:45 AM

M. Berkhout
Philips Semiconductors, Nijmegen, The Netherlands

An integrated class-D output stage has been realized with zero dead time, thereby removing one of the dominant sources of distortion in class-D amplifiers. Dead time is eliminated through proper dimensioning of the power transistor drivers and accurate matching of switch timing. Open-loop distortion of this output stage stays below 0.1% up to 35W.

7.6 A Baseband Gain-Controlled Amplifier with a Linear-in-dB Gain Range from 14dB to 76dB and a Fixed Corner Frequency DC Offset Canceler

11:15 AM

T. Arai[1], T. Itakura[2]
[1]Toshiba Semiconductor, Kawasaki, Japan
[2]Toshiba R&D Center, Kawasaki, Japan

A linear-in-dB gain-control amplifier for direct conversion systems employs linearized transconductors in a core amp, a dc offset canceller, and a gain control circuit. The offset compensation circuit achieves a constant corner frequency over a gain range of 14 to 76dB by simultaneous tuning of the transconductors.

7.7 A 3A 20MHz BiCMOS/DMOS Power Operational Amplifier: A Structural Design Approach

11:45 AM

V. Ivanov, D. Baum
Texas Instruments, Tucson, AZ

Design of a power op-amp using a structural design methodology is presented. The BiCMOS/DMOS op-amp features rail-to-rail output, 3A maximum output current, adjustable current limit without delay, a class AB input stage with a 50V/μs slew rate, and 100dB open-loop gain with a 2Ω load. It consumes 50mA from a single 7-16V supply.

CONCLUSION 12:15 PM

COMMUNICATION SIGNAL PROCESSING

Chair: **Bernard Shung,** *Broadcom, San Jose, CA*
Associate Chair: **Thucydides Xanthopoulos,** *Cavium Networks, Marlborough, MA*

8.1 A High Performance SSL, IPSEC Protocol Aware Security Processor

8:30 AM

D. Carlson, D. Brasili, A. Hughes, A. Jain, T. Kiszely, P. Kodandapani, A. Vardharajan, T. Xanthopoulos, V. Yalala
Cavium Networks, Santa Clara, CA

A 64M transistor security macro processor enabling 40k full SSL handshakes per second with 1024b RSA. The 3DES, AES, ARC4, SHA-1, MD5 and modular exponentiation cryptographic primitives are also supported. The processor is fabricated in a 0.13µm 8M CMOS process and consumes 12W at 500MHz.

8.2 A Single-Chip 802.11a MAC/PHY with a 32b RISC Processor

9:00 AM

T. Fujisawa[1], J. Hasegawa[1], K. Tsuchie[1], T. Shiozawa[1], T. Fujita[1], K. Seki-Fukuda[2], T. Higashi[2], R. Bandai[2], N. Yoshida[3], K. Shinohara[3], T. Watanabe[3], H. Hatano[3], K. Noguchi[3], T. Saito[1], Y. Unekawa[1], T. Aikawa[1]
[1]Toshiba Semiconductor, Kawasaki, Japan
[2]Toshiba Microelectronics, Kawasaki, Japan
[3]Toshiba Information System, Kawasaki, Japan

An 802.11a compliant MAC/PHY processing chip has been successfully fabricated in 0.18µm CMOS. Thirty million transistors are integrated on a 10.91 x 10.91mm^2 die in a 361-pin PFBGA. The MAC functions are fully implemented by firmware on an embedded 32b RISC processor and hardware acceleration logic. The PHY supports a complete set of data rates up to 54Mb/s.

8.3 Dual Antenna UMTS Mobile Station Transceiver ASIC for 2Mb/s Data Rate

9:30 AM

A. Eltawil[1], E. Grayver[1], H. Zou[1], J. Frigon[1], G. Poberezhskiy[1], B. Daneshrad[2]
[1]Innovics Wireless, Los Angeles, CA
[2]University of California, Los Angeles, CA

A silicon implementation of a dual antenna mobile station modem for 3G WCDMA is presented. Diversity processing is used to support data rates up to 2Mb/s while reducing power consumption. An average SNR improvement of 7dB has been observed yielding up to a 4x increase in capacity with no change to the exisiting network infrastructure.

BREAK 10:00 AM

8.4 A 13.3Mb/s 0.35μm CMOS Analog Turbo Decoder IC with a Configurable Interleaver

10:15 AM

V. Gaudet, G. Gulak
University of Toronto, Toronto, Canada

A 0.35μm CMOS analog decoder for a 4-state, rate 1/3, block length 16 turbo code operates at 13.3Mb/s and latency of 1.2μs and consumes 13.9nJ per decoded bit with a 3.3V supply. The 1.42mm^2 core IC implements two logarithmic domain MAP decoders and a fully programmable analog interleaver that is configured at power-up.

8.5 A 24 Mb/s Radix-4 LogMAP Turbo Decoder for 3GPP-HSDPA Mobile Wireless

10:45 AM

M. Bickerstaff, L. Davis, C. Thomas, D. Garrett, C. Nicol
Bell Labs, Lucent Technologies, North Ryde, Australia

A 24Mb/s 3GPP-HSDPA radix-4 logMAP turbo decoder is designed for 3G data terminals. It features an approximate radix-4 logsum circuit to achieve 145MHz operation. Power is reduced using 1/2-iteration early termination and extrinsics are interleaved in companded format. The decoder core is 14.5mm^2 in 0.18μm CMOS.

8.6 A Scalable 8.7nJ/bit 75.6Mb/s Parallel Concatenated Convolutional (Turbo) CODEC

11:15 AM

B. Bougard, A. Giulietti, V. Derudder, J-W. Weijers, S. Dupont, L. Hollevoet, F. Catthoor, L. Van der Perre, H. De Man, R. Lauwereins
IMEC, Leuven, Belgium

A 6 to 75.6Mb/s turbo CODEC with block size from 32 to 432, code rate from 1/3 to 3/4, 5.35μs/block decoding latency and up to 8.25dB coding gain is described. This IC is fabricated in a 0.18μm process and has a core area of 7.16mm^2. Energy-optimized architecture reduces the energy per bit to 8.7nJ and is almost constant over the throughput range.

8.7 A Programmable Turbo Decoder for Multiple 3G Wireless Standards

11:45 AM

M-C. Shin, I-C. Park
KAIST, Daejeon, Republic of Korea

A programmable turbo decoder designed for multiple 3G wireless standards consists of a configurable SISO decoder and a 16b SIMD processor equipped with 5 processing elements and custom instructions for incremental block interleavers. The decoder core occupies 8.9mm^2 in 0.25μm 5M CMOS and exhibits a maximum decoding rate of 5.83Mb/s.

CONCLUSION 12:15 PM

TD: DIGITAL ARCHITECTURE AND SYSTEMS

Chair: **Stephan Kosonocky,** *IBM T. J. Watson Research Center, Yorkton Heights, NY*
Associate Chair: **Krste Asanovic,** *Massachusetts Institute of Technology, Cambridge, MA*

9.1 Filling the Gap Between System Conception and Silicon/Software Implementation

8:30 AM

H. De Man[1], F. Catthoor[1], R. Marichal[2], C. Verdonck[2], J. Sevenhans[2], L. Kiss[2]
[1]IMEC, Leuven, Belgium
[2]Alcatel, Antwerp, Belgium

The convergence of silicon and embedded software, accompanied by increasing design complexity, exposes a gap between system conception and silicon/software implementation. Design methodologies are presented that make the connection from high level system specification to integrated system solution. These techniques are demonstrated on a digital audio broadcast application.

9.2 Complementary Ferroelectric-Capacitor Logic for Low-Power Logic-in-Memory VLSI

9:00 AM

H. Kimura[1], T. Hanyu[1], M. Kameyama[1], Y. Fujimori[2], T. Nakamura[2], H. Takasu[2]
[1]Tohoku University, Sendai, Japan
[2]Rohm, Kyoto, Japan

Series connection of two ferroelectric capacitors with complementary stored data allows both switching operations and non-destructive storage. This circuitry, used in a fully parallel 32b CAM, results in a dynamic power reduction by 2/3 and static power reduction by 1/9000 compared to a CMOS implementation using 0.6μm ferroelectric CMOS.

9.3 Ultra-High Resolution Image Capturing and Processing for Digital Cinematography

9:30 AM

J. Coghill[1], L. Ion[1], F. Shu[1], H. Siefken[1], C. Smith[1], A. Theuwissen[2]
[1]DALSA, Waterloo, Canada
[2]DALSA, Eindhoven, The Netherlands

The influence of digital cinematography on silicon ICs is described with primary emphasis on the image capturing function. The CCD imager combines 8Mpixels resolution, up to 60 frames/s and a linear dynamic range of 12b. The imager generates 720MB/s which needs to be further processed in the camera.

BREAK 10:00 AM

9.4 A CPU on a Glass Substrate Using CG-Silicon TFTs

10:15 AM

B. Lee[1], Y. Hirayama[1], Y. Kubota[1], S. Imai[1], A. Imaya[1], M. Katayama[1], K. Kato[2], A. Ishikawa[2], T. Ikeda[2], Y. Kurokawa[2], T. Ozaki[2], K. Mutaguch[2], S. Yamazaki[2]
[1]Sharp, Nara, Japan
[2]Semiconductor Energy Laboratory, Atsugi, Japan

A CPU is produced on a glass substrate using continous-gain silicon TFTs. Corning 1737 glass with a distortion point of 640°C forms the glass substrate and the process temperature never exceeds 550°C. The 8b CPU contains 13,000 TFTs and the chip area is 13 x 13mm^2. Operation at a frequency of 3MHz was confirmed at 5V.

9.5 Timekeeping Techniques for Predicting and Optimizing Memory Behavior

10:45 AM

Z. Hu[1], S. Kaxiras[2], M. Martonosi[1]
[1]Princeton University, Princeton, NJ
[2]Agere Systems, Allentown, PA

Computer architects have long exploited observed memory referencing characteristics to optimize memory performance. We introduce timekeeping metrics for improving program memory performance and power dissipation. Performance and power results for previously proposed timekeeping structures are briefly summarized and implementation options are presented. Simulation focusses on implementation issues.

9.6 A Wire-Delay Scalable Microprocessor Architecture for High Performance Systems

11:15 AM

S. Keckler, D. Burger, C. Moore, R. Nagarajan, K. Sankaralingam, V. Agarwal, M. Hrishikesh, N. Ranganathan, P. Shivakumar
University of Texas, Austin, TX

This scalable processor architecture consists of chained ALUs to minimize the physical distance between dependent instructions, thus mitigating the effect of long on-chip wire delays. Simulation studies demonstrate 1.3-15x more instructions per clock than conventional superscalar architectures.

9.7 A 16-Issue Multiple-Program-Counter Microprocessor with Point-to-Point Scalar Operand Network

11:45 AM

M. Taylor, J. Kim, J. Miller, D. Wentzlaff, F. Ghodrat, B. Greenwald, H. Hoffman, P. Johnson, W. Lee, A. Saraf, N. Shnidman, V. Strumpen, S. Amarasinghe, A. Agarwal
Massachusetts Institute of Technology, Cambridge, MA

This microprocessor explores an architectural solution to scalability problems in scalar operand networks. The 0.15µm 6M process, 331mm^2 research prototype issues 16 unique instructions per cycle and uses an on-chip point-to-point scalar operand network to transfer operands among distributed functional units.

CONCLUSION 12:15 PM

HIGH SPEED BUILDING BLOCKS

Chair: **Rick Walker,** *Agilent Technologies, Palo Alto, CA*
Associate Chair: **Hirotaka Tamura,** *Fujitsu Laboratories, Kawasaki, Japan*

10.1 A 20-Input 20-Output 12.5Gb/s SiGe Cross-Point Switch with Less Than 2ps RMS Jitter

8:30 AM

H. Veenstra[1], P. Barré[2], E. van der Heijden[1], D. van Goor[1], N. Lecacheur[2], B. Fahs[2], G. Gloaguen[2], S. Clamagirand[2], O. Burg[2]
[1]Philips, Eindhoven, The Netherlands
[2]Philips, Caen, France

A cross-point switch IC in 0.25μm SiGe technology, for optical networking applications with 20 inputs and 20 outputs achieves an aggregate bandwidth of 250Gb/s. Jitter remains below 2ps RMS and is achieved using impedance matched on-chip signal transfer. The 36mm^2 IC dissipates 4W from a 2.5V supply.

10.2 A 30Gb/s 1:4 Demultiplexer in 0.12μm CMOS

9:00 AM

A. Rylyakov, S. Rylov, H. Ainspan, S. Gowda
IBM, Yorktown Heights, NY

A 1:4 demultiplexer, implemented in 0.12μm SOI and bulk CMOS technology, operates with a BER below 10^{-13} at 30Gb/s (SOI) and 26Gb/s (bulk) input data rates (2^7-1 PRBS), drawing 200mA from a 2V supply. At 1.2V, the chips draw 100mA and operates at input data rates of 21Gb/s (SOI) and 18Gb/s (bulk). The design has an active area of 300μm x 90μm.

10.3 A 2.5 to 10GHz Clock Multiplier Unit with 0.22ps RMS Jitter in 0.18μm CMOS Technology

9:30 AM

R. van de Beek[1], C. Vaucher[2], D. Leenaerts[2], N. Pavlovic[2], K. Mistry[3], E. Klumperink[1], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands
[2]Philips Research Laboratories, Eindhoven, The Netherlands
[3]University of Southampton, Southampton, United Kingdom

A fully integrated clock multiplier unit uses 100mW to generate a 10GHz output clock with 0.22ps RMS jitter, exceeding the SONET OC-192 jitter generation specifications. An LC VCO is controlled by a PLL employing a fast linear phase detector in combination with a frequency detector, both running at 2.5GHz. The jitter and power dissipation are lower than that of previous CMOS implementations.

10.4 Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Equalization

9:45 AM

H. Wu[1], J. Tierno[2], P. Pepeljugoski[2], J. Schaub[2], S. Gowda[2], J. Kash[2], A. Hajimiri[1]
[1]California Institute of Technology, Pasadena, CA
[2]IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Differential 4-tap and 7-tap transverse filters are designed in a 0.18μm SiGe BiCMOS technology for equalization of 10Gb/s multimode fiber optic signals. The 7-tap equalizer reduced the ISI of a 10Gb/s signal received through 300m of 50μm noncompliant next generation multimode fiber from 4.2dB to 0.8dB. The circuit dissipates 40mW from a 3.3V supply.

BREAK 10:00 AM

10.5 Broadband ESD Protection Circuits in CMOS Technology

10:15 AM

S. Galal, B. Razavi
University of California, Los Angeles, CA

Two broadband circuits for I/O protection employ on-chip T-coil networks and standard ESD devices. Fabricated in 0.18μm CMOS technology, the input and output circuits tolerate 1000V and 800V, respectively, and introduce 3dB eye closure at 10Gb/s.

10.6 A 1.6Gb/s/pair Electromagnetically Coupled Multidrop Bus Using Modulated Signaling

10:30 AM

T. Simon[1], R. Amirtharajah[1], J. Benham[1], J. Critchlow[1], T. Knight[2]
[1]Intel, Hudson, MA
[2]Massachusetts Institute of Technology, Cambridge, MA

AC coupling and pulse modulation are presented for high speed multidrop busses. A prototype eight module memory bus operates at a 400MHz symbol rate with 4 bits of modulated data per symbol, for 1.6Gb/s/pair. Test chips in 0.25μm 3M CMOS dissipate 40mW peak and occupy 340x200μm per pair.

10.7 1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme

10:45 AM

K. Kanda[1], D. Antono[1], K. Ishida[1], H. Kawaguchi[1], T. Kuroda[2], T. Sakurai
[1]The University of Tokyo, Tokyo, Japan
[2]Keio University, Yokohama, Japan

A low-power high-speed chip-to-chip interface scheme is described having a density of 625pins/mm^2. The interface utilizes capacitively coupled contactless minipads, return-to-half-V_{DD} signaling and sense amplifying F/F. The measured test chip fabricated in 0.35μm CMOS delivers up to 1.27Gb/s/pin at 3mW/pin.

10.8 10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18μm CMOS Technology

11:15 AM

S. Galal, B. Razavi
University of California, Los Angeles, CA

A limiting amplifier employs active feedback to achieve a bandwidth of 9.4GHz and a gain of 50dB dissipating 150mW. A laser driver uses T-coil peaking and negative capacitance to deliver 100mA at 10Gb/s, while dissipating 675mW. Fabricated in 0.18μm CMOS technology, both circuits operate at 1.8V.

10.9 A 10Gb/s SiGe Compact Laser Diode Driver Using Push-Pull Emitter Followers and Miller Compensated Output Switch

11:45 AM

A. Maxim[1], G. Link[2], E. Smith[1], B. Kirkland[1], J. Prakash[1], R. Lam[1]
[1]Maxim Integrated Products, Austin, TX
[2]Maxim Integrated Products, Hillsboro, OR

A low power 10Gb/s laser diode driver is realized in a 0.2μm SiGe HBT technology. A Miller compensated output switch driven by a push-pull emitter follower reduces the predriver supply current by 30%. A common-mode feedback loop sets the output modulation current. IC specifications include 25ps rise/fall time, 11ps deterministic jitter, 100mA maximum modulation current, 70mA supply current, 4.75-5.5V supply voltage and 1.69mm^2 die area.

CONCLUSION 12:15 PM

MICROSENSORS AND BIOMEMS

Chair: **Ming Wu,** *University of California, Los Angeles, CA*
Associate Chair: **Euisik Yoon,** *KAIST, Daejeon, Korea*

11.1 A CMOS Chip for Individual Cell Manipulation and Detection
8:30 AM

N. Manaresi[1], A. Romani[2], G. Medoro[1], L. Altomare[2], A. Leonardi[2], M. Tartagni[2], R. Guerrieri[2]
[1]Silicon Biosystems, Bologna, Italy
[2]University of Bologna, Bologna, Italy

Investigation of individual biological cell interactions on a large scale creates applications in drug screening, cell separation and cell analysis. The IC is designed to detect and manipulate more than 10k cells in parallel and include a 320x320 sensing and actuation array. The chip is implemented in 0.35μm 2P 3M CMOS.

11.2 Low-Power Interface Circuits for Bio-Implantable Microsystems
9:00 AM

H. Yu, K. Najafi
University of Michigan, Ann Arbor, MI

Low-power interface circuits used in wireless bio-implantable microsystems are described. Regulators have line regulation of 3mV/V, load regulation of 8mV/mA, and ripple rejection of 45dB. An ASK demodulator achieves a bit rate of 60kb/s, and the frequency of the recovered clock reaches 10MHz. An on-chip active transmitter achieves a bit rate of 2Mb/s. Total power dissipation is 2.17mW for a 4.84mm^2 IC fabricated in 0.8μm CMOS.

11.3 A 136μW/channel Autonomous Strain Gauge Datalogger
9:30 AM

W. Claes, M. De Cooman, W. Sansen, R. Puers
Katholieke Universiteit Leuven, Heverlee, Belgium

A single-chip 18-channel strain gauge datalogger IC is integrated in a 0.7μm CMOS technology. The chip combines a 10 microstrain accuracy sensor interface with digital offset-compensation, a wireless 132kHz/66kHz transceiver and a 23.4kgate digital unit with adjustable data-processing. The datalogger's maximum power consumption, including an external 2Mb RAM, is 136 μW/channel at 3.1V.

BREAK 10:00 AM

11.4 A High Density Conduction Based Micro-DNA-Identification-Array Fabricated in a CMOS Compatible Process
10:15 AM

M. Xue[1], J. Li[2], Z. Lu[2], P. Ko[1], M. Chan[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Southeast University, Nanjing, China

A high-density CMOS-compatible DNA array fabricated using a modified metalization process is demonstrated. The array produces a conductivity difference of nine orders of magnitude for matched and single-based mismatched DNA molecules, which can be easily detected by a simple sensing circuit.

11.5 A CMOS Temperature Sensor with a 3σ Inaccuracy of ±0.5°C from -50°C to 120°C
10:30 AM

M. Pertijs[1], A. Niederkorn[2], X. Ma[2], B. McKillop[2], A. Bakker[3], J. Huijsing[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Philips Semiconductors, Tempe, Arizona
[3]Philips Semiconductors, Delft, The Netherlands

A temperature sensor in 0.5μm CMOS achieves an accuracy of ±0.5°C (3σ) from -50°C to 120°C. It combines chopping, dynamic element matching and curvature correction with calibration at room temperature. Calibration time has been reduced to less than 1s by using an on-chip transistor to measure the die temperature.

11.6 A Multi-Step Electromechanical ΣΔ Converter for Micro-g Capacitive Accelerometers

10:45 AM

H. Kulah, N. Yazdi[1], K. Najafi
University of Michigan, Ann Arbor, MI
[1]Now with Corning Intellisense, Boston, MA

A multi-step electromechanical ΣΔ modulator for μg accelerometers is desribed. A two-element sensor array is used in two ΣΔ loops and resolution improves by >2x compared to a conventional 2nd-order ΣΔ modulator. This CMOS chip operates at 1MHz and provides 0.2-1.2V/pF sensitivity, <20aF resolution, >120dB dynamic range, and dissipates <12mW.

11.7 Integrated Multiple-Device IMU Systems with Continuous-Time Sensing Circuitry

11:15 AM

H. Luo, G. Fedder, L. Carley
Carnegie Mellon University, Pittsburgh, PA

This multiple IMU system integrates lateral accelerometers and vertical gyroscopes with signal processing circuits in a post CMOS MEMS process. A direct-coupled continuous-time sensing buffer for MEMS capacitive sensing has a -3dB frequency corner lower than 10Hz. The integration of multiple sensors makes cross-device compensation possible.

11.8 An Above-IC RF-MEMS Switch

11:45 AM

D. Saias[1], S. Boret[1], P. Robert[2], C. Billard[2], P. L. Charvet[2], G. Bouche[1], P. Berruyer[2], M. Laurens[1], J-C. Grasset[1], M. Aid[2], D. Belot[1], P. Ancey[1]
[1]STMicroelectronics, Crolles, France
[2]CEA-Leti, Grenoble, France

A MEMS switch is driven by a 0.25μm BiCMOS IC and achieves 0.4dB insertion loss and 54dB isolation at 2GHz. The 400μmx50μm MEMS device is built together on top of the wafers enabling a system-on-chip design.

11.9 An Active Range Finder with the Capability of -18dB SBR, 48dB Dynamic Range and 120 x 110 Pixel Resolution

12:15 PM

Y. Oike, M. Ikeda, K. Asada
University of Tokyo, Tokyo, Japan

The active range finder with 120x110 pixels achieves a projected light detection with high SBR (Signal-to-Background Ratio). The sensing scheme realizes a selective light detection under -18dB SBR with a dynamic range exceeding 48dB. The maximum frame rate is 2000frames/s and the maximum range error is 1.5mm at a distance of 1000mm.

CONCLUSION 12:30 PM

CMOS IMAGERS, SENSORS AND DISPLAYS

Chair: **Bill Bidermann,** *PIXIM, Mountain View, CA*
Associate Chair: **Ralph-Etienne Cummings,** *University of Maryland, College Park, MD*

12.1 A 0.18μm High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer

1:30 PM

W. Bidermann, S. Ewedemi, J. Reyneri, H. Tian, D. Wile, D. Yang
Pixim, Mountain View, CA

The CMOS imaging system-on-chip includes an embedded frame buffer and operates at 100MHz. The programmable chip produces color video at up to 500frames/s with over 100dB dynamic range using multi-capture. The sensor utilizes a 0.18μm 1P 4M CMOS process and dissipates 600mW including I/O.

12.2 A Capacitive Hybrid Flip-Chip ASIC and Sensor for Fingerprint, Navigation and Pointer Detection

2:00 PM

O. Vermesan[1], K. Riisnæs[2], L. Le-Pailleur[3], J. Nysaether[2], M. Bauge[3], H. Rustad[4], S. Clausen[2], L-C. Blystad[1], H. Grindvoll[1], R. Pedersen[2], R. Pezzani[5], D. Kaire[3]
[1]SINTEF Electronics and Cybernetics, Oslo, Norway
[2]IDEX ASA, Asker, Norway
[3]STMicroelectronics, Grenoble, France
[4]SINTEF Telecom and Informatics, Trondheim, Norway
[5]STMicroelectronics, Tours, France

A fingerprint detection technology that supports navigation, pointer and fingerprint acquisition is described. The hybrid system consists of a silicon sensor substrate flip-chipped onto a mixed signal ASIC. The sensor is linear and the finger is swept over to scan the fingerprint. To achieve 500dpi accuracy, separate process optimization for both the ASIC and the sensor substrate gives a alternative solution compared to all silicon sensor approaches. The ASIC is 18mm^2 in 0.25μm CMOS and the sensor is 105mm^2.

12.3 A 1¼ Inch 8.3M Pixel Digital Output CMOS APS for UDTV Application

2:30 PM

I. Takayanagi[1], M. Shirakawa[2], K. Mitani[2], M. Sugawara[2], S. Iversen[3], J. Moholt[3], J. Nakamura[1], E. Fossum[4]
[1]Micron Imaging, Tokyo, Japan
[2]NHK, Tokyo, Japan
[3]Micron Technology, Oslo, Norway
[4]Micron Technology, Pasadena, CA

A 3936x2196 pixel CMOS APS has a 10b column-based ADC. It operates at 49.5MHz in a progressive scanning mode at 60 frames/s and achieves a 2000 TV line resolution, sensitivity of 4200b/lux-s, and power consumption of less than 760mW.

12.4 SXGA Pinned Photodiode CMOS Image Sensor in 0.35μm technology

2:45 PM

K. Findlater[1], R. Henderson[1], D. Baxter[1], J. Hurwitz[1], L. Grant[1], Y. Cazaux[2], F. Roy[2], D. Herault[2], Y. Marcellier[2]
[1]STMicroelectronics, Edinburgh, United Kingdom
[2]STMicroelectronics, Crolles, France

A 30frames/s SXGA 5.6μm pinned photodiode pixel column parallel CMOS image sensor achieves 340μV noise floor and 40pA/cm^{-2} dark current. Performance is limited by pixel 1/f noise, not by the ADC noise floor of 140μV. The column ADC memory employs a custom DRAM to save area. The sensor utilizes a 0.35μm 1P 3M CMOS process.

BREAK 3:00 PM

12.5 0.79" Single Panel Liquid Crystal on Silicon Backplane IC with 1408 8b DACs for HDTV Applications

3:15 PM

S. Baik[1], Y. Cha[1], Y. Hwang[1], J. Chung[1], K. Kang[2], J. Jeong[2], Y. Kim[3], B. Cho[3], Y. Shin[1]
[1]ATLab, Yongin Si, Republic of Korea
[2]Samsung SDI, Yongin Si, Republic of Korea
[3]Samsung Electronics, Suwon Si, Republic of Korea

The architecture and circuit design of a single panel liquid crystal on silicon (LCoS) backplane IC that includes 1408 x 844 pixels and drives 8 color sub-frames/one video frame is described. There are 1408 DACs to improve picture uniformity and one analog frame buffer to reduce video bandwidth. Each pixel has 256 gray levels and 12µm pitch. The IC, fabricated in UMC 0.35µm 5M LCoS technology, is used successfully in projection applications.

12.6 A 128 x 128 CMOS Bio-Sensor Array for Extracellular Recording of Neural Activity

3:45 PM

B. Eversmann[1], M. Jenkner[1], C. Paulus[1], F. Hofmann[1], R. Brederlow[1], B. Holzapfl[1], P. Fromherz[2], M. Brenner[3], M. Schreiter[3], R. Gabl[3], K. Plehnert[3], M. Steinhauser[3], G. Eckstein[3], D. Schmitt-Landsiedel[4], R. Thewes[1]
[1]Infineon Technologies, Munich, Germany
[2]Max-Planck-Institute for Biochemistry, Martinsried, Germany
[3]Siemens, Munich, Germany
[4]Technical University of Munich, Munich, Germany

A CMOS sensor array for monitoring neural signals of living cells with 128 x 128 pixels in a 1mm^2 area is described. A standard 0.5µm, 5V CMOS process extended by top electrodes covered by a relatively thin bio-compatible dielectric is used. Detection circuitry is based on a sensor-MOSFET mismatch-compensating current-mode technique.

12.7 A Column-Based Pixel-Gain-Adaptive CMOS Image Sensor for Low-Light-Level Imaging

4:15 PM

S. Kawahito[1], M. Sakakibara[1], D. Handoko[1], N. Nakamura[2], H. Satoh[2], M. Higashi[2], K. Mabuchi[2], H. Sumi[2]
[1]Shizuoka University, Shizuoka, Japan
[2]Sony, Atsugi, Japan

A 0.25µm technology CMOS image sensor employs a 4.2µm pitch pinned-photodiode pixel. A column amplifier and digital domain processing reduces the fixed pattern noise to 55µV. The saturation voltage is 1V with a 2.5V supply voltage and the dynamic range is 69dB.

12.8 A 128 x 128 Pixel 120dB Dynamic Range Vision Sensor Chip for Image Contrast and Orientation Extraction

4:30 PM

P-F. Ruedi, P. Heim, F. Kaess, E. Grenet, F. Heitger, P-Y. Burgi, S. Gyger, P. Nussbaum
CSEM, Neuchatel, Switzerland

This vision sensor outputs luminance, contrast magnitude and contrast orientation of image features for surveillance and automotive applications. The sensor produces a contrast representation with a dynamic range of 120dB and a sensitivity of 2%. The chip is fabricated in a 0.5µm 3M 2P process and dissipates 300mW at 3.3V.

CONCLUSION 4:45 PM

40GB/S COMMUNICATION ICS

Chair: **Yuriy Greshishchev,** *PMC-Sierra, Kanata, Canada*
Associate Chair: **John Khoury,** *Multilink Technology, Somerset, NJ*

13.1 A 0.18μm SiGe BiCMOS Receiver and Transmitter Chipset for SONET OC-768 Transmission Systems

1:30 PM

M. Meghelli[1], A. Rylyakov[1], S. Zier[2], M. Sorna[2]
[1]IBM Thomas J. Watson Research Center, Yorktown Heights, NY
[2]IBM Microelectronics, Hopewell Junction, NY

A BiCMOS CDR/1:4-DEMUX and CMU/4:1-MUX chipset targeting 40-43Gb/s optical communications is implemented in 0.18μm SiGe. At 43Gb/s and up to 100°C chip temperature, both ICs operate at BER $<10^{-15}$ and <210fs RMS clock jitter. The receiver and transmitter chips dissipate 2.8W and 2.3W, respectively, from a -3.6V supply.

13.2 43Gb/s Full-Rate-Clock 16:1 Multiplexer and 1:16 Demultiplexer with SFI-5 Interface in SiGe BiCMOS Technology

2:00 PM

A. Koyama[1], T. Harada[1], H. Yamashita[2], R. Takeyari[2], N. Shiramizu[2], K. Ishikawa[2], M. Ito[2], S. Suzuki[3], T. Yamashita[1], S. Yabuki[1], H. Ando[1], T. Aida[1], K. Watanabe[1], K. Ohhata[4], S. Takeuchi[5], H. Chiba[5], A. Ito[1], H. Yoshioka[1], A. Kubota[1], T. Takahashi[5], H. Nii[5]
[1]Device Development Center, Hitachi, Ome, Japan
[2]Central Research Laboratory, Hitachi, Kokubunji, Japan
[3]OpNext Japan, Yokohama, Japan
[4]Hitachi Device Engineering, Kokubunji, Japan
[5]Hitachi ULSI Systems, Ome, Japan

Fabricated in 0.18μm SiGe BiCMOS, 16:1 MUX and 1:16 DMUX MCMs equipped with an SFI-5 interface operate at 43Gb/s. The on-chip CDR with external VCO recovers a full-rate clock with 2.5° RMS jitter from 2^{31}-1 PRBS. The SFI-5 bus also operates error-free at 2.7Gb/s, and tolerates a ±6.6UI static skew.

13.3 A 40-43Gb/s Clock and Data Recovery IC with Integrated SFI-5 1:16 Demultiplexer in SiGe Technology

2:30 PM

A. Ong, S. Benyamin, V. Condito, Q. Lee, J. Mattia, D. Shaeffer, A. Shahani, X. Si, H. Tao, M. Tarsia, W. Wong, M. Xu
Big Bear Networks, Milpitas, CA

A fully integrated OC-768 clock and data recovery IC with SFI-5 1:16 demultiplexer is designed in a 120GHz/100GHz (f_T/f_{max}) SiGe technology. The 16 2.5Gb/s outputs and additional deskew channel are compliant with the SFI-5 specification. The measured BER is $<10^{-15}$. Power dissipation is 7.5W using 1.8V and -5.2V supplies.

BREAK 3:00 PM

13.4 A 40 / 43Gb/s SONET OC-768 SiGe 4:1 MUX / CMU

3:15 PM

D. Shaeffer, H. Tao, Q. Lee, A. Ong, V. Condito, S. Benyamin, W. Wong, X. Si, S. Kudszus, M. Tarsia
Big Bear Networks, Milpitas, CA

A 40/43Gb/s SONET OC-768 4:1 MUX / CMU is implemented in a 120GHz f_T SiGe BiCMOS process. When co-packaged with a companion 16:4 multiplexer, the chip produces less than 3ps of pattern dependent jitter and 175fs RMS random jitter. A packaged BER of better than 10^{-14} is measured with 2^{31}-1 PRBS data inputs. The chip consumes 4.9W from 1.8V and -5.2V supplies.

13.5 An SFI-5 Compliant 16:4 Multiplexer for the OC-768 System

3:45 PM

M. Xu, S. Benyamin, X. Si, W. Wong, D. Shaeffer, H. Tao, A. Shahani, V. Condito, A. Ong, M. Tarsia
Big Bear Networks, Milpitas, CA

A fully integrated SFI-5 Compliant 16:4 Multiplexer for OC-768/STM-256 systems is implemented in a 0.18µm 120GHz SiGe technology. The chip recovers sixteen 2.488Gb/s inputs, aligns them according to the deskew channel and multiplexes them onto 4 streams of 10Gb/s data. The measured BER is $<10^{-12}$. The chip dissipates 4.8W from 1.8V and 3.3V power supplies.

13.6 A Fully Integrated 43.2Gb/s Clock and Data Recovery and 1:4 DEMUX IC in InP HBT Technology

4:15 PM

J. Yen, M. Case, S. Nielsen, J. Rogers, N. Srivastava, R. Thiagarajah
Inphi, Westlake Village, CA

A 43.2Gb/s CDR/DMUX IC implemented in InP HBT technology is fully integrated, requiring only a single external capacitor for complete functionality. Sensitivity is $27mV_{p-p}$ differential with a BER of 10^{-12}. The IC exceeds extrapolated SONET jitter tolerance specifications, operates with a 3.3V power supply, and dissipates 3.3W in 10.2mm^2.

13.7 A 40Gb/s Clock Recovery Circuit in 0.18µm CMOS Technology

4:45 PM

J. Lee, B. Razavi
University of California, Los Angeles, CA

A 40-Gb/s clock recovery circuit incorporates a quarter-rate phase detector and a multiphase LC oscillator to retime the data and demultiplex it into four 10Gb/s outputs. Fabricated in 0.18µm CMOS technology, the circuit produces a clock jitter of 0.9ps RMS and 9.67ps peak-to-peak while consuming 144mW.

CONCLUSION 5:15 PM

MICROPROCESSORS

Chair: **Héctor Sánchez,** *Motorola, Austin, TX*
Associate Chair: **Norman Rohrer,** *IBM, Essex Junction, VT*

14.1 A 1.3GHz Fifth Generation SPARC64 Microprocessor

1:30 PM

H. Ando, Y. Yoshida, A. Inoue, I. Sugiyama, T. Asakawa, K. Morita, T. Muta, T. Motokurumada, S. Okada, H. Yamashita, Y. Satsukawa, A. Konmoto, R. Yamashita, H. Sugiyama
Fujitsu, Kawasaki, Japan

A fifth generation SPARC64 processor implemented in 130nm CMOS process with 8 layers of Cu metallization operates with a 1.3GHz clock and dissipates 34.7W. The processor is a 4-issue out-of-order design with 2MB on-chip level-2 cache. Error checking is added on the datapath in addition to memory. An instruction is retried for correction when an error is detected in the datapath.

14.2 Implementation of an Alpha Microprocessor in SOI

2:00 PM

J. Kowaleski, T. Truex, D. Dever, D. Ament, W. Anderson, L. Bair, S. Bakke, D. Bertucci, R. Castelino, D. Clay, J. Clouser, A. Dipace, V. Germini, R. Hokinson, C. Houghton, H. Kolk, B. Miller, G. Moyer, R. Mueller, N. O'Neill, D. Ramey, Y. Seok, J. Sun, G. Zelic, V. Zlatkovic
Hewlett Packard, Shrewsbury, MA

Conversion of a 150 million transistor microprocessor from a 0.18µm bulk process to a 0.13µm SOI process is described. Shorter channels and SOI characteristics cause leakage that must be managed. System requirements drive duplication of signal characteristics and integrity for all I/O. Adaptation of the Si to a 200µm bump structure that is 50µm smaller than the previous generation is shown.

14.3 A VLIW Processor with Reconfigurable Instruction Set for Embedded Applications

2:30 PM

F. Campi[1], R. Canegallo[2], A. Cappelli[1], A. Lodi[1], M. Toma[1], R. Guerrieri[1]
[1]University of Bologna, Bologna, Italy
[2]STMicroelectronics, Agrate Brianza, Italy

A RISC VLIW processor implements dynamic instruction set extension integrating a pipelined, run-time reconfigurable datapath. A 0.18µm 6M CMOS chip prototype achieves energy consumption reduction up to 90% and time reduction of 13X on a signal processing algorithm benchmark. The IC contains 12M transistors and dissipates 120mW at 80MHz from a 1.8V supply.

BREAK 3:00

14.4 A 1.5GHz Third Generation Itanium® Processor

3:15 PM

J. Stinson, S. Rusu
Intel, Santa Clara, CA

A third-generation 1.5GHz Itanium® processor implements the Explicitly Parallel Instruction Computing (EPIC) architecture and features an on-die 6MB, 24-way set associative L3 cache. The 374mm^2 die contains 410M transistors and is implemented in a dual-V_T 0.13µm technology saving 6-level Cu interconnects with FSG dielectric and dissipates 130W.

14.5 A 600MHz Single-chip Multiprocessor with 4.8GB/s Internal Shared Pipelined Bus and 512kB Internal Memory

3:45 PM

S. Kaneko, K. Sawai, N. Masui, K. Ishimi, T. Itou, M. Satou, H. Kondo, N. Okumura, Y. Takata, H. Takata, M. Sakugawa, T. Higuchi, S. Ohtani, K. Sakamoto, N. Ishikawa, M. Nakajima, S. Iwata, K. Hayase, S. Nakano, S. Nakazawa, O. Tomisawa, T. Shimizu
Mitsubishi Electric, Itami, Japan

This 600MHz single-chip multiprocessor consists of two M32R 32b CPU cores and 512kB shared SRAM and is designed for embedded systems. Embedded processors are required with increased performance while power dissipation is paramount for battery-operated applications. The design is implemented in a single-chip in a 0.15µm 4M CMOS process and operates at 600MHz with 800mW peak power dissipation.

14.6 A 600MHz NT3 Network Processor

4:15 PM

S. McMahan
Cisco Systems, Richardson, TX

A 97M transistor custom-designed network processor integrating 16 VLIW CPUs implements the Cisco Toaster instruction set at 600MHz in a 0.18µm process. The chip area is 349mm^2 and consumes 20W at 500MHz. The frequency is 2.5 that of an ASIC Toaster implementation in a similar process.

14.7 A 10GHz TCP Offload Accelerator for 10Gb/s Ethernet in 90nm Dual-V_T CMOS

4:45 PM

Y. Hoskote, V. Erraguntla, D. Finan, J. Howard, D. Klowden, S. Narendra, G. Ruhl, D. Somasekhar, S. Tang, J. Tschanz, S. Vangal, V. Veeramachaneni, H. Wilson, J. Xu, N. Borkar
Intel, Hillsboro, OR

This prototype offloads TCP input processing on minimum packet sizes at wire speed for 10Gb/s Ethernet. The design employs a 10GHz core with a specialized instruction set and includes hardware support for dynamically reordering packets. In a 90nm dual-V_T CMOS process, the 8mm^2 chip has 260K transistors. Simulation predicts a power dissipation of 1.9W at 1.2V and 10GHz.

CONCLUSION 5:15 PM

TIMETABLE OF ISSCC2003 SESSIONS

Sunday, February 9th — **ISSCC 2003 TUTORIALS**

8:00 AM	T1: Basics of Serial Backplane Transceivers T2: Design for Test and Debug T3: Introduction to BioMEMS T4: MRAM Technology and Circuits	T5: Wireless LAN: Architectures and Design T6: Highly Integrated RF and Wireless Transceivers T7: DSL Splitters and Drivers

	ATACC WORKSHOP	SSCTC WORKSHOP
8:30 AM	W1: Analog Telecom and Circuit Concepts (Salon 7)	W2: Implications of Near-Limit CMOS on Circuits and Applications (Golden Gate B2/B3)

ISSCC 2003 SPECIAL-TOPIC EVENING SESSIONS

7:30 PM	SE1: Highlights of DAC (Salon 7)	SE2: Circuits in Emerging Technologies (Salon 8)	SE3: How Far Can Integration Go For 3G Cellphones? (Salon 9)

Monday, February 10th — **ISSCC 2003 PAPER SESSIONS**

8:30 AM	Session 1: Plenary Session (Salons 7-9)				
1:30 PM	Session 2: Multimedia Signal Processing (Salon 1-6)	Session 3: Oversampled A/D Converters (Salon 7)	Session 4: Clock Recovery and Backplane Transceivers (Salon 8)	Session 5: Wireless PAN Transceivers (Salon 9)	Session 6: Low-Power Digital Techniques (Salon 10-15)
5:15 PM	Author Interviews and Social Hour (Golden Gate Hall)				

ISSCC 2003 DISCUSSION SESSIONS

8:00 PM	E1: Analog IP - Stairway to SoC Heaven? (Salon 7)	E2: Will MEMS, Imagers, and Displays Be Key to the Growth of the IC Industry? (Salon 8)	E3: Good, Bad, Ugly - 50 Years of Memory Evolution. What Next? (Salon 9)

Tuesday, February 11th — **ISSCC 2003 PAPER SESSIONS**

7:30 AM	IEEE - Member Digital Library - Webcast (Salon 9)				
8:30 AM	Session 7: DACs and AMPs (Salon 1-6)	Session 8: Communication Signal Processing (Salon 7)	Session 9: TD: Digital Architecture and Systems (Salon 8)	Session 10: High-Speed Building Blocks (Salon 9)	Session 11: Microsensors and BioMEMS (Salon 10-15)
1:30 PM	Session 12: CMOS Imagers, Sensors and Displays (Salon 1-6)	Session 13: 40Gb/s Commuication ICs (Salon 7)	Session 14: Microprocessors (Salon 8)	Session 15: Cellular Communications (Salon 9)	Session 16: Non-Volatile Memory (Salon 10-15)
5:15 PM	Author Interviews (Golden Gate Hall)				

ISSCC 2003 DISCUSSION SESSIONS

8:00 PM	E4: Future Mobile Phones: A Beautiful Dream or Smoke in LSI Technology (Salon 7)	E5: Fineline Prototyping: Breaking New Ground or Breaking the Bank? (Salon 8)	E6: SoC: DOA? RIP? (Salon 9)

Wednesday, February 12th — **ISSCC 2003 PAPER SESSIONS**

8:30 AM	Session 17: SRAM and DRAM (Salon 1-6)	Session 18: Nyquist A/D Converters (Salon 7)	Session 19: Processor Building Blocks (Salon 8)	Session 20: Wireless Local Area Networking (Salon 9)	Session 21: TD: Organic and Nanoscale Technologies (Salon 10-15)
1:30 PM	Session 22: TD: Embedded Technologies (Salon 1-6)	Session 23: Mixed-Signal and Wireline Techniques (Salon 7)	Session 24: Clock Generation (Salon 8)	Session 25: RF Infotainment (Salon 9)	Session 26: Embedded Memory and Digital Systems (Salon 10-15)
5:15 PM	Author Interviews (Ballroom Foyer South)				

Thursday, February 13th — **ISSCC 2003 SHORT COURSE**

8:00 AM	System-on-a-Chip Design (Sessions at 8:00 in Salon 10-15; 10:00 AM in Salon 1-6; 1:30 PM in Nob Hill)

	MICROPROCESSOR WORKSHOP	GIRAFE WORKSHOP
8:30 AM	W3: Microprocessor Design in the Power-Constrained Era (Salon 8)	W4: Gigahertz Radio Front Ends (Salon 7)

50TH-ANNIVERSAY MUSEUM
Sunday, February 9th, 7:00 AM - 10:00 PM (Golden Gate A1)
Monday, February 10th, 7:00 AM - 10:00 PM (Golden Gate A1)
Tuesday, February 11th, 7:00 AM - 10:00 PM (Golden Gate A1)
Wednesday, February 12th, 7:00 AM - 5:00 PM (Golden Gate A1)

BOOK DISPLAY
Monday, February 10th, 12:00 PM - 6:30 PM (Golden Gate Hall)
Tuesday, February 11th, 9:30 AM - 5:30 PM (Golden Gate Hall)
Wednesday, February 12th, 9:30 AM - 1:00 PM (Golden Gate Hall)

CELLULAR COMMUNICATIONS

Chair: **Paul Davis,** Consultants, *Reading, PA*
Associate Chair: **Arya Behzad,** *Broadcom, San Diego, CA*

15.1 Automatic Phase Alignment for a Fully Integrated CMOS Cartesian Feedback PA System

1:30 PM

J. Dawson, T. Lee
Stanford University, Stanford, CA

A phase alignment system is used in an IC that fully integrates a 13.4dBm PA, Cartesian feedback, and phase-alignment circuitry. The alignment system consumes 8.5mW from a 2.5V supply, uses a 2GHz carrier, and rejects phase disturbances over a 180° range. The IC was fabricated in a 0.25μm CMOS process.

15.2 A 1.9GHz Image-Reject Front-End with Automatic Tuning in a 0.15μm CMOS Technology

2:00 PM

M. Koroglu[1], P. Allen[2]
[1]Mindspeed Technologies, Newport Beach, CA
[2]Georgia Institute of Technology, Atlanta, GA

A 1.9GHz front-end consists of an LNA, an image-reject notch filter with automatic frequency and Q tuning circuits, and a down-conversion mixer. Implemented in a 0.15μm CMOS process, the 0.45mm^2 front-end achieves 5.4dB noise figure, -12dBm IIP3 and consumes 19mW from 1.5V supply.

15.3 A Silicon BiCMOS Direct Up-Conversion Transmitter IC for CDMA2000 with Linear-in-dB Power Optimized RF Level Control

2:30 PM

A. Daanen[1], S. Aggarwal[1], M. Locher[1], W. Redman-White[1], O. Charlon[1], A. Landesman[1], M. Judson[1], M. Bracey[1], D. Duperray[1], C. Razzell[1], V. Akylas[1], D. Brunel[2], R. Comte[2]
[1]Philips Semiconductors, San Jose, CA
[2]Philips Semiconductors, Caen, France

A direct up-conversion transmitter design for CEL and PCS band CDMA cellular radio is presented. Linear-in-dB power control gives reduced supply consumption at low output levels. Current from the 2.85V supply is 68mA at +8dBm and 38mA at minimum power including both TX and RX synthesizers and TX VCO.

BREAK 3:00 PM

15.4 A 1.5V 45mW Direct Conversion WCDMA Receiver IC in 0.13μm CMOS

3:15 PM

J. Rogin, I. Kouchev, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

A complete WCDMA receiver IC is integrated in 0.13μm CMOS. Circuit features include: 1.5V operation, high compression in FDD mode, baseband filter/AGC gain accuracy (70dB±0.2dB), cutoff frequency accuracy (±1.5%) and low output offset (<20mV). Overall NF is 6.5dB, IIP3 = -9dBm, IIP2 = 27dBm and power consumption is 45mW.

15.5 Carrier Leakage Suppression in Direct-Conversion WCDMA Transmitters

3:45 PM

G. Brenna, D. Tschopp, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

Carrier leakage suppression techniques are employed to enable direct up-conversion transmitters to meet WCDMA specifications. Implemented in 0.13µm CMOS, the complete TX IC delivers +2.5dBm output power and consumes 45mA at 1.5V. The IC achieves +19dBm OIP3, 4.3% EVM, -38dBc ACLR and an output noise in the DCS band of -146dBm/Hz.

15.6 Direct Conversion Dual-Band SiGe BiCMOS Transmitter and Receive PLL IC for CDMA/WCDMA/AMPS/GPS Applications

4:15 PM

K. Gard, K. Barnett, J. Dunworth, T. Segoria, B. Walker, J. Zhou, D. Maldonado, A. See, P. Peterzell, C. Persico
Qualcomm, San Diego, CA

A direct conversion 0.4µm SiGe BiCMOS transmitter and receiver PLL consists of two transmitters, two PLLs, and an integrated VCO for cellular, PCS/IMT and GPS applications. The chip consumes 71mA at 2.7V with -55dBc ACPR at 885kHz offset and -134dBm/Hz noise at 45MHz offset for cellular, and 79mA, -56dBc ACPR at 1.25MHz offset, and -132dBm/Hz noise at 80MHz offset for PCS.

15.7 A Fully Integrated Zero-IF Transceiver for GSM-GPRS Quad Band Application

4:45 PM

E. Duvivier, S. Cipriani, L. Carpineto, P. Cusinato, B. Bisanti, F. Galant, F. Chalet, F. Coppola, S. Cercelaru, G. Puccio, N. Mouralis, J. Jiguet
Texas Instruments, Villeneuve Loubet, France

A GPRS GSM850/GSM/DCS/PCS fully integrated transceiver occupies 14mm^2 in 0.35µm SiGe technology. A direct conversion receiver, transmitter, synthesizer, VCO, voltage regulators and loop filters are fully integrated. The chip meets the GPRS specifications including settling time of 105µs in RX mode, NF of 3dB for GSM, TX phase error of 2° RMS, and PLL phase noise of -84dBc/Hz at a 1kHz offset at 3.6GHz.

CONCLUSION 5:15 PM

NON-VOLATILE MEMORY

Chair: **Takayuki Kawahara,** *Hitachi, Kokubunji, Tokyo, Japan*
Associate Chair: **Mark Bauer,** *Intel, Folsom, CA*

16.1 A 512kb Cross-Point Cell MRAM

1:30 PM

N. Sakimura, T. Honda, T. Sugibayashi, S. Miura, H. Numata, H. Hada, S. Tahara
NEC, Sagamihara, Japan

A 512kb MRAM comprising cross-point cells, magnetic tunnel junctions, bit lines and word lines is designed using a 0.25μm CMOS and a 0.6μm MRAM process. The design provides a new sensing method without a large area overhead despite a low current cross-point signal. The MRAM operates with read access time of 1.0μs at 2.5V.

16.2 A 0.24μm 2.0V 1T1MTJ 16kb NV Magnetoresistance RAM with Self Reference Sensing

2:00 PM

G. Jeong, W. Cho, S. Ahn, H. Jeong, G. Koh, Y. Hwang, K. Kim
Samsung Electronics, Yongin, Republic of Korea

A non-volatile 16kb magneto-RAM with a 0.24μm design rule uses a self reference sensing scheme for reliable sensing margin. This sensing method is achieved by storing the voltage of the magneto-tunnel junction (MTJ) and afterwards storing a reference voltage of the same MTJ (self-reference), thus eliminating variation in tunneling oxide thickness. Cell size is 2.06μm^2 and read access is 120ns.

16.3 A 32Mb Chain FeRAM with Segment / Stitch Array Architecture

2:30 PM

S. Shiratake[1], T. Miyakawa[1], Y. Takeuchi[1], R. Ogiwara[1], M. Kamoshida[1], K. Hoya[1], K. Oikawa[1], I. Kunishima[1], K. Yamakawa[1], S. Sugimoto[1], D. Takashima[1], H-O. Joachim[2], N. Rehm[2], J. Wohlfahrt[2], N. Nagel[2], G. Beitel[2], M. Jacob[2], T. Roehr[2]
[1]Toshiba, Yokohama, Japan
[2]Infineon Technologies, Yokohama, Japan

A 96mm^2, 32Mb chain FeRAM in 0.20μm 3M CMOS and stacked capacitor technology is described. Cell efficiency of 65.6% is realized by compact memory cell structure and segment/stitch WL architecture. The word line power-on/off sequence protects the data from startup noise. A 3μA standby current bias generator and compatible access mode SRAM are implemented for mobile applications.

BREAK 3:00 PM

16.4 512Mb PROM with 8 Layers of Antifuse/Diode Cells

3:15 PM

M. Crowley, A. Al-Shamma, D. Bosch, M. Farmwald, L. Fasoli, A. Ilkbahar, M. Johnson, B. Kleveland, T. Lee, T-Y. Liu, Q. Nguyen, R. Scheuerlein, K. So, T. Thorp
Matrix Semiconductor, Santa Clara, CA

A 3.3V, 512Mb PROM uses a transistorless memory cell containing an antifuse and diode. A bit area of $1.4F^2$ including all overhead is achieved by stacking cells 8 high above the 0.25µm CMOS substrate. Read bandwidth is 1MB/s and write bandwidth is 0.5MB/s. A 72b Hamming code provides fault tolerance.

16.5 A 1.8V 128Mb 125MHz Multi-level Cell Flash Memory with Flexible Read While Write

3:45 PM

D. Elmhurst, S. Monasa, R. Bains, T. Bressie, C. Bueb, E. Carrieri, B. Chauhan, N. Chrisman, M. Daley, R. DeLuna, K. Fan, M. Goldman, P. Govindu, A. Huq, M. Khandaker, J. Kreisfels, S. Krishnamachari, P. Lavapie, K. Loe, T. Ly, et al.
Intel, Folsom, CA

A 128Mb flash memory with a two bit-per-cell design on a 0.13µm technology achieves a random access time of 55ns and 125MHz synchronous operation. The design incorporates a flexible multi-partition memory architecture which allows a program or erase operation to occur in one partition of the memory while bursting data out of another partition. The die is $27.3mm^2$ with a $0.154\mu m^2$ cell size.

16.6 A 1Gb Multilevel AG-AND-Type Flash Memory with 10MB/s Programming Throughput for Mass Storage Application

4:15 PM

K. Yoshida[1], O. Tsuchiya[1], Y. Yamaguchi[1], J. Kishimoto[1], Y. Takase[1], T. Yoshitake[1], Y. Ikeda[1], S. Narumi[1], K. Furusawa[1], K. Izawa[1], T. Kobayashi[1], H. Kurata[1], M. Kanamitsu[2]
[1]Hitachi, Ome, Japan
[2]Hitachi ULSI Systems, Ome, Japan

A 1Gb multilevel flash memory is fabricated in a 0.13µm CMOS process. The chip area of $95mm^2$ is achieved using AG-AND-type cells with a multilevel program cell technique and compact write-buffer. By use of constant-charge-injection programming and multi-bank operation, high-speed programming throughput of 10MB/s is achieved.

16.7 A 1.8V 2Gb NAND Flash Memory for Mass Storage Applications

4:45 PM

J. Lee, S-S. Lee, O-S. Kwon, K-H. Lee, K-H. Lee, D-S. Byeon, I-Y. Kim, Y-H. Lim, B-S. Choi, J-S. Lee, W-C. Shin, J-H. Choi, K-D. Suh
Samsung Electronics, Hwasung, Republic of Korea

A 1.8V 2Gb NAND flash memory is fabricated in a 90nm process resulting in a $141mm^2$ die and a $0.044\mu m^2$ effective cell. To achieve the high level of integration, critical layers are patterned with KF photolithography and phase-shift masks with proximity correction.

CONCLUSION 5:15 PM

E4: Future Mobile Phones: A Beautiful Dream or Smoke in LSI Technology?

(Salon 7)

Co-organizer: **Masayuki Mizuno,** Assistant Manager, *NEC, Sagamihara, Kanagawa, Japan*
Co-organizer: **Akira Matsuzawa,** General Manager, *Matsushita Electric, Osaka, Japan*
Moderator: **Tadahiro Kuroda,** Professor, *Keio University, Yokohama, Japan*

We will discuss technical obstacles to realizing chips that will be necessary for mobile phones in 2010. We will focus on applications in future mobile phones and chips that provide high-quality video codecs, fingerprint certification, voice recognition, dictation, Java, GPS, wireless LAN, and baseband modems.

— What is the biggest technical obstacle to realizing such application chips?
— What kind of chip architecture, circuits, and devices are preferred in overcoming this obstacle?

Panelists:

Avner Goren, Architecture Marketing Manager, *Texas Instruments Inc., Dallas, TX*
Hoi-Jun Yoo, Professor, *KAIST, Daejon, Korea*
Hugo De Man, Professor, *Katholieke Universiteit Leuven and Senior Research Fellow IMEC, Leuven, Belgium*
Jay Heeb, Senior Architect, *Intel Corporation, Chandler, AZ*
Katsuhiko Ueda, Director, *Matsushita Electric Industiries, Kyoto, Japan*
Naohiko Irie, Senior Researcher, *Hitachi, Tokyo, Japan*

E5: Fineline Prototyping: Breaking New Ground or Breaking the Bank?

(Salon 8)

Organizer/Moderator: **Roger Minear,** Distinguished Member of Technical Staff, *Agere Systems, Allentown, PA*

With giga$ wafer fabs, near-mega$ mask sets, and several kilo$ wafers already here, the cost of prototyping high-performance fineline designs is large and rapidly increasing. This panel will explore the options available to fab providers and designers. We will discuss:

— What prototyping cost control strategies are design organizations following today?
— Are prototyping costs or process standardization requirements inhibiting novel, aggressive, or small-volume designs?
— Could new fab services improve the current situation?

Panelists:

Qiuting Huang, *Swiss Federal Institute of Technology, Zurich, Switzerland*
Dale Pearson, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
Wolfgang Pribyl, *Austriamicrosystems, Schloss Premstätten, Austria*
Stefanos Sidiropoulos, A*eluros, Mountain View, CA*
David Sheng, *Taiwan Semiconductor Manufacturing, San Jose, CA*
Vahid Manian, *Broadcom, Irvine, CA*

E6: SoC: DOA? RIP?

(Salon 9)

Organizer: **K. Nagaraj,** *Texas Instruments, Warren, NJ*
Moderator: **David Allstot,** *University of Washington, Seattle, WA*

While a "True System-on-a-Chip" is the dream of all major chip makers, it is not clear if and when and how this dream will be realized. How are we going to integrate RF circuits including high-quality passives and precision analog circuits with ULSI digital circuitry? Will the issues of noise coupling and/or MOSFET gate leakages become show stoppers for SoCs? Will cost considerations mandate multi-chip multi-technology solutions? Are small-signal and large-signal functions more suited to different technologies than SoC solutions? Will production testing issues mandate multi-chip solutions? This panel will address these issues.

Panelists:

Bruce Wooley, Professor, *Stanford University, Stanford, CA*
Dennis Buss, Vice President, *Texas Instruments, Dallas, TX*
Ken Hansen, Vice President, *Motorola, Austin, TX*
Greg Atwood, Director, *Intel, Portland, OR*
Chris Mangelsdorf, Director, *Analog Devices, Japan*
Robert Mertens, Senior Vice President, *IMEC, Leuven, Belgium*

SRAM AND DRAM

Chair: **Alex Shubat,** *Virage Logic, Fremont, CA*
Associate Chair: **Katsuyuki Sato,** *Elpida Memory, Kanagawa, Japan*

17.1 A 1.2V 1.5Gb/s 72Mb DDR3 SRAM

8:30 AM

U-R. Cho, T-H. Kim, Y-J. Yoon, J-C. Lee, D-G. Bae, N-S. Kim, K-Y. Kim, Y-J. Son, J-S. Yang, K-I. Sohn, S-T. Kim, I-Y. Lee, K-J. Lee, T-G. Kang, S-C. Kim, K-S. Ahn, H-G. Byun
Samsung Electronics, Hwasung, Republic of Korea

A 1.2V 72Mb DDR3 SRAM in a 0.10µm CMOS process achieves a data rate of 1.5Gb/s using dynamic self-resetting circuits. Single-ended main data lines reduce the power dissipation and the number of data lines by half. Clocks phase-shifted by 0°, 90° and 270° are generated by clock adjustment circuits. On-chip input termination with linearity of ±4.1% is developed to improve signal integrity at higher data rates.

17.2 16.7fA/cell Tunnel-Leakage-Suppressed 16Mb SRAM for Handling Cosmic-Ray-Induced Multi-Errors

9:00 AM

K. Osada[1], Y. Saitoh[1], E. Ibe[2], K. Ishibashi[2]
[1]Hitachi, Tokyo, Japan
[2]Hitachi, Kanagawa, Japan

A 16Mb SRAM based on an electric-field-relaxed scheme and an alternate error checking and correction architecture for handling cosmic-ray-induced multi-errors is realized in 0.13µm CMOS technology. The IC has a 16.7fA/cell standby current, a cell size of 2.06µm^2 and a 99.5% smaller SER.

17.3 A Current-Saving Match-Line Sensing Scheme for Content-Addressable Memories

9:30 AM

I. Arsovski, A. Sheikholeslami
University of Toronto, Toronto, Canada

A match-line sensing scheme that reduces power consumption in content-addressable memories by dynamically allocating less power to match-lines with more mismatches is described. This scheme is implemented in a 256x144bit CAM using 1.2V 0.13µm CMOS achieving a 2ns search time at 1.3fJ/bit/search.

BREAK 10:00 AM

17.4 A High Density Memory for SoC with a 143MHz SRAM Interface Using Sense-Synchronized-Read/Write

10:15 AM

Y. Taito[1], T. Tanizaki[1], M. Kinoshita[1], F. Igaue[2], T. Fujino[1], K. Arimoto[1]
[1]Mitsubishi Electric, Itami, Japan
[2]Mitsubishi Electric Engineering, Itami, Japan

A high density memory (HDRAM) for SoC with SRAM interface is described. This macro achieves no-wait fast random-cycle operation owing to a sense-synchronized read/write scheme. A 4Mb test device is fabricated in a 0.15µm process and achieves 143MHz operation. Its size and standby power are 4.59mm^2 and 92mW, which are 30% and 4.8%, respectively, of an embedded SRAM macro fabricated identically.

17.5 A 5.6ns Random Cycle 144Mb DRAM with 1.4Gb/s/pin and DDR3-SRAM Interface

10:45 AM

H. Pilo, D. Anand, J. Barth, S. Burns, P. Corson, J. Covino, R. Houghton, S. Lamphier
IBM, Essex Junction, VT

A 144Mb DRAM operates at a random cycle of 5.6ns and is capable of producing data rates of 1.4Gb/s/pin. The 121mm^2 die is fabricated in a 0.13µm logic-based process. The cycle-time is achieved using an early-write sensing technique. Dynamic-precharge decoding and improved data-formatting circuits produce latencies of 5.0ns.

17.6 A 1.0V 256Mb SDRAM with Offset-Compensated Direct Sensing and Charge-Recycled Precharge

11:15 AM

J-Y. Sim, K-W. Kwon, J-H. Choi, S-H. Lee, D-M. Kim, H-R. Hwang, K-C. Chun, Y-H. Seo, H-S. Hwang, D-I. Seo, C. Kim, S-I. Cho
Samsung Electronics, Hwasung, Republic of Korea

A 1.0V, 256Mb SDRAM is designed in a 0.1µm CMOS technology. For low voltage applications, an offset compensated direct current sensing scheme improves refresh time as well as sensing performance. A charge-recycled precharge reuses the word-line discharge current to generate the boosted voltage required for equalization without charge pumping. At 1.0V, the access time is 25ns and the current is 15mA.

17.7 A 1.8V 700Mb/s/pin 512Mb DDR-II SDRAM with On-Die Termination and Off-Chip Driver Calibration

11:45 AM

C. Yoo, K-H. Kyung, G-H. Han, K. Lim, H. Lee, J. Chai, N-W. Heo, G. Byun, D-J. Lee, H-I. Choi, H-C. Choi, C-H. Kim, S-I. Cho
Samsung Electronics, Hwa-Sung, Republic of Korea

A 1.8V 700Mb/s/pin 512Mb DDR-II SDRAM is JEDEC standard compliant. With the hierarchical I/O line and local sensing, $t_{AA}/t_{RCD}/t_{RP}$ of 3/3/3 at 533Mb/s are achieved in the design. For signal integrity at 533Mb/s, off-chip driver calibration and on-die termination are employed.

17.8 A 1.2Gb/s/pin Double Data Rate SDRAM with On-Die-Termination

12:00 PM

H. Song, S. Jang, J. Kwak, Y. Jun, C. Kim, C. Kang, D. Jeong, Y. Park, M. Park, K. Byun, W. Lee, Y. Cho, W. Shin, Y. Jang, S. Hwang, S. Cho
Samsung Electronics, Hwa-sung, Republic of Korea

For operating frequencies exceeding 500MHz, the timing margin of the I/O interface is critical and requires the data input-output timing accuracy to be within 200ps. To meet the requirement, the designed SDRAM adopts a digitally self-calibrated on-die-termination with linearity error of ±1% and achieves over 1.2Gbps/pin stable operation by using window matching and latency control. The chip is fabricated in a 0.13µm triple-well DRAM process.

CONCLUSION 12:15 PM

NYQUIST A/D CONVERTERS

Chair: **Venu Gopinathan,** *Broadcom, Irvine, CA*
Associate Chair: **Bram Nauta,** *University of Twente, Endschede, The Netherlands*

18.1 A 20GS/s 8b ADC with a 1MB Memory in 0.18μm CMOS

8:30 AM

K. Poulton[1], R. Neff[1], B. Setterberg[1], B. Wuppermann[1], T. Kopley[1], R. Jewett[1], J. Pernillo[1], C. Tan[1], A. Montijo[2]
[1]Agilent Laboratories, Palo Alto, CA
[2]Agilent Technologies, Colorado Springs, CO

A 20GS/s 8-bit ADC achieves a bandwidth of 6GHz in 0.18μm CMOS. The implementation uses 80 time-interleaved current-mode pipeline sub-ADCs and stores data at 20GB/s into a 1MB on-chip memory. The ADC is packaged with a BiCMOS input buffer chip in a 438-ball BGA, and total power consumption is 10W.

18.2 A 20GHz Bandwidth, 4b Photoconductive-Sampling Time-Interleaved CMOS ADC

9:00 AM

L. Nathawad[1], R. Urata[2], B. Wooley[1], D. Miller[2]
[1]Center for Integrated Systems, Stanford University, Stanford, CA
[2]E. L. Ginzton Laboratory, Stanford University, Stanford, CA

GaAs photoconductive switches are integrated with two parallel 4b CMOS ADC channels for time-interleaved sampling of wideband signals. Peak SNDR exceeding 23dB has been measured for inputs up to 20GHz. Each channel dissipates 70mW and occupies an area of 150μm×450μm in a 0.25μm CMOS technology.

18.3 A 2GS/s 6b ADC in 0.18μm CMOS

9:30 AM

X. Jiang, Z. Wang, M-C. Chang
University of California, Los Angeles, California

A 2GS/s 6-bit ADC with time-interleaving is demonstrated in 0.18μm CMOS. Three cross-connected and pre-distorted reference voltages improve the averaging performance. Circuit techniques enabling an SNDR of 30dB at Nyquist input frequency and a FOM of 3.5pJ per conversion step are discussed, and experimental results validating the simulated performance metrics are presented.

BREAK 10:00

18.4 A 69mW 10b 80MS/s Pipelined CMOS ADC

10:15 AM

B-M. Min, P. Kim, D. Boisvert
National Semiconductor, Salem, NH

A 10b 80MHz pipelined ADC with an active area of 1.85mm^2 is realized in a 0.18μm dual gate oxidation CMOS process and achieves 72.8dBc SFDR, 57.92dB SNR, and 9.29 ENOB for a 100MHz input at full sampling rate. The ADC shares an amplifier between two successive pipeline stages in order to achieve a power consumption of 69mW at 3V.

18.5 A 10b 150MS/s 123mW 0.18μm CMOS Pipelined ADC

10:45 AM

S-M. Yoo[1], J-B. Park[2], H-S. Yang[2], H-H. Bae[2], K-H. Moon[1], H-J. Park[1], S-H. Lee[2], J-W. Kim[1]
[1]Samsung Electronics, Yongin, Republic of Korea
[2]Sogang University, Seoul, Republic of Korea

A 10b 150MHz multi-bit-per-stage single-channel CMOS pipelined ADC incorporating temperature- and supply-insensitive CMOS references and improved gate-bootstrapping techniques for a wideband SHA achieves a SNDR of 52dB and SFDR of 65dB at 150MS/s. The ADC, fabricated in 0.18μm CMOS, occupies an active die area of 2.2mm^2 and consumes 123mW at 1.8V.

18.6 A 12b 75MS/s Pipelined ADC using Open-Loop Residue Amplification

11:15 AM

B. Murmann, B. Boser
University of California, Berkeley, CA

The multi-bit first stage of a 12b 75MS/s pipelined ADC uses an open-loop gain stage to achieve more than 60% residue amplifier power savings over a conventional implementation. Statistical background calibration removes linear and nonlinear residue errors in the digital domain. The prototype IC achieves 68.2dB SNR, -76dB THD, occupies 7.9mm^2 in 0.35μm CMOS and consumes 290mW at 3V.

18.7 Impact of Dielectric Relaxation on a 14b Pipeline ADC in 3V SiGe BiCMOS

11:45 AM

A. Zanchi, F. Tsay, I. Papantonopoulos
Texas Instruments, Dallas, TX

Dielectric relaxation in PECVD SiN capacitors of a 45GHz 0.4μm SiGe BiCMOS process degrades performance even at low frequencies. In the design of pipelined 14b 70MS/s ADC, the effects of dielectric relaxation are identified via behavioral/circuit simulations and ad-hoc tests. After LPCVD oxide capacitors are introduced, a 5.3x5.3mm^2 test chip delivers 72dB SNR, 81dBc SFDR, and 11.5 ENOB at 70MS/s. The IC operates at a 1MHz input and dissipates 1W from 3.3V.

CONCLUSION 12:00 PM

PROCESSOR BUILDING BLOCKS

Chair: **Samuel Naffziger,** *Hewlett Packard, Fort Collins, CO*
Associate Chair: **Georgios Konstadinidis,** *Sun Microsystems, Sunnyvale, CA*

19.1 A 5GHz Floating Point Multiply-Accumulator in 90nm Dual V_T CMOS

8:30 AM

S. Vangal, Y. Hoskote, D. Somasekhar, V. Govindarajulu, V. Erraguntla, H. Wilson, J. Howard, Y. Niu, G. Ruhl, A. Pangal, V. Veeramachaneni, D. Finan, J. Tschanz, S. Mathew, N. Borkar, S. Borkar
Intel, Hillsboro, OR

A 32b single-cycle floating point accumulator that uses base 32 and carry-save format with delayed addition is described. Combined algorithmic, logic and circuit techniques enable multiply-accumulate operation at 5GHz. In a 90nm 7M dual-V_T CMOS process, the 2mm^2 prototype contains 230K transistors and dissipates 1.2W at 5GHz, 1.2V and 25°C.

19.2 A Double Precision Floating Point Multiplier

9:00 AM

R. Montoye, W. Belluomini, H. Ngo, C. McDowell, J. Sawada, T. Nguyen, B. Veraa, J. Wagoner, M. Lee, M. Canada
IBM, Austin, TX

A 2.2GHz 53x54 bit pipelined multiplier is fabricated in 130nm CMOS technology with an area of 0.15mm^2. The circuit implementation results in a 50% size reduction over the previously reported values. The circuit operates at 2.2GHz and uses 522mW at 80% switching factor, a 1.2V supply and 25°C.

19.3 A 400MT/s 6.4GB/s Multiprocessor Bus Interface

9:30 AM

H. Muljono, B. Lee, K. Tian, Y. Wang, M. Atha, T. Huang, M. Adachi
Intel, Santa Clara, CA

A 0.13μm 1.2V GTL bus interface with compensated slew rate and termination achieves 400MT/s at a 6.4GB/s data rate in a 5-load MP environment. Packaged on an FCBGA and interposer with 5:1:4 signal to power and ground ratio and routed on 12mm 45Ω traces, the interface incorporates I/O timing self test supported by a DLL and an interpolator with 25ps peak-to-peak jitter.

BREAK 10:00 AM

19.4 A 2X Load/Store Pipe for a Low-Power 1GHz Embedded Processor

10:15 AM

Z. Chen, M. Pearce, D. Murray, S. Nishimoto, M. Oyker, D. Rodriguez, D. Suh, E. Supnet, G. Yiu
Broadcom, Santa Clara, CA

The load/store pipe in an embedded processor is clocked at 2X the processor clock frequency. It sustains two load or store operations per core clock cycle with zero load-to-use issue latency. The design is implemented in 0.13µm 7M process and dissipates between 650 and 1090mW for core clock frequencies between 600MHz and 1GHz.

19.5 A Clock Skew Absorbing Flip-Flop

10:45 AM

N. Nedovic[1], V. Oklobdzija[2], W. Walker[1]
[1]Fujitsu Laboratories of America, Sunnyvale, CA
[2]University of California, Davis, CA

A 0.11µm 1.2V CMOS flip-flop absorbs up to 50ps of clock skew. Measured results confirm 27% delay and 33% energy-delay product improvement over previously reported flip-flops, regardless of clock skew.

19.6 40Gb/s 2:1 Multiplexer and 1:2 Demultiplexer in 120nm CMOS

11:15 AM

D. Kehrer[1], H-D. Wohlmuth[1], H. Knapp[1], M. Wurzer[1], A. Scholtz[2]
[1]Infineon, Munich, Germany
[2]Technical University of Vienna, Vienna, Austria

A 40Gb/s 2:1 multiplexer in 120nm 1.2V CMOS uses inductive peaking and output series inductor. A companion 1:2 demultiplexer is also described.

19.7 A Scalable Sub-10ps Skew Global Clock Distribution for a 90nm Multi-GHz IA Microprocessor

11:45 AM

N. Bindal[1], T. Kelly[1], N. Velastegui[2], R. Raman[1], K. Wong[1]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA

A three-level clock distribution design for a next generation IA microprocessor is implemented in a 1.2V, 90nm process that scales to a 5GHz range. It achieves sub-10ps global clock uncertainty and addresses in-die variation, RLC delay matching, and scalability with die size and process issues without additional clock jitter or layout area. Risk management of practical constraints due to schedule, changing floor plan, loading and process are discussed

CONCLUSION 12:15 PM

WIRELESS LOCAL AREA NETWORKING

Chair: **Charles Chien,** *G-Plus, Santa Monica, CA*
Associate Chair: **David Ngo,** *Micro Devices, Chandler, AZ*

20.1 A Multi Standard Single-Chip Transceiver Covering 5.15 to 5.85GHz

8:30 AM

T. Schwanenberger, M. Ipek, S. Roth, H. Schemmann
Thomson Multimedia, Villingen-Schwenningen, Germany

This transceiver achieves a transmit 1dB output compression point of +15dBm, and the overall receiver noise figure is 5dB. A power gain range of > 45dB/65dB for transmit/receive and a PLL synthesizer frequency range of 4.9 to 5.85GHz with -79dBc/Hz phase noise at 10kHz offset have been measured. The IC is realized in 0.5μm SiGe BICMOS technology and occupies 17mm^2.

20.2 A Digitally Calibrated 5.15 - 5.825GHz Transceiver for 802.11a Wireless LANs in 0.18μm CMOS

9:00 AM

I. Bouras[1], S. Bouras[1], T. Georgantas[1], N. Haralabidis[1], G. Kamoulakos[1], C. Kapnistis[1], S. Kavadias[1], Y. Kokolakis[1], P. Merakos[1], J. Rudell[2], S. Plevridis[1], I. Vassiliou[3], K. Vavelidis[1], A. Yamanaka[3]
[1]Athena Semiconductors, Athens, Greece
[2]Berkana Wireless, San Jose, CA
[3]Athena Semiconductors, Fremont, CA

A 5GHz transceiver operating in all three 802.11a bands is manufactured in 0.18μm CMOS and occupies 18.5mm^2. It consumes 250mW in RX and 300mW in TX. The fully integrated VCO and synthesizer achieve an integrated phase noise of less than -37.4dBc. The receiver includes programmable low-pass filters. Overall NF is less than 5.5dB, and digital calibration enables sensitivity better than -70dBm for the 54Mb/s mode.

20.3 A Direct Conversion CMOS Transceiver for IEEE 802.11a Wireless LANs

9:30 AM

P. Zhang[1], T. Nguyen[1], C. Lam[1], D. Gambetta[1], C. Soorapanth[1], J. Cheng[1], S. Hart[1], I. Sever[1], T. Bourdi[1], A. Tham[1], B. Razavi[2]
[1]Resonext Communications, San Jose, CA
[2]University of California, Los Angeles, CA

A 0.18μm CMOS transceiver fully compliant with IEEE 802.11a in the U-NII band (5.15-5.35GHz) achieves a sensitivity of -69dBm and an EVM of -29.3dB for 64 QAM. Power dissipation is 171mW in RX and 138mW in TX using a 1.8V supply.

BREAK 10:00 AM

20.4 Direct-Conversion CMOS Transceiver with Automatic Frequency Control for 802.11a Wireless LANs

10:15 AM

A. Behzad[1], L. Lin[2], Z. Shi[1], S. Anand[3], K. Carter[3], M. Kappes[1], T. Nguyen[2], D. Yuan[1], V. Fong[4], A. Rofougaran[3]
[1]Broadcom, San Diego, CA
[2]Broadcom, Sunnyvale, CA
[3]Broadcom, El Segundo, CA
[4]Broadcom, San Jose, CA

A 11.7mm^2 5GHz direct-conversion 0.18μm CMOS transceiver achieves a sensitivity of -93dBm, a system NF of 4.5dB (high gain), and IIP3 of -4.8dBm (low gain). Dissipation is 150mW in RX mode and 380mW while transmitting 15dBm OFDM signal.

20.5 A 2.4GHz CMOS Transceiver and Baseband Processor Chipset for 802.11b Wireless LAN Application

10:45 AM

G. Chien, W. Feng, Y. Hsu, L. Tse
Marvell Semiconductor, Sunnyvale, CA

A fully integrated 2.4GHz CMOS transceiver in 0.25µm CMOS and its associated baseband processor in 0.15µm CMOS are described. The RF transceiver IC occupies 16mm^2. The total power consumption is 350mW in RX and 1.25W in TX with +20dBm output power. The chipset complies with the IEEE 802.11b and achieves a RX sensitivity of -87dBm at 11Mb/s.

20.6 A 2.4GHz CMOS Transceiver for 802.11b Wireless LANs

11:15 AM

W. Kluge, L. Dathe, R. Jaehne, S. Ehrenreich, D. Eggert
Advanced Micro Devices, Dresden, Germany

A 0.25µm CMOS zero-IF transceiver with VCO and PLL (-111dBc/Hz at 1MHz) has been implemented. The 3.1x3.1mm^2 IC draws 86mA (RX) and 73mA (TX) from a 2.5V supply. The receiver exhibits a 5dB noise figure and 5µs AGC settling time. RX channel filter, TX pulse shaping filter, filter calibration circuitry, 6b ADC, bandgap reference and TX preamplifier are included and controlled by a digital interface.

20.7 An Integrated 5.2GHz CMOS T/R Switch with LC-tuned Substrate Bias

11:45 AM

N. Talwalkar[1], C. Yue[2], S. Wong[1]
[1]Stanford University, Stanford, CA
[2]Atheros Communications, Sunnyvale, CA

A 0.56mm^2 T/R switch in 0.18µm CMOS achieves 1.5dB insertion loss, 28dBm P_{1dB}, 30dB isolation and 4kV HBM ESD rating. The switch uses an on-chip LC-tuned substrate biasing technique to enhance linearity and allows the LNA and PA to be matched independently. Power dissipation is 30µW.

20.8 A SiGe Low Noise Amplifier for 2.4/5.2/5.7GHz WLAN Applications

12:00 PM

P-W. Lee[1], H-W. Chiu[1], T-L. Hsieh[1], G-W. Huang[2], S-S. Lu[1]
[1]National Taiwan University, Taipei, Taiwan, Republic of China
[2]National Nano Device Lab., Hsinchu, Taiwan, Republic of China

A 355µmx155µm LNA in 0.35µm SiGe CMOS uses a simple bias switching technique to operate in all three WLAN bands. Noise figure is 2.73dB at 2V, 6.5mA and 5.7GHz.

CONCLUSION 12:15 PM

TD: ORGANIC AND NANOSCALE TECHNOLOGIES

Chair: **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
Associate Chair: **Yukihito Oowaki,** *Toshiba, Kanagawa, Japan*

21.1 Topolithography and its Application to the Manufacture of 3D Diode-based Memories

8:30 AM

D. Shepard
Nüp2, North Hampton, NH

Topolithography is a process wherein all of the information necessary to define a circuit is applied to a substrate in a single step. A multi-level surface topology defines the circuit for subsequent self-assembly so no photolithographic steps are required to manufacture a circuit resulting in substantially reduced costs. A transistor-less memory circuit is designed where high density storage, address decoding and I/O are implemented using an array of diodes.

21.2 Carbon Nanotube Field Effect Transistors - Fabrication, Device Physics, and Circuit Implications

9:00 AM

H-S. Wong, J. Appenzeller, V. Derycke, R. Martel, S. Wind, P. Avouris
IBM Thomas J. Watson Research, Yorktown Heights, NY

The device and circuit implications of carbon nanotube field effect transistors (CNFET) as a logic technology are assessed. The salient device characteristics and fabrication techniques are described based on measured device parameters. The device/circuit performance of CNFET are estimated and the key technical challenges to developing the CNFET as a logic technology are discussed.

21.3 Sea of Dual Mode Polymer Pillar I/O Interconnects for GSI

9:30 AM

M. Bakir, A. Mule, T. Gaylord, P. Kohl, K. Martin, J. Meindl
Georgia Institute of Technology, Atlanta, GA

Sea of Polymer Pillars offers highly compliant electrical, optical, and RF wafer-level I/O interconnects at an I/O density larger than $10^5/cm^2$. Dual mode I/O pillars function simultaneously as both electrical and optical interconnects to offer circuit/system designers essentially unlimited I/O bandwidth at potentially the lowest cost.

21.4 SiGe Pin-Photodetectors Integrated on Silicon Substrates for Optical Fiber Links

9:45 AM

G. Wöehl, C. Parry, E. Kasper, M. Jutzi, M. Berroth
University of Stuttgart, Stuttgart, Germany

100% Ge pin-photodetectors grown on SiGe strain relaxed buffer (SRB) layers are presented. For integrated detectors the SRB layer growth as well as the subsequent SiGe photodiode technology processing must be compatible with standard CMOS technology. DC-photoresponsivities of 145mA/W at 1.3µm and 25mA/W at 1.55µm can be achieved. In first experiments the 100% Ge pin-photodetector exhibits an RC limited 3dB opto-electrical bandwidth of 0.9GHz.

BREAK 10:00 AM

21.5 Strained SOI Technology for High-Performance, Low-Power CMOS Applications

10:15 AM

S-I. Takagi[1], T. Mizuno[1], T. Tezuka[1], N. Sugiyama[1], T. Numata[1], K. Usuda[1], Y. Moriyama[1], S. Nakaharai[1], J. Koga[1], A. Tanabe[1], T. Maeda[2]
[1]MIRAI-ASET, Kawasaki, Japan
[2]MIRAI-AIST, Kawasaki, Japan

Advantages of strained-SOI CMOS and the impact on circuit performance are presented from the viewpoint of ring oscillator speed, floating body effects, threshold voltage control and gate leakage reduction. Circuit performance enhancement of about 1.7 times over conventional SOI CMOS is verified experimentally at 0.95μm gate lengths and theoretically expected even at gate lengths of 50nm.

21.6 Evaluation of the Performance Potential of Organic TFT Circuits

10:45 AM

R. Brederlow[1], S. Briole[1], H. Klauk[2], M. Halik[2], U. Zschieschang[2], G. Schmid[2], J-M. Gorriz-Saez[1], C. Pacha[1], R. Thewes[1], W. Weber[1]
[1]Infineon Technologies, Munich, Germany
[2]Infineon Technologies, Erlangen, Germany

Organic thin film transistors (TFTs) on flexible substrates are promising candidates for low-cost, low-performance electronic applications. Based on experimental data from the fastest organic circuits reported, the performance potential of organic TFTs is evaluated using a new physics-based compact model for the simulation of basic logic circuits.

21.7 Plastic Transistors in Active-matrix Displays

11:15 AM

E. Huitema, G. Gelinck, J. van der Putten, E. Cantatore, E. van Veenendaal, L. Schrijnemakers, B-H. Huisman, D. de Leeuw
Philips Research, Eindhoven, The Netherlands

An active-matrix display driven by a pixel circuit with polymer-based thin film transistors is demonstrated. The circuit contains 4096 solution-processed plastic transistors, which is among the largest organic circuits reported to date. The relation between the transistor parameters such as mobility and leakage current to the display performance is analyzed.

21.8 Circuit Yield of Organic Integrated Electronics

11:45 AM

E. Cantatore, C. Hart, M. Digioia[1], G. Gelinck, T. Geuns, H. Huitema, L. Schrijnemakers, E. van Veenendaal, D. de Leeuw
Philips Research, Eindhoven, The Netherlands
[1]now with STMicroelectronics, Milan, Italy

Research on organic electronics is focussed on materials and on the performance of discrete devices. Reliability and circuit yield is largely unexplored. Yield, based on measurements on digital organic circuits up to 1000 transistors, is described. The causes of yield loss are analyzed and design solutions to improve the yield are discussed.

CONCLUSION 12:15 PM

TD: EMBEDDED TECHNOLOGIES

Chair: **John Long,** *Delft University of Technology, The Netherlands*
Associate Chair: **Raf Roovers,** *Philips Research, Eindhoven, The Netherlands*

22.1 Enabling Technologies for Disappearing Electronics in Smart Textiles

1:30 PM

S. Jung, C. Lauterbach, M. Strasser, W. Weber
Infineon Technologies, Corporate Research, Munich, Germany

Enabling technologies for 'wearable electronics', such as packaging and interconnect, are key to the integration of electronics in textiles. A silicon-based micromachined thermoelectric generator chip for energy harvesting from body heat, and an interwoven antenna concept for textile radio frequency identification labels are presented.

22.2 A Batteryless Wireless System Uses Ambient Heat with a Reversible-Power-Source Compatible CMOS/SOI DC-DC Converter

2:00 PM

T. Douseki[1], Y. Yoshida[2], F. Utsunomiya[2], N. Itoh[3], N. Hama[4]
[1]NTT, Atsugi, Japan
[2]Seiko Instruments, Matsudo, Japan
[3]Seiko Epson, Suwa, Japan
[4]Seiko Epson, Fujimi, Japan

A 1mW, self-powered wireless system that utilizes ambient heat is described. A switched-capacitor DC-DC converter composed of fully-depleted SOI MOSFETs and a microthermoelectric module makes use of such heat possible. An experimental 300MHz band short-range wireless transmitter transmits from a distance of 5m using only heat from a hand or from water. The chip is fabricated in a 0.8μm fully-depleted SOI process.

22.3 An On-Chip High Speed Serial Communication Method Based on Independent Ring Oscillators

2:30 PM

S. Kimura[1], T. Hayakawa[2], T. Horiyama[3], M. Nakanishi[4], K. Watanabe[4]
[1]Waseda University, Kitakyushu, Japan
[2]Japan Patent Office, Tokyo, Japan
[3]Kyoto University, Kyoto, Japan
[4]Nara Institute of Science and Technology, Ikoma, Japan

An on-chip module to module serial data transfer method uses parallel-to-serial conversion with a high frequency clock generated by internal ring oscillators. Both sender and receiver have their own rings which are synchronized by a one bit control line. A 7.84mm^2 prototype in 0.18μm technology operates from a 1GHz clock.

22.4 Low-Noise Monolithic Oscillator with an Integrated Three-Dimensional Inductor

2:45 PM

K. Van Schuylenbergh[1], B. Griffiths[2], C. Chua[1], D. Fork[1], J-P. Lu[1]
[1]PARC, Palo Alto, CA
[2]Mixed Signal Systems, Scotts Valley, CA

A balanced silicon BiCMOS oscillator using self-assembled curled circular spring 3D inductor with peak Q of 40 reduces phase noise by 12.3dB at 100kHz offset compared to conventional planar spiral inductor approach. The addition of a 5μm copper underlayer raises Q to 85.

BREAK 3:00 PM

22.5 Portable MEMS Power Sources

3:15 PM

M. Schmidt
Massachusetts Institute of Technology, Cambridge, MA

Two devices are described that realize MEMS-based power sources as alternatives to batteries. The first is thermoelectric which utilizes a SiGe thermopile on a silicon nitride membrane. The device generates power at 500°C. The second device is an engine that consists of a high-speed rotating silicon turbine.

22.6 On-Chip Interconnect for mm-Wave Applications Using an All-Copper Technology and Wavelength Reduction

3:45 PM

D. Cheung[1], J. Long[2], K. Vaed[3], R. Volant[3], A. Chinthakindi[3], C. Schnabel[3], J. Florkey[3], K. Stein[3]
[1]University of Toronto, Toronto, Canada
[2]Delft University of Technology, Delft, The Netherlands
[3]IBM Microelectronics, Hopewell Junction, NY

Transmission lines are implemented using an all-copper backend developed for RF and microwave applications. Wavelength reduction is used to achieve a Q factor >20 from 20GHz to 40GHz, about three times higher than conventional transmission lines implemented with the same technology. It has 0.3dB/mm loss, and reduces the wavelength of a conventional transmission line by half thereby minimizing the space for on-chip microwave devices.

22.7 Powder LSI: An Ultra Small RF Identification Chip for Individual Recognition Applications

4:15 PM

M. Usami[1], A. Sato[1], K. Sameshima[1], K. Watanabe[1], H. Yoshigi[1], R. Imura[2]
[1]Hitachi Central Research Laboratory, Tokyo, Japan
[2]Hitachi Mu-Solutions Venture Company, Tokyo, Japan

A powder-like 0.09mm^2 2.45GHz RF identification chip for wireless recognition applications is described. This chip is fabricated in a 0.18μm CMOS process, and its thickness is 60μm. A two-surface connection technique is adopted to facilitate antenna attachment. The distance between the chip and a reader is 300mm for a reader power of 300mW.

22.8 Zigzag Super Cut-off CMOS Logic Block Activation with Self-Adaptive Voltage Level Controller

4:45 PM

K-S. Min[1], T. Sakurai[2]
[1]Kookmin University, Seoul, Republic of Korea
[2]University of Tokyo, Tokyo, Japan

A block activation/deactivation technique uses zigzag super cut-off CMOS to improve wake up time by 8x in 0.6μm CMOS versus super cut-off CMOS.

22.9 Self-corrective Device and Architecture to Ensure LSI Operation at 0.5V Using Bulk Dynamic Threshold MOS FET with a Self-Adaptive Power Supply

5:00 PM

S. Kakimoto, T. Okuno, Y. Iwase, Y. Yaoi, F. Yoshioka, K. Kimoto, M. Nakano, K. Kawashima, S. Morishita, K. Sugimoto, T. Shiomi, T. Okumine, K. Kataoka, A. Shibata, S. Toyoyama, Y. Satoh, K. Fujimoto, K. Tatsumi, H. Kotaki, A. Kito
Sharp, Tenri, Japan

520k transistor CDMA matched filter operation at 0.5V is achieved using Bulk Dynamic Threshold MOSFET device and self-adaptive power supply system. B-DTMOS reduces threshold voltage dispersion. SAPS architecture maximizes performance under worst case conditions.

CONCLUSION 5:00 PM

MIXED-SIGNAL AND WIRELINE TECHNIQUES

Chair: **Cormac Conroy,** *Berkana Wireless, San Jose, CA*
Associate Chair: **Axel Thomsen,** *Silicon Laboratories, Austin, TX*

23.1 A MOS Capacitor-Based Discrete-Time Parametric Amplifier with 1.2V Output Swing and 3μW Power Dissipation

1:30 PM

S. Ranganathan, Y. Tsividis
Columbia University, New York, NY

Experimental results are reported for an amplifier based on a little-known effect in MOS capacitors: a voltage sampled on the gate rises when the channel charge is pulled out. It is demonstrated that this phenomenon can be used to provide micro-power, low-gain, and low-noise signal amplification.

23.2 A 0.9V 0.5μW CMOS Single Switched-Op-amp Signal-Conditioning System for Pacemaker Applications

2:00 PM

V. Cheung, H. Luong
Hong Kong University of Science and Technology, Hong Kong, China

A 0.5μW switched-capacitor signal-conditioning system with integrated switched-op-amp filter and ΣΔ modulator is implemented in a 0.35μm CMOS process. A power-efficient single op-amp architecture employing half-delay SC integrators is utilized for the whole system. Operated from a 0.9V supply, the system has a dynamic range of 45dB.

23.3 A 100MHz DDS With Synchronous Oscillator-Based Phase Interpolator

2:30 PM

F. Badets, D. Belot
STMicroelectronics, Crolles, France

A synchronous oscillator-based phase interpolator is used to lower spurious tones of a 100MHz 16b DDS. The synchronous oscillator locked-loop produces an eight-phase clock with coarse phase interpolation, while eight identical oscillators coupled with a DAC provide accurate phase adjustment. Spurious tone reduction obtained with the accurate phase interpolation is about 20dB.

BREAK 3:00 PM

23.4 A 610mW Zero-Overhead Class G Full-Rate ADSL Central-Office Line Driver

3:15 PM

K. Maclean, M. Corsi, R. Hester, J. Quarfoot, P. Melsa, R. Halbach, C. Kozak
Texas Instruments, Dallas, TX

A full-rate ADSL central-office line driver consumes 610mW through active termination and a zero-overhead class G technique. The supply switching scheme features very low overhead voltage, logic control, and controlled supply-rail ramp rate, and requires analog signal-peak prediction to be performed on the digital data stream.

23.5 A 700 mW CMOS Line Driver for ADSL Central Office Applications

3:45 PM

S-S. Lee[1], A. Bicakci[1], C-S. Kim[1], C. Conroy[2]
[1]LSI Logic, San Jose, CA
[2]Berkana Wireless, San Jose, CA

A CMOS line driver for ADSL central-office applications dissipates 700mW while delivering 20dBm power into 100Ω load. The measured linearity of the line driver is 72dB using a discrete multi-tone signal with 5.6 PAR and spanning an ADSL downstream band from 160kHz to 1.1MHz. Die size is 5.3mm^2 in a 0.25μm CMOS process.

23.6 A 700/900mW/Channel CMOS Dual Analog Front-End IC for VDSL with Integrated 11.5/14.5dBm Line Drivers

4:15 PM

M. Moyal, M. Groepl, H. Werker, G. Mitteregger, J. Schambacher
Xignal Technologies, Unteraching, Germany

A dual-channel analog front-end for ANSI/ETSI standards compliant VDSL in 0.25/0.5μm 1P 5M CMOS is presented. The chip includes a non-linearity cancelling multi-path line driver achieving -76dBc 3rd harmonic distortion at 12MHz, a 75mW continuous-time multi-bit 3rd-order self-calibrating ΣΔ ADC, a 14b current-steering DAC with PSD mask post filter, a 0-35dB variable-gain amplifier with adjustable hybrid, and a 12ps jitter LC PLL.

23.7 A 300mW Programmable QAM Transceiver for VDSL Applications

4:45 PM

H. Nam[1], T. Kim[1], C. Ryu[1], M. Kim[1], H. Kim[1], Y. Song[1], J. Shim[1], I. Hwang[1], C. Seo[1], Y. Kim[1], Y. Lee[1], B. Kim[2]
[1]KAIST, Daejeon, Republic of Korea
[2]Berkana Wireless, San Jose, CA

A complete VDSL QAM transceiver including ADC, DAC, clock generator, and micro-controller interface, fabricated in 0.18μm 1P 6M CMOS technology is described. A new IIR notch filter and dual loop AGC are incorporated in the design. Total power consumption is 300mW and the IC supports a 13Mb/s data rate over a 9000 ft distance with a BER <10^{-7}.

CONCLUSION 5:15 PM

CLOCK GENERATION

Chair: **Ken Yang,** *University of California, Los Angeles, CA*
Associate Chair: **Dennis Fischette,** *Advanced Micro Devices, Santa Clara, CA*

24.1 Cascaded PLL Design for a 90nm CMOS High-Performance Microprocessor

1:30 PM

K. Wong[1], E. Fayneh[2], E. Knoll[2], R. Law[1], C. Lim[1], R. Parker[1], F. Wang[1], C. Zhao[1]
[1]Intel, Hillsboro, OR
[2]Intel, Haifa, Israel

PLL clock generators are designed for a third-generation NetBurst™ processor implemented in a 90nm CMOS process. A cascade configuration offers improved jitter attenuation and facilitates a wide synthesis range. Parameter design takes into account a dual-sloped VCO control. A new charge pump topology offers superior symmetry.

24.2 Self-Biased, High-Bandwidth, Low-Jitter 1-to-4096 Multiplier Clock-Generator PLL

2:00 PM

J. Maneatis[1], J. Kim[1], I. McClatchie[1], J. Maxey[2], M. Shankaradas[2]
[1]True Circuits, Los Altos, CA
[2]Texas Instruments, Dallas, TX

A self-biased PLL uses a sampled feed-forward filter network and a multistage inverse-linear programmable current mirror for constant loop dynamics that scale with reference frequency and are independent of multiplication factor, output frequency, and PVT. The PLL achieves a multiplication range of 1 to 4096 with < 3.8% period jitter at 1.5V supply. Fabricated in 0.13µm CMOS, the area is 0.182mm^2 and the supply is 1.5V.

24.3 A Replica-Biased 50% Duty Cycle PLL Architecture with 1x VCO

2:30 PM

N. Kurd, J. Griffin, J. Barkatullah, I. Young
Intel, Hillsboro, OR

A replica-biased PLL providing wider-frequency-range lower-power consumption and improved clock jitter and loop stability, is fabricated in 0.13µm CMOS technology. A wide common-mode input range, matched-current amplifier provides a stable duty cycle at all operating conditions. Comparison of 1x and 2x VCO architectures 1x VCO shows improved core timing.

BREAK 3:00 PM

24.4 10 GHz Clock Distribution using Coupled Standing-wave Oscillators

3:15 PM

F. O'Mahony[1], P. Yue[2], M. Horowitz[1], S. Wong[1]
[1]Stanford University, Stanford, CA
[2]Atheros Communications, Sunnyvale, CA

A global clock network comprised of coupled, standing-wave oscillators is prototyped in a 0.18µm 6M CMOS process. The clock network operates from 9.8 to 10.5 GHz with 0.6ps skew and contributes only 0.5ps jitter when referencing a clock source with 1.4ps rms jitter.

24.5 A Low-Power Low-Jitter Adaptive-Bandwidth PLL and Clock Buffer

3:45 PM

M. Mansuri, C-K. Yang
University of California, Los Angeles, CA

This paper describes a fully-integrated low-jitter PLL and clock buffer for low-power digital systems with wide frequency range. To reduce supply-induced jitter, programmable passive circuits with opposite sensitivity compensate for the delay variations. Both circuits have supply sensitivity of < 0.1%/%ΔVDD. The design is fabricated in 0.25μm CMOS technology and consumes 10 mW from a 2.5V supply.

24.6 A Delay-line Based DCO for Multimedia Applications Using Digital Standard Cells Only

4:15 PM

E. Roth[1], M. Thalmann[2], N. Felber[1], W. Fichtner[1]
[1]Swiss Federal Institute of Technology, Zurich, Switzerland
[2]BridgeCo, Dubendorf, Switzerland

A digital clock synthesizer consisting of digital standard cells with 0.5ppm frequency resolution for multimedia applications is implemented in a 0.6μm CMOS process. The synthesizer produces an output frequency ranging from 11.1MHz to 12.5MHz with a 100MHz input clock. A DLL-based calibration mechanism tracks PTV variations during operation.

24.7 A Low-Jitter and Precise Multiphase Delay-Locked Loop Using Shifted Averaging VCDL

4:45 PM

H-H. Chang, C-H. Sun, S-I. Liu
National Taiwan University, Taipei, Taiwan, Republic of China

The DLL, in 0.35μm CMOS, uses the shifted averaging VCDL to reduce the mismatch-induced timing error among the delay stages without extra hardware. The DLL can generate precise multiphase outputs with improved duty cycle, reduced skew errors, and lowered jitter. Compared with a conventional DLL, this design improves the peak-to-peak jitter by a factor of 1.4 at 150MHz.

24.8 A 125MHz 8b Digital-to-Phase Converter

5:00 PM

J-M. Chou, Y-T. Hsieh, J-T. Wu
National Chiao-Tung University, Taiwan, Republic of China

A digital-to-phase converter (DPC) generates a 125 MHz clock with phase shift controlled by an 8b digital input. Averaging resistor rings are used for phase interpolation and phase error reduction by averaging. Implemented in a standard 0.35μm CMOS technology, the DPC achieves ±1LSB differential nonlinearity and ±2LSB integral nonlinearity. Power dissipation is 110mW with a 3.3V supply.

CONCLUSION 5:15 PM

RF INFOTAINMENT

Chair: **Bud Taddiken,** *Microtune, Plano, TX*
Associate Chair: **Tom Schiltz,** *Linear Technology, Colorado Springs, CO*

25.1 A SiGe Transmitter Chipset for CATV Video-on-Demand Systems

1:30 PM

K. Ashby, R. Greene, B. Nise, M. Womac, D. Stout, A. Taddiken
Microtune, Plano, TX

A 3-chip, 6.5W CATV transmitter for video-on-demand applications is implemented in a 0.5µm SiGe BiCMOS process. A 38dBmV IF input at 44MHz or 36.125MHz is upconverted to an output between 50 and 860MHz at a level adjustable between 41 and 58dBmV in <0.1dB steps. The 75Ω input return loss is <-25dB and the 75Ω output return loss is <-16dB. The wideband noise floor is <-80dBmV/Hz. Spurious signals in the CATV band are <-60dBc and phase noise is <-88dBc/Hz at 10kHz offset.

25.2 A CMOS Up-Conversion Receiver Front-End For Cable and Terrestrial DTV Applications

2:00 PM

G. Retz[1], P. Burton[2]
[1]University of Limerick, Limerick, Ireland
[2]PEI Technologies, Limerick, Ireland

A CMOS up-conversion receiver front end consists of a low-noise variable-gain amplifier with an input-frequency range from 48 to 860MHz and a mixer with an output frequency of 1.1GHz. The IC exhibits a gain range of 55dB, noise figure of 6.2dB at a gain of 19dB, and a maximum IIP3 of 26dBm. The chip consumes 125mW and is fabricated in a 0.18µm 5M process.

25.3 A 48-860MHz Digital Cable Tuner IC with Integrated RF and IF Selectivity

2:30 PM

J. van Sinderen[1], F. Seneschal[2], E. Stikvoort[1], F. Mounaim[2], M. Notten[1], H. Brekelmans[1], O. Crand[2], F. Singh[2], M. Bernard[2], V. Fillatre[2], A. Tombeur[1]
[1]Philips Research, Eindhoven, The Netherlands
[2]Philips Semiconductors, Caen, France

A single-chip digital cable tuner with an active splitter for cable data modems and set-top boxes is realized in a 0.5µm, 30GHz BiCMOS technology. The IC employs a single down-conversion, low-IF architecture and can receive signals in the 48-860MHz range. Fully integrated selectivity is obtained in combination with a channel decoder. Power consumption is 1.5W with a 3.3V supply.

BREAK 3:00 PM

25.4 A 9dBm IIP3 Direct-Conversion Satellite Broadband Tuner-Demodulator

3:15 PM

B-E. Kim[1], H-M. Yoon[1], Y-H. Cho[1], J-H. Lee[1], S-Y. Kim[1], T-J. Lee[1], J-K. Lim[1], M-S. Jeong[1], K. Kim[1], S-U. Kim[1], S-H. Park[1], B-K. Ko[1], S-H. Yoon[2], I. Jung[2], Y-U. Oh[2], Y-H. Kim[2]
[1]Integrant Technologies, Kyeongki-do, Republic of Korea
[2]PnpNetwork Technologies, Seoul, Republic of Korea

A direct-conversion satellite tuner-demodulator IC is realized using 0.18µm CMOS technology. The IC down-converts a 950-2150MHz satellite broadcasting signal to base band and demodulates the signal to an MPEG data stream. The IC conforms to both DVB-S and DSS standards. Experimental results show a 9dBm IIP3 while consuming 230mA from 1.8V supply.

25.5 A Digitally-Programmable Zero External Component FM Radio Receiver with 1μV Sensitivity

3:45 PM

H. van Rumpt[1], D. Kasperkovitz[1], J. van der Tang[2]
[1]Semiconductor Ideas to the Market, Breda, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

A digitally-programmable FM radio IC, implemented in an 11GHz f_T BiCMOS process, utilizes a low-IF architecture to eliminate all external components. The 11mm^2 die draws 17mA from 2.7 to 7.0V supply and exhibits an input sensitivity of 1μV.

25.6 A 1.9GHz Fully Integrated CMOS DECT Transceiver

4:15 PM

A. Leeuwenburgh, A. Hoogstraate, J. ter Laak, P. van Laarhoven, A. Mulders, M. Nijrolder, J. Prummel, P. Kamp
National Semiconductor, 's-Hertogenbosch, The Netherlands

A 2.5V DECT RF transceiver IC utilizes a low-IF receiver architecture with a 4th-order complex band-pass filter. The transmitter utilizes direct VCO modulation and a frequency doubler. The 9.4mm^2 die is implemented in a 0.25μm CMOS process. The receiver sensitivity is -94dBm, and supply current is 75mA. Transmitter output power is 0dBm with a supply current of 33mA.

25.7 A 2GHz 16dBm IIP3 Low Noise Amplifier in 0.25μm CMOS Technology

4:45 PM

Y-S. Youn[1], J-H. Chang[2], K-J. Koh[1], Y-J. Lee[3], H-K. Yu[1]
[1]Electronics and Telecommunications Research Institute, Daejeon, Republic of Korea
[2]KAIST, Daejeon, Republic of Korea
[3]Hynix Semiconductor, Cheongju, Republic of Korea

A 2GHz LNA implemented in a 0.25μm CMOS technology delivers 14dB gain, 2.8dB NF and 16dBm IIP3. High linearity is obtained by a third-harmonic cancellation technique using a stacked triode structure with differential signals. The method, based on DC non-linear characteristics, improves delay equalization from DC-2GHz with a 17% power increase, 0.8dB gain reduction, and <0.1dB NF increase.

25.8 60GHz and 76GHz Oscillators in 0.25μm SiGe:C BiCMOS

5:00 PM

W. Winkler[1], J. Borngraeber[1], B. Heinemann[1], P. Weger[2]
[1]IHP, Frankfurt, Germany
[2]Technical University of Cottbus, Cottbus, Germany

A 60GHz VCO and 76GHz oscillator with integrated resonators are fabricated in a 0.25μm SiGe: C BiCMOS technology. The circuits are suitable for millimeter wave systems including the 60GHz ISM band for broadband communication and the 76-77GHz region for automotive radar. Results derived from on-wafer measurements and mm-wave modules show wide tuning range and low phase noise.

CONCLUSION 5:15 PM

EMBEDDED MEMORY AND DIGITAL SYSTEMS

Chair: **Paul Landman,** *Texas Instruments, Dallas, TX*
Associate Chair: **Young-Hyun Jun,** *Samsung, Hwasung-City, Republic of Korea*

26.1 A 750MHz 144Mb Cache DRAM LSI with Speed Scalable Design and Programmable at-Speed Function-Array BIST

1:30 PM

H. Sakakibara[1], M. Nakayama[1], M. Kusunoki[1], K. Kurita[1], H. Otori[1], M. Hasegawa[1], S. Iwahashi[1], K. Higeta[1], T. Hanashima[2], H. Hayashi[2], K. Kuchimachi[3], K. Uehara[3], T. Nishiyama[3], M. Kume[3], K. Miyamoto[3], E. Kamada[3]
[1]Hitachi, Ome, Japan
[2]Hitachi ULSI Systems, Ome, Japan
[3]Hitachi, Hadano, Japan

A 750MHz 144Mb cache DRAM LSI incorporates speed-scalable embedded DRAM and SRAM macros, and is realized using a logic-merged DRAM process. The LSI has a built-in at-speed test engine with programmable test pattern and timing, merging logic and memory test. The die area is 285mm^2 in a 0.18μm 6M logic-merged DRAM process.

26.2 A 320ps Access, 3GHz Cycle, 144kb SRAM Macro in 90nm CMOS Technology Using an All-stage Reset Control Signal Generator.

2:00 PM

H. Akiyoshi, H. Shimizu, T. Matsumoto, K. Kobayashi, Y. Sanbonsugi
Fujitsu, Akiruno, Japan

A 320ps access, 3GHz cycle, 144kb SRAM macro was developed in 90nm CMOS technology. This macro adopts an all-reset control signal generator and hierarchical bit line. These techniques enable both the cycle and access speeds to be 1.7 times faster than those available with 130nm technology.

26.3 A 1.5V, 1.7ns 4kx32 SRAM with a Fully-Differential Auto-Power-Down Current Sense Amplifier

2:30 PM

B. Wicht[1], J-Y. Larguier[2], D. Schmitt-Landsiedel[1]
[1]Technical University Munich, Munich, Germany
[2]Infineon Technologies, Sophia Antipolis, France

A fully-differential current sense amplifier operates as low as 0.7V, automatically turns off after reading and features fast precharge. An implementation of a 1.5V 4kx32 dual-port SRAM macro in a 130nm CMOS process achieves an access time of 1.7ns.

BREAK 3:00 PM

26.4 A 500-MHz MP/DLL Clock Generator for a 5Gb/s Backplane Transceiver in 0.25μm CMOS

3:15 PM

G-Y. Wei[1], J. Stonick[2], D. Weinlader[2], J. Sonntag[2], S. Searles[2]
[1]Harvard University, Cambridge, MA
[2]Accelerant Networks, Beaverton, OR

Low-jitter clock generation is a critical component for enabling robust high-speed operation of 5Gb/s backplane transceivers. The implementation of a 500MHz clock synthesizer that operates either as a multiplying phase-locked loop (MPLL) or a multiplying delay-locked loop (MDLL) is described. The choice depends on the noise characteristics of the input clock source. This MP/DLL design is implemented in a 0.25μm CMOS process and operates with a 2.5V supply.

26.5 A Multi-Context 6.4Gb/s/Channel On-Chip Communication Network Using 0.18μm Flash-EEPROM Switches and Elastic Interconnects

3:45 PM

M. Borgatti, C. Auricchio, R. Pelliconi, R. Canegallo, C. Gazzina, A. Tosoni, P. Rolandi
STMicroelectronics, Agrate Brianza, Italy

A multi-context programmable on-chip communication network is implemented using a matrix of Flash-EEPROM pass-transistor switches (FPT) in a 0.18μm technology. The prototype 8-context, 8x8 64b crossbar includes 576k FPT and >8k bi-directional tristate repeaters in an area of 1.38mm^2. Based on 2x2 building blocks, wave pipelining and elastic interconnect, data is transferred at 6.4Gb/s per channel, with independent clocks at both ends.

26.6 An 800MHz Star-Connected On-Chip Network for Application to Systems on a Chip

4:15 PM

S-J. Lee, S-J. Song, K. Lee, J-H. Woo, S-E. Kim, B-G. Nam, H-J. Yoo
KAIST, Daejeon, Republic of Korea

A 10.8x6.0mm^2 prototype chip is implemented with a star-connected on-chip network. The chip consists of a PLL, 1kB SRAM, two 2x2 crossbar switches, Up/Down-Samplers, two off-chip gateways, and synchronizers. The on-chip network contains 81k transistors, dissipates 264mW at 2.3V and 800MHz, and provides 1.6GB/s per port and 12.8GB/s aggregated bandwidth, supporting plesiochronous communication without global synchronization.

26.7 A Variable-Kernel Flash-Convolution Image Filtering Processor

4:45 PM

K. Ito, M. Ogawa, T. Shibata
The University of Tokyo, Tokyo, Japan

A VLSI image filtering processor is designed for single-clock-cycle kernel convolution employing quaternary-tile pixel-data mapping and variable data masking techniques. The concept has been verified by a test chip fabricated in 0.18μm CMOS 5M technology. Without pipelining the IC operates at 50MHz with a 1.8V supply.

26.8 A 250MHz Direct Digital Frequency Synthesizer with ΣΔ Noise Shaping

5:00 PM

Y. Song[1], B. Kim[2]
[1]KAIST, Daejeon, Republic of Korea
[2]Berkana Wireless, San Jose, CA

A 14b direct digital frequency synthesizer in 0.25μm CMOS uses a 2b second-order ΣΔ modulator. The ΣΔ noise shaping significantly reduces spurs caused by phase truncation and the measured SFDR is >110dB. The prototype IC consumes 100mW with a 2.5V supply and works to 250MHz.

CONCLUSION 5:15 PM

SYSTEM-ON-A-CHIP DESIGN

This Short Course is intended to provide both entry-level and experienced engineers with practical design insight for first-pass success when designing integrated systems on a chip. Course completion provides an overall perspective on the system-design considerations and detailed circuit design strategies for key circuit building blocks. Topics covered which address the future of systems on a chip include an overview of technology scaling issues, design methodologies for fully-integrated systems, and analog and RF circuit design in primarily digital switching environments.

For Registration, please use the ISSCC 2003 Registration Form included in the ISSCC Advance Program centerfold. Sign-in is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00 AM, February 13.

The Short Course will be offered three times on Thursday, February 13, 2003.

The first session is scheduled for **8:00AM to 4:30PM.**
The second session is scheduled for **10:00AM to 6:30PM.**
The third session is scheduled for **1:30PM to 9:30PM.**

CD of the Short Course & Relevant Papers: Short-Course registrants will receive a CD-ROM at the Short Course. The CD-ROM includes: (1) The four Short-Course visuals in PDF format for printing of hard copies of the slides, (2) Bibliographies of relevant papers for all four presentations, and (3) PDF copies of relevant background material and important papers in the field (10 to 20 papers per presentation).

OUTLINE

FUTURE SYSTEM-ON-A-CHIP DESIGN ISSUES
(8:00AM-9:30AM), (10:00AM-11:30AM), (1:30PM-3:00PM)

This talk addresses the difficulty of scaling analog functions, power-limited processor performance, and the mapping of complex algorithms into logic. Because these must be simultaneously considered in each evermore-complex co-design task, new design methodologies are needed. Examples of what will be necessary for the future will be presented using wireless-system SoC's as the design example.

Instructor: Robert Broderson received his PhD from MIT and an honorary doctorate from the University of Lund, Sweden. He is the John Whinnery Professor in the Department of Electrical Engineering and Computer Science at the University of California, Berkeley. His research is focused in the areas of low-power design and wireless communications and the CAD tools necessary to support these activities. He has won numerous Best Paper awards and Technical-Achievement awards including the 1996 IEEE Solid-State Circuits Award, the 2000 Millennium Award from the Circuits and Systems Society, and the IEEE Golden Jubilee Award. He is a fellow of the IEEE and a member of the National Academy of Engineering.

MIXED-SIGNAL DESIGN AND SIMULATION
(10:00AM-11:30AM), (12:00PM-1:30PM), (3:30PM-5:00PM)

Developing mixed-signal systems-on-a-chip presents enormous challenges in the future. This talk presents many of the issues that act to complicate the development of large single-chip mixed-signal systems, and how they will be addressed, either through changes in the design methodology or through enhancements to the associated CAD systems.

Instructor: Kenneth S. Kundert is a fellow at Cadence Design Systems where he is the principle architect of the Spectre circuit-simulation family. He has led the development of Spectre, SpectreHDL, and SpectreRF, and he has also played a key role in the development of Cadence's AMS Designer and Agilent's harmonic-balance simulator, and made substantial contributions to both the Verilog-AMS and VHDL-AMS languages. He has authored two books on circuit simulation, received nine patents, and published over two-dozen papers in refereed conferences and journals.

CURRENT TRENDS IN ANALOG DESIGN FOR SoCs
(1:00PM-2:30PM), (3:00PM-4:30PM), (5:30PM-7:00PM)

This talk addresses the design of analog circuit blocks for systems-on-a-chip under the difficult constraints enforced at present, and the expected severe constraints in the future. Bandwidths and signal-to-noise ratios must be maintained in the face of decreasing power-supply voltages, tighter supply-current budgets, increasingly noisy substrate environments, and shrinking devices with poor intrinsic analog-processing capability.

Instructor: John W. Fattaruso received his Ph.D in Electrical Engineering from the University of California, Berkeley. Since 1987, he has been with various research and product-development departments of Texas Instruments, Dallas, TX, working on analog VLSI technology. He was elected Distinguished Member of Technical Staff in 2001. His research interests include analog and RF circuit design, circuit simulation and optimization, neural networks and numerical analysis. He currently holds 23 patents in circuit design, and has authored or co-authored 20 conference and journal papers.

HIGHLY-INTEGRATED RF TRANSCEIVERS
(3:00PM-4:30PM), (5:00PM-6:30PM), (8:00PM-9:30PM)

Without the ability to integrate a large system on a few chips, cellular phones and WLAN modems would have been unthinkable. After providing the background concerning the radio-network environment, receiver and transmitter architectures will then be discussed, in terms of their integration level and performance, as well as design considerations. Examples of highly integrated transceivers will be given, to highlight the architectural as well as circuit issues in practical design.

Instructor: Qiuting Huang received his Ph.D degree from Katholieke Universiteit Leuven in 1987. After five years as lecturer at the University of East Anglia, Norwich, UK, he joined the Integrated Systems Laboratory, of the Swiss Federal Institute of Technology, Zurich. His research interests are in the design of radio-frequency and baseband ICs for wireless communications. He was awarded the Transactions on Electronics Best Paper Award in 1997, and participated in the ISSCC Best Panel of _____. He is a Fellow of the IEEE.

W3: Microprocessor Design in the Power-Constrained Era

Organizer: **ISSCC Digital Committee**
Chair: **David Greenhill,** *Sun Microsystems, Sunnyvale, CA*
Committee:

Dennis Fischette, *Advanced Micro Devices, Santa Clara, CA*
David Greenhill, *Sun Microsystems, Sunnyvale, CA*
Georgios Konstadinidos, *Sun Microsystems, Sunnyvale, CA*
Samuel Naffziger, *Hewlett Packard, Fort Collins, CO*
Ron Preston, *Intel, Shrewsbury, MA*
Robert Rogenmoser, *Broadcom, Santa Clara, CA*
Norman Rohrer, *IBM Microelectronics, Essex Junction, VT*
Hector Sanchez, *Motorola, Austin, TX*
Simon Segars, *ARM, Cambridge, England*
Stefanos Sidiropoulos, *Aeluros, Mountain View, CA*
James Warnock, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
C.K. Ken Yang, *University of California, Los Angeles, CA*
Ian Young, *Intel, Hillsboro, OR*

This all-day workshop is dedicated to all aspects of power dissipation in leading-edge microprocessors.

The target participants are microprocessor designers who must design to power budgets that are becoming increasingly rigid. We will cover the reasons why power is becoming a significant constraint across the spectrum of microprocessor applications, from battery-powered portables through desk-top and server-class machines. Designers of other kinds of VLSI that have power issues may also find this workshop useful. The workshop will be at an advanced level aimed at experienced design engineers.

Sunit Tyagi will set the stage by discussing technology trends and the impact of technology on the power consumption of circuits. We will then move into an overview of architectural and microarchitectural modelling and tradeoffs. Architecture and modelling for both low-power designs and high-performance servers will be reviewed in talks by Simon Segars and Pradip Bose.

In the afternoon, circuit-design issues will be covered. First with James Warnock (IBM) will discuss approaches to designing with leaky transistors in low-Vdd processes and then Tadahiro Kuroda will discuss design with multiple power supplies.

Power delivery to the chip will be reviewed by Larry Smith and on-chip power distribution by Dave Ayers. Finally, Ken Goodson will help us extract the heat generated with techniques based on his leading-edge research on cooling technology.

Breakfast and Lunch will be included as part of the workshop to give participants a chance to mingle and discuss the isssues.

Workshop Program

Time	Topic
	Sunit Tyagi, *Intel*
	Pradip Bose, *IBM*
	Simon Segars, *ARM*
	James Warnock, *IBM*
	Tadahiro Kuroda, *Keio University*
	Dave Ayers, *Intel*
	Larry Smith, *Sun*
	Ken Goodson, *Stanford University, Stanford, CA*

W4: Gigahertz Radio Front Ends

Organizer: **Jan Sevenhans,** *Alcatel, Anterwer, Belgium*
Chair: **Michiel Steyaert,** *Katholieke Universiteit, Leuven, Belgium*
Committee:
Wanda Gass, *Texas Instruments, Dallas, TX*
Yoshiaki Hagiwara, *Sony, Tokyo, Japan*
Akira Kanuma, *Toshiba, Kawasaki, Japan*
Dave Robertson, *Analog Devices, Wilmington, MA*
Trudy Stetzler, *Texas Instruments, Stafford, TX*

Integrated semiconductor radios evolved over the last decade to the point where single-chip solutions are now available in Si bipolar, SiGe, CMOS and GaAs. At 900MHz and 1800MHz, zero-IF radios were integrated with apparent ease. DACs, ADCs, VCOs and active filters were soon added to the best of circuits that could be included in a single IC. As the market for small-size, low-power handsets increased, so, too, did the pressure to integrate the entire front end of gigahertz personal communications.

In this workshop, focus is both on circuit and system design considerations for integrated radios. The first pair of talks provide an overview of RF transceiver architecture and trends in cellular front ends. Three talks focus on circuit constraints in the design of DACs, ADCs and low-voltage RF circuits. System applications for low-rate WPANs, OFDM transceivers and constraints impressed in a fully integrated CMOS front end are treated in the three other presentations.

Workshop program:

Time	Topic
8:00	BREAKFAST
8:30	**Welcome** **Michiel Steyaert,** *Katholieke Universiteit, Leuven, Belgium*
8:40	**RF Transceiver Architectures** **Behzad Razavi,** *University of California, Los Angeles, CA*
9:25	**Trends in GHz Cellular Front Ends for the Next and the Previous Decade?** **Jozef Fenk,** *Infineon, Germany*
10:10	COFFEE BREAK
10:25	**Towards Full Integration of Low-Power CMOS RF-Frontends** **Wouter Decock,** *Katholieke Universiteit, Leuven, Belgium*
11:10	**Low-Voltage RF Circuits** **Tchamov Nikolay,** *Tampere University, Tampere, Finland*
11:55	**An Experimental 2.4GHz Low Power and Low-Cost CMOS Radio System for Low Rate WPAN application** **Kwyro Lee,** *KAIST, Republic of Korea*
12:40	LUNCH
1:40	**Challenges of Fully-Integrated OFDM Transceivers for 802.11 Wireless-LAN Systems.** **Mihai Banu,** *Agere, USA*
2:25	**ADCs and DACs march toward the antenna** **Richard Schreier,** *Analog Devices, USA*
3:10	**Harmonic Mixers for Direct-Conversion Receiver** **Hiroshi Tanimoto,** *Kitami Institute of Techn., Japan*
3:55	PANEL DISCUSSION
4:40	**Conclusion**

CONFERENCE REGISTRATION

This year ISSCC will again offer online registration. This is the fastest most-convenient way to register, and will give you immediate confirmation of whether or not you have a place in the Tutorial and Short-Course sessions of your choice, as well as space in any of the four Workshops offered. If you register online using a credit card, your registration is processed while you are online, and your written confirmation can be downloaded and printed for your record keeping. If you register by fax or mail, you will not receive confirmation for several days. **Registration forms received without full payment will not be processed until payment is received at Event Solutions.**

To register online, go to the ISSCC website at www.isscc.org **or go directly to the registration website at** www.yesevents.com/isscc/index.asp. All payments must be made in U.S. Dollars, by credit card or check. Checks are to be made payable to **"ISSCC 2003."** Payments by credit card will appear on your monthly statement as a charge from ISSCC.

For those who wish to register by fax or mail, the Advance Registration form can be found at the center of this booklet. Please read the explanations and instructions on the back of the form, carefully.

The deadline for receipt of Early Registration fees is **December 28, 2002. After December 28th, and on or before January 18, 2003,** registrations will be processed only at the Late-Registration rates. **As of January 19th, you must pay the onsite/highest registration fees.** Because of limited seating capacity in the meeting rooms, and hotel fire regulations, onsite registration may be limited. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2003.

Full conference registration includes one copy each of the Digest of Technical Papers, the Digital Archive DVD of the ISSCC, JSSC, VLSI Circuits, the Visuals Supplement (mailed in March) and the ISSCC 2003 CD (mailed in June). **Student registration does not include the Visuals Supplement or the ISSCC 2003 CD.** All students must present their student ID at the Conference Registration Desk to receive the student rate. Anyone registering at the IEEE Member rate must also provide his/her IEEE Membership number.

The Onsite and Advance-Registration Desks at ISSCC 2003 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except presenting authors, must pick up their registration materials at these desks as soon as they arrive at the hotel. **The Presenting Author for each paper must go directly to the Twin Peaks Room to register and to collect their materials.**

REGISTRATION HOURS:

Saturday, 2/8:	4:00 PM to 7:00 PM	**(Tutorial and Workshops Attendees Only)**
Sunday, 2/9:	6:30 AM to 1:30 PM	**(Tutorial and Workshops Attendees Only)**
	4:00 PM to 7:00 PM	
Monday, 2/10:	6:30 AM to 3:00 PM	
Tuesday, 2/11:	8:00 AM to 3:00 PM	
Wednesday, 2/12:	8:00 AM to 12:00 PM	
Thursday, 2/13:	7:00 AM to 1:00 PM	**(Short Course and Workshops Attendees Only)**

INFORMATION

NEXT ISSCC DATES AND LOCATION
ISSCC 2004 will be held February 8-12, 2004 at the San Francisco Marriott Hotel.

FURTHER INFORMATION
Please visit the ISSCC website at www.isscc.org.
To be placed on the Conference Mailing List, please contact the Conference Office, c/o Courtesy Associates, 2025 M Street, N.W., Suite 800, Washington, DC 20036
Email: isscc@courtesyassoc.com; Fax: 202-973-8722

HOTEL RESERVATIONS
This year, ISSCC participants can again make their hotel reservations online. To do this, go to the Conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott. The special ISSCC group rates are $191/single, $211/double. $231/triple $251/quad. The dates of your reservation must fall within the period of February 6 -14, 2003. All online reservations require the use of a credit card. Online reservations are confirmed immediately, while you are online. We suggest that you **print the page containing your confirmation number and reservation details, and bring it with you** when you travel to ISSCC. Once made and confirmed, your online reservation can be changed only by calling the Marriott at 1-800-228-9290 (toll free) or 415-896-1600, or by faxing your change to the Marriott at 415-442-0141.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet. In order to receive the special group rates, you will need to enter the following Group Codes: SSCSSCA for a single/double; SSCSSCB for a triple. SSCSSCC for a quad. **Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax.**

Reservations must be received at the San Francisco Marriott no later than January 10, 2003 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached and/or after January 10th, the group rate will no longer be available. After the 10th, reservation requests will be filled at the best available rate.

CONFERENCE PUBLICATIONS
Additional ISSCC publications can be purchased at the Conference Registration Desk. Prices are lower for purchases collected onsite than for those publications ordered after the Conference that must be shipped to the purchaser.

TECHNICAL-BOOK DISPLAY
A number of technical publishers will have a collection of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The book display is in the Golden Gate Hall, located one level above the ballroom and technical sessions. The Book Display will be open on Monday from 12:00 PM - 6:30 PM; on Tuesday from 9:30 AM to 5:30 PM; and on Wednesday from 9:30 AM to 1:00 PM.

ACCESSING IEEE TECHNICAL INFORMATION: THE IEEE-MEMBER DIGITAL LIBRARY

In 2003, the IEEE will introduce a new service that allows its members to access papers from IEEE journals, magazines, transactions and conference proceedings with one convenient subscription. Through the IEEE Member Digital Library, subscribers may access up to 25 articles a month from any of more than 120 journals and 300 conference proceedings published over the last five years. Covering a broad range of topics from all areas of electrical and electronic engineering and computer science, the IEEE-Member Digital Library also includes an online filing cabinet which allows subscribers to access the accumulated results of their research at any time.

Learn how the IEEE-Member Digital Library can help with the work you are doing today. Participate in a live session on February 11, 2003 at 7:30 AM in Salon 9, that will be simultaneously broadcast on the Web to a worldwide audience. Research librarian Rachel Berrington will show you how to make your research easier and more efficient.

For more information on the IEEE-Member Digital Library, visit www.ieee.org/ieeemdl

NOW, IEEE MEMBERSHIP DELIVERS MORE THAN EVER

The IEEE promotes the development of electro-technology and allied sciences and the application of these technologies for the benefit of humanity, the advancement of the profession, and the well-being of its members. Now, no matter where your career takes you, IEEE will follow with benefits that help to further both your personal and professional life. From the 37 societies dedicated to diverse aspects of electro-technology and the periodicals published in your specialty, to local chapter meetings and financial benefits available, the IEEE provides the resources you need to enhance your career. Join the more than 375,000 members who have taken advantage of the opportunities offered by IEEE.

Receive membership in the society of your choice when you join the IEEE at the 2003 ISSC Conference! Visit the IEEE exhibit in Golden Gate Hall.

As a member, you'll have the ability to search the abstracts of the almost 800,000 journal, magazine, letters, transactions articles and conference papers contained in IEEE *Xplore*™ at www.ieee.org/ieeexplore.

INFORMATION FOR SOLID-STATE CIRCUITS DESIGNERS: ON DVD AND ONLINE

The Solid-State Circuits Digital Archive 2002 on DVD is provided for all ISSCC 2003 registrants. Claim it during your attendance at the Conference in the registration area. A coupon in each registration packet is needed to redeem your DVD. ***Don't forget!***

To order an additional copy after the Conference, access sscs.org/archive.

The 2002 Archive DVD includes the complete collection of all articles of

- the JSSC since its first issue in 1966
- the ISSCC Digests and Slide/Visuals Supplements since their inception
- Digests of the Symposium on VLSI Circuits.

Members of the IEEE Solid-State Circuits Society have access to the JSSC articles online through IEEE *Xplore*. Online access to the collection of ISSCC Digests and the proceedings of the Symposium on VLSI Circuits, along with Custom Integrated Circuits Conference is also available to members who subscribe to the *SSCS Digital Library*.

COMMITTEES

EXECUTIVE COMMITTEE

Chair: **Timothy Tredwell,** *Eastman Kodak Research Labs, Rochester, NY*
Executive Dir.: **Dave Pricer,** *Charlotte, VT*
Exectuive Sec.: **Frank Hewlett, Jr.,** *Sandia National Labs, Albuquerque, NM*
Director of Finance: **John Kennedy,** *Howard Hughes Medical Institute, Palo Alto, CA*
Program Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
Prog. Vice Chair: **Akira Kanuma,** *Toshiba, Semiconductor, Kawasaki, Japan*
Program Sec.: **Jan van der Spiegel,** *University of Pennsylvania, Philadelphia, PA*
Far East Chair: **Yoshiaki Hagiwara,** *Sony, Tokyo, Japan*
Far East Sec.: **Masayuki Katakura,** *Sony, Kanagawa, Japan*
Far East Asst. Sec.: **Takao Yamazaki,** *Sony, San Jose, CA*
European Chair: **Jan Sevenhans,** *Alcatel Bell, Antwerp, Belgium*
European Vice Chair: **Albert Theuwissen,** *DALSA, Eindhoven, The Netherlands*
European Sec.: **Rudolf Koch,** *Infineon Technologies Wireless Products, Munich, Germany*
Short Course: **Terri Fiez,** *Oregon State University, Corvallis, OR*
Tutorials: **Willy Sansen,** *Katholieke Universiteit, Leuven, Belgium*
Dir. of Publications/Presentations:
Laura Fujino, *University of Toronto, Toronto, Canada*
Press/Awards: **Kenneth C. Smith,** *University of Toronto, Toronto, Canada*
Dir. of Operations: **Diane Suiters,** *Courtesy Associates, Washington, D.C.*
Digest Editors: **Arvin Grabel,** *Northeastern University Boston, MA*
Richard Jaeger, *Alabama Microelectronics Center, Auburn University, AL*
TD Subcommittee Chair:
William Bowhill, *Intel, Shrewsbury, MA*
TD Steering Committee:
Tak Baba, *Panasonic, Cupertino, CA*
50th Anniversary Chair/Audio-Visual Coordinator
John Trnka, *IBM, Rochester, MN*

Liaison Members of Representatives:

Europe: **Jan van der Spiegel,** *Univeristy of Pennsylvania, Philadelphia, PA*
IEEE SSC Society: **Bryan Ackland,** *Agere Systems, Holmdel, NJ*
IEEE SSC Society: **Gary Baldwin,** *University of California, Berkeley, CA*
IEEE Bay Area Council: **Robert P. Tu**
IEEE San Francisco Section: **James B. Lekas**

US PROGRAM COMMITTEE

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
Vice Chair: **Akira Kanuma,** *Toshiba, Semiconductor, Kawasaki, Japan*
Secretary: **Jan van der Spiegel,** *University of Pennsylvania, Philadelphia, PA*

COMMITTEES

Analog:

David Robertson (Chair), *Analog Devices, Wilmington, MA*
David Allstot, *University of Washington, Seattle, WA*
Brian Brandt, *Maxim Integrated Products, North Chelmsford, MA*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Venu Gopinathan, *Broadcom, Irvine, CA*
David Johns, *University of Toronto, Toronto, Canada*
Roy Scott Kaller, *Standard Microsystems, Phoenix, AZ*
Akira Matsuzawa, *Matsushita Electric, Moriguchi, Japan*
Krishnaswamy Nagaraj, *Texas Instruments, Warren, NJ*
Bram Nauta, *University of Twente, Enschede, The Netherlands*
Ken Poulton, *Agilent Laboratories, Palo Alto, CA*
*__Bill Redman-White,__ *Philips Semiconductors, San Jose, CA*
Michiel Steyaert, *Katholieke Universiteit Leuven, Heverlee, Belgium*
Axel Thomsen, *Silicon Laboratories, Austin, TX*

Digital:

Ian Young (Chair), *Intel, Hillsboro, OR*
*__Krste Asanovic,__ *Massachusetts Institute of Techology, Cambridge, MA*
Dennis Fischette, *Advances Micros Devices, Santa Clara, CA*
David Greenhill, *Sun Microsystems, Sunnyvale, CA*
Georgios Konstadinidos, *Sun Microsystems, Sunnyvale, CA*
Paul Landman, *Texas Instruments, Dallas, TX*
Masayuki Mizuno, *NEC Corporation, Sagamihara, Japan*
Shannon Morton, *SGI, Boston, MA*
Samuel Naffziger, *Hewlett Packard, Fort Collins, CO*
Ron Preston, *Intel Corporation, Shrewsbury, MA*
Robert Rogenmoser, *Broadcom, Santa Clara, CA*
Norman Rohrer, *IBM Microelectronics, Essex Junction, VT*
Hector Sanchez, *Motorola, Austin, TX*
Simon Segars, *ARM, Cambridge, England*
Stefanos Sidiropoulos, *Aeluros, Mountain View, CA*
Werner Simbuerger, *Infineon Technologies, Corporate Research, Munich, Germany*
James Warnock, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
C.K. Ken Yang, *University of California, Dept. of Elec. Eng., Los Angeles, CA*
Hoi-Jun Yoo, *KAIST, Yuseong, Republic of Korea*

Imagers, Displays, and MEMS

H.S. Philip Wong (Chair), *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
Akintunde Akinwande, *Massachusetts Institute of Technology, Cambridge, MA*
Bill Bidermann, *PIXIM, Mountain View, CA*
Abbas El Gamal, *Stanford University, Stanford, CA*
Ralph Etienne-Cummings, *University of Maryland, College Park, MD*
Yoshiaki Hagiwara, *Sony, Tokyo, Japan*
Jed Hurwitz, *STMicroelectronics, Edinburgh, Scotland*
Daniel McGrath, *Imaging Devices, Burlington, MA*
*__Khalil Najafi,__ *University of Michigan, Ann Arbor, MI*
Dennis Polla, *SurroMed, Singapore*
Charles Stancampiano, *Eastman Kodak, Rochester, NY*
Albert Theuwissen, *DALSA, Eindhoven, The Netherlands*
Ming C. Wu, *University of California, Los Angeles, CA*
Woodward Yang, *Harvard University, Cambridge, MA*
Euisik Yoon, *KAIST, Daejeon, Korea*

Memory:

Jagdish Pathak (Chair), *Sub Micron Circuits, San Jose, CA*
John Barth, *IBM, Essex Junction, VT*
Mark Bauer, *Intel, Folsom, CA*
Martin Brox, *Infineon Technologies, Munchen, Germany*
Jinyong Chung, *Hynix Semiconductor, Ichon, Korea*
Young-Hyun Jun, *Samsung Electronics, Hwasung, Korea*
*__Takayuki Kawahara,__ *Hitachi, Central Lab, Kokubunji, Japan*
Sreedhar Natarajan, *ATMOS, Kanata, Canada*
Isao Nojima, *Silicon Storage Technology, Sunnyvale, CA*
*__Yukihito Oowaki,__ *Toshiba,Yokohama, Japan*
Frankie Roohparvar, *Micron Technology, San Jose, CA*
Katsuyuki Sato, *Elpida Memory, Technical Marketing Division, Sagamihara, Japan*
*__Ali Sheikholeslami,__ *University of Toronto, Toronto, Canada*
Alex Shubat, *Virage Logic, Fremont, CA*
Don Weiss, *Hewlett-Packard, Fort Collins, CO*
Ban-Pak Wong, *Sun Microsystems, Santa Clara, CA*

Signal Processing:

Wanda Gass (Chair), *Texas Instruments, Dallas, TX*
Jack Berg, *Cypress Semiconductor, San Jose, CA*
Giorgio Maurizio Betti, *STMicroelectronics, Cornaredo, Italy*
Stephen Fischer, *Intel, Folsom, CA*
Jim Goodman, *Engim, Ottawa, Canada*
Hideto Hidaka, *Mitsubishi Electric, Itami-shi, Japan*
*__Stephen Kosonocky,__ *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
Steve Molloy, *Netergy Microelectronics, Santa Clara, CA*
Steve Morein, *ATI Research, Marlborough, MA*
David Shoemaker, *Engim, Acton, MA*
Bernard Shung, *Broadcom, San Jose, CA*
Lars Thon, *Aeluros, Mountain View, CA*
Albert Van der Werf, *Philips Research Laboratories, Eindhoven, The Netherlands*
Joseph Williams, *Agere Systems, Holmdel, NJ*
Thucydides Xanthopoulos, *Cavium Networks, Marlboro, MA*

Technology Directions Steering Committee:

William Bowhill (Chair), *Intel, Shrewsbury, MA*
Tak Baba, *Panasonic Technology, Cupertino, CA*
Jan van der Spiegel, *University of Pennsylvania, Philadlephia, PA*

Wireless & RF Communications:

Trudy Stetzler (Chair), *Texas Instruments, Stafford, TX*
Arya Behzad, *Broadcom, San Diego, CA*
William Camp, *Sony Ericsson Mobile Communications, Research Triangle Park, NC*
Charles Chien, *G-Plus, Santa Monica, CA*
Ken Cioffi, *Independent Consultant, Cupertino, CA*
Paul Davis, *Consultant, Reading, PA*
Qiuting Huang, *Swiss Federal Institute of Technology, Zurich, Switzerland*
Tetsuro Itakura, *Toshiba, Kawasaki, Japan*
Rudolf Koch, *Infineon Technologies, Munich, Germany*
Thomas Lee, *Stanford University, Stanford, CA*
*__John Long,__ *Delft University of Technology, Delft, The Netherlands*
Tony Montalvo, *Analog Devices, Raleigh, NC*
MaryJo Nettles, *Mobilian, San Diego, CA*
David Ngo, *Micro Devices, Chandler, AZ*
Ernesto Perea, *STMicroelectronics, Grenoble Cedex, France*
Tom Schiltz, *Linear Technology, Colorado Springs, CO*
Bud Taddiken, *Microtune, Plano, TX*

Wireline Communications:

Russell Apfel (Chair), *Legerity, Austin, TX*
Cormac Conroy, *Berkana Wireless, San Jose, CA*
Larry Devito, *Analog Devices, Wilmington, MA*
Franz Dielacher, *Infineon Tech., Villach, Austria*
Yuriy Greshishchev, *PMC - Sierra, Kanata, Canada*
John Khoury, *Multilink Technology, Somerset, NJ*
Roger Minear, *Agere Systems, Reading, PA*
Jan Sevenhans, *Alcatel Bell, Antwerp, Belgium*
Mehmet Soyuer, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
Hirotaka Tamura, *Fujitsu Laboratories, Kawasaki, Japan*
*__Loke Tan,__ *Broadcom, Irvine, CA*
Rick Walker, *Agilent Technologies, Palo Alto, CA*

EUROPEAN PROGRAM COMMITTEE

Chair:	**Jan Sevenhans,** *Alcatel Bell, Antwerpen, Belgium*
Vice-Chair:	**Albert Theuwissen,** *DALSA BV, Eindhoven, The Netherlands*
Secretary:	**Rudolf Koch,** *Infineon Technologies Munich, Germany*

Members:

Giorgio Maurizio Betti, *STMicroelectronics, Cornaredo, Italy*
Martin Brox, *Infineon Technologies, Munchen, Germany*
Klaas Bult, *Broadcom Netherlands, Bunnik, The Netherlands*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Jose Epifanio da Franca, *Chipldea Microelectronica SA, Porto Salvo, Portugal*
Franz Dielacher, *Infineon Technologies, Villach, Austria*
Pietro Erratico, *STMicroelectronics, Cornaredo, Italy*
Michel Harrand, *STMicroelectronics, Crolles Cedex, France*
Qiuting Huang, *Swiss Federal Institute of Technology, Zurich, Switzerland*
Jed Hurwitz, *STMicroelectronics, Edinburgh, Scotland*
John Long, *Delft University of Technology, Delft, The Netherlands*
Bram Nauta, *University of Twente, Enschede, The Netherlands*
Olivier Nys, *Xemics, Neuchatel, Switzerland*
Frank Op't Eynde, *IMEC, Haverlee, Belgium*
*__Ernesto Perea,__ *STMicroelectronics, Grenoble Cedex, France*
Christian Piguet, *CSEM, Neuchatel, Switzerland*
Wolfgang Pribyl, *Austria Mikro Systems, Unterpremstatten, Austria*
*__Bill Redman-White,__ *Philips Semiconductors, San Jose, CA*
*__Raf Roovers,__ *Philips Research, Eindhoven, The Netherlands*
Willy Sansen, *Katholieke Universiteit, Leuven, Belgium*
Simon Segars, *ARM, Cambridge, England*
Patrice Senn, *France Telecom R&D, Meylan Cedex, France*
Werner Simbuerger, *Infineon Technologies, Munich, Germany*
Michiel Steyaert, *Katholieke Universiteit, Heverlee, Belgium*
Christer Svensson, *Linkoping University, Linkoping, Sweden*
Hannu Tenhunen, *Kungl Tekniska Hogskaolan, Kista, Sweden*
Rudy van de Plassche, *Broadcom Netherlands, Bunnik, The Netherlands*
Jan van der Spiegel, *University of Pennsylvania, Philadelphia, PA*
Albert van der Werf, *Philips Research, Eindhoven, The Netherlands*
*__Werner Weber,__ *Infineon Technologies, Munich, Germany*

FAR EAST PROGRAM COMMITTEE

Chair: **Yoshiaki Hagiwara,** *Sony, Tokyo, Japan*
Secretary: **Masayuki Katakura,** *Sony, Kanagawa, Japan*
Asst. Sec.: **Takao Yamazaki,** *Sony Electronics, San Jose, CA*

Members:

Kunihiro Asada, *University of Tokyo, Tokyo, Japan*
Tak Baba, *Panasonic Technology, Cupertino, CA*
Jinyong Chung, *Hynix Semiconductor, Inchon, Korea*
Hiroyuki Fujita, *CIRMM, University of Tokyo, Meguro, Japan*
Takahiro Hanyu, *Tohoku University, Sendai, Japan*
Hideto Hidaka, *Mitsubishi Electric, Itami, Japan*
Kunihiko Iizuka, *Sharp, Tenri, Japan*
Takeshi Imamura, *Fujitsu Labs., Kawasaki, Japan*
Tetsuro Itakura, *Toshiba Corporation, Kawasaki-shi, Japan*
Marwan Jabri, *Oregon Health and Science University, Beaverton, OR*
Seh-Woong Jeong, *Samsung Electronics, Suwon, Korea*
Young-Hyun Jun, *Samsung Electronics, Hwasung, Korea*
Tae-Sung Jung, *Samsung Electronics, Yongin, Korea*
Yuichi Kado, *NTT Telecommunications Energy Labs, Atsugi, Japan*
Akira Kanuma, *Toshiba Corporation, Kawasaki, Japan*
***Takayuki Kawahara,** *Hitachi, Ltd., Kokubunji-shi, Japan*
Ban Won Lee, *@Lab Inc., Yongin City, Korea*
Nicky C.C. Lu, *Ltron Technology, Inc., Hsinchu, Taiwan*
Akira Matsuzawa, *Matsushita Electric, Moriguchi, Japan*
Masayuki Mizuno, *NEC, Sagamihara, Japan*
Tadashi Nakagawa, *National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan*
Koichi Ono, *Sony Corporation, Atsugi, Japan*
***Yukihito Oowaki,** *Toshiba, Yokohama, Japan*
***Takayasu Sakurai,** *University of Tokyo, Meguro, Japan*
Katsuyuki Sato, *Elpida Memory, Sagamihara, Japan*
Hirotaka Tamura, *Fujitsu Labs., Kawasaki, Japan*
Satoru Tanoi, *Oki Electric Industry, Hachioji, Japan*
Yang Yuan Wang, *Peking University, Beijing, China*
Hiroyuki Yamauchi, *Matsushita Electric Industrial, Nagaokakyo, Japan*
Hoi-Jun Yoo, *KAIST, Yusong, Korea*
Euisik Yoon, *KAIST, Daejeon, Korea*

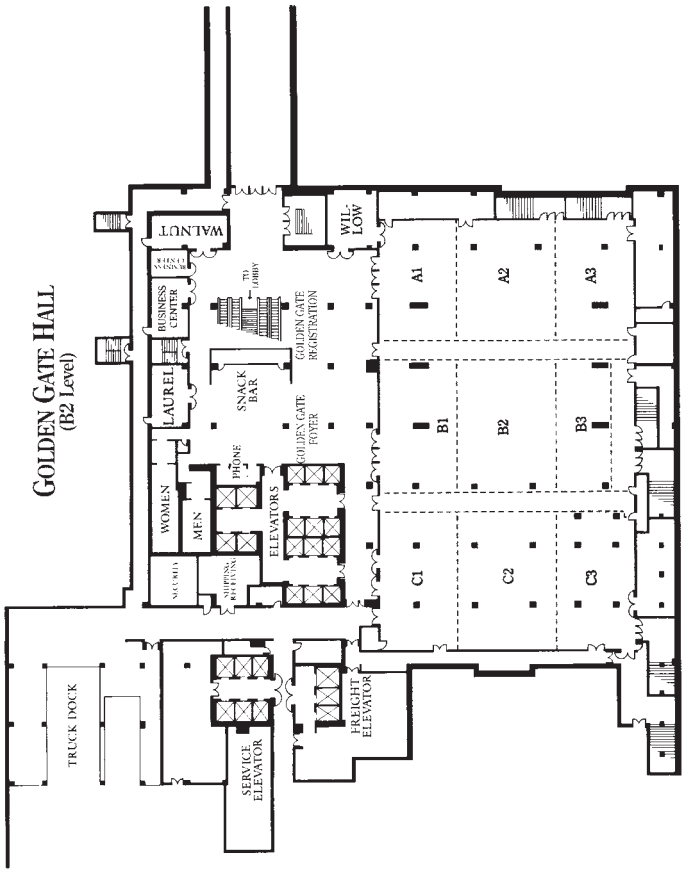
Far East Liaison Members:

Katsutoshi Akagi, *NEC Electronics, Santa Clara, CA*
Motosuga Hamada, *Toshiba, Kawasaki, Japan*
Junji Ogawa, *Sunnyvale, CA*
Hiroyuki Sakai, *Panasonic Industrial, Elgin, IL*
Takuma Tanimot, *Hitachi Semiconductor, San Jose, CA*
Michihiro Yamada, *Mitsubishi Electric and Electronics USA, Sunnyvale, CA*

* Committee Representative on Technology Directions Subcommittee.

CONFERENCE SPACE LAYOUT

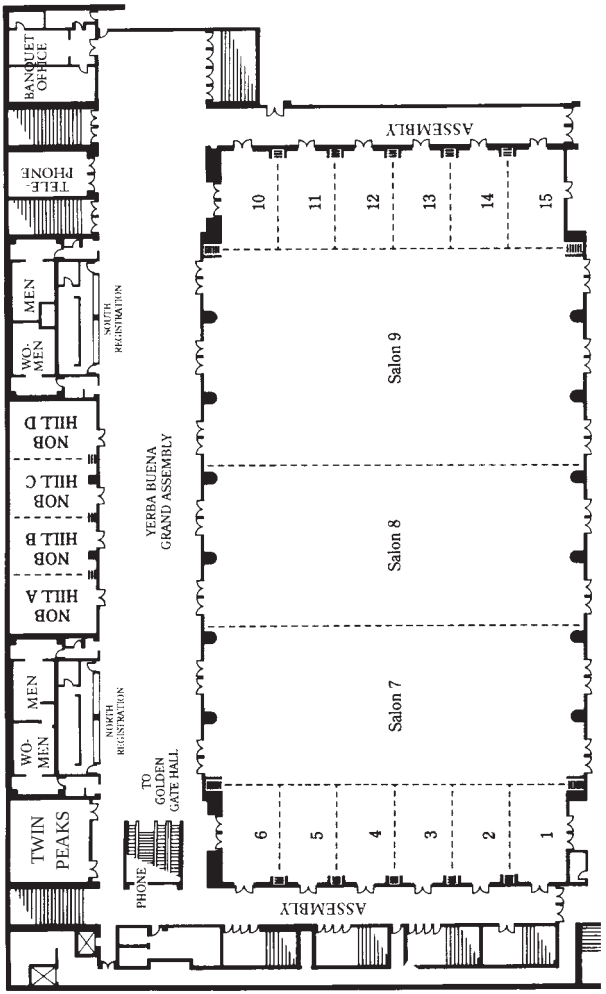
The Conference Book Display and Social Hour will be held in Golden Gate Hall. The layout appears below:



CONFERENCE SPACE LAYOUT

All Conference Technical Paper Sessions are in the Yerba Buena Ballroom at the San Francisco Marriott Hotel. The layout appears below:

YERBA BUENA BALLROOM
(Lower B2 Level)



To celebrate the 50th-anniversary of the International Solid-State Circuits Conference, a number of special program events have been planned:

The ISSCC Digest of Technical Papers will contain a special historical section. This section will include overviews of key ISSCC papers over the past 50 years arranged by subject. Topics of these special articles include Digital, Memory, Signal Processing, Analog, Communications/microwave, Sensors & MEMS, and Imagers. Also included are historical overviews of the formation and history of the Conference, and a listing of the Chairs of the US, Far East, and European committees from the early history to the present.

An Author Honor Roll is included to identify and recognize those authors who have provided at least 10 regular contributions to the ISSCC Digest of Technical Papers. The top author in this listing has co-authored over 40 papers to date at ISSCC!

A History-of-ISSCC Museum will be open for viewing Sunday through Wednesday afternoon in Golden Gate A1. This museum will contain historical memorabilia and photographs from the archives of the Conference. Key papers and die photos will be displayed in their topic areas of Digital, Memory, Signal Processing, Analog, Communications/microwave, Sensors & MEMS, and Imagers. Viewing times will be from 7:30 AM until 10 PM daily, except Wednesday when closing will be 5 PM.

In addition, a short living-history video containing interviews with five ISSCC pioneers will be available for viewing in the Willow Room, next to Golden Gate A1. The pioneers are Arthur Stern of General Electric, John Linvill of Bell Laboratories, Jerry Seran also of General Electric, Merlin Corrington of RCA, and Richard Baker from MIT Lincoln Labs. All of these pioneers were involved in the initial formation of ISSCC. The interviews answer the questions concerning what led to the formation of the early meetings, and the involvement of the University of Pennsylvania in this early success. As well, a full-length version of this video will be available for your personal viewing in your hotel room on one of the Marriott Hotel TV channels.

Finally, there will be some Anniversary-related events during the Monday morning Plenary session, and a special anniversary cake served during the Monday-evening Social Hour.

back cover