IEEE SOLID-STATE CIRCUITS SOCIETY/IEEE SAN FRANCISCO SECTION, BAY AREA COUNCIL/UNIV. OF PA.

ADVANCE PROGRAM

2004 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 15, 16, 17, 18, 19

CONFERENCE THEME:
EMBEDDED-SYSTEMS FOR A CONNECTED WORLD

SAN FRANCISCO MARRIOTT HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY: 2 Forums: GHz Radio; NV Memory; 7 TUTORIALS
3 SPECIAL-TOPIC SESSIONS: UWB Radio; BIO CMOS; Highlights of DAC

THURSDAY ALL-DAY: 2 Forums: Analog Telecom; Microprocessor Circuits; Short Course: Deep-Submicron Analog & RF

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE HIGHLIGHTS

On Sunday, February 15, ISSCC 2004 offers:

- A choice of up to 3 of a total of 7 Tutorials
- Two ISSCC Advanced Circuit Forums:
- GIRAFE Forum (Gigahertz Radio Front Ends): "RF Power Amplifiers"
- Memory Design Forum: "Non-Volatile Memories—Technology and Design"

The 90-minute tutorials offer background information and a review of the current state-of-the-art in specific circuit design topics. In the all-day Advanced Circuits Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, three Special-Topic Evening Sessions addressing next-generation circuit-design challenges will be offered starting at 7:30PM:

- Communications Architectures and System Design of Ultra Wideband Radio
- CMOS Meets BIO
- Highlights from DAC
- The Special-Topic Evening Sessions are open to all ISSCC attendees.

On Monday, February 16, ISSCC 2004 offers three plenary papers followed by five parallel technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will feature posters from the winners and the runners-up of the joint DAC – ISSCC student design contest. Evening panels will be held on Monday and Tuesday evenings from 8:00PM to 10:00PM.

On Thursday, February 19, ISSCC 2004 offers a choice of three events:

- ISSCC Short Course: Deep Sub-micron Analog and RF Circuit Design. Two sessions of the Short Course will be offered, with staggered starting times.
- ISSCC Advanced Circuit Forum on Analog Telecom ASIC and Circuit Concepts (ATACC): A/D and D/A Building Blocks for Telecom Transceiver Applications.
- ISSCC Advanced Circuit Forum on Microprocessor Design: Managing Variability in sub-100nm Designs.

Registration is limited for the Sunday and Thursday events. Registration will be filled on a first-come, first-served basis. Use of the ISSCC registration website (www.isscc.org) is strongly encouraged. You will be provided with immediate confirmation on registration for tutorials, Advanced Circuits Forums and the Short Course.

CONTENTS

T1: Tuning of Analog Parameters

Variability of basic parameters like transconductances, time-constants and gains due to process, voltage and temperature variations, can have first-order effect in the performance and manufacturability of most analog circuits. This tutorial focuses on negative feedback circuits that can be implemented on-chip to combat these variations. A discussion of pros and cons of various circuits that tune time-constants (for continuous-time filters), gm's of transistors, quality-factors of resonators etc will be discussed.

Instructor: Venu Gopinathan obtained his B.Tech in Electronics from IIT Chennai, India in 1986 and MS and PhD from Columbia University in 1987 and 1990 respectively. He then worked at Texas Instruments and Bell Labs, Lucent technologies. He is presently at Broadcom Corporation, Irvine CA.

T2: Wireless-LAN Radio Design

As one of the few rising stars of the semiconductor industry, WLAN design is engaging more and more engineers and companies. Essential to the overall system design, is the radio design. This tutorial will introduce the various flavors of the 802.11 WLAN PHY standards (a/b/g), and describe their specifications and its impact on the radio design. The possible choices for the radio architecture (direct-conversion, low-IF, super-heterodyne) will be examined and their impact on the transistor-level design will be studied. The impact of the radio architecture on die size, system cost, and power consumption will be evaluated. The effect of certain analog/RF impairments on the overall system performance will be described. The impact of the choice of process technology on the radio architecture will also be discussed. Some analog/digital/mixed-mode calibration techniques for improving system performance and chip yield will also be discussed. Finally, a specific case-study will be examined in some detail.

Instructor: Arya Behzad is currently Senior Manager of Engineering working on radios for future generation wireless systems at Broadcom. He worked at United Technology from 1991-1992 as a Special-Project Engineer. In 1994 he obtained his M.S.E.E. from UC Berkeley after completing his thesis on the Infopad project. He worked at MicroUnity Systems Engineering from 1994-1996 as a Senior Analog and System Engineer implementing RF and analog front-ends for set-top boxes and cable modems. From 1996-1998 he worked at Maxim Integrated Products implementing high-precision analog components, infra-red receivers, and cellular phone ICs. Since 1998, he has been with Broadcom Corporation working on integrated tuners, gigabit Ethernet and wireless LAN systems and ICs. He has over 20 patents issued and pending, as well as several publications in the areas of precision analog circuits, cellular transceivers, integrated tuners, gigabit Ethernet, and wireless LANs. Mr. Behzad is a member of the ISSCC Wireless Technical Program Committee and a Senior Member of the IEEE.

T3: Electronic Circuits in an Automotive Environment

Many automotive-electronic circuits are mixed-signal systems, and are subject to the design difficulties of such chips including analog/digital interference, power/accuracy interference. An extra design difficulty for automotive chips is due to the electronics-hostile environment in a car. This tutorial explores these specific automotive requirements, and their impact on circuit design. Topics, to be discussed are: limitations of a car-battery as supply, high operational temperature, automotive high-energy interferences (Load dump, Schaffner pulses), system ESD, low susceptibility for large EM fields and low EM radiation, high reliability and safety (DFMEA). Several practical design examples will be given for these topics.

Instructor: Herman Casier received his MS in electronics from the Katholieke Universiteit Leuven in 1970. As assistant at the university, he worked on bipolar technology, device modeling, and mixed signal design in bipolar and MOS technologies. From 1977 to 1980, he was with BARCO N.V. as senior designer, and later became responsible for new technologies. In 1980, he was one of the founders of the designhouse INCIR in Belgium. From 1983 to 2002, he was with Alcatel Microelectronics, where he first held several design and R&D management positions, and later became engineering officer. Since 2002, he is an engineering fellow at AMI Semiconductor, Belgium.

T4: Introduction to PLL and DLL Design for Digital Systems

Used to generate clocks in most VLSI designs, the phase-locked loop (PLL), is often a feared and misunderstood beast. Black-box designs from IP vendors are integrated on-chip with little understanding of the PLL's sensitivities to process peculiarities and digital noise. Inexperienced designers read the latest literature and try to hit a "home run" with their first PLL. Ignorance of the PLL's internal workings may lead to impossible-to-meet specs and inadequate test features. This tutorial provides a practical introduction to basic PLL design for clock generation, including feedback stability, common circuit implementations, spec writing, and design for test. Examples of PLL "gotchas" and real-world failures are presented.

Instructor: Dennis Fischette is a Senior Member of the Technical Staff at Advanced Micro Devices (AMD) in Sunnyvale, CA. In 1986, he graduated from Cornell University, Ithaca, NY, with a Physics BSc, and briefly studied History of Science at the University of California, Berkeley. From 1988 to 1991, he worked for Integrated CMOS Systems (Sunnyvale) on device and circuit modeling. From 1991 to 1996, he worked for Hal Computer Systems (Campbell,CA) on clock synthesizers and circuit design automation. Before joining AMD, he worked for Chromatic Research (Sunnyvale) on clock synthesizers, D/A circuits, and memories. His technical interests include PLL and DLL design, clock-and-data recovery, circuit-analysis software, and high-speed I/O circuits. He has been a member of the ISSCC Digital Program Sub-Committee since 2001.

T5: Noise in Solid-State Imagers : Basics and Specsmanship

If the data-sheets of image sensors are studied, a lot of confusion can be seen. For example, the same noise specification can have a completely different meaning depending on the vendor, and on the technology used. Where does this misunderstanding and inconsistency arise? This tutorial will deal with the various noise sources that are present in a solid-state image sensor (CCD and CMOS) and their theoretical origins. Then, the traps in specifying various sensor characteristics involving one or another noise source (noise level, signal-to-noise ratio, dynamic range) will be discussed. To demonstrate the inconsistency in commercial specification, a data-sheet taken from the Internet will be analyzed.

Instructor: Albert J.P. Theuwissen (IEEE Fellow) has been involved in solid-state imaging since 1976. After his M.Sc. and Ph.D. studies at the Katholieke Universiteit Leuven (Belgium), he joined Philips Research in Eindhoven (Netherlands). Since 2002 he is the CTO of DALSA Inc. He has (co-)authored many technical papers in the solid-state imaging field and has been issued several patents. He was co-editor of the special issues of the IEEE Transactions on Electron Devices on image sensors('91, '97, '03), and served as general chair of the IEEE International Workshop on CCDs & AIS ('97, '03). He founded The Walter Kosonocky Award, which highlights the best paper in the field of solid-state image sensors. In 1995, he authored a textbook "Solid-State Imaging with Charge-Coupled Devices". In 1998 he became an IEEE distinguished lecturer, and in 2001 he joined the Delft University of Technology, the Netherlands, as a part-time professor.

T6: Design for Testability of Embedded Memories

Whether using an in-house-designed memory or using a purchased-IP memory macro cell, embedded memories present significant testing challenges. Proper Design for Testability becomes critical to achieving high-efficient manufacturing test of embedded SRAM, DRAM, and NVRAM. Inadequate Design for Testability can result in increased test time, poor defect test-coverage, additional design releases, and delays getting to market. Design-for-Testability methods are also critical to enabling and simplifying many aspects of the silicon and system-validation process. This tutorial covers memory-test basics, additional challenges of embedded memory, and Design-for-Testability techniques, and solutions for manufacturing test, silicon debug, electrical characterization, and system-level test.

Instructor: Don Weiss is a Senior Design Engineer in the Systems VLSI Technology Division of Hewlett-Packard Co. He received the BSEE and MSEE degrees from the University of Wisconsin-Madison in 1975 and 1976 respectively, and has worked for Hewlett-Packard on the design and test of VLSI CPUs and system-interface chips since then. He was lead designer on the PL7300LC cache memory, the TLB design for the PA8000, and lead architect for the 3MB L3 cache on the IA-64 Itanium 2 processor. Additional interests include the design and reliability of high-performance CMOS circuits and systems. He holds 17 patents on memory and CMOS-circuit design, and has been a member of the ISSCC Program Committee since 2000.

T7: The Reality and Promise of Reconfigurable Computing in Digital Signal Processing

Reconfigurable Computing (RC) has been a topic of academic and industrial interest since the advent of Field-Programmable Gate-Array technology, offering use models ranging from the pedestrian (field upgradability) to the exotic (self-modifying circuits). This tutorial will review the recent history of RC, as well as future challenges in device architecture, design methodology, and DSP algorithms. Examples from application areas such as Software-Defined Radio, and Multimedia will be used to illustrate the potential benefits, pitfalls and decision-making processes that the system architect faces when considering RC.

Instructor: David B. Parlour received the B.S. degree in engineering from Carleton University, Ottawa, Canada, in 1980 and the M.S. degree from the California Institute of Technology, Pasadena, in 1981. In 1990, he joined Xilinx Inc., San Jose, CA, where he has worked on a variety of projects involving the design of circuits, architectures, tools and methodologies for field-programmable gate arrays. He is currently a member of Xilinx Research Labs, where his area of research is domain-specific high-level tools for FPGA design.

F1: Gigahertz Radio Front Ends: RF Power Amplifiers

(Salon 7)

Organizer/Chair: **Michiel Steyaert** , *K.U.Leuven, Belgium*

Committee:
Dave Robertson, *Analog Devices, Wilmington, MA*
Trudy Stetzler, *Texas Instruments, Stafford, TX*
Tetsuro Itakura, *Toshiba, Kawasaki, Japan*

One of the missing building blocks in highly integrated RF circuits is the power amplifier. The intention of this Advanced Solid-State Circuits Forum (ASSCF) is to analyse the problems of integrated power amplifiers, and to discuss the state-of-the-art progress towards integrated RF power-amplifier circuits. Technology requirements, architectures, and performances for different applications are addressed.

Sunday, February 15th 8:30 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topic
8:00	Continental Breakfast
8:30	***Welcome and Introduction*** **M.Steyaert**, *K.U.Leuven, Belgium*
8:35	***Power Amplifiers in Cellular Phones*** **Rob McMorrow**, *Analog Devices, USA*
9:15	***Power Amplifiers*** **Pieter Lok**, *Philips, The Netherlands*
10:00	Break
10:30	***Design Strategies for Fully-Integrated Bluetooth Power Amplifiers*** **Koen Mertens**, *K.U.Leuven, Belgium*
11:15	***Fully-Integrated Watt-Level CMOS Power Amplifiers: No Longer an Oxymoron*** **Ali Hajimiri**, *CALTECH, USA*
12:00	Lunch
1:30	***SiGe/CMOS Power Amplifiers for Wireless Terminals*** **Noriharu Suematsu**, *Mitsubishi Electric, Japan*
2:15	***Case Study: CMOS Power Amplifier —- Nonlinear, Linear, Linearized*** **David Su**, *Atheros Communications, USA*
3:00	Break
3:30	Panel Discussion
4:30	Conclusion

F2: Memory Circuit Design Forum: Non-Volatile Memories Technology and Design

(Golden Gate Hall)

Organizer/Chair: **Jagdish Pathak**, *Sub Micron Circuits Inc., San Jose, CA*

Committee:
Stefan Lai, *Intel Corporation, Santa Clara, CA*
Mark Bauer, *Intel Corporation, Folsom, CA*
Koji Sakui, *Toshiba Corporation, Tokyo, Japan*
Frankie Roohparvar, *Micron Technology, San Jose, CA*
Thomas Jew, *Motorola Inc. Austin, TX*
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
Takayuki Kawahara, Hitachi Ltd., Tokyo, Japan

Non-volatile memories are one of the oldest memories used in computer applications. From the earliest core memories to modern day Flash, this technology has seen significant innovations and surmounted many challenges. Non-volatile memories are surpassing the DRAM's in density. They are also becoming the technology drivers for some of the semiconductor fabs – their application in memory cards, digital photography, cellular telephones, and program storage have surpassed the densities of any other memory technology. In addition to high density, data retention of many years (even after the power supply is turned off) makes non-volatile memories very attractive for battery powered applications and portable consumer devices.

The present day workhorse of non-volatile memories is the floating gate structure. These structures utilize channel hot electron injection and Fowler-Nordheim tunneling for program and erase mechanisms. There have been many architectures proposed like; NOR, NAND, AND, DINOR etc. These architectures tried solving the basic memory requirement of higher density and faster speed. This floating gate structure is now showing significant limitations: it requires high voltages and thick tunnel oxide for program and erase, and the program and erase times are very slow. It is becoming increasingly difficult to scale these structures to smaller geometries. In addition, the process complexity of the floating gate structure also creates problems when embedding these memories in a logic process.

There have been many circuit design and architectural innovations in last decade to solve the scaling and speed issues of non-volatile memories. Multi level cell designs, and page buffers for read / program are some of them. New interest in SONOS structures with multi-bit designs is another field of interest. Serial memory architectures with USB interface and a controller are the backbone of memory sticks.

This advanced circuits forum will present several of the various technologies, architectures and design techniques used in modern day non-volatile memories. The quality, reliability, and test issues of non-volatile memories will be presented. The challenges of scaling, multi-level cell, and embedding these technologies in SoC environment will be discussed. Many new non-volatile technologies are emerging in the field and this forum will discuss the potential and challenges for these technologies.

This year an evening panel discussion session also organized (What is the Next Embedded Non-Volatile Technology?) to complement this forum. This session will debate as to which emerging Non-Volatile technology has a potential to replace the existing floating gate Flash technology for embedded applications.

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topics
8:00	Continental Breakfast
8:30	***Introduction, and historical overview*** **Jagdish Pathak**
9:15	***Cell structures and Array architectures*** **Stefan Lai**
10:15	Break
10:30	***NOR Flash Design*** **Mark Bauer**
11:30	***NAND Flash Design*** **Koji Sakui**
12:30	Lunch
1:15	***Flash Architectures, Application & Testing*** **Frankie Roohparvar**
2:15	***Embedded Flash Memory Considerations*** **Thomas Jew**
3:00	Break
3:15	***Ferro-Electric Memories*** **Ali Sheikholeslami**
4:00	***Emerging Technologies & Future of Non-Volatile Memories*** **Takayuki Kawahara**
5:00	***Concluding Remarks*** **Jagdish Pathak**

SE1: Architectures and Circuits for Ultra Wideband Radio

(Salon 9)

Organizer: **Anantha Chandrakasan**, Professor, *MIT, Cambridge, MA*
Co-Organizer: **Trudy Stetzler,** Senior Member of The Technical Staff, *Texas Instruments, Stafford, TX*
Chair: **Rudolf Koch,** *Infineon Technologies Wireless Products, Munich, Germany*

Ultra-wideband (UWB) signals have been used in military applications such as radar for several decades. More recently, these signals have been used for communication applications. Impulse Radio, one form of UWB signaling, uses short sub-nanosecond pulses resulting in signal spreading over several gigahertz of bandwidth. The IEEE 802.15.3a standardization effort is addressing high-data-rate communication (in excess of 100Mbits/sec) using UWB in the 3.1-10.6 GHz band. This Special Evening Topic Session provides an overview of the design considerations for UWB communication. The session will cover basic communication principles and signaling schemes, channel models, co-existence issues, architectural trade-offs, such as analog/digital partitioning and precision requirements, circuit techniques for wideband processing, and technology choices.

The session starts with a tutorial overview of different signaling schemes, including pulse-based and OFDM-based approaches, along with detailed channel models for wideband communication. Coexistence concerns with narrowband systems will be addressed. The next presentation describes architectural trade-offs and detailed circuit techniques for dual-band CDMA-based UWB. The trade-offs of process technologies for the various UWB functions will also be highlighted. The third presentation describes architectures and circuits for OFDM-based UWB communication. A time-frequency interleaved OFDM approach, using QPSK modulation is presented, and will highlight the implementation of front-end blocks using short-channel CMOS. The final presentation will cover a pulse-based transceiver design using pulse-position modulation and polarity modulation. The design features a one-bit high-speed sampler on the receiver side.

Sunday, February 15th 7:30 PM

SE1: Architectures and Circuits for Ultra Wideband Radio

Time	Topics
7:30	***UWB Basics: Signaling Schemes, Channel Models, and Co-Existence Issues*** **Jeffrey Foerster,** *Wireless Researcher, Intel R&D, Hillsboro, OR*
8:00	***Circuit Techniques for Dual-Band UWB Wireless Communication*** **Raj S. Sengottaiyan,** *XtremeSpectrum, VP of Engineering, Vienna, VA*
8:30	***A Time-Frequency Interleaved OFDM Scheme for UWB*** **Ranjit Gharpurey,** *Senior Member of the Technical Staff, Texas Instruments, Dallas, TX*
9:00	***Flexible Pulse-Based Ultra-Wide-Band RF Transceiver,*** **Lydi Smaïni,** *RF System Design Engineer, STMicroelectronics, Geneva, Switzerland*

SE2: CMOS Meets BIO

(Salon 8)

Organizer/Chair: **Roland Thewes,** *Infineon Technologies, Corporate Research, Munich, Germany*

The invention of the transistor some fifty years ago, the development of integrated circuits, the availability of systems-on-a-chip have all had an essential impact on today's way of life; the next revolution of similar significance may arise from developments in the area of bio-technology and life sciences. In this field, however, tools are required which can be provided - in some cases only - by means of semiconductor fabrication technologies and by means of intelligent bio-sensor and bio-actuator chips. In this Special-Topic Evening Session, emerging developments in this area are highlighted.

First, an introduction will be presented on DNA microarrays, which represent the most prominent biochip application today. Basic questions and techniques, needs, challenges and problems, as well as the technical and economical boundary conditions will be discussed.

Then the benefits of CMOS integration and on-chip electronics are considered. Examples will focus on electronic DNA chip functionalization, electronic readout, and relevant, state-of-the-art application scenarios also approaching the nanofabrication area.

In addition to the DNA-related thrust, an approach is presented on the realization of an enzyme chip. This chip measures proteolytic activity combination of an array of peptide substrates on a solid surface by means of a high-performance image sensor.

Finally, the scope is broadened from molecule-related considerations to consideration of sensors and actuators handling and recording the signals from living cells.

Time	Topic
7:30 pm	***Introduction to DNA Microarrays*** **Martin J. Goldberg,** *Affymetrix Santa Clara, CA*
8:00 pm	***Advanced Integrated Microelectronic DNA Array Devices for Research, Diagnostic and Nanofabrication Applications*** **Michael J. Heller,** *University California San Diego, and Nanogen, San Diego, CA*
8:30 pm	***A Concept of Image Sensor for Enzymatic Activity*** **Takaaki Baba and *Norikazu Nishino,** *Waseda University, *Kyushu Institute of Technology, Japan*
9:00 pm	***Cell-Based Biosensors*** **Martin Jenkner,** *Infineon Technologies, Munich, Germany*

SE3: Highlights of DAC

(Salon 7)

Organizer: **Wanda Gass**, Fellow, *Texas Instruments, Dallas, TX*
Chair: **Joseph Williams,** Distinguished Member of Technical Staff, *Agere Systems, Holmdel, NJ*

Advances in deep-submicron IC technology continue to introduce new challenges for circuit designers. Shrinking device features have caused process variation, interconnect parasitics, and noise to become a limiting factor in multi-GHz designs. Designs approaching 1 billion transistors are increasingly difficult to implement and verify.

The design methods track of the Design Automation Conference (DAC) presents real world experience and solutions from IC designers. The presentations report on tools, methodologies, circuits, and design results. In the ISSCC special session "Highlights of DAC" four invited speakers will present results reported at DAC.

Two presentations deal with the issue of electrical impairments due to process technology and solutions for overcoming them in high speeds designs. One presentation characterizes die process, voltage and temperature variations and their impact on circuits and microarchitecture. Body bias and supply voltage control are techniques proposed to improve tolerance to variation and improve yield. The other presentation characterizes crosstalk and noise in high frequency designs. Techniques for noise analysis are described and methodologies for noise robust design are described based on wire repeaters and noise tolerant cell libraries.

The verification of complex protocols is addressed in a presentation on a formal specification of hardware designs and techniques for directing simulation to check the implementation. Finally, a solution to increasing complexity is addressed by proposing to relax the requirement for bleeding edge design and exploiting the regularity of arrays of logic elements. This presentation argues that the design productivity of deep submicron will become so low that regular fabrics will provide a better tradeoff.

Time	Topic
7:30	***Interconnect and Noise Immunity Design for the Pentium 4 Processor*** **Rajesh Kumar**, *Intel Corporation, Hillsboro, OR*
8:00	***Exploring Regular Fabrics to Optimize the Performance-Cost Trade-Off*** **Larry Pileggi,** *Carnegie Mellon University, Pittsburgh, PA*
8:30	***Parameter Variations and Impact on Circuits and Microarchitecture*** **Tanay Karnik,** *Intel Labs, Hillsboro, OR*
9:00	***Using a Formal Specification and Model Checker to Monitor and Direct Simulation*** **Serdar Tasiran,** *KOC University, Istanbul, Turkey*

SESSION 1 SALON 7-9

PLENARY SESSION — INVITED PAPERS

Chair: **Timothy Tredwell,** *Eastman Kodak Research Labs, Rochester, NY*
ISSCC Executive-Committee Chair

Associate Chair: **Akira Kanuma,** *Toshiba Corporation, Kawasaki, Japan*
ISSCC Program-Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 **Processors and Memory: The Drivers of Embedded Systems Toward the Networked World** **8:40 AM**

Nicholas M. Donofrio, Senior Vice-President, Technology and Manufacturing, IBM, Armonk, NY

The exploding demand for embedded chips is being fueled by a need for versatile system-on-a-chip solutions that provide a high-performance processor core with memory and other elements required to enable a wide range of electronics and computing devices. Historically found in communications equipment, printers, and other computing gear, embedded chips have also become essential components within PDAs, consumer electronics, and wireless handsets, as well in many unconventional IT products, such as automobiles, washing machines, coffee makers, and a vast range of everyday devices. Due to this growing proliferation, along with advancements in materials, manufacturing techniques, and design tools, embedded processors with memory are poised to reign as a dominant force in the semiconductor industry, for years to come. This paper will examine this trend, and will explore the technology, system, and design challenges to be overcome, in fulfilling the promise of pervasive application.

ISSCC, SSCS, JSSC, & IEEE AWARD PRESENTATIONS **9:30 AM**

BREAK 10:00 AM

1.2 **Emerging Technology and Business Solutions for System Chips** **10:15 AM**

Nicky C. Lu, President & CEO, Etron Technology, Hsinchu, Taiwan

In three decades, the IC industry grew from nothing to today's GSI levels (with 10^9 devices on a chip). Its major driving force has been the use of device scaling, which has been especially effective in enhancing the performance of digital chips. But, increasingly, diverse system applications have created an additional driving force - the development of more and more system chips with an increased need to integrate more diverse functionality (digital, analog, memory, RF, etc.) within a limited form factor. In addition to current SoCs on a 2-D die, a trend for the coming decade will be multidimensional die integration on interconnected substrates in a compact package. Correspondingly, a metric analyzing technology trends will be presented.

At the same time, beyond the innovative foundry/fabless business structure of the1990s, new business models are evolving for the realization of system chips. Such models, leading to an effective solution called Virtual Vertical Integration, will be discussed.

System-chip development must also be vertically integrated to achieve optimized performance. But advanced technologies required to realize such integration cover various horizontal segments of knowledge, such as multidimensional-die architecture design, circuit design, and related design automation, as well as novel testing and packaging techniques, leading-edge device and wafer-fabrication technologies, and solution-oriented software coding. In this regard, critical challenges will be highlighted in terms of power partitioning, integrated design, and built-in quality assurance for known-good-die, signal integrity in field applications, and technology optimization across different segments. The parallelism of technology solutions with business models, and their conjoined optimization in the coming system-chip era, will be illustrated in this paper.

1.3 Cellular-Phones as Embedded Systems 11:05 AM

Yrjö Neuvo, Professor; Executive Vice President, CTO, Nokia Mobile Phones, Member of Nokia Group Executive Board, Finland

The trend in handheld devices is toward smaller multifunctional terminals with continuously-improving end-user satisfaction. In addition to being difficult to fulfill separately, the different requirements are often contradictary. This statement applies especially well in the case of cellular phones. The speed of their development has been unequalled, while delivery volumes have grown all the time, being now over 400 million per annum. The high level of integration and other technical challenges make the cellular phone an ideal example of an embedded communications system with tough requirements.

In this paper, technologies needed to assemble a cellular phone are studied from different angles. Overall power consumption is one of the key performance indicators. This translates to concern, both for power-amplifier and DSP efficiency in the talk mode, and for various leakage currents in analog and digital receiver circuits in the standby mode. The emerging multimedia capabilities call for better displays and enhanced audio performance. The increasing amount of software needed sets wholly new requirements for the processing power and memory size of the device.

Third-generation cellular standards support high data rates, and are based on the most recent advances in the telecommunications sphere. Packet-switched traffic and Internet protocols are growing in importance, whereas other more-traditional radio interfaces are integrated into cellular phones to form multi-radio devices. Evidently, the power consumption is affected simultaneously.

In this review paper, the cellular phone is analyzed as an embedded system from the integration, performance, and power-consumption angles. We will discuss the following key issues concerning cellular phones:

- Terminal trends and their impact on power economy
- Radio technologies and multiradio concepts
- Technological implementations
- Integration challenges
- Related solid-state-circuit research-and-development expectations

NON-VOLATILE MEMORY

Chair: **Frankie Roohparvar,** *Micron Technology, San Jose, CA*
Associate Chair: **Yukihito Oowaki,** *Toshiba, Yokahama, Japan*

2.1 A 0.18μm 3V 64Mb Non-Volatile Phase-Transition Random Access Memory

1:30 PM

W. Cho[1], B-H. Cho[1], B-G. Choi[1], H-R. Oh[1], S-B. Kang[1], K-S. Kim[1], K-H. Kim[1], D-E. Kim[1], C-K. Kwak[1], H-G. Byun[1], Y-N. Hwang[1], S-J. Ahn[1], G-T. Jung[2], H-S. Jung[2], K. Kim[2]
[1]Samsung Electronics, Hwasung, Korea
[2]Samsung Electronics, Yongin, Korea

A non-volatile 64Mb phase-transition RAM is developed by fully integrating a chalcogenide alloy GST($Ge_2Sb_2Te_5$) into 0.18μm CMOS technology. This alloy is programmed by resistive heating. To optimize SET/RESET distribution, a 512kb sub-core architecture, featuring meshed ground line, is proposed. Random read access and write access for SET/RESET are 60ns, 120ns and 50ns, respectively, at 3.0V and 30°C.

2.2 An Experimental 256Mb Non-Volatile DRAM with Cell Plate Boosted Programming Technique

2:00 PM

J-H. Ahn[1], S. Hong[1], S. Kim[1], J-B. Ko[1], S-D. Lee[1], Y-W. Kim[1], K-S. Lee[1], S-K. Lee[1], G-H. Bae[1], S-W. Park[1], Y-J. Park[2]
[1]Hynix Semiconductor, Icheon, Korea
[2]Seoul National University, Seoul, Korea

A 256Mb NVDRAM is fabricated with a modified 0.115μm DRAM process. The cell transistor has a scaled polysilicon-oxide-nitride-oxide-silicon (SONOS) structure that traps electrons or holes at a relatively low voltage stress. NVDRAM utilizes DRAM storage node boost from the cell plate for programming to ensure more reliable operation.

2.3 A 4Mb 0.18μm 1T1MTJ Toggle MRAM Memory

2:30 PM

T. Andre[1], B. Garni[1], H. Lin[1], W. Martino[1], J. Nahas[1], A. Omair[2], C. Subramanian[1]
[1]Motorola, Austin, TX
[2]Motorola, Chandler, AZ

The 4.5x6.3mm² 25ns cycle-time 4Mb Toggle MRAM memory, built in 0.18μm 5M CMOS technology, uses a 1.55μm² bit cell with a single toggling magneto tunnel junction. The memory uses uni-directional programming currents with isolated write and read paths and balanced current mirror sense amplifier.

BREAK 3:00 PM

2.4 Embedded Flash Memory for Security Applications in a 0.13μm CMOS Logic Process (NOVeA)

3:15 PM

J. Raszka, M. Advani, N. Der Hacobian, A. Mittal, M. Han, V. Tiwari, L. Varisco, A. Shirdel, A. Shubat
Virage Logic, Fremont, CA

Many applications require moderate amounts of embedded NVM (<16Kb) for security encryption. Conventional approaches (EEPROM, Flash) are expensive due to the need for several additional masks and process steps relative to CMOS. NOVeA is a scalable embedded Flash technology manufactured on a standard CMOS logic process with an integrated SRAM array that facilitates password authentication.

2.5 A 55mm² 256Mb NROM Flash Memory with Embedded Microcontroller Using an NROM-Based Program File ROM

3:45 PM

Y. Sofer, M. Idan, Y. Betser, E. Maayan, M. Grossgold
Saifun Semiconductors, Netanya, Israel

A 256Mb flash memory based on 2b/cell 0.17μm NROM technology supports 90ns random read access, 66MHz synchronous read, and 3μs/word programming. This 55mm² device includes an 8b embedded microcontroller for program and erase operations, power-up sequence, BIST, and more. The microcontroller executes its code from an NROM-based embedded ROM, performing 30ns/word read access.

2.6 A 0.9V 1T1C SBT-Based Embedded Non-Volatile FeRAM with a Reference Voltage Scheme and Multi-Layer Shielded Bit-Line Structure

4:15 PM

K. Yamaoka[1], S. Iwanari[1], Y. Murakuki[1], H. Hirano[2], M. Sakagami[2], T. Nakakuma[2], T. Miki[2], Y. Gohou[1]
[1]Matsushita Electric Industrial, Nagaokakyo, Japan
[2]Matsushita Electric Industrial, Kyoto, Japan

A 1T1C embedded FeRAM operates at an ultra low voltage of 0.9V with 550ns access even after 10 years of imprint degradation. The ultra low voltage operation and high-reliability characteristics are attained by using a reference-voltage scheme and a multi-layer shielded bit-line structure.

2.7 A 3.3V 4Gb Four-Level NAND Flash Memory with 90nm CMOS Technology

4:45 PM

S. Lee, Y-T. Lee, W-G. Hahn, D-W. Kim, M-S. Kim, H. Cho, S-H. Moon, J-W. Lee, D-S. Byeon, Y-H. Lim, H-S. Kim, S-H. Hur, K-D. Suh
Samsung Electronics, Hwasung, Republic of Korea

A 4Gb NAND flash memory with 2b/cell uses 90nm CMOS to achieve simultaneous data load during program operation with 1.6MB/s program throughput. Fuse or pad-bonding switches it to a 2Gb 1b/cell NAND flash memory. The row decoder located in the middle of the cell array reduces W/L rise time and coupling noise. A program-after-erase technique and lowered floating poly thickness minimize cell Vth distribution.

CONCLUSION 5:15 PM

PROCESSORS

Chair: **Simon Segars,** *ARM, Cambridge, England*
Associate Chair: **Robert Rogenmoser,** *Broadcom, Santa Clara, CA*

3.1 Design and Implementation of the POWER5 Microprocessor

1:30 PM

J. Clabes[1], J. Friedrich[1], M. Sweet[1], J. DiLullo[1], S. Chu[1], D. Plass[2], J. Dawson[2], P. Muench[2], L. Powell[1], M. Floyd[1], M. Lee[1], M. Goulet[1], J. Wagoner[1], N. Schwartz[1], S. Runyon[1], G. Gorman[1], P. Restle[3], R. Kalla[1], J. McGill[1], S. Dodson[1]
[1]IBM, Austin, TX
[2]IBM, Poughkeepsie, NY
[3]IBM, Yorktown Heights, NY

POWER5 offers ~4x performance over the previous design by incorporating simultaneous multithreading, a latency-optimized memory subsystem, extensive reliability, availability and serviceability (RAS), and power management support. The 276M-transistor processor is implemented in a 0.13μm, 8M silicon-on-insulator technology and operates above 1.5GHz.

3.2 A Dual-Core 64b UltraSPARC Microprocessor For Dense Server Applications

2:00 PM

T. Takayanagi, J. Shin, B. Petrick, J. Su, A. Leon
Sun Microsystems, Sunnyvale, CA

A processor core, previously implemented in a 0.25μm Al process, is redesigned for a 0.13μm Cu process to create a dual-core processor with 1MB integrated L2 cache, offering an efficient performance/power ratio for compute-dense server applications. Circuit design challenges, including negative bias temperature instability (NBTI), leakage and coupling noise are discussed.

3.3 A 40Gb/s Network Processor with PISC™ Dataflow Architecture

2:30 PM

J. Carlström, G. Nordmark, J. Roos, T. Strömqvist, L-O. Svensson, P. Westlund
Xelerated, Stockholm, Sweden

This 40Gb/s network processor has a dataflow architecture with 200 PISC™ processors, organized in a linear array, also containing 11 I/O processors which interconnect to on-chip or off-chip engines. Implemented in a 0.13μm CMOS process, the chip has 114M transistors and typically dissipates 9.5W at 200MHz.

BREAK 3:00 PM

3.4 A Scalable X86 CPU Design for 90nm Process

3:15 PM

C. Webb, J. Schutz
Intel, Hillsboro, OR

A third generation Pentium®4 processor is designed to meet the challenges of a 90nm technology. Design methodology allows scalability with increased transistor performance over the life of the process. Improved design for test techniques are developed to facilitate the debug process. We also discuss improved design automation techniques to reduce hand-drawn schematics.

3.5 Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor

3:45 PM

S. Akui, K. Seno, M. Nakai, T. Meguro, T. Seki, T. Kondo, A. Hashiguchi, H. Kawahara, K. Kumano, M. Shimura
Sony, Shinagawa, Japan

A dynamic voltage and frequency management scheme that autonomously controls the clock frequency (8 to 123MHz at 0.5MHz step) and adaptively controls the voltage (0.9 to 1.6V at 0.5mV step) with a leakage power compensation effect is developed for a low-power embedded microprocessor. It achieves 82% power reduction in personal information management (PIM) application.

3.6 A 4MB On-Chip L2 Cache for a 90nm 1.6GHz 64b SPARC Microprocessor

4:15 PM

D. Wendell[1], J. Lin[1], P. Kaushik[1], S. Seshadri[1], V. Sunararaman[2], A. Wang[1], P. Wang[1], H. McIntyre[1], S. Kim[1], W. Hsu[1], G. Levinsky[1], D. Tang[1], S. Wong[1], J. Lu[1], V. Melamed[1], S. Narayanan[1], G. Liu[1], C. Yuan[1], M. Chirania[1], R. Heald[1], J. Kaku[1], P. Lazar[1], S. Bhutani[1], S. Hirose[1], J. Thomas[1].
[1]Sun Microsystems, Sunnyvale, CA
[2]Intel, Bangalore, India

A next-generation 1.6GHz 4-issue CPU supports high-end servers and has a 4MB L2 cache. The chip uses 315M transistors in a 90nm 8M CMOS process with an area of 234mm^2.

3.7 PowerPC 970 in 130nm and 90nm Technologies

4:45 PM

N. Rohrer[1], M. Canada[1], M. Mayfield[2], E. Cohen[1], M. Ringler[1], P. Sandon[1], T. Pflueger[3], P. Kartschoke[1], J. Heaslip[1], P. McCormick[1], C. Lichtenau[3], J. Allen[2], J. Zimmerman[1], T. Werner[3], G. Salem[1], M. Ross[1], D. Appenzeller[1], D. Thygesen[1]
[1]IBM, Essex Junction, VT
[2]IBM, Austin, TX
[3]IBM, Boeblingen, Germany

A 64b PowerPC microprocessor is introduced in 130nm and redesigned in 90nm SOI technology. PowerPC 970 implements a SIMD instruction set with 512kB L2 cache. It runs at 2.0GHz with a 1.0GHz bus in 130nm. The 90nm design features PowerTune for rapid frequency and power scaling and electronic fuses.

CONCLUSION 5:15 PM

OVERSAMPLED ADCs

Chair: **Axel Thomsen,** *Silicon Laboratories, Austin, TX*
Associate Chair: **Bram Nauta,** *University of Twente, The Netherlands*

4.1 A Cascaded Continuous-Time ΣΔ Modulator with 67dB Dynamic Range in 10MHz Bandwidth

1:30 PM

L. Breems
Philips Research, Eindhoven, The Netherlands

A 2-2 cascaded ΣΔ modulator with continuous-time loop filters and 4b quantizers is presented. The dynamic range is 67dB in a 10MHz bandwidth at a 160MS/s with a full-scale input range of 200mV$_{rms}$. Inherent anti-aliasing filtering is over 50dB. The 0.18μm CMOS chip measures 1.7mm^2 and draws 68mA from a 1.8V supply.

4.2 A 25MS/s 14b 200mW ΣΔ Modulator in 0.18μm CMOS

2:00 PM

P. Balmelli, Q. Huang
ETH Zurich, Zurich, Switzerland

Sampled at 200MHz, a 5th-order 4b-quantizer single-loop ΣΔ modulator achieves a 25MS/s conversion rate with 84dB DR and 82dB SNR, a performance suitable for VDSL. Implemented in 0.18μm CMOS the 0.95mm^2 chip has a power consumption of 200mW from a 1.8V supply.

4.3 ΣΔ ADC with Finite Impulse Response Feedback DAC

2:30 PM

B. Putter
Philips Research, Eindhoven, The Netherlands

A continuous-time 1b ΣΔ ADC with a finite impulse response DAC in the feedback path is presented. The FIRDAC reduces the susceptibility to clock jitter by 18dB while maintaining linearity. S/N ratio is 77dB in a 1MHz bandwidth, and IM2 and IM3 are 77dB and 82dB, respectively. The 0.18μm CMOS chip consumes 6.0mW.

BREAK 3:00 PM

4.4 A 0.9V 1.5mW Continuous-Time ΔΣ Modulator for WCDMA

3:15 PM

T. Ueno, T. Itakura
Toshiba, Kawasaki, Japan

A second-order continuous-time ΔΣ modulator for a WCDMA RX is implemented with inverter-based OTAs, enabling operation at a voltage of 0.9V. The OTAs are balanced by using CMFB. The modulator consumes only 1.5mW and occupies 0.12mm^2 in a 0.13μm CMOS process. SNDR is 50.9dB over a bandwidth of 1.92MHz.

4.5 A 1V 88dB 20kHz ΣΔ Modulator in 90nm CMOS

3:45 PM

L. Yao, M. Steyaert, W. Sansen
Katholieke Universiteit Leuven, Leuven, Belgium

A third-order single-loop SC ΣΔ modulator is realized in a standard 90nm digital CMOS technology. The modulator achieves 88dB dynamic range for a 20KHz signal bandwidth with an OSR of 100. Power consumption is 140μW from a 1V supply, and the chip core size is 0.18mm^2.

4.6 A Power-Optimized 14b SC ΔΣ Modulator for ADSL CO Applications

4:15 PM

R. Gaggl, M. Inversi, A. Wiesbauer
Infineon Technologies, Villach, Austria

A switched-capacitor multi-bit ΔΣ ADC including a reference-voltage buffer is implemented in 0.13μm CMOS. The single loop 3b modulator features 14b and 13b dynamic range over 276kHz and 1.1MHz signal bandwidths, respectively. Clocked at 105MHz, the ADC core consumes 8mW from a 1.5V supply.

4.7 A Mirror-Image-Free Two-Path Bandpass ΣΔ Modulator with 72dB SNR and 86dB SFDR

4:30 PM

F. Ying[1], F. Malobert[2]
[1]Texas Instruments, Dallas, TX
[2]The University of Texas at Dallas, Richardson, TX

A cross-coupled two-path ΣΔ architecture generates transmission zeros at 1/3 of the clock frequency, thereby achieving a mirror image free response. The chip uses 0.18μm CMOS technology and is clocked at 2x60MHz with a 40MHz IF. The modulator achieves an 86dB SFDR with a 2.5MHz bandwidth and consumes 150mW from a 1.8V supply.

4.8 A 2mW 89dB DR Continuous-Time ΣΔ ADC with Increased Wide-Band Interference Immunity

4:45 PM

K. Philips[1], P. Nuijten[1], R. Roovers[1], F. Munoz[2], M. Tejero[2], A. Torralba[2]
[1]Philips Research, Eindhoven, The Netherlands
[2]Universidad de Sevilla, Sevilla, Spain

A continuous-time ΣΔ ADC with merged channel filter and programmable-gain functionality is presented. Interferers above full-scale can be applied without jeopardizing reception of weak desired signals. The merged design occupies 0.14mm^2 in 0.18μm CMOS, consumes 2mW, and achieves 89dB of dynamic range in a 1MHz bandwidth.

CONCLUSION 5:15 PM

WLAN TRANSCEIVERS

Chair: **Tony Montalvo,** *Analog Devices, Raleigh, NC*
Associate Chair: **David Su,** *Atheros Communications, Sunnyvale, CA*

5.1 A Direct-Conversion CMOS Transceiver for 4.9-5.95GHz Multi-Standard WLANs

1:30 PM

T. Maeda, H. Yano, T. Yamase, N. Yoshida, N. Matsuno, S. Hori, K. Numata, R. Walkington, T. Tokairin, Y. Takahashi, M. Fujii, H. Hida
NEC, Tsukuba, Japan

A 0.18μm CMOS direct-conversion transceiver consumes only 60mA in RX mode and 74mA in TX. System NF is 4.4dB, and IIP3 is -2dBm. The transceiver supports world-wide multi-standard WLAN systems with a frequency range of 4.9-5.95GHz and channel bandwidths of 5-20MHz.

5.2 A Single Chip CMOS Transceiver for 802.11a/b/g WLANs

2:00 PM

R. Ahola[1], A. Aktas[2], J. Wilson[2], K. Rama Rao[2], F. Jonsson[3], I. Hyyryläinen[1], A. Brolin[3], T. Hakala[1], A. Friman[1], T. Mäkiniemi[1], J. Hanze[3], M. Sanden[3], D. Wallner[3], Y. Guo[3], T. Lagerstam[1], L. Noguer[3], T. Knuuttila[1], P. Olofsson[3], M. Ismail[2]
[1]Spirea, Espoo, Finland
[2]Spirea Microelectronics, Dublin, OH
[3]Spirea, Stockholm, Sweden

A 0.18μm dual-band tri-mode CMOS radio, fully compliant with the IEEE 802.11a/b/g standards, achieves a system noise figure of 5.2/5.6dB (high gain), and an EVM of 2.7/3.0% for the 2.4/5GHz bands, respectively. Die area is 12mm^2, and power consumption is 200mW in RX and 240mW in TX using a 1.8V supply.

5.3 A Dual-Band 802.11a/b/g Radio in 0.18μm CMOS

2:30 PM

L. Perraud, C. Pinatel, N. Sornin, J-L. Bonnot, M. Recouly, F. Benoist, M. Massei, O. Gibrat
NewLogic, Sophia-Antipolis, France

A radio compliant with 802.11a/b/g standards occupies 12mm^2 in 0.18μm CMOS. In the 54Mb/s mode, the receivers have a sensitivity level below -73dBm while consuming 230mW. The transmitters, implementing a wide-band Cartesian feedback loop, deliver -2dBm average power with an EVM of 3% while consuming 300mW.

BREAK 3:00 PM

5.4 A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN

3:15 PM

M. Zargari[1], S. Jen[1], B. Kaczynski[1], M. Lee[1], M. Mack[1], S. Mehta[1], S. Mendis[1], K. Onodera[1], H. Samavati[1], W. Si[1], K. Singh[1], A. Tabatabaei[2], M. Terrovitis[1], D. Weber[1], D. Su[1], B. Wooley[3]
[1]Atheros Communications, Sunnyvale, CA
[2]IRF Semiconductor, Cupertino, CA
[3]Stanford University, Stanford, CA

A 2.4/5GHz transceiver implements the RF and analog front-end of an IEEE 802.11a/g/b WLAN system in 0.25μm CMOS technology. The IC transmits 9dBm/8dBm EVM-compliant output power at 5GHZ/2.4GHz for a 64QAM OFDM signal. The overall receiver NF is 5.5/4.5dB at 5/2.4GHz.

5.5 A 3.2 to 4GHz 0.25μm CMOS Frequency Synthesizer for IEEE 802.11a/b/g WLAN

3:45 PM

M. Terrovitis, M. Mack, K. Singh, M. Zargari
Atheros Communications, Sunnyvale, CA

A fully integrated 3.2 to 4GHz frequency synthesizer, part of an IEEE 802.11a/b/g transceiver, is implemented in a 0.25μm standard CMOS technology. The phase noise is -105dBc/Hz at 10kHz offset, and the spurs are below -64dBc when measured at the 5GHz transmitter output. The settling time is less than 150μs.

5.6 A CMOS Dual-Band Fractional-N Synthesizer with Reference Doubler and Compensated Charge Pump

4:15 PM

H. Huh[1], Y. Koo[2], K-Y. Lee[2], Y. Ok[2], S. Lee[2], D. Kwon[1], J. Lee[2], J. Park[2], K. Lee[2], D-K. Jeong[1], W. Kim[1]
[1]Seoul National University, Seoul, Korea
[2]GCT Semiconductor, San Jose, CA

A fully integrated dual-band frequency synthesizer in 0.35μm CMOS technology achieves a phase noise of -141dBc/Hz at 1.25MHz offset in the PCS band with a reference frequency doubler. Fractional spurs are reduced by 8.6dB at 50kHz offset with a replica compensated charge pump.

5.7 A 2.5dB NF Direct-Conversion Receiver Front-End for HiperLAN2/IEEE802.11a

4:45 PM

P. Rossi, A. Liscidini, M. Brandolini, F. Svelto
Università di Pavia, Pavia, Italy

A voltage-voltage feedback, frequency-tunable LNA and I&Q variable-gain mixers are realized in a 0.25μm SiGe BiCMOS technology. The front-end, suitable for multi-standard applications, shows the following performance in the 4.9 to 5.825GHz band: 31.5dB gain, 2.5dB NF, -9.5dBm IIP3, and 23dBm IIP2 while drawing 16mA from 2.5V.

5.8 A 4.3GHz 44μW CMOS Frequency Divider

5:00 PM

K. Yamamoto, M. Fujishima
University of Tokyo, Tokyo, Japan

A microwatt frequency divider for the 2.5GHz ISM band is proposed. The outputs are generated by pulse modulation of a ring oscillator. A power of 44μW at 4.3GHz is achieved with a 0.2μm CMOS process. The core size is 10.8x10.5μm^2, and locking range is 2.3GHz.

CONCLUSION 5:15 PM

IMAGING

Chair: **Jed Hurwitz,** *ST Microelectronics, Edinburgh, Scotland*
Associate Chair: **Daniel McGrath,** *Kodak, Rochester, NY*

6.1 A 3.9μm Pixel Pitch VGA Format 10b CMOS Image Sensor with 1.5-Transistor/Pixel

1:30 PM

H. Takahashi, M. Kinoshita, K. Morita, T. Shirai, T. Sato, T. Kimura, H. Yuzurihara, S. Inoue
Canon, Ayase, Japan

A CMOS image sensor with a shared 1.5 transistor/pixel architecture and buried photodiode with complete charge transfer capability is described. The sensor achieves a 330μV noise floor and 50pA/cm^2 dark current at 45°C. The chip is fabricated in a thin planarized 0.35μm 1P2M CMOS process.

6.2 A 1/4in 2M Pixel CMOS Image Sensor with 1.75Transistor/pixel Architecture

2:00 PM

M. Mori, M. Katsuno, S. Kasuga, T. Murata, T. Yamaguchi
Matsushita Electric, Nagaokakyo, Japan

A 2.5V CMOS image sensor using a pixel configuration of four photodiodes in one unit sharing seven transistors is presented. This image achieves a 2.25μm pixel pitch with 25% fill factor in a 0.25μm IP2M CMOS process.

6.3 CMOS Image Sensors Using Floating Diffusion Driving Buried Photodiode

2:30 PM

K. Mabuchi, N. Nakamura, E. Funatsu, T. Abe, T. Umeda, T. Hoshino, R. Suzuki, H. Sumi
Sony, Atsugi, Japan

Two 2.5V VGA CMOS image sensors with 3.45μm and 3.1μm buried photodiode-pixels on a 0.25μm 2P3M CMOS technology are described. The test chips utilize a floating diffusion driving technique to achieve 3-transistors/pixel and 2-transistors/pixel respectively, and operate at 60 frames/s with 49mW dissipation.

BREAK 3:00 PM

6.4 A CMOS Image Sensor Uses a Dynamic Reset Current Source for Noise Suppression

3:15 PM

K-H. Lee, E. Yoon
KAIST, Daejeon, Korea

A 512 x 384 CMOS image sensor in 0.18μm 1P4M technology with 5.9μm pixel pitch and a dynamic reset current source to compensate for kTC reset noise and fixed pattern noise is presented. A total of 390μV(rms) readout noise, and a factor of two improvement over conventional reset is achieved. The chip operates at 1.8V and consumes 40mW excluding I/O and off-chip DAC for a single-slope ADC at 24frames/s.

6.5 Combined Linear-Logarithmic CMOS Image Sensor

3:45 PM

G. Storm[1], J. Hurwitz[2], D. Renshaw[1], K. Findlater[2], R. Henderson[2], M. Purcell[2]
[1]University of Edinburgh, Edinburgh, United Kingdom
[2]STMicroelectronics, Edinburgh, United Kingdom

A 352 x 288 pixel array achieves >120dB dynamic range through merging sequential linear and logarithmic images. Calibration is used to match offset and gain. A 7-transistor pixel is built in a 0.18μm 1P4M CMOS process.

6.6 A 375 x 365 3D 1kframe/s Range-Finding Image Sensor with 394.5kHz Access Rate and 0.2 Sub-Pixel Accuracy

4:15 PM

Y. Oike, M. Ikeda, K. Asada
University of Tokyo, Tokyo, Japan

Row-parallel search architecture and focal plane processing using light sections acquires range images at 1052frames/s with accuracy of 11mm at 600mm distance. The 24-transistor, 11.25μm pitch pixel with 28% fill factor is built in a 0.18μm IP5M CMOS process.

6.7 A CMOS Single Photon Avalanche Diode Array for 3D Imaging

4:45 PM

C. Niclass, A. Rochas, P-A. Besse, E. Charbon
Swiss Federal Institute of Technology, Lausanne, Switzerland

An 8x4 avalanche diode array in a 0.8μm CMOS process uses single photon counting for time-of-flight range finding with 100ps 40mW decollimated laser pulses. An accuracy of 618μm is achieved from 15cm to 1m with 10^4 pulses.

6.8 A Zero-Sink-Current Schmitt Trigger and Window-Flexible Counting Circuit for Fingerprint Sensing and Identification

5:00 PM

H. Morimura, T. Shimamura, K. Fujii, S. Shigematsu, Y. Okazaki, K. Machida
NTT, Atsugi, Japan

A pixel-parallel architecture with 1b ADC per pixel achieves 6.4μW dissipation. Pixel memory element and event counting sensing circuitry control fingerprint acquisition. A 224 x 256 pixel array is built in a 0.25μm CMOS process.

CONCLUSION 5:15 PM

E1: To UWB or Not To Be

(Salon 9)

Organizer: **David Su,** Director of Analog, *Atheros Communications, Sunnyvale, CA*
Moderator: **Thomas H. Lee,** Professor*, Stanford University, Stanford, CA*

Today, wireless networking is dominated by the IEEE 802.11-based systems. Will *very-wideband* wireless networking with speeds exceeding 200Mb/s be available soon? The panel will explore how to achieve very wideband wireless communication systems including Ultra Wideband (UWB) and debate their merits. Which wireless technology has what it takes to enable the next killer app? Each panelist will make a prediction and answer the question: *To UWB or not to be*.

Panelists:

Bob Brodersen, Professor, *UC Berkeley, Berkeley, CA*
Don Cox, Professor, *Stanford University, Stanford, CA*
Jeff Foerster, Wireless Researcher, *Intel R&D, Hillsboro, OR*
Ali Hajimiri, Professor, *Caltech, Pasadena, CA*
Keiichi Ohata, Principal Researcher, *Photonic and Wireless Devices Research Labs, NEC Corp, Otsu, Japan*
Ian Oppermann, Adj Professor (Docent), Director of CWC-Oulu, *University of Oulu, Finland*

E2: Is the Golden Age of Analog Circuit Design Over?

(Salon 8)

Organizer: **John Khoury,** VP of Product Development, *Vitesse Semiconductor, Somerset, NJ*
Moderator: **Lawrence Devito,** Fellow, *Analog Devices, Wilmington, MA*

The 1980s and 1990s witnessed great advances in analog integrated circuit design, particularly in CMOS technology. High resolution circuits such as data converters and high performance RF CMOS circuits were created. In the future as technology scales resulting in sub 1V power supplies, is any transistor level circuit innovation possible or will all innovation be at the system level ?

Panelists:

Asad Abidi, Professor, *UCLA, Los Angeles, CA*
Chris Mangelsdorf , *Design Center Manager, Analog Devices*
Akira Matsuzawa, Professor, *Tokyo Institute of Technology, Tokyo, Japan*
Yannis Tsividis, Professor, *Columbia University, New York, NY*
Eric Vittoz, Chief Scientist, *CSEM, Neuchetal, Switzerland*
Rick Walker, Consultant, *Palo Alto , CA*

SE4: Circuits and Applications for Organic Electronics

(Salon 7)

Organizer: **C.K. Ken Yang,** *UCLA, Los Angeles, CA*
Chair: **Werner Weber,** *Infineon Technologies, Munich, Germany*

Organic materials can be created which are semiconductors similar to silicon. Functioning semiconductor devices and circuits have already been fabricated using those materials. However, important device parameters such as the mobility and the contact resistance are inferior to silicon.

Why then, do we want to develop a process based on such organic materials? It is the potential of low-cost manufacturing, and the flexibility of the substrate that makes this technology worthwhile for a variety of applications, each having specific requirements. This technology may further reduce manufacturing infrastructure costs compared to conventional integrated electronics. RFID tags, flexible displays, and sensor arrays are among the most important ones.

This session contains presentations that discuss the devices, circuits, and applications that are currently pursued and explores the potential of this technology.

The first talk presents an overview of the technology by summarizing the recent activities of researchers. Current devices under investigation such as LEDs, photodetectors, and transistors, including their potential applications, are discussed. The second talk addresses circuit implications of organic electronics fabricated by printed organic thin-film-transistors (OTFTs).

The latter two talks focus on the development of commercial products with OTFTs by two industry laboratories. The first from Sony describes the transistor characteristics and their application for displays. The second describes current efforts by Infineon in applications such as RFIDs.

These talks cover the flexibility and potential of this broad area with only some examples of application drivers. As with many budding technologies, their continued development depends greatly on the urgency of the application drivers. The presenters look forward to discussing with the attendees other innovative application drivers.

Time	Topic
8:00	***Application Driven Organic Electronics*** **Vladimir Bulovic**, *MIT, Cambridge, MA*
8:30	***Organic Electronics: What Is It Good For?*** **Michael Kane,** *Sarnoff Corporation*
9:00	***A Bottom-Contact Organic-Thin-Film-Transistorfor Flexible Display Application*** **Kazumasa Nomoto,** *Sony Fusion Domain Laboratory, Japan*
9:30	***Polymer Electronics: Perspectives Towards Applications*** **Güenter Schmid,** *Infineon Technologies AG*

TD: SCALING TRENDS

Chair: **Hiroyuki Mizuno,** *Hitachi, Tokyo, Japan*
Associate Chair: **Christian Enz,** *Swiss Center for Electronics, Neuchatel, Switzerland*

7.1 How Scaling Will Change Processor Architecture

8:30 AM

M. Horowitz, W. Dally
Stanford University, Stanford, CA

For the past 30 years processors have hidden scaling from the programmer, presenting the same opaque computational interface. Power and wire scaling issues are causing this interface to cease being opaque. For efficiency, future machines must be distributed and heterogeneous and will add at least a "stream" programming interface.

7.2 Designing Beyond the Rails

9:00 AM

A-J. Annema[1], B. Nauta[1], H. Tuinhout[2], R. van Langevelde[2]
[1]University of Twente, Enschede, The Netherlands
[2]Philips Research, Eindhoven, The Netherlands

CMOS evolution introduces several problems in analog design. Gate-leakage mismatch exceeds matching tolerances requiring active cancellation techniques. One stategy to deal with the use of lower supply voltages is to operate critical parts at higher supply voltages, by exploiting combinations of thin- and thick-oxide transistors.

7.3 Circuit Design and Noise Considerations for Future Blu-ray Disc Optical Storage Technology

9:30 AM

B. Stek, G. de Jong, T. Jansen, J. Bergervoet, P. Woerlee
Philips, Eindhoven, The Netherlands

The Blu-ray optical disc format for 25GB capacity is described. Low SNR is an issue for high-speed read-out and dual-layer discs. A non-linear equalizer circuit reduces low frequency media noise. Low-noise CMOS preamplifiers and the impact of CMOS scaling on SNR are presented.

BREAK 10:00 AM

7.4 3D Interconnection and Packaging: 3D-SiP, 3D-SoC or 3D-IC

10:15 AM

E. Beyne
IMEC, Leuven, Belgium

Traditional interconnect schemes are basically two-dimensional. It has long been a dream for system designers to be able to combine multiple integrated circuits by connecting them in the third dimension. Three approaches to the 3D interconnect problem are described: system in a package (3D-SiP), system on a chip (3D-SoC) and 3D integrated circuits (3D-IC).

7.5 A 160Gb/s Interface Design Configuration for Multichip LSI
10:45 AM

T. Ezaki, K. Kondo, H. Ozaki, N. Sasaki, H. Yonemura, M. Kitano, S. Tanaka, T. Hirayama
Sony, Shinagawa, Japan

The Multichip LSI (MCL) comprised of both an embedded 123MHz CPU and a 64Mb memory in one package is introduced. 1300 signal lines are directly connected by microbumps between the two chips and achieve 160Gb/s signal interface performance. Both the CPU and memory are fabricated in a 0.15μm CMOS technology.

7.6 A 1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-Chip Signaling
11:15 AM

D. Mizoguchi[1], Y. Yusof[1], N. Miura[1], T. Sakurai[2], T. Kuroda[1]
[1]Keio University, Yokohama, Japan
[2]University of Tokyo, Japan

A wireless bus for stacked chips is designed with the interface using inductive coupling with metal spiral inductors. Transceiver circuits for non-return-to-zero signaling are developed. Test chips stacked at a distance of 300μm communicate at data rates of up to 1.2Gb/s/pin. Fabricated in 0.35μm CMOS technology, TX and RX dissipation are 43 and 2.5mW, respectively.

7.7 Electronic Alignment for Proximity Communication
11:30 AM

R. Drost, R. Ho, D. Hopkins, I. Sutherland
Sun Microsystems, Mountain View, CA

This work presents an electronic alignment mechanism for capacitively-coupled proximity communication. On an experimental chip, position offsets of up to +/-100μm are electrically corrected to within 6.25μm. A 0.35μm experimental CMOS chip communicates at 1.35Gb/s with a BER $\leq 10^{-10}$.

7.8 A High-Voltage Output Driver in a Standard 2.5V 0.25μm CMOS Technology
11:45 AM

B. Serneels, T. Piessens, M. Steyaert, W. Dehaene
[1]Katholieke Universiteit, Leuven, Belgium

A robust 7.5V output driver is realized in standard 2.5V 0.25μm CMOS. The chip delivers an output swing of 6.46V to a 50Ω load with a 10MHz input square wave. A dual-tone PWM signal at 70kHz and 250kHz results in an IM3 of -65dBm. The on-resistance is 5.9Ω.

CONCLUSION 12:00 PM

CIRCUITS FOR DIGITAL SYSTEMS

Chair: **Jim Warnock,** *IBM, Yorktown Heights, NY*
Associate Chair: **Hoi-Jun Yoo,** *KAIST, Daejon, Korea*

8.1 100MPackets/s Fully Self-Timed Priority Queue: FQ

8:30 AM

M. Iwata, M. Ogura, Y. Ohishi, H. Hayashi, H. Terada
Kochi University of Technology, Tosayamada, Japan

This priority queuing module is integrated as part of QoS functions in a data-driven network processor chip. Since the whole FQ circuit is realized by a fully self-timed folded pipeline, each prioritized 128b packet arriving at 100Mpackets/s is queued and scheduled autonomously in a self-timed manner.

8.2 A 51mW 1.6GHz On-Chip Network for Low-Power Heterogeneous SoC Platform

9:00 AM

K. Lee, S-J. Lee, S-E. Kim, H-M. Choi, D. Kim, S. Kim, M-W. Lee, H-J. Yoo
KAIST, Daejeon, Korea

A 1.6GHz on-chip network integrating two processors, memories, and an FPGA provides 11.2GB/s bandwidth in 0.18μm 6M CMOS technology. The 2-level hierarchical star-connected network using serialized low-energy transmission coding, crossbar partial activation and low-swing signaling dissipates 51mW at 1.6V supporting globally asynchronous, locally synchronous mode and programmable clocking.

8.3 Low-Voltage-Swing Logic Circuits for a 7GHz X86 Integer Core

9:30 AM

D. Deleganes, M. Barany, G. Geannopoulos, K. Kreitzer, A. Singh, S. Wijeratne
Intel, Hillsboro, OR

Pentium®4 processor architecture uses a 2x core clock to implement low latency integer operations. Low-voltage-swing logic circuits in 90nm technology meet the frequency demands of a 3rd generation integer core, with operation demonstrated for frequencies in excess of 7GHz.

BREAK 10:00 AM

8.4 Ultra-Low Voltage Circuits and Processor in 180nm to 90nm Technologies with a Swapped-Body Biasing Technique

10:15 AM

S. Narendra, J. Tschanz, J. Hofsheier, B. Bloechel, S. Vangal, Y. Hoskote, S. Tang, D. Somasekhar, A. Keshavarzi, V. Erraguntla, G. Dermer, N. Borkar, S. Borkar, V. De
Intel, Hillsboro, OR

A low-voltage swapped-body biasing technique where PMOS bodies are connected to ground and NMOS bodies to Vcc is evaluated. Measurements show more than 2.6x frequency improvement at 0.5V Vcc and the ability to reduce Vcc by 0.2V for the same frequency compared to no body bias in 180 to 90nm CMOS technologies.

8.5 Mixed Body-Bias Techniques with Fixed V_t and I_{ds} Generation Circuits

10:45 AM

M. Sumita, S. Sakiyama, M. Kinoshita, Y. Araki, Y. Ikeda, K. Fukuoka
Matsushita Electric Industrial, Nagaokakyou, Japan

In sub-1V CMOS VLSIs, body-bias generation circuits are proposed in which I_{ds} and V_t of PMOS/NMOS are always fixed. The mixed body bias techniques result in positive temperature dependence of the delay, an 85% reduction of the delay variation, and a 75% improvement in the power consumption of an SRAM on a mobile processor.

8.6 An On-Chip Active Decoupling Circuit to Suppress Crosstalk in Deep Sub-micron CMOS Mixed-Signal SoCs

11:15 AM

T. Tsukada, Y. Hashimoto, K. Sakata, H. Okada, K. Ishibashi
STARC, Yokohama, Japan

A decoupling circuit using an op-amp is proposed to suppress noise coupling in mixed-signal SoCs. It solves the parasitic inductance problem of on-chip capacitor decoupling. A 0.13μm CMOS test chip shows that substrate noise at 40MHz to 1GHz is suppressed by each circuit operating at 3.3mA and 1V. These circuits reduce noise by 68% at 200MHz.

8.7 A 4GHz 300mW 64b Integer Execution ALU with Dual Supply Voltages in 90nm CMOS

11:45 AM

S. Mathew, M. Anders, B. Bloechel, T. Nguyen, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

A 64b integer execution ALU is described for 4GHz single-cycle operation with a 32b mode ALU latency of 7GHz. The 0.073mm^2 chip is fabricated in a 90nm dual-V_t CMOS technology and dissipates 300mW. Sparse-tree adder architecture, single-rail dynamic circuits, and a semi-dynamic implementation enable a 20% performance improvement and a 56% energy reduction compared to a Kogge-Stone implementation.

CONCLUSION 12:15 PM

GBIT-TRANSCEIVERS

Chair: **Yuriy Greshishchev,** *PMC-Sierra, Kanata, Canada*
Associate Chair: **Vadim Gutnik,** *Consultant, Irvine, CA*

9.1 A Low-Jitter 16:1 MUX and a High-Sensitivity 1:16 DEMUX with Integrated 39.8 to 43GHz VCO for OC768 Communication Systems

8:30 AM

K. Watanabe, A. Koyama, T. Harada, R. Satomura, T. Aida, A. Ito, T. Murata, H. Yoshioka, M. Sonehara, K. Ishikawa, M. Ito, T. Masuda, N. Shiramizu, K. Ohhata, F. Arakawa, T. Kusunoki, H. Chiba, T. Kurihara, M. Kuraishi
Hitachi, Tokyo, Japan

A fully integrated 39.8 to 43Gb/s OC768 16:1 MUX/DEMUX chipset is implemented in a 0.18μm BiCMOS process. Full-rate operation is realized with an on-chip VCO, and the chipset dissipates 11.6W. The measured output jitter of the packaged MUX is 714fs, and the sensitivity of DEMUX is $31mV_{pp}$ single-ended with a BER $<10^{-12}$.

9.2 An 800mW 10Gb Ethernet Transceiver in 0.13μm CMOS

9:00 AM

S. Sidiropoulos, N. Acharya, P. Chau, J. Dao, A. Feldman, H-J. Liaw, R. Narayanaswami, M. Loinaz, C. Portmann, S. Rabii, A. Salleh, S. Sheth, L. Thon, K. Vleugels, P. Yue, D. Stark
Aeluros, Mountain View, CA

A fully integrated 10Gb Ethernet transceiver IC using a standard 0.13μm CMOS process integrates 10.3Gb/s and 4x3.12Gb/s analog front-ends, with Layer-1 coding and management functionality. The 2.5x5mm^2 IC exceeds both 10GE and SONET specifications, and dissipates 800mW from its 1.2/2.5V supplies.

9.3 A Fully Integrated 0.13μm CMOS 10Gb Ethernet Transceiver with XAUI Interface

9:30 AM

H-R. Lee[1], M-S. Hwang[1], B-J. Lee[1], Y-D. Kim[1], D. Oh[1], J. Kim[1], D-K. Jeong[1], W. Kim[1], S-H. Lee[2]
[1]Seoul National University, Seoul, Korea
[2]Silicon Image, Sunnyvale, CA

A 10Gb Ethernet transceiver chip integrated with 10Gb/s serial and quad 3.125Gb/s XAUI interfaces is implemented in 0.13μm CMOS and consumes 970mW from 1.2V. A digital coarse control algorithm for VCOs reduces the VCO gains for noise immunity. A blind oversampling technique enables synthesis of the XAUI interface.

BREAK 10:00 AM

9.4 A 10Gb/s SONET-Compliant CMOS Transceiver with Low Cross-Talk and Intrinsic Jitter

10:15 AM

H. Werker[1], S. Mechnig[1], C. Holuigue[1], C. Ebner[1], E. Romani[1], F. Roger[1], G. Mitteregger[1], T. Blon[1], M. Moyal[1], M. Vena[1], A. Melodia[1], J. Fisher[1], G. Le Grande de Mercey[2], H. Geib[1]
[1]Xignal Technologies, Unterhaching, Germany
[2]Universität der Bundeswehr, Munich, Germany

A single-chip full-rate transceiver in 0.13μm standard CMOS consumes less than 1W. By using a special power-supply concept and a notched high-Q inductor in the VCO, the IC achieves a 0.2ps rms jitter. A limiting amplifier with a sensitivity of 20mV at 7GHz BW enables the CDR to recover data with a BER of $<10^{-12}$.

9.5 A 12.5Gb/s BER Test Using a Jitter-Tolerant Parallel CDR

10:45 AM

Y. Ohtomo, T. Kawamura, K. Nishimura, M. Nogawa, M. Togashi, H. Koizumi
NTT, Atsugi, Japan

Implemented in a 0.13μm CMOS process, pulse pattern generation and BER test functions are integrated in a chip. A parallel CDR circuit provides 12.5Gb/s operation and wide tolerance of over 0.5UIpp for 4 to 80MHz sinusoidal jitter.

9.6 A Quad-Channel 3.125Gb/s/ch Serial-Link Transceiver with Mixed-Mode Adaptive Equalizer in 0.18μm CMOS

11:15 AM

J. Yang[1], J. Kim[2], S. Byun[1], C. Conroy[1], B. Kim[1]
[1]Berkana Wireless, Campbell, CA
[2]KAIST, Daejon, Korea

A quad-channel serial-link transceiver provides 12.5Gb/s full duplex raw data rate for a single 10Gb XAUI interface. A mixed-mode LMS adaptive equalizer is adopted, which achieves 3dB SNR improvement over pre-emphasis techniques. A delay-immune CDR circuit recovers the receive clock with 64ps-pp jitter. The IC consumes 718mW at 3.125Gb/s/ch with full duplex data rate.

9.7 A 20GHz VCO with 5GHz Tuning Range in 0.25μm SiGe BiCMOS

11:45 AM

B. Jung, R. Harjani
University of Minnesota, Minneapolis, MN

This paper presents a 20GHz VCO with 5GHz tuning range in 0.25μm SiGe BiCMOS. A differential capacitive emitter degenerated structure is used as a negative resistance cell that has extremely low parasitic capacitance. The VCO core consumes 9mW, and the measured phase noise at 1MHz offset is -101.2dBc/Hz.

CONCLUSION 12:00 PM

CELLULAR SYSTEMS AND BUILDING BLOCKS

Chair: **Jacques Rudell,** *Berkana Wireless, Campbell, CA*
Associate Chair: **Charles Chien,** *G-Plus, Santa Monica, CA*

10.1 A Digital-IF WCDMA Handset Transmitter IC in 0.25μm SiGe BiCMOS

8:30 AM

V. Leung, L. Larson, P. Gudem
University of California, La Jolla, CA

A 1.8x2.2mm^2 WCDMA handset transmitter IC reduces power consumption by employing a high-order-hold DAC, an adaptively-biased mixer, and an RF VGA. Implemented in a 0.25μm SiGe BiCMOS process, the IC consumes 58mA at maximum output power of 3.5dBm, and 41mA at reduced output from a 3V supply.

10.2 An Analog GFSK Modulator in 0.35μm CMOS

9:00 AM

H. Darabi, B. Ibrahim, A. Rofougaran
Broadcom, Irvine, CA

An analog GFSK modulator designed in 0.35μm CMOS consumes 600μA from a 3V supply and realizes an analog implementation of the FM differential equation. The modulator operates at base-band and is integrated in a direct-conversion Bluetooth transmitter. The circuit achieves a frequency deviation of 160kHz with better than ±3% accuracy.

10.3 Quad-band GSM/GPRS/EDGE Polar Loop Transmitter

9:30 AM

T. Sowlati[1], D. Rozenblit[1], E. Mccarthy[1], M. Damgaard[1], R. Pullela[1], D. Koh[1], D. Ripley[2]
[1]Skyworks, Irvine, CA
[2]Skyworks, Cedar Rapids, IA

A 0.35μm BiCMOS 8x10mm^2 EDGE transmitter module with a non-linear GSM type PA uses a dual feedback loop to ensure robust performance even under VSWR variations. No isolator or external PA filtering is required. The EDGE spectral mask is met with an rms EVM below 4% and an ACPR of -60dBc at 400kHz offset at 29dBm 2dB output power.

BREAK 10:00 AM

10.4 A 1.5V 28mA Fully Integrated Fast-Locking Quad-Band GSM-GPRS Transmitter with Digital Auto-Calibration in 0.13μm CMOS

10:15 AM

S. Lee[1], S. Fang[1], D. Allstot[1], A. Bellaouar[2], A. Fridi[2], P. Fontaine[2]
[1]University of Washington, Seattle, WA
[2]Texas Instruments, Dallas, TX

A 1.5V 28mA quad-band GSM-GPRS transmitter with digital auto-calibration is implemented in 2.1mm^2 using a 0.13μm CMOS process. It achieves a lock time of 43μs, GSM receive band phase noise of -158dBc/Hz and -165dBc/Hz for the high- and low-bands, respectively, and reference feed through less than -95dBc.

10.5 A Polar Modulator For EDGE

10:45 AM

M. Elliott[1], T. Montalvo[2], F. Murden[1], B. Jeffries[1], J. Strange[3], S. Atkinson[3], A. Hill[1], S. Nandipaku[4], J. Harrebek[5]
[1]Analog Devices, Greensboro, NC
[2]Analog Devices, Raleigh, NC
[3]Analog Devices, Kent, United Kingdom
[4]Analog Devices, Wilmington, MA
[5]Analog Devices, Aalborg, Denmark

This 0.5μm SiGe BiCMOS polar modulator IC adds EDGE transmit capability to a GSM transceiver IC without any RF filters. The modulator achieves phase noise of -152 dBc/Hz and -164 dBc/Hz at 10MHz and 20MHz, respectively, with a measured EVM of 3%. The IC consumes 55mA and 75mA with 2.7V to GSM and EDGE, respectively.

10.6 A 10μs Fast Switching PLL Synthesizer for GSM/EDGE Base-Stations

11:15 AM

M. Keaveney[1], P. Walsh[1], M. Tuthill[1], C. Lyden[2], B. Hunt[1]
[1]Analog Devices, Limerick, Ireland
[2]Analog Devices, Cork, Ireland

A fractional-N PLL synthesizer with 10μs lock time, 0.25° rms phase error, and -100dBc/Hz in-band phase noise suitable for GSM/EDGE base-stations is implemented in 2.29x2.32mm² using a 0.35μm BiCMOS process. Up/down mismatch from the PFD to the differential charge pump's outputs is eliminated via a chopping scheme that permits full use of bandwidth switching.

10.7 A VSWR-Protected Silicon Bipolar PA with Smooth Power-Control Slope

11:45 AM

A. Scuderi[1], A. Scuderi[2], F. Carrara[1], G. Palmisano[1]
[1]University of Catania, DIEES, Catania, Italy
[2]STMicroelectronics, Catania, Italy

A 1.8GHz silicon bipolar PA is presented. A protection circuit enables the amplifier to sustain a 10:1 load VSWR at 5V supply despite a low BV_{ceo} of 6.5V. A temperature-compensated bias network allows a moderate power-control slope of less than 80dB/V. A 50% PAE is attained at a 33.8dBm output power level. The 1.2x1.5mm² die is implemented in 0.8μm BiPMOS.

10.8 A Small GSM Power Amplifier Module Using Si-LDMOS Driver MMIC

12:00 PM

T. Shimizu[1], Y. Nunogawa[2], T. Furuya[1], S. Yamada[2], I. Yoshida[1], M. Hotta[1]
[1]Renesas Technology, Takasaki, Japan
[2]Renesas Technology, Komoro, Japan

A small quad-band Si-MOS high-power amplifier module with a package size of 8x8mm² includes a driver MMIC in an LDMOS process and provides a built-in power control loop employing a current-sense method. The IC achieves 53% power efficiency at 35dBm output power over the 824 to 915MHz GSM band using a 3.6V supply.

CONCLUSION 12:15 PM

DRAM

Chair: **Katsuyuki Sato,** *Elpida Memory, Tokyo, Japan*
Associate Chair: **Martin Brox,** *Infineon, Munich, Germany*

11.1 A 0.6V 205MHz 19.5ns tRC 16Mb Embedded DRAM

8:30 AM

K. Hardee[1], O. Jones[1], D. Butler[1], M. Parris[1], M. Mound[1], H. Calendar[1], G. Jones[1], C. Gruenschlaeger[1], M. Miyabayashi[2], K. Taniguchi[2], T. Arakawa[2]
[1]United Memories, Colorado Springs, CO
[2]Sony, Tokyo, Japan

A 0.6V 16Mb embedded DRAM macro is presented as a solution for mobile personal consumer applications. The macro has 128 separate I/Os and employs positive and negative on-chip body bias, boosted and staggered power gating, and Vcc/2 sensing to achieve 205MHz operation with 19.5ns tRC and 39mW operating power.

11.2 A 312MHz 16Mb Random-Cycle Embedded DRAM Macro with 73μW Power-Down Mode for Mobile Applications

9:00 AM

F. Morishita[1], I. Hayashi[1], H. Matsuoka[1], K. Takahashi[1], K. Shigeta[1], T. Gyohten[1], M. Niiro[1], M. Okamoto[2], A. Hachisuka[1], A. Amo[1], H. Shinkawata[1], T. Kasaoka[1], K. Dosaka[1], K. Arimoto[1]
[1]Renesas Technology, Itami, Japan
[2]Daioh Electric, Itami, Japan

An embedded DRAM macro with self-adjustable timing control and a power-down data retention scheme is described. A 16Mb test chip is fabricated in a 0.13μm low-power process and it achieves 312MHz random cycle operation. Data retention power is 73μW, which is 5% compared to a conventional one.

11.3 A 500MHz Multi-Banked Compilable DRAM Macro with Direct Write and Programmable Pipelining

9:30 AM

J. Barth, J. Dreibelbis, D. Anand, J. Fifield, K. Gorman, M. Nelms, G. Pomichter, D. Pontius
IBM, Essex Junction, VT

A 500MHz compiled DRAM macro fabricated in 90nm logic-based process is presented. The random bank cycle is reduced by 50% over the previous generation through segmentation and a direct write scheme. 500MHz operation is achieved with a configurable 4-stage pipeline.

11.4 An 800MHz Embedded DRAM with a Concurrent Refresh Mode

9:45 AM

T. Kirihata, P. Parries, D. Hanson, H. Kim, J. Golz, G. Fredeman, R. Rajeevakumar, J. Griesemer, N. Robson, A. Cestero, M. Wordeman, S. Iyer
IBM Microelectronics, Hopewell Junction, NY

The embedded DRAM employs a transfer gate formed from a 22A Gox, 1.5V logic IO device resulting in 3.2ns cycle and latency. A concurrent refresh mode and a refresh scheduler prove ≥99% memory availability for a 64μs cell retention time. In-macro circuitry supports redundancy allocation during 800MHz multi-banking operation.

BREAK 10:00 AM

11.5 A 143MHz 1.1W 4.5Mb Dynamic TCAM with Hierarchical Searching and Shift Redundancy Architecture

10:15 AM

H. Noda[1], K. Inoue[1], M. Kuroiwa[1], A. Amo[1], A. Hachisuka[1], H. Mattausch[2], T. Koide[2], S. Soeda[1], K. Dosaka[1], K. Arimoto[1]
[1]Renesas Technology, Itami, Japan
[2]Hiroshima University, Hiroshima, Japan

A 4.5Mb dynamic ternary CAM (DTCAM) is designed in 0.13μm embedded DRAM technology. A performance of 143M searches/sec is achieved at a power dissipation of 1.1W and on a small silicon area of 32mm^2. A 3.6-times yield improvement is estimated by employing pipelined hierarchical searching and row/column-shift redundancy.

11.6 A 1.6Gb/s Double-Data-Rate SDRAM with Wave-Pipelined CAS Latency Control

10:45 AM

S-B. Lee, S-J. Jang, J-S. Kwak, S-J. Hwang, S-H. Cho, M-S. Park, H-H. Lee, W-J. Lee, Y-R. Lee, Y-C. Cho, H-J. Heo, W-H. Shin, S-J. Kim, Y-U. Jang, S-W. Hwang, Y-H. Jun, S-I. Cho
Samsung Electronics, Hwasung, Korea

An 8Mx32 graphic DDR (GDDR) SDRAM operating at 800MHz is introduced. It needs a large number of CAS latencies(CLs) to support the frequency range of 300 to 800MHz. A wave-pipelined CL control circuit is proposed to provide stable operation for the wide number of CLs. The gapless write-to-read scheme is applied to improve the efficiency of the data bus at high-speed operation with large number of CLs.

11.7 1.4Gb/s DLL Using 2nd Order Charge-Pump Scheme for Low Phase/Duty Error for High-Speed DRAM Application

11:15 AM

K-H. Kim, J-B. Lee, W-J. Lee, B-H. Jeong, G-H. Cho, J-S. Lee, G-S. Byun, C. Kim, Y-H. Jun, S-I. Cho
Samsung Electronics, Hwasung, Korea

A technique for reducing phase error of DLL/PLL due to non-ideal characteristics of the charge pump is proposed. It makes the output of the charge pump virtually grounded to eliminate the current mismatch and to seamlessly convert the locking information into digital form. A DLL is designed and fabricated to exhibit duty-cycle corrector performance with the speed of 1.4Gb/s.

11.8 A 2Gb/s Point-to-Point Heterogeneous Voltage-Capable DRAM Interface for Capacity-Scalable Memory Subsystems

11:45 AM

R. Mooney[1], J. Kennedy[1], R. Ellis[1], J. Jaussi[1], S. Borkar[1], J-H. Choi[2], J-K. Kim[2], C-K. Kim[2], W-S. Kim[2], C-H. Kim[2], S-I. Cho[2], S. Loeffler[3], J. Hoffmann[3], W. Hokenmaier[3], R. Houghton[3], T. Vogelsang[3]
[1]Intel, Hillsboro, OR
[2]Samsung Electronics, Hawsung, Korea
[3]Infineon, Williston, VT

We describe a DRAM interface operating at 2Gb/s/pin. It utilizes simultaneous bidirectional signaling in a daisy-chained, point-to-point configuration to enable scalable memory subsystems, and also provides direct attach capability for logic devices. We present results from a system using both logic and DRAM test-chips.

CONCLUSION 12:15 PM

BIOMICROSYSTEMS

Chair: **Dennis Polla,** *University of Minnesota, Minneapolis, MN*
Associate Chair: **Ralph Etienne-Cummings,** *John Hopkins University, Baltimore, MD*

12.1 A Retinal Prosthesis

1:30 PM

W. Liu[1], M. Humayun[2]
[1]University of California, Santa Cruz, CA
[2]University of Southern California, Los Angeles, CA

A prosthesis device is designed to replace the functionality of defective photoreceptors in patients suffering from Retinitis Pigmentosa and age-related Macula Degeneration. The circuit designs include a telemetry link used for power transmission and a bidirectional data communication bus. The 28.9mm^2 IC dissipates 50mW and is fabricated in 1.2μm technology. Experimental results on human subjects are included.

12.2 A Fully Electronic DNA Sensor with 128 Positions and In-Pixel A/D Conversion

2:00 PM

M. Schienle, A. Frey, F. Hofmann, B. Holzapfl, C. Paulus, P. Schindler-Bauer, R. Thewes
Infineon Technologies, Munich, Germany

A 16x8 CMOS sensor array for fully electronic DNA detection is presented. Each position contains a complete A/D converter with a dynamic range of five decades. The 3σ-homogeneity of the electrical response of the sensor array is better than 6% (10^{-11}A to 10^{-7}A). The 28.8mm^2 IC is fabricated in a 0.5μm 2M CMOS process extended to form Au sensors.

12.3 A 0.18μm CMOS 10^{-6}lux Bioluminescence Detection SoC

2:30 PM

H. Eltoukhy, K. Salama, A. El Gamal, M. Ronaghi, R. Davis
Stanford University, Stanford, CA

A chip comprising a 8x16 pseudo-differential pixel array, 128-channel 13b ADC and column-level DSP is fabricated in a 0.18μm CMOS process. Detection of 10^{-6}lux at 30s integration time is achieved via on-chip background subtraction, correlated multiple sampling and averaged 128 13b digitizations/readout. The IC is 25mm^2 and contains 492k transistors.

BREAK 3:00 PM

12.4 Capacitive Sensor Array for Localization of Bioparticles in CMOS Lab-on-a-chip

3:15 PM

A. Romani[1], N. Manaresi[2], L. Marzocchi[1], G. Medoro[2], A. Leonardi[1], L. Altomare[1], M. Tartagni[1], R. Guerrieri[1]
[1]University of Bologna, Bologna, Italy
[2]Silicon Biosystems, Bologna, Italy

Fully-electronic detection of cells and microbeads is achieved on a 320x320 array of capacitive sensors in 0.35μm 2P3M CMOS technology that also integrates particle actuation by dielectrophoresis. Particle-associated equivalent input capacitance variations larger than 0.42fF are measured with 39dB SNR. Output noise is ≤1.6mV, the resolution of the 12b ADC.

12.5 A Modular 32-Site Wireless Neural Stimulation Microsystem

3:45 PM

M. Ghovanloo, K. Najafi
University of Michigan, Ann Arbor, MI

A modular 32-site wireless neural stimulation microsystem is described. Up to 64 modules (2 per chip) can operate in parallel, while receiving inductive power and data at 2.5Mb/s from a 5/10MHz FSK carrier. The 4x4mm^2 chip, fabricated in a 5V, 1.5μm 2M2P CMOS process, generates up to 65.8kpulses/s. Each module dissipates 8.25mW.

12.6 A Power-efficient Voltage-based Neural Tissue Stimulator with Energy Recovery

4:15 PM

S. Kelly, J. Wyatt
Massachusetts Institute of Technology, Cambridge, MA

A voltage-based neural stimulator for an implant is fabricated in 1.5μm CMOS. Wireless power transmission and synchronous rectification allow the use of a set of intermediate voltage supplies. This system achieves power consumption 42% lower than traditional current-source stimulators delivering the same charge to electrodes.

CONCLUSION 4:30 PM

HIGH-SPEED DIGITAL AND MULTI Gb/s I/O

Chair: **Mehmet Soyuer,** *IBM, Yorktown Heights, NY*
Associate Chair: **Herbert Knapp,** *Infineon, Munich, Germany*

13.1 110Gb/s Multiplexing and Demultiplexing ICs

1:30 PM

Y. Suzuki[1], Y. Amamiya[1], Z. Yamazaki[1], S. Wada[1], H. Uchida[2], C. Kurioka[2], S. Tanaka[1], H. Hida[1]
[1]NEC, Tsukuba, Japan
[2]NEC, Kawasaki, Japan

A 120Gb/s multiplexer and a 110Gb/s demultiplexer are implemented in an InP HBT process. They feature a direct drive series-gating configuration selector, an asymmetrical latch flip-flop, and broadband impedance matching with inverted micro-strip lines. Their input sensitivity is less than 100mVpp, and the output swing is more than 400mVpp.

13.2 Under 0.5W 50Gb/s Full-Rate 4:1 MUX and 1:4 DEMUX in 0.13μm InP HEMT Technology

2:00 PM

T. Suzuki, T. Takahashi, K. Makiyama, K. Sawada, Y. Nakasha, T. Hirose, M. Takikawa
Fujitsu, Atsugi, Japan

50Gb/s full-rate 4:1 MUX and 1:4 DEMUX ICs are fabricated in an InP HEMT technology. The MUX has an rms jitter of 283fs and a peak-to-peak jitter of 1.78ps. The DEMUX has a phase margin of 250° and a sensitivity of 80mV at 40Gb/s. The MUX and DEMUX consume 450mW and 490mW from a -1.5V supply, respectively.

13.3 A 108Gb/s 4:1 Multiplexer in 0.13μm SiGe-Bipolar Technology

2:30 PM

M. Meghelli
IBM, Yorktown Heights, NY

A 4:1 multiplexer implemented in a 210GHz f_T 0.13μm SiGe-bipolar technology and operating beyond 100Gb/s is reported. Control of on-chip clock distribution is critical to achieve such data rate. The chip consumes 1.45W from a -3.3V supply and exhibits less than 340fs rms jitter on the output data.

13.4 A 43Gb/s 2:1 Selector IC in 90nm CMOS Technology

2:45 PM

T. Yamamoto[1], M. Horinaka[1], D. Yamazaki[1], H. Nomura[2], K. Hashimoto[2], H. Onodera[1]
[1]Fujitsu, Kawasaki, Japan
[2]Fujitsu, Akiruno, Japan

The 2:1 selector IC consists of three stages of input buffers, a 2:1 selector stage, and two stages of output buffers. By using multiple inductive peaking and selector architecture to suppress interference, the proposed circuit operates at a data rate of 43Gb/s and it is implemented in 90nm CMOS technology with 48nm transistors.

BREAK 3:00 PM

13.5 A 25GHz Clock Buffer and a 50Gb/s 2:1 Selector in 90nm CMOS

3:15 PM

D. Yamazaki, T. Yamamoto, M. Horinaka, H. Nomura, K. Hashimoto, H. Onodera
Fujitsu, Kawasaki, Japan

A 25GHz clock buffer and 50Gb/s 2-to-1 selector, implemented in 90nm CMOS using 48nm transistors, operate off a 1V supply. An inductor-peaked CMOS inverter for the clock buffer is employed. The selector is equipped with a tail transistor whose gate is switched by the rail-to-rail clock signal produced by the buffer.

13.6 An 8Gb/s Capacitive-Coupled Receiver with High Common-Mode Rejection for Un-Coded Data

3:30 PM

X. Maillard, M. Kuijk
Vrije Universiteit, Brussels, Belgium

An 8Gb/s differential receiver is demonstrated in 0.35μm SiGe with on-chip 60fF capacitors for AC-coupling that allows uncoded data transmission for a common-mode input range of ±690V, with input sensitivity of 0.5 to 1.1Vpp. It especially resists to strong common-mode edges of 4V/ns for enhanced EMI rejection.

13.7 A 2Gb/s 2-tap DFE Receiver for Multi-Drop Single-Ended Signaling Systems with Reduced Noise

3:45 PM

S. Bae, H. Chi, Y. Sohn, H. Park
Pohang University of Science and Technology, Pohang, Korea

A 2Gb/s integrating 2-tap decision feedback equalizer receiver is implemented in a 0.25μm CMOS process to reduce high-and-low frequency noise for multi-drop single-ended signaling system. Voltage margin is enhanced by 110%(90%) for a stubless channel at 2Gb/s (an SSTL channel at 1.2Gb/s).

13.8 An 8Gb/s Source-Synchronous I/O Link with Adaptive Receiver Equalization, Offset Cancellation, and Clock Deskew

4:15 PM

J. Jaussi[1], G. Balamurugan[2], D. Johnson[1], B. Casper[1], A. Martin[1], J. Kennedy[1], R. Mooney[1], N. Shanbhag[1]
[1]Intel, Hillsboro, OR
[2]University of Illinois, Urbana, IL

An 8Gb/s binary source-synchronous I/O link with adaptive receiver-equalization, offset cancellation and clock deskew is implemented in 0.13μm CMOS. The analog equalizer is implemented as an 8-way interleaved, 4-tap discrete-time linear filter. On-die adaptation logic determines optimal receiver settings.

13.9 A 4Gb/s/pin 4-Level Simultaneous Bi Directional IO Using a 500MHz Clock for High-Speed Memory

4:45 PM

J-H. Kim[1], S-A. Kim[1], W-S. Kim[1], J-H. Choi[1], C. Kim[1], S-I. Cho[1], S. Kim[2]
[1]Samsung Electronics, Hwasung, Korea
[2]Korea University, Seoul, Korea

A simultaneous 4-level bidirectional I/O interface for high-speed DRAM is presented. It performs at a data rate of 4Gb/s/pin with the use of a 500MHz clock generator and a full CMOS power rail swing. This I/O interface is fabricated on a 0.10μm DRAM CMOS process in 330x66μm^2. The transceiver performs 200mVx690ps passing eye-windows on the channel over 1.8V supply.

CONCLUSION 5:15 PM

SESSION 14 SALON 8

HIGH-SPEED A/D CONVERTERS

Chair: **Robert Neff,** *Agilent Laboratories, Palo Alto, CA*
Associate Chair: **Krishnaswamy Nagaraj,** *Texas Instruments, Warren, NJ*

14.1 A 1.8V 1.6GS/s 8b Self-Calibrating Folding ADC with 7.26 ENOB at Nyquist Frequency

1:30 PM

R. Taft, C. Menkus, R. Tursi, O. Hidri, V. Pons
National Semiconductor, Fuerstenfeldbruck, Germany

A 1.8V folding-interpolating ADC in 0.18μm CMOS uses small device sizes to achieve a conversion rate exceeding 1.6GS/s. The inherent mismatch offsets are calibrated transparently, and at 1.6GS/s the ADC achieves 0.15LSB DNL, 0.35LSB INL, 7.5 ENOB at 100MHz input, and 7.26 ENOB at Nyquist.

14.2 An 8b 600MS/s 200mW CMOS Folding ADC using Amplifier Preset

2:00 PM

G. Geelen, E. Paulus
Philips Semiconductors, Eindhoven, The Netherlands

An 8b CMOS folding ADC with resistive averaging and interpolation exhibits 7.5 ENOB and a maximum sample frequency of 600MS/s while dissipating only 200mW. The ADC utilizes preset switches at the outputs of the pre-amplifiers. Chip area is 0.2mm^2, and supply voltage is 3.3/1.8V in 0.35/0.18μm CMOS.

14.3 A 1.2V 220MS/s 10b Pipeline ADC Implemented in 0.13μm Digital CMOS

2:30 PM

B. Hernes, A. Briskemyr, T. Andersen, F. Telstø, T. Bonnerud, Ø. Moldsvor
Nordic VLSI, Trondheim, Norway

A 10b pipeline ADC fabricated in a 0.13μm pure digital CMOS process is presented. The supply voltage is 1.2V and the conversion rate is 120MS/s. The ADC maintains its performance down to 0.9V supply voltage and up to 220MS/s at a signal swing near full scale ($1V_{p-p}$). Power consumption at 220MS/s is 135mW.

BREAK 3:00 PM

14.4 A 150MS/s 8b 71mW Time-Interleaved ADC in 0.18μm CMOS

3:15 PM

S. Limotyrakis, S. Kulchycki, D. Su, B. Wooley
Stanford University, Stanford, CA

A 150MS/s 8b time-interleaved ADC has been built in 0.18μm CMOS. Segmentation of the track-and-hold into separate circuits driving the 1st stage comparators and two interleaved residue paths, together with signal scaling, results in a 45.4dB SNDR for an 80MHz input frequency, while dissipating 71mW from a 1.8V supply.

14.5 A 21mW 8b 125MS/s ADC Occupying 0.09mm² in 0.13μm CMOS

3:45 PM

J. Mulder[1], C. Ward[1], C-H. Lin[1], D. Kruse[2], J. Westra[1], M. Lugthart[1], E. Arslan[1], R. van de Plassche[1], K. Bult[1], F. van der Goes[1]
[1]Broadcom, Bunnik, The Netherlands
[2]Broadcom, Irvine, CA

An 8b subranging ADC uses interpolation, averaging, offset compensation and pipelining techniques to accomplish 7.6b ENOB at 125MS/s. The 0.13μm CMOS ADC occupies 0.09mm² and consumes 21mW.

14.6 A 3b 40GS/s ADC-DAC in 0.12μm SiGe

4:15 PM

W. Cheng, W. Ali, M-J. Choi, K. Liu, T. Tat, D. Devendorf, L. Linder, R. Stevens
TelASIC Communications, El Segundo, CA

A 3b SiGe ADC-DAC produces a conversion rate of 40GS/s with >20dB dynamic range over 12GHz bandwidth for receiver exciter applications. The 40GHz design and test methodology, as well as a new wideband quantizer front end, are described.

14.7 A 6b 500MHz 10mW ADC Array in 90nm Digital CMOS

4:45 PM

D. Draxelmayr
Infineon Technologies, Villach, Austria

A 6b converter array operates at a 500MHz clock frequency with input signals up to 500MHz and only 10mW power consumption. The array consists of 8 interleaved successive approximation converters implemented in a 90nm digital CMOS technology.

CONCLUSION 5:00 PM

Sunday, February 15th		**ISSCC 2004 TUTORIALS**				
	8:00 AM	T1: Tuning Analog Parameters T2: Wireless LAN Radio Design T3: Automotive Electronics T4: Introduction to PLL and DLL Design for Digital Systems			T5: Specsmanship in Imagers T6: Design for Testability in Embedded Memories T7: The Reality and Promise of Reconfigurable Computing in Signal Processing	
		GIRAFE FORUM			**MEMORY FORUM**	
	8:30 AM	F1: RF Power Amplifiers (Salon 7)			F2: Non-Volatile Memories Technology and Design (Golden Gate Hall)	
		ISSCC 2004 SPECIAL-TOPIC EVENING SESSIONS				
	7:30 PM	SE1: Architectures and Circuits for Ultra Wideband Radio (Salon 9)		SE2: CMOS Meets BIO (Salon 8)		SE3: Highlights of DAC (Salon 7)
Monday, February 16th		**ISSCC 2004 PAPER SESSIONS**				
	8:30 AM	Session 1: Plenary Session (Salons 7-9)				
	1:30 PM	Session 2: Non-Volatile Memory (Salon 1-6)	Session 3: Processors (Salon 7)	Session 4: Oversampled ADCs (Salon 8)	Session 5: WLAN Transceivers (Salon 9)	Session 6: Imaging (Salon 10-15)
	5:15 PM	Author Interviews; Social Hour; Poster Session (DAC Student Design Contest Winners) (Golden Gate Hall)				
		ISSCC 2004 DISCUSSION SESSIONS				
	8:00 PM	E1: To UWB or Not To Be? (Salon 9)		E2: Is the Golden Age of Analog Circuit Design Over? (Salon 8)		SE4: Circuits and Electronics for Organic Electronics (Salon 7)
Tuesday, February 17th		**ISSCC 2004 PAPER SESSIONS**				
	8:30 AM	Session 7: TD: Scaling Trends (Salon 1-6)	Session 8: Circuits for Digital Systems (Salon 7)	Session 9: Gbit-Transceivers (Salon 8)	Session 10: Cellular Systems and Building Blocks (Salon 9)	Session 11: DRAM (Salon 10-15)

		1:30 PM	Session 12: Biomicrosystems (Salon 1-6)	Session 13: High-Speed Digital and Multi-Gb-I/O (Salon 7)	Session 14: High-Speed A/D Converters (Salon 8)	Session 15: Wireless Consumer ICs (Salon 9)	Session 16: TD: Emerging Technologies and Circuits (Salon 10-15)
		5:15 PM	Author Interviews (Golden Gate Hall)				
			ISSCC 2004 DISCUSSION SESSIONS				
		8:00 PM	SE5: Noise Coupling in Mixed Signal/RF SoCs (Salon 9)		E3: Processors and Performance: When Do GHz Hurt? (Salon 8)		E4: What is the Next Embedded Non-Volatile Memory Technology? (Salon 7)
Wednesday, February 18th			**ISSCC 2004 PAPER SESSIONS**				
8:30 AM	Session 17: MEMs and Sensors (Nob Hill)	8:30 AM	Session 18: Consumer Signal Processing (Salon 1-6)	Session 19: Clock Generation and Distribution (Salon 7)	Session 20: Digital-to-Analog Converters (Salon 8)	Session 21: RF Potpourri (Salon 9)	Session 22: DSL and Multi-Gb/s I/O (Salon 10-15)
		1:30 PM	Session 23: Channel Coding (Salon 1-6)	Session 24: TD: Wireless Trends: Low-Power and 60GHz (Salon 7)	Session 25: High Resolution Nyquist ADCs (Salon 8)	Session 26: Optical and Fast I/O (Salon 9)	Session 27: SRAM (Salon 10-15)
		5:15 PM	Author Interviews (South Grand Assembly)				
	Thursday, February 19th		**ISSCC 20043 SHORT COURSE**				
		8:00 AM	Deep-Submicron Analog and RF Circuit Design (Sessions at 8:00 in Salon 1-6; 10:00 AM in Nob Hill)				
			ATACC FORUM			**MICROPROCESSOR CIRCUIT DESIGN FORUM**	
		8:30 AM	F3: A/D and D/A Building Blocks for Telecom Transceiver Applications (Golden Gate Hall)			F4: Managing Variability in Sub-100nm Designs (Salon 10-15)	

BOOK DISPLAY
Monday, February 16th, 12:00 PM - 8:00 PM (Golden Gate Hall)
Tuesday, February 17th,10:00 AM - 8:00 PM (Golden Gate Hall)
Wednesday, February 18th, 10:00 AM - 5:00 PM (Golden Gate Hall)

WIRELESS CONSUMER ICs

Chair: **John Long,** *Delft University of Technology, Delft, The Netherlands*
Associate Chair: **Bud Taddiken,** *Microtune, Plano, TX*

15.1 A Discrete-Time Bluetooth Receiver in a 0.13μm Digital CMOS Process

1:30 PM

K. Muhammad, D. Leipold, Y-C. Ho, C. Fernando, T. Jung, J. Wallberg, J-S. Koh, S. John, I. Deng, O. Moreira, C-M. Hung, B. Staszewski, V. Mayega, R. Staszewski, K. Maggio
Texas Instruments, Dallas, TX

A discrete-time receiver architecture for a wireless application is presented. Analog signal processing concepts are used to directly sample the RF input at Nyquist rate. Maximum receiver sensitivity is -83dBm, and the 10mm^2 chip consumes a total of 41mA from a 1.575V internally regulated supply. The receiver is implemented in a 0.13μm digital CMOS process.

15.2 A Dual-Mode 802.11b/Bluetooth Receiver in 0.25μm BiCMOS

2:00 PM

A. Emira, A. Valdes-Garcia, B. Xia, A. Mohieldin, A. Valero-Lopez, S. Moon, C. Xin, E. Sanchez-Sinencio
Texas A&M University, College Station, TX

A dual-mode direct-conversion 802.11b/Bluetooth receiver is integrated from LNA to ADC in a 0.25μm BiCMOS process. The baseband circuits are programmable to accommodate both standards while the RF front-end is shared. Die area is 21mm^2, and the IC consumes 45.6/41.3mA (802.11b/Bluetooth). Sensitivity is -86/-91dBm and IIP3 is -13/-13dBm.

15.3 All-Digital Phase-Domain TX Frequency Synthesizer for Bluetooth Radios in 0.13μm CMOS

2:30 PM

B. Staszewski[1], C-M. Hung[1], K. Maggio[1], J. Wallberg[1], D. Leipold[1], P. Balsara[2]
[1]Texas Instruments, Dallas, TX
[2]University of Texas at Dallas, Richardson, TX

An all-digital frequency synthesizer for a single-chip Bluetooth radio is fabricated in 0.13μm CMOS, and operates in a digitally-synchronous phase domain that naturally incorporates wideband GFSK modulation. The synthesizer includes a pulse-shaping TX filter and near class-E PA with digital amplitude control. Close-in phase noise is -86.2dBc/Hz, integrated rms phase noise is 0.9°, and settling time is ≤ 50μs.

BREAK 3:00 PM

15.4 A Multi-Mode 0.3-128kb/s Transceiver for the 433/868/915MHz ISM Bands in 0.25μm CMOS

3:15 PM

P. Quinlan[1], P. Crowley[2], M. Chanca[2], S. Hudson[2], B. Hunt[2], K. Mulvaney[2], G. Retz[2], C. O'Sullivan[2], P. Walsh[2]
[1]Analog Devices, Cork, Ireland
[2]Analog Devices, Limerick, Ireland

A fully integrated ISM-band transceiver in 0.25μm CMOS for low data-rate wireless networks consumes 17mA from a 3V supply in RX mode. At

+10dBm output power, the part consumes 24mA. G/FSK and OOK/ASK modulation formats are supported at data rates from 0.3-128kb/s in the 433/868/915MHz ISM bands.

15.5 A 12GHz Silicon Bipolar Receiver for Digital Satellite Applications

3:45 PM

G. Girlando[1], T. Copani[2], S. Smerzi[1], A. Castorina[1], G. Palmisano[2]
[1]STMicroelectronics, Catania, Italy
[2]University of Catania, Catania, Italy

A 12GHz monolithic silicon bipolar receiver for DVB-S applications is presented. The conversion gain is 33.6dB, SSB NF is 5.9dB, and output P_{-1dB} is +5.5dBm. The VCO exhibits a phase noise of -102dBc/Hz at 100kHz offset from a 5.3GHz carrier. The VCO tuning range is 1.1GHz.

15.6 A Digital Terrestrial Television (ISDB-T) Tuner for Mobile Applications

4:15 PM

S. Azuma, H. Kawamura, S. Kawama, S. Toyoyama, T. Hasegawa, K. Kagoshima, M. Koutani, H. Kijima, K. Sakuno, K. Iizuka
Sharp, Tenri, Japan

A 160mW low-IF single-chip tuner for a mobile ISDB-T receiver is realized in SiGe BiCMOS. Its 25mW variable gain LNA shows 2.7dB NF and 62dB variable gain range. The 20mW switched-capacitor channel selection filter exhibits 80dB out-of-band rejection and 11nV/√Hz input referred noise.

15.7 A 4μA Quiescent Current Dual-Mode Buck Converter IC for Cellular Phone Applications

4:45 PM

J. Xiao[1], A. Peterchev[2], J. Zhang[2], S. Sanders[2]
[1]National Semiconductor, Longmont, CO
[2]University of California, Berkeley, CA

This digitally-controlled buck converter IC occupies 2mm^2 active area in 0.25μm CMOS, and the quiescent current is 4μA, representing more than a 10-fold improvement over traditional analog approaches. Light load efficiency is improved from 25% to 72%. Thus, cellular phone standby time can be extended by almost 3 times.

15.8 Compact Realization of Active Channel-Select Filters in Wireless Receivers

5:00 PM

A. Ismail[1], A. Abidi[2]
[1]Skyworks Solutions, Irvine, CA
[2]University of California, Los Angeles, CA

FDNR-based biquads are better suited to channel-select filter requirements in wireless receivers than other industry-standard biquad implementations. A CMOS implementation of a 5th-order elliptic filter for a zero-IF WCDMA receiver uses 6-times less capacitance than the same filter realized conventionally with identical dynamic range.

CONCLUSION 5:15 PM

TD: EMERGING TECHNOLOGIES AND CIRCUITS

Chair: **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
Associate Chair: **Loke Tan,** *Broadcom, Irvine, CA*

16.1 All-Polymer Thin Film Transistor Fabricated by High-Resolution Inkjet Printing

1:30 PM

T. Shimoda, T. Kawase
Seiko Epson, Suwa-gun, Japan

All-polymer TFTs are developed using an inkjet printing process. Conductive polymer is deposited onto a substrate having a wettability contrast to realize a channel length of 10μm and 500μm width. Polymer integrated circuits and active-matrix backplanes are also developed and their operation demonstrated.

16.2 Cut-and-Paste Organic FET Customized ICs for Application to Artificial Skin

2:00 PM

T. Someya, H. Kawaguchi, T. Sakurai
[1]University of Tokyo, Tokyo, Japan

A flexible, large-area pressure sensor suitable for artificial-skin applications is fabricated using organic transistors and rubbery sensors. Row decoders, column selectors and a pressure-sensitive array comprise the IC. Design customization is introduced by making the circuit scalable and realizing an arbitrary sensor area. Both sensor and circuit use the same sheet of organic circuits, so cutting and pasting with a connecting plastic tape is feasible.

16.3 A Non-Volatile Programmable Solid Electrolyte Nanometer Switch

2:30 PM

T. Sakamoto[1], S. Kaeriyama[2], H. Sunamura[1], M. Mizuno[2], H. Kawaura[1], T. Hasegawa[3], K. Terabe[3], T. Nakayama[3], M. Aono[3]
[1]NEC, Tsukuba, Japan
[2]NEC, Sagamihara, Japan
[3]NIMS, Tsukuba, Japan

A nanometer-scale nonvolatile switch composed of a solid electrolyte is <30nm and has an on-resistance <100Ω. A field programmable logic device and 1kb nonvolatile memory using the switch are demonstrated. The crossbar switch is fabricated in a 1.8V 0.18μm CMOS process.

BREAK 3:00 PM

16.4 A 180mV FFT Processor Using Sub-threshold Circuit Techniques

3:15 PM

A. Wang, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

Minimizing energy requires scaling supply voltages below device thresholds. Logic and memory design techniques allowing sub-threshold operation are developed and demonstrated. The fabricated 1024-pt FFT processor operates down to 180mV using a standard 0.18μm CMOS logic process while using 130nJ/FFT at the optimal operating point.

16.5 Si Nanodevices for Random-Number-Generating Circuits for Cryptographic Security

3:45 PM

S. Fujita, K. Uchida, S-I. Yasuda, R. Ohba, H. Nozaki, T. Tanamoto
Toshiba, Kawasaki, Japan

Small random-number-generating circuits for cryptographic security using Si nano-devices are described. The basis of these circuits is that nano-devices hold random electrical properties naturally that were previously regarded as a negative feature. Results of statistical tests indicate that these circuits generate extremely high-quality random numbers with relatively few transistors.

16.6 Superconducting Quantum Storage and Processing

4:15 PM

M. Amin[1], M. Grajcar[2], E. Il'ichev[3], A. Izmalkov[3], A. van den Brink[1], G. Rose[1], A. Smirnov[1], A. Zagoskin[1]
[1]D-Wave Sys., Vancouver, BC, Canada
[2]Comenius University, Bratislava, Slovakia
[3]IPHT, Jena, Germany

Superposition and entanglement are the two quantum-mechanical effects required to build a quantum computer. Based on these effects, a method for building quantum circuits using superconducting flux quantum bits (qubits) that are inductively coupled to a high quality LC circuit is described.

16.7 A Single-Flux-Quantum Logic Prototype Microprocessor

4:45 PM

M. Tanaka[1], F. Matsuzaki[2], T. Kondo[1], N. Nakajima[2], Y. Yamanashi[2], A. Fujimaki[1], H. Hayakawa[1], N. Yoshikawa[2], H. Terai[3], S. Yorozu[4]
[1]Nagoya University, Nagoya, Japan
[2]Yokohama National University, Yokohama, Japan
[3]Communications Research Laboratory, Kobe, Japan
[4]ISTEC, Tsukuba, Japan

The complete operation of a microprocessor prototype based on the Single-Flux-Quantum (SFQ) logic is described. The 8b SFQ microprocessor, fabricated using niobium Josephson-junction technology, performs computation at a 15.2GHz clock rate with power consumption of 1.6mW. The μP contains 5000 Josephson junctions and 1300 cells on a 5mm^2 IC.

16.8 A 13GHz CMOS Distributed Oscillator Using MEMS Coupled Transmission Lines for Low Phase Noise

5:00 PM

E-C. Park, T-S. Song, S-H. Baek, E. Yoon
KAIST, Daejeon, Korea

A coupled distributed oscillator is designed using low-loss MEMS coupled transmission lines to achieve phase noise improvement of 7dB, and an additional 2dB improvement is attributed to the MEMS transmission lines. The oscillators are fabricated in a 0.18μm 6M CMOS process, operate with a 1V supply and consume 26mW.

CONCLUSION 5:15 PM

SE5: Noise Coupling in Mixed-Signal/RF SoCs
(Salon 9)

Organizer: **David J. Allstot**, Professor, *Dept. of Electrical Engineering, Univ. of Washington, Seattle, WA*

Session Chair: **Raf Roovers**, Research Scientist, *Mixed Signal Circuits and Systems Group, Philips Research Labs, Eindhoven, The Netherlands*

The coupling of switching noise into analog/RF circuits via the substrate, power grids, and interconnects, is a potential "show stopper" for SoC. Even after a decade of intensive research, it is a poorly understood phenomenon. This Special-Topic Evening Session addresses the analysis of noise coupling in SoC designs, and techniques to suppress or eliminate it. Design examples show that the problem is getting worse. The decreased matching performance resulting from relentless device scaling according to Moore's Law demands ever-greater substrate noise suppression. As a radical alternative, consideration is given to architectural and packaging options that avoid the problem completely.

On-chip noise probing circuits and techniques that enable quantitative evaluation of noise generation in digital circuits and coupling strengths within a mixed-signal chip are presented, as are simple ways of modeling digital noise sources and estimating substrate impedances. Designs are often guard-banded even though its effectiveness is uncertain; in some cases, guard rings actually increase noise coupling. A unified CAD approach to analyzing noise coupling using suitable models of the substrate, power grid and package along with techniques to efficiently model switching digital circuits is described.

Even static logic designs must control crosstalk and switching noise. Adding analog circuitry comes at the cost of special packaging, custom chip floor-planning, custom power bus routing, strict partitioning of switching and non-switching functions, custom shielding and isolation structures, extensive use of CAD, a fully custom design effort for the analog portions of the chip, etc. Design strategies to prevent noise interactions are illustrated.

Time	Topic
8:00	***A Designer's View of Substrate Noise***, **Marcel Pelgrom**, Research Scientist, *Philips Research Labs, Eindhoven, The Netherlands*
8:30	***Substrate Noise Measurements and Analysis Case Studies*****,** **Makota Nagata**, Associate Professor, *Kobe University, Kobe, Japan*
9:00	***A Unified CAD Approach to Tackling Noise Coupling Problems in Mixed-Signal SoCs*****,** **Nishath Verghese,** Engineering Director, *Cadence Design Systems, San Jose, CA*
9:30	***IC Noise Isolation and Signal Integrity: A Resource and Time to Market Challenge*****,** **Timothy J. Schmerbeck**, Principal IC Design Engineer, *JDS Uniphase, Rochester, MN*

E3: Processors and Performance: When Do GHz Hurt?

(Salon 8)

Organizer: **Samuel Naffziger,** Fellow - VLSI Design, *Hewlett-Packard, Fort Collins, CO*
Moderator: **Shannon V. Morton,** Staff Engineer, *Icera Semiconductor, Bristol, U.K.*

In the performance-driven microprocessor-design community, a serious internal conflict is underway: The irresistible force of marketing of GHz is colliding with the immovable object of process-scaling slowdown. This panel will debate the future of using GHz to gain performance:

1. Will GHz still be what customers care about, or can they be trained to value performance?
2. Do the power, complexity, schedule, and area costs of pushing for GHz outweigh the benefits?
3. What is the realistic minimum number of fanout-of-4 inverters per cycle?
4. What are the alternatives for increasing performance?

Panelists:

Doug Carmean, Sr. Principal Architect, *Intel, Hillsboro, OR*
Philip Emma, Manager of Systems Technology and Microarchitecture, *IBM, Yorktown Heights, NY*
Hisashige Ando, CTO, E*nterprise Systems Group, Fujitsu, Kawasaki, Japan*
Mark Horowitz, Yahoo! Professor of Electrical Engineering and Computer Science, *Stanford University, Stanford, CA*
Alisa Scherer, Fellow, *AMD, Sunnyvale, CA*
Marc Tremblay, VP & Fellow, *Sun Microsystems, Sunnyvale, CA*

E4: What Is The Next Embedded Non-Volatile Memory Technology?

(Salon 7)

Organizer: **Young-Hyun Jun,** Vice President, *Memory Division, Samsung Electronics, HwaSung, GyeongGi, Korea*
Moderator: **Thomas Jew,** Manager, *Semiconductor Products Sector, Motorola Inc, Austin, Texas*

This panel will discuss the design and technology trade-offs to be fared in selecting a cost-effective embedded Non-Volatile technology. Current NVM technology requires high-voltage operation with slow write rates. To overcome these problems, technologies like FRAM, MRAM, PCM (Phase Change Memory), and Nano-Crystal memories are potential contenders for the next-generation NVM technology. The panelists will discuss which/when one of these technologies will become the main-stream Non-Volatile solution for the next generation.

Panelists:

Ki-Nam Kim, Vice President, *Memory Division, Samsung Electronics GiHeung, GyeongGi, Korea*
Tomoyuki Ishii, Senior Researcher, *System LSI Department, Hitachi Central Research Lab., Tokyo, Japan*
Sitaram Arkalgud, Director, *MRAM Development Alliance, Infineon Technologies, Hopewell Jct., NY*
Saied Tehrani, Director, *MRAM Technology Development, Motorola, Chandler, AZ*
Greg Atwood, Intel Fellow, *Flash Memory Development, Intel, Santa Clara, CA*
Tom Davenport, Vice President, *FRAM Development Ramtron Intl., Colorado Springs, CO*

MEMS AND SENSORS

Chair: **Farrokh Ayazi,** *Georgia Institute of Technology, Atlanta, GA*
Associate Chair: **Akintunde Akinwande,** *MIT, Cambridge, MA*

17.1 Reconfigurable RF Circuits Based on Integrated MEMS Switches

8:30 AM

J. DeNatale
Rockwell Scientific, Thousand Oaks, CA

MEMS phase shifters based on switchable passive components are used to achieve a variety of circuits with low insertion loss, wide bandwidth and compact die size. Integration of MEMS switches with active GaAs pHEMT MMIC achieves reconfigurable LNA and PA devices. A 4b true time-delay phase-shifter achieves ≤1.2dB insertion loss on a 7mm^2 die.

17.2 A Single-Chip CMOS Micro-Hotplate Array for Hazardous Gas Detection and Material Characterization

9:00 AM

D. Barrettino[1], M. Graf[1], S. Hafizovic[1], S. Taschini[1], C. Hagleitner[2], A. Hierlemann[1], H. Baltes[1]
[1]Swiss Federal Institute of Technology, Zurich, Switzerland
[2]IBM, Zurich, Switzerland

A single-chip microsystem for the detection and discrimination of hazardous gases and solid-state material characterization is presented. The circuit features three micro-hotplates, and each requires mixed-signal circuitry. The microsystem is fabricated in industrial 0.8μm CMOS technology with post-CMOS micromachining. The power efficiency of the micro-hotplate is 10°C/mW and represents a 60% improvement.

17.3 A 2.5V 14b ΣΔ CMOS-SOI Capacitive Accelerometer

9:30 AM

B. Vakili Amini, S. Pourkamali, F. Ayazi
Georgia Institute of Technology, Atlanta, GA

This paper presents a 2.5V 14b fully-differential ΣΔ interface IC in 0.25μm CMOS based on a programmable front-backend architecture for a high-resolution SOI capacitive accelerometer. Capacitive resolution is 22aF at 75Hz (RBW = 1Hz), equivalent to 110μg with a dynamic range of 85dB and sensitivity of 0.5V/g. The chip occupies 2mm^2 and consumes 6mW.

BREAK 10:00 AM

17.4 An Ultra-Low Energy Microcontroller for Smart Dust Wireless Sensor Networks

10:15 AM

B. Warneke[1], K. Pister[2]
[1]Dust, Berkeley, CA
[2]University of California, Berkeley, CA

A 12pJ/instruction microcontroller with embedded SRAM designed specifically for use in mm^3 wireless sensor nodes is described. It features highly independent subsystems for sensor sampling, transmission, and receiving that maximize the datapath sleep time as well as 100nW integrated oscillators with rapid power-cycling. Designed in 0.25μm technology, the 0.38mm^2 core-area IC comsumes 5.9μW from a 1V supply when running at 500kHz.

17.5 A Very-Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications

10:45 AM

L. Wong, S. Hossain, A. Ta, L. Weaver, C. Shaquer, A. Walker, J. Edvinsson, D. Rivas, H. Naas, A. Fawzi, A. Uhrenius, J. Lindberg, J. Johansson, P. Arvidsson
St Jude Medical, Sunnyvale, CA

A single-chip, very-low-power interface IC used in implantable pacemaker systems is presented. It contains LNAs, filters, ADCs, a battery management system, voltage multipliers, high voltage pulse generators, programmable logic and timing control. The 200k transistor IC occupies 49mm^2, is fabricated in a 0.5μm 2P3M multi-V_t CMOS process and consumes 8μW from a 2.8V supply.

17.6 A Fourth-Order ΣΔ Interface for Micromachined Inertial Sensors

11:15 AM

V. Petkov, B. Boser
University of California, Berkeley, CA

A high-order electromechanical ΣΔ modulator uses additional electronic filtering in the loop to eliminate excessive in-band quantization noise inherently present in second-order implementations. The interface is fabricated in a 0.5μm CMOS process and tested with a gyroscope and accelerometer achieving 1°/s/√Hz and 150μg/√Hz of resolution, respectively. Active chip area is 0.9mm^2 and the IC consumes a total of 18mW.

17.7 60-MHz Wine-Glass Micromechanical-Disk Reference Oscillator

11:30 AM

Y-W. Lin, S. Lee, S-S. Li, Y. Xie, Z. Ren, C. Nguyen
University of Michigan, Ann Arbor, MI

A reference oscillator utilizing a 60MHz, MEMS-based, wine glass disk vibrating micromechanical resonator with a Q of 48,000 and sufficient power handling capability to achieve a far-from-carrier phase noise of -130dBc/Hz is demonstrated. When divided down to 10MHz, this corresponds to an effective level of -145dBc/Hz.

CONCLUSION 11:45 AM

CONSUMER SIGNAL PROCESSING

Chair: **Jim Goodman,** *Engim, Ottawa, Canada*
Associate Chair: **Toyu Shimizu,** *Renasas Technology, Tokyo, Japan*

18.1 A 1440x1080Pixel 30Frames/s Motion-JPEG 2000 Codec for HD-Movie Transmission

8:30 AM

H. Yamauchi, S. Okada, K. Taketa, Y. Matsuda, T. Mori, T. Watanabe, K. Mochizuki
Sanyo, Gifu, Japan

The Motion-JPEG 2000 codec processor uses 0.18μm CMOS technology. It integrates 18.6M transistors on a 9.2mmx9.2mm die and performs both decoding and compressing of 1440x1080 pixels with 30frames/s at 54MHz. A tile size obtained is 4096x2048 pixels and is sufficient for transmitting an HD movie. The IC runs up to 104MHz and dissipates 400mW at 1.8V and 54MHz.

18.2 81MS/s JPEG 2000 Single-Chip Encoder with Rate-Distortion Optimization

9:00 AM

H-C. Fang[1], C-T. Huang[1], Y-W. Chang[1], T-C. Wang[2], P-C. Tseng[1], C-J. Lian[1], L-G. Chen[1]
[1]National Taiwan University, Taipei, Taiwan
[2]Chin Fong Machine, Zhang-hua, Taiwan

An 81MS/s JPEG 2000 single-chip encoder is implemented on a 5.5mm^2 die using 0.25μm CMOS technology. This IC can encode HDTV 720p resolution at 30 frames/s in real time. The rate-distortion optimized chip encodes tile size of 128x128, code block size of 64x64, and image size up to 32Kx32K.

18.3 An SoC with Two Multimedia DSPs and a RISC Core for Video Compression and Surveillance

9:30 AM

H-J. Stolberg, S. Moch, L. Friebe, A. Dehnhardt, M. Kulaczewski, M. Berekovic, P. Pirsch
University of Hannover, Hannover, Germany

An SoC is comprised of a 16-way SIMD DSP core with a 2D matrix memory, a 64b VLIW DSP core with subword parallelism, and a 32b RISC core. The 81mm^2 chip is implemented in a 0.18μm 6M standard-cell technology and runs at 145MHz. The device can perform MPEG-4 Advanced Simple Profile decoding at D1 resolution in real-time.

BREAK 10:00 AM

18.4 A 109.5mW 1.2V 600M texels/s 3-D Graphics Engine

10:15 AM

J. Fujita, M. Imai, T. Nagasaki, J. Sakamoto, H. Takeuchi, H. Nagano, S. Iwasaki, M. Hatakenaka, H. Tomikawa, K. Keino, T. Motomura, T. Ueda, T. Niki
Sony, Shinagawa, Japan

A 3D graphics engine consists of a programmable floating-point geometry engine and a rasterization engine. To adapt to various memory systems, the rasterization engine has a coordinate-based set associative cache mechanism. The IC achieves 4.7M vertex/s and 600M texel/s and dissipates 109.5mW. A 0.18μm 5M CMOS process is used to implement the 25.4mm^2 IC operating at 1.2V.

18.5 An Embedded Processor Core for Consumer Appliances with 2.8GFLOPS and 36M Polygons/s FPU

10:45 AM

F. Arakawa[1], T. Yoshinaga[2], T. Hayashi[2], Y. Kiyoshige[2], T. Okada[1], M. Nishibori[3], T. Hiraoka[2], M. Ozawa[1], T. Kodama[1], T. Irita[3], T. Kamei[4], M. Ishikawa[1], Y. Nitta[3], O. Nishii[2], T. Hattori[2]
[1]Hitachi, Tokyo, Japan
[2]SuperH, Tokyo, Japan
[3]Renesas Technology, Tokyo, Japan
[4]Renesas Technology, Kodaira, Japan

An embedded-processor core implemented in a 130nm CMOS process runs at 400MHz and achieves 720MIPS with a power of 250mW and 2.8GFLOPS. The processor employs a dual-issue seven-stage pipeline architecture while maintaining 1.8MIPS/MHz instruction efficiency of the previous five-stage processor. The processor is suitable for digital consumer appliances.

18.6 A Resume-Standby Application Processor for 3G Cellular Phones

11:15 AM

T. Kamei[1], M. Ishikawa[2], T. Hiraoka[3], T. Irita[1], M. Abe[1], Y. Saito[1], Y. Tawara[1], H. Ide[1], M. Furuyama[1], S. Tamaki[1], Y. Yasu[1], Y. Shimazaki[3], M. Yamaoka[2], H. Mizuno[2], N. Irie[2], O. Nishii[3], F. Arakawa[2], K. Hirose[1], S. Yoshioka[1], T. Hattori[3]
[1]Renesas Technology, Kodaira, Japan
[2]Hitachi, Kokubunji, Japan
[3]SuperH, Kodaira, Japan

A 360MIPS application processor for 3G cellular phones is implemented in a 0.13μm dual-V_t process. This dual-issue superscalar CPU with DSP runs at 216MHz at 1.2V and provides a resume-standby mode with a quick recovery feature using data retention of memory. The leakage current is estimated to be 98μA when the power supply is internally cut off.

18.7 A DSL Customer-Premises Equipment Modem SoC with Extended Reach/Rate for Broadband Bridging and Routing

11:45 AM

A. Saha[1], S. Oswal[1], S. Prasad[1], J. Kennedy[2], S. Kumar[1], B. Datta[1], A. Sharma[1], R. Singhal[1], P. Srikanth[1], R. Srinivasa[1], R. Mundhada[1], J. Malliah[1], F. Mujica[2], D. Beaudoin[2], B. Karguth[2], B. Egr[2], A. Redfern[2]
[1]Texas Instruments, Bangalore, India
[2]Texas Instruments, Dallas, TX

A highly-integrated DSL modem for residential gateway applications is described. Challenges encountered in the integration of the analog front end, networking, and DSL PHY subsystems are discussed. A 0.13μm 5M CMOS process is used to implement the 2.3W chip. Supplies are 1.5V for digital and 3.3V for analog subsystems.

CONCLUSION 12:15 PM

CLOCK GENERATION AND DISTRIBUTION

Chair: **Masayuki Mizuno,** *NEC, Sagamihara, Japan*
Associate Chair: **Nasser Kurd,** *Intel, Hillsboro, OR*

19.1 A 4.8GHz Resonant Global Clock Distribution Network

8:30 AM

S. Chan[1], P. Restle[2], K. Shepard[1], N. James[3], R. Franch[2]
[1]Columbia University, New York, NY
[2]IBM, Yorktown Heights, NY
[3]IBM, Austin, TX

A resonant global clock-distribution network operating at 4.6GHz is designed in a 90nm 1.0V CMOS technology. Unique to this approach is the set of on-chip spiral inductors that resonate with the clock capacitance and reduce global clock power by 35%. Jitter reduction is realized using this scheme as well.

19.2 Parallel Clocking: A Multi-Phase Clock-Network for 10GHz SoC

9:00 AM

K. Nose, M. Mizuno
NEC, Sagamihara, Japan

The realization of SoCs operating at 10GHz and multiple frequency IP-cores is possible using parallel clocking. With 2.5GHz 4-phase parallel clocking, the skew reduction circuits and multi-phase flip-flops successfully operate at 10GHz.

19.3 A 160-2550MHz Active Clock Deskewing PLL Using Analog-Phase Interpolation

9:30 AM

A. Maxim
Maxim Integrated Products, Austin, TX

An active clock-deskewing PLL uses analog-phase interpolation to generate the local shifted clocks. It provides a uniform and process independent phase-step over the entire deskew range, and a zero-latency phase shifter to speed-up the deskewing process. This 400x800μm^2 IC is fabricated in a 0.15μm CMOS process having a frequency range of 160 to 2550MHz, phase step of 2.8°, RMS jitter <1% T_{osc}, and draws 60mW from a 1.5V supply.

BREAK 10:00 AM

19.4 Realizing a Production ATE Custom-Processor and Timing IC Containing 400 Independent Low-Power and High-Linearity Timing Verniers

10:15 AM

B. Arkin
Credence Systems, Fremont, CA

An ATE processor and timing IC that includes 400 low-power timing verniers with a linearity error of less than 35ps is described. The timing vernier design approach is presented in detail. This 16x16mm^2 62M transistor IC is implemented in foundry portable 0.18μm CMOS technology.

19.5 On-Chip Jitter-Spectrum Analyzer for High-Speed Digital Designs

10:45 AM

M. Takamiya[1], H. Inohara[2], M. Mizuno[1]
[1]NEC, Sagamihara, Japan
[2]NEC, Fuchu, Japan

An on-chip jitter-spectrum analyzer (JSA) implemented in 0.18μm CMOS can locate and analyze trouble-spots in on- and off-chip power and 1GHz-clock distribution networks during the actual operations in the field. A feedback design-flow using JSA improves the performance of digital LSIs.

19.6 Design and Analysis of a Jitter-Tolerant Digital DLL-Based Fraction-of-Clock Delay Line

11:15 AM

J. Burnham[1], G. Yeh[2], E. Sun[2], C. Yang[3]
[1]IRF Semiconductor USA, Cupertino, CA
[2]Zoran, Sunnyvale, CA
[3]University of California, Los Angeles, CA

A digital DLL-based fraction-of-clock delay line is described. It uses a combination of scaling and phase-detector window alignment to improve jitter tolerance and loop stability without requiring a loop filter or reducing tracking bandwidth.

19.7 Timing Uncertainty Measurements on the Power5 Microprocessor

11:45 AM

P. Restle[1], R. Franch[1], N. James[2], W. Huott[3], T. Skergan[2], S. Wilson[3], N. Schwartz[2], J. Clabes[2]
[1]IBM, Yorktown Heights, NY
[2]IBM, Austin, TX
[3]IBM, Poughkeepsie, NY

On-chip timing measurement (Skitter) circuits are included on the Power5 microprocessor. By cross-coupling the 3 Skitter instances, the combined effect of jitter, skew, and supply noise can be measured for all cycles of a pattern or an application. System results show a maximum of 27ps timing impact on a 500ps path.

19.8 PowerTune: Advanced Frequency and Power Scaling on 64b PowerPC Microprocessor

12:00 PM

C. Lichtenau[1], M. Ringler[2], T. Pflueger[1], S. Geissler[2], R. Hilgendorf[1], J. Heaslip[2], U. Weiss[1], P. Sandon[2], N. Rohrer[2], E. Cohen[2], M. Canada[2]
[1]IBM, Boeblingen, Germany
[2]IBM, Essex Junction, VT

PowerTune is a power-management technique for a multi-gigahertz superscalar 64b PowerPC® processor in a 90nm technology. This paper discusses the challenges and implementation of a dynamically controlled clock frequency with noise suppression as well as a synchronization circuit for a multi-processor system.

CONCLUSION 12:15 PM

DIGITAL-TO-ANALOG CONVERTERS

Chair: **Roy Scott Kaller,** *SMSC, Phoenix, AZ*
Associate Chair: **Masayuki Katakura,** *Sony, Atsugi, Japan*

20.1 A 14b 1.4 GS/s 3V CMOS DAC for Multi-Carrier Applications

8:30 AM

B. Schafferer, R. Adams
Analog Devices, Wilmington, MA

An uncalibrated 0.18μm CMOS 14b 1.4GS/s DAC with an LVDS interface achieves 67dB SFDR for a 260MHz full-scale tone and 70dB ACLR for a two-carrier output centered at 470MHz. The IC dissipates a core power of 200mW.

20.2 A 10b 250MS/s Binary-Weighted Current-Steering DAC

9:00 AM

J. Deveugele, M. Steyaert
Katholieke Universiteit, Leuven, Belgium

A 10b binary-weighted current-steering DAC has over 60dB SFDR at 250 MS/s for signals from DC to Nyquist. The chip draws 4mW from a dual 1.5/1.8V supply (plus load currents). Active area is less than 0.35mm^2 in a standard 0.18μm 1P5M 1.8V CMOS process, and both INL and DNL are below 0.1LSB.

20.3 A 200MS/s 14b 97mW DAC in 0.18μm CMOS

9:30 AM

Q. Huang[1], P. Francese[1], C. Martelli[1], J. Nielsen[2]
[1]Swiss Federal Institute of Technology, Zurich, Switzerland
[2]Technical University of Denmark, Lyngby, Denmark

A fully analog loop calibrates 32 MSB floating current sources in the background to achieve 14b accuracy. Operating at 200MS/s, the 97mW DAC achieves maximum SFDR of 85dB in NRZ mode, 76dB in RZ mode, and maintains -160dBm/Hz noise spectral density. Implemented in 0.18μm CMOS, the core area is less than 1mm^2.

BREAK 10:00 AM

20.4 A 2GS/s 3b ΔΣ-Modulated DAC with a Tunable Switched-Capacitor Bandpass DAC Mismatch Shaper

10:15 AM

T. Kaplan[1], J. Jensen[2], C. Fields[2], M. Chang[1]
[1]University of California, Los Angeles, CA
[2]HRL Laboratories, Malibu, CA

A 3b ΔΣ-modulated mismatch-shaped DAC is presented. The mismatch shaper uses 7 tunable 1.5b switched-capacitor bandpass ΔΣ modulators to dynamically route the digital signals to the DACs. The DAC can generate narrowband signals from 250 to 750MHz with ≥68 dB SNR, ≥74dB SFDR, and ≤-80 dBc intermodulation distortion.

20.5 A 128f_s Multi-Bit ΣΔ CMOS Audio DAC with Real-Time DEM and 115dB SFDR

10:45 AM

E. van Tuijl, J. van der Homberg, D. Reefman, C. Bastiaansen, L. van der Dussen
Philips, Eindhoven, The Netherlands

A continuous-time 5b ΣΔ audio DAC operates at 5.65MS/s (128f_s). SFDR of -115dB and noise of -119dB (unweighted) are achieved by real-time DEM that cancels mismatch completely in each sample. Chip area is 2mm^2 in a 0.18μm, thick oxide 3.3V CMOS process. Total power consumption is 150mW.

20.6 A 13b 1.1MHz Oversampled DAC with Semi-Digital Reconstruction Filtering

11:15 AM

P. Francese, P. Ferrat, Q. Huang
Swiss Federal Institute of Technology, Zurich, Switzerland

A 1b and 5b digital ΣΔ modulator cascade sharpens noise shaping while maintaining linearity. A semi-digital SC FIR reconstruction filter combined with an IIR SC/RC filter reduce clock harmonics below the ADSL spurious emission mask. The 0.18μm 1P6M CMOS chip achieves 80dB SFDR, 78dB SNR and 74dB SNDR within 1.1MHz.

20.7 A 110dB Ternary PWM Current-Mode Audio DAC with Monolithic 2V_{rms} Driver

11:45 AM

T. Rueger[1], B. Duewer[1], S. Hodapp[1], T. Lei[1], J. Melanson[2], B. Trotter[1]
[1]Cirrus Logic, Austin, TX
[2]Cirrus Logic, Broomfield, CO

A ΔΣ audio DAC uses a 4b quantizer, ternary PWM encoding, and semi-digital current-mode FIRs for 110dB dynamic range over 20kHz. The IC achieves -99dB THD driving a single-ended 2V_{rms} signal into a 5kΩ load. Die area is 5.98mm^2 in a 0.35μm/3.3V process with a 3μm/18V module.

20.8 Audio-Amplifier Protection Based Upon Temperature Measurements in Power Transistors

12:15 PM

B. Krabbenborg
Philips, Nijmegen, The Netherlands

An audio amplifier IC has been realized with protection circuitry based directly upon power-transistor temperature measurements. In contrast to current- or voltage-based measurements, this method gives optimal protection independent of supply voltage (9-28V), load (2-16Ω BTL), ambient temperature and heat sinking.

CONCLUSION 12:30 PM

RF POTPOURRI

Chair: **Thomas Lee,** Stanford University, Stanford, CA
Associate Chair: **Tetsuro Itakura,** Toshiba, Kawasaki, Japan

21.1 Circular-Geometry Oscillators

8:30 AM

R. Aparicio, A. Hajimiri
California Institute of Technology, Pasadena, CA

A 5.3GHz 0.18μm CMOS circular-geometry oscillator exploits high Q of slab inductors. The oscillator draws 10mA from 1.4V with a phase noise of -147.3dBc/Hz at 10MHz offset. A second 5.4GHz circular-geometry VCO has a tuning range of 8% with phase noise of -142.2dBc/Hz at 10MHz offset while drawing 12mA from a 1.8V supply.

21.2 A Circular Standing Wave Oscillator

8:45 AM

W. Andress, D. Ham
Harvard University, Cambridge, MA

A circular standing wave oscillator that generates sinusoids by forming standing waves on a ring transmission line is presented. Incorporating an even-mode suppression technique, a 10GHz prototype realized in a SiGe bipolar technology has a phase noise of -110dBc/Hz at 1MHz offset with a 1.95mA current drawn from 1.5V.

21.3 An Ultra-Wideband CMOS LNA for 3.1 to 10.6GHz Wireless Receivers

9:00 AM

A. Bevilacqua[1], A. Niknejad[2]
[1]Universita di Padova, Padova, Italy; [2]University of California, Berkeley, CA

A UWB 3.1 to 10.6GHz LNA employing an input three-section band-pass Chebyshev filter is reported. Fabricated in a 0.18μm CMOS process, the IC achieves a power gain of 9.3dB with an input match of -10dB over the band, a NF of 4dB, and an IIP3 of -6.7dBm while consuming 9mW.

21.4 A 3 to 10GHz LNA Using Wideband LC-ladder Matching Network

9:15 AM

A. Ismail[1], A. Abidi[2]
[1]Skyworks Solutions, Newport Beach, CA; [2]University of California, Los Angeles, CA

Reactive matching is extended to wide bandwidths using the impedance property of LC-ladder filters. A SiGe amplifier with on-chip matching network spanning 3 to 10GHz delivers 22dB peak gain, 2.5dB NF and 0dBm input IP3 at 5GHz, with 10mA bias current.

21.5 A Fully Integrated 13GHz ΔΣ Fractional-N PLL in 0.13μm CMOS

9:30 AM

M. Tiebout[1], C. Sandner[2], H-D. Wohlmuth[1], N. Da Dalt[2], E. Thaller[2]
[1]Infineon Technologies, Munich, Germany; [2]Infineon Technologies, Villach, Austria

A 13GHz PLL designed for future WLAN systems in the 17GHz ISM band includes a differentially tuned LC VCO, IQ-divider, 212-217 low power multi-modulus prescaler, differential phase-frequency detector, charge pump with loop filter, and a 2nd-order noise-shaping ΔΣ modulator. Total power consumption is 60mW from a 1.5V supply.

BREAK 10:00 AM

21.6 A 17.1 to 17.3GHz Image-Reject Down-Converter with Phase-Tunable LO Using 3x Subharmonic Injection Locking

10:15 AM

S. Yue[1], D. Ma[1], J. Long[2], B. Jagganathan[3], D. Harame[4]
[1]University of Toronto, Toronto, Canada; [2]Delft University of Technology, Delft, The Netherlands; [3]IBM Microelectronics, Hopewell Junction, NY; [4]IBM Microelectronics, Burlington, VT

A 17GHz RF receiver consisting of an LNA and doubly-balanced mixers cou-

pled by a monolithic 3.7:1 step-down transformer realizes over 70dB of image-rejection in a 100GHz-f_T SiGe BiCMOS technology. Quadrature LO signals are generated with electronically tunable phase from a subharmonically injection-locked oscillator. The measured IIP3 is -5.1dBm with 17.3dB conversion gain and 6.5dB NF (SSB, 50Ω) at 17.2GHz. The 1.9x1.0mm^2 IC consumes 62.5mW from a 2.2V supply.

21.7 A Fully Integrated 24GHz 8-Channel Phased-Array Receiver in Silicon

10:45 AM

H. Hashemi, X. Guan, A. Hajimiri
California Institute of Technology, Pasadena, CA

A fully integrated 8-channel phased-array receiver at 24GHz is demonstrated. Each channel achieves a gain of 43dB, noise figure of 8dB, and an IIP3 of -11dBm, consuming 29mA of current from a 2.5V supply. The 8-channel array has a beam-forming resolution of 22.5°, a peak-to-null ratio of 20dB (4-bits), a total array gain of 61dB, and improves the signal-to-noise ratio by 9dB.

21.8 A Low-Loss Phase Shifter in 180nm CMOS for Multiple-Antenna Receivers

11:15 AM

H. Zarei, D. Allstot
University of Washington, Seattle, WA

A negative resistance approach decreases the loss of reflective-type passive phase shifters by as much as 5.9dB over 2.27-2.45GHz for use in multiple-antenna receivers. Conventional and low-loss prototypes each exhibit a phase-control range of ~105° and consume 1.08mm^2 in 180nm CMOS.

21.9 A 35.2-37.6GHz LC VCO in a 70/100GHz f_T/f_{max} SiGe Technology

11:30 AM

H. Veenstra, E. van der Heijden
Philips, Eindhoven, The Netherlands

An LC VCO circuit uses two cascaded emitter followers with resistive loads and combines negative resistance and output buffers. The VCO is particularly suited for frequencies above the limit of the cross-coupled differential pair, and a 35.2-37.6GHz VCO achieves a phase noise of -105dBc/Hz at 2MHz from the carrier in a 0.25μm production SiGe technology.

21.10 A Monolithic Low-Phase-Noise 1.7GHz CMOS VCO for Zero-IF Cellular CDMA Receivers

11:45 AM

Y. Wu, V. Aparin
Qualcomm, San Diego, CA

A 1.7GHz CMOS VCO with low-noise regulator is implemented in a 0.25μm 5M process for zero-IF cellular CDMA receivers. A grounded varactor topology using a junction diode of an NFET transistor is employed for fine tuning. The VCO has 350MHz tuning range and achieves phase noise <-134dBc/Hz at 900kHz offset under a noisy supply (0.37μV/√Hz PSD). The DC power sensitivity is smaller than 25kHz/V.

21.11 A +10dBm IIP3 SiGe Mixer with IM3 Cancellation Technique

12:00 PM

S. Otaka[1], M. Ashida[1], M. Ishii[2], T. Itakura[1]
[1]Toshiba, Kawasaki, Japan; [2]Toshiba, Yokohama, Japan

A 3rd-order intermodulation (IM3) cancellation technique using a sub-mixer is proposed for low-power, low-distortion mixers. The technique reduces IM3 by 18dB with a current increase of less than 10%. The mixer achieves an IIP3 of 10dBm, a gain of 8.7dB, a NF of 9.8dB and dissipates 30mW from 2.9V.

CONCLUSION 12:15 PM

DSL AND MULTI-Gb/s I/O

Chair: **Roger Minear,** *Agere Systems, Allentown, PA*
Associate Chair: **Héctor Sánchez,** *Motorola, Austin, TX*

22.1 A 0.13μm CMOS Four-Channel ADSL2+ Analog Front-End for CO Applications with 75mW per Channel

8:30 AM

P. Pessl, J. Hohl, R. Gaggl, A. Marak, G. Glanzer, J. Hauptmann, A. Kahl, S. Walter
Infineon, Villach, Austria

A 0.13μm CMOS four-channel analog front-end IC is presented. Each channel contains all analog and digital codec blocks, such as PGA, tuned filter, 14b ADC/DAC and digital filters. The core works with 1.5V beside the 2.5V and 3.3V interface supplies. In idle mode less than 75mW per channel is consumed.

22.2 An Integrated ADSL CPE Analog Front-End in a 0.13μm CMOS SoC

9:00 AM

S. Oswal[1], F. Mujica[2], S. Prasad[1], R. Srinivasa[1], B. Sharma[1], A. Raychoudhary[1], H. Khasnis[1], A. Sharma[1], S. Ramadoss[1], V. Baireddy[1], R. Menon[1], R. Gireesh[1], N. Ahuja[1], M. Gambhir[1], M. Sadafale[1]
[1]Texas Instruments, Bangalore, India
[2]Texas Instruments, Dallas, TX

An analog-front-end design including the power-management circuits to achieve an SoC ADSL CPE modem solution is presented. The integrated AFE with less than 2nV/√Hz input referred noise, dynamically adaptive hybrid and combination of the analog and digital filtering provides a single-chip solution.

22.3 A 3V CMOS Quad-Spectrum ADSL CPE Analog Front-End with 5V Integrated Line Driver

9:30 AM

R. Hogervorst[1], B. Tourette[1], N. Monier[1], O. Metayer[1], E. Afif[2], J-C. Delefosse[1], J-Y. Michel[1]
[1]Centillium Communications, Vallauris, France
[2]Centillium Communications, Fremont, CA

The analog front-end (AFE) for ADSL customer premise equipment (CPE) permits quad-spectrum down-stream (138kHz to 3.75MHz). The AFE includes a 5V line driver in a standard 0.18μm 3V CMOS process. The receive path contains an ADC with an 80dB SNDR over 3.75MHz bandwidth. Down-stream data rates of more than 50Mb/s are measured on short loops.

BREAK 10:00 AM

22.4 7th-Order Low-Voltage CMOS POTS/ADSL Splitter for DSL Access Multiplexer Size Reduction

10:15 AM

H. Dedieu[1], G. Nallatamby[1], T. Fernandez[1], P. Golden[1], J. Sevenhans[2], J. Bardyn[3], E. Moons[4], F. Krummenacher[5]
[1]LEA, Cesson-Sévigné, France
[2]LEA, Antwerp, Belgium
[3]XEMICS, Neuchâtel, Switzerland
[4]Alcatel, Antwerp, Belgium
[5]Smart Silicon Systems, Lausanne, Switzerland

Silicon ADSL/POTS splitter filter integration is the challenge for size and cost reduction of DSL equipment. This paper describes the implementation in 0.5μm CMOS of a wire by wire configuration of this filter. The area of the chip is 3mm². Proof of concept and measurements on the prototype silicon are reported.

22.5 A Scalable 160Gb/s Switch Fabric-Processor with 320Gb/s Memory Bandwidth

10:45 AM

G. Paul[1], M. Zeiger[1], A. Khan[2], A. Cohn[1], D. Dramon[1], D. Le[2], E. Grigoriants[1], G. Malkin[1], I. Malobani[1], I. Yanuka[1], J. Yu[2], J. Kung[2], L. Gnor[1], M. Shiterit[1], R. Rozen[1], R. Gabe[1], S. Hadas[1], T. Kelly[2], T. Wilson[2], T. Nguyen[2], W. Evans[2], Y. Hayon[1]
[1]Terachip, Lod, Israel
[2]Cadence Design Systems, San Jose, CA

The cost-effective, scalable, single-chip-switch fabric processor with 320Gb/s full duplex throughput, using a 320Gb/s shared memory architecture, delivers an 8x improvement in functional efficiency. 30M transistors, 64 SerDes ports and four 3.125GHz PLLs are integrated in a 0.13μm 8M process.

22.6 A 4Gb/s/pin Dual-Reference Simultaneous Bidirectional I/O Circuit for Memory-Bus Interface

11:15 AM

W-S. Kim[1], J-H. Choi[2], J-H. Kim[2], S-B. Cho[2], C-H. Kim[2], S-I. Cho[2], S. Kim[1]
[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Hwasung, Korea

This paper proposes a receiver with dual reference levels and a pre-emphasis circuit, which reduces ISI and improves input margin and linearity characteristics by 100% for data communication in memory applications. A test chip fabricated with a 0.10μm 1.8V CMOS memory process achieves a data rate of 4Gb/s/pin.

22.7 A 3.6Gb/s/pin Simultaneous Bidirectional (SBD) I/O Interface for High-Speed DRAM

11:45 AM

J. Kim, J. Choi, S. Shin, C. Kim, H. Kim, W. Kim, C. Kim, S. Cho
[1]Samsung Electronics, Hwasung-City, Korea

A point-to-point I/O interface for high-speed DRAM is described. The interface utilizes simultaneous bidirectional signaling that enables transmitting/receiving data through a line at the same time. The test scheme is implemented in 0.10μm DRAM process. It achieves 3.6Gb/s/pin in SBD mode and an I/O cell consumes 35mW.

CONCLUSION 12:15 PM

CHANNEL CODING

Chair: Giorgio Betti, *SE Microelectronics, Cornaredo, Italy*
Associate Chair: Albert van der Werf, *Phillips, Eindhoven, The Netherlands*

23.1 A 600MHz DSP with 24Mb Embedded DRAM with an Enhanced Instuction Set for Wireless Communication

1:30 PM

Y. Adelman, D. Agur, T. Bennun, O. Chalak, Z. Greenfield, R. Holzer, M. Jalfon, A. Kadry, F. Lange, H. Meirov, A. Olofsson, O. Raikhman, D. Treves, S. Zur, R. Talmudi
Analog Devices, Herzelia, Israel

A 600MHz general-purpose DSP with 24Mb of embedded DRAM, 154GOPS, 4800MMACS, and 40Gb/s I/O throughput is presented. The chip contains over 60M transistors and is implemented in 0.13μm 8M CMOS technology.

23.2 A 28.8 Mb/s 4x4 MIMO 3G High-Speed Downlink Packet Access Receiver with Normalized Least Mean Square Equalization

2:00 PM

D. Garrett, G. Woodward, L. Davis, G. Knagge, C. Nicol
Lucent Technologies, Sydney, Australia

A receiver for high-speed downlink packet access supporting 28.8Mb/s using QPSK over a 5MHz frequency selective 4x4 MIMO wireless channel (5.76b/s/Hz). A key feature is the normalized least mean squares space-time equalizer using a pilot correlator for more accurate adaptation. Fabricated in 0.18μm 6M CMOS, the chip covers an 11.6mm^2 area.

23.3 A Highly-Integrated 3G CDMA2000 1X Cellular-Baseband Chip with GSM/AMPS/GPS/Bluetooth/Multimedia Capabilities and ZIF RF Support

2:30 PM

G. Uvieghara, M-C. Kuo, J. Arceo, J. Cheung, J. Lee, X. Niu, R. Sankuratri, M. Severson, O. Arias, Y. Chang, S. King, K-C. Lai, Y. Tian, S. Varadarajan, J. Wang, K. Yen, L. Yuan, N. Chen, D. Hsu, D. Lisk, S. Khan, A. Fahim, C-L. Wang, J. Dejaco, Z. Mansour, M. Sani
Qualcomm, San Diego, CA

A 3G CDMA2000 1X cellular-baseband chip with GSM/AMPS/GPS/Bluetooth/Multimedia capabilities uses embedded ARM and two DSP processors. It is implemented with 27M transistors in 46.9mm^2 using a 130nm dual-V_t CMOS process and achieves a three to four times standby- time improvement by the selective use of footswitches.

BREAK 3:00 PM

23.4 A Generic 350Mb/s Turbo-Codec Based on a 16-state SISO Decoder

3:15 PM

P. Urard[1], L. Paumier[1], H. Michel[1], M. Viollet[1], E. Lantreibecq[1], B. Gupta[2], S. Muroor[2], B. Coates[2]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Berkeley, CA

The implementation of a 350Mb/s 16-state SISO turbo decoder and its corresponding coder are described. It performs within 1.8dB of Shannon's limit in terms of error correction. Implemented in 0.13μm low-leakage technology, this codec occupies 10mm^2 and is designed using a Matlab-to-RTL design flow.

23.5 A 0.18μm CMOS Front-End Processor for a Blu-Ray Disc Recorder with an Adaptive PRML

3:45 PM

G. Choi, J. Kim, H. Park, Y. Ahn, H. Park, J. Hong, J. Bae, I. Park, D. Shin
Samsung Electronics, Suwon, Korea

A single-chip front-end SoC, comprising a PRML with an adaptive equalizer, a data processor, a modem, an error-correcting code and digital servo with a 16b DSP, is for Blu-ray disc application. The chip dissipates 0.9W at 1.8V and 132MHz, contains 12M transistors and occupies 50mm^2 in 0.18μm CMOS technology.

23.6 A CMOS SoC for 56/32/56/16 COMBO Driver Applications

4:15 PM

C-L. Tsai[1], H-K. Liao[1], H-C. Chang[2], K-S. Hou[1], Y-L. Yang[1], H-C. Kuo[1], L-C. Tu[1], C-C. Chen[1], Y-K. Chou[1], Y-C. Chen[1], Y-H. Lin[1], C-L. Wu[1], H-C. Chen[1], Y-R. Liang[1], C-H. Chu[1], H-C. Peng[1], P-H. Lu[1]
[1]MediaTek, Hsin-Chu, Taiwan
[2]National Chiao-Tung University, Hsin-Chu, Taiwan

A single-chip solution for COMBO driver applications is presented. The approach features a multiple-word accessing mechanism to increase SDRAM bandwidth. After fabrication in 0.22μm 1P5M CMOS process, the proposed COMBO SoC supports a 16x DVD speed with 965mW dissipation.

23.7 A 1GHz CMOS Analog Front-End for a Partial-Response Read Channel

4:45 PM

D. Sun[1], A. Xotta[2], A. Abidi[1]
[1]University of California, Los Angeles, CA
[2]University of Padova, Padova, Italy

An analog front-end including a continuous-time equalizer to shape the received waveform into a 6-sample target, and a DFE-driven timing recovery loop is presented. With soft Viterbi detection, sensitivity is within 1.5dB of simulations at a rate of 24/25 and user density of 3.4. The 0.35μm CMOS chip consumes 240mW at 800MHz, and 380mW at 1GHz clock rates.

CONCLUSION 5:15 PM

TD: WIRELESS TRENDS: LOW-POWER AND 60GHz

Chair: **Ernesto Perea,** *ST Microelectronics, Grenoble, France*
Associate Chair: **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*

24.1 A Wireless Integrated Microsystem for Environmental Monitoring

1:30 PM

K. Wise, K. Najafi, R. Sacks, E. Zellers
University of Michigan, Ann Arbor, MI

A wireless sensing platform employing digital compensation, self-test, and distributed power management is reported. For use with this platform, key components of a gas chromatograph have been integrated. The assembled parts, occupying no more than a few cc, analyze multi-component mixtures ≤10cc, with detection limits below 1ppb. It can potentially separate an 11-compoent gaseous mixture in 90s.

24.2 A Multi-Channel Programmable FM Receiver for Hearing-Aid Applications

2:00 PM

N. Boom[1], E. Peeters[1], J. Crols[1], F. Callias[2], R. Philp[2]
[1]AnSem, Heverlee, Belgium
[2]Phonak Communications, Murten, Switzerland

A remotely controllable and programmable multi-channel 72-225MHz miniature FM receiver for hearing aids draws 2.2mA from a 0.9V-1.6V supply. The receiver achieves an SNR of 43dB and a sensitivity of -103dBm for an audio bandwidth of 7.5kHz. The IC is realized in 0.25μm CMOS and occupies 22.7mm^2.

24.3 AC-Only RFID Tags for Barcode Replacement

2:30 PM

S. Briole[1], C. Pacha[1], K. Goser[2], A. Kaiser[3], R. Thewes[1], W. Weber[1], R. Brederlow[1]
[1]Infineon Technologies, Munich, Germany
[2]Universität Dortmund, Dortmund, Germany
[3]IEMN-ISEN, Villeneuve d'Ascq, France

An RFID concept using ac-powered circuits without DC conversion is demonstrated for barcode replacement. A 32b codeword ID tag including an RF front-end, voltage limiter, frequency divider, ROM and power modulator has a 0.02mm^2 area in a 0.13μm CMOS process. A packaging technology uses a sidewall contact to facilitate the assembly process.

BREAK 3:00 PM

24.4 Design of CMOS for 60GHz Applications

3:15 PM

C. Doan, S. Emami, A. Niknejad, R. Brodersen
University of California, Berkeley, CA

The viability of digital CMOS as a future mm-wave technology, capable of exploiting the 60GHz band, is explored. Optimal device design and appropriate mm-wave models are presented. From modeling of transistors in 0.13μm technology a three cascode-stage amplifier at 1.5 volts would provide11dB of gain at 60GHz using 54mW.

24.5 A 60GHz Direct-Conversion Transceiver Circuits in SiGe Bipolar Technology

3:45 PM

S. Reynolds, B. Floyd, U. Pfeiffer, T. Zwick
IBM, Yorktown Heights, NY

A 60GHz LNA, direct-downconverter, PA, and 20GHz VCO are built in a 200GHz f_t/f_{max}, 0.12μm SiGe technology. The 10.8mW LNA has 15dB gain, 3.4-4.4dB noise figure and -8.5dBm IIP3. The down converter has 16dB gain, >50dB LO-RF isolation, and 13.4-14.8dB noise figure. The PA delivers 10dBm at 9dB gain.

24.6 64GHz and 100GHz VCOs in 90nm CMOS Using Optimum Pumping

4:15 PM

L. Franca-Neto, R. Bishop, B. Bloechel
Intel, Hillsboro, OR

A method to optimally pump energy from the transistors to the passive network is presented for the design of integrated 64GHz and 100GHz VCOs in 90nm CMOS. The VCOs use an on-die distributed network, draw ≈25mA from a 1V supply and produce oscillations with 0.4Vp-p amplitudes. Phase noise is <-110dBc/Hz at 10MHz offset, and VCO gain is 2GHz/V.

24.7 A 63GHz VCO Using a Standard 0.25μm CMOS Process

4:30 PM

R-C. Liu, H-Y. Chang, C-H. Wang, H. Wang
National Taiwan University, Taipei, Taiwan

A 63GHz VCO using a 0.25μm 1P6M CMOS is presented. It achieves an output power of -4dBm without any output amplifier. This VCO is tunable over a 2.5GHz range and its phase noise is -85 dBc/Hz at 1MHz offset. The IC covers an area of 0.315mm^2 and consumes 118mW maximum.

24.8 Millimeter-Wave Photonic IC Technologies for High-Speed Wireless Communications

4:45 PM

T. Nagatsuma, A. Hirata, M. Harada, H. Ishii, K. Machida, T. Minotani, H. Ito, T. Kosugi, T. Shibata
NTT, Atsugi, Japan

An IC technology for high-speed wireless-link systems using photonic techniques provides 10Gb/s at 120GHz. Optical signals are converted to electrical signals and radiated into freespace using Si-based circuitry. Both the preamp and PA utilize 0.1μm gate InAlAs/InGaAs HEMTs with gains of 6-10dB and 8.5dB, respectively.

CONCLUSION 5:15 PM

HIGH-RESOLUTION NYQUIST ADCs

Chair: **Zhongyuan Chang,** *IDT-Newave Technology, Shanghai, China*
Associate Chair: **Bill Redman-White,** *Phillips Semiconductors, Southampton, UK*

25.1 A Digitally Enhanced 1.8V 15b 40MS/s CMOS Pipelined ADC

1:30 PM

E. Siragusa, I. Galton
University of California, La Jolla, CA

A 1.8V 15b 40MS/s CMOS pipelined ADC with 90dB SFDR and 72dB peak SNR over the full Nyquist band is described. ADC performance is enhanced by digital background calibration of DAC noise and interstage gain error. The IC is realized in a 0.18μm CMOS process, consumes 392mW, and has a die size of 4mm x 5mm.

25.2 A 15b 20MS/s CMOS Pipelined ADC with Digital Background Calibration

2:00 PM

H-C. Liu, Z-M. Lee, J-T. Wu
National Chiao-Tung University, Hsin-Chu, Taiwan

A 15b 20MS/s CMOS pipelined ADC is fabricated in a 0.18μm dual-gate CMOS technology and achieves 94dB SFDR and 74dB SNDR for a 8MHz input. Digital calibration can proceed continuously in the background to maintain the ADC resolution. The chip occupies an area of 3.3 x 3.4mm^2 and dissipates 235mW with 1.8V and 3.3V dual supplies.

25.3 A 96dB SFDR 50MS/s CMOS Pipeline A/D Converter

2:30 PM

K. Nair, R. Harjani
University of Minnesota, Minneapolis, MN

A 96dB SFDR 50MS/s pipeline A/D converter has been designed in a 0.25μm CMOS process. An improved sample-and-hold and SD-CGC digital calibration are used to increase linearity. Prototype measurements show that the SNDR increases from 49dB to 75dB and the SFDR increases from 62dB to 96dB using the technique.

BREAK 3:00 PM

25.4 A 1.8V 14b 10MS/s Pipelined ADC in 0.18μm CMOS with 99dB SFDR

3:15 PM

Y. Chiu, P. Gray, B. Nikolic
University of California, Berkeley, CA

A 1.8V, 14b pipelined ADC using passive capacitor error-averaging and nested CMOS gain boosting achieves 99dB SFDR for signal frequencies up to 5.1MHz without trimming or calibration. With a 1MHz analog input, DNL is 0.31LSB, INL is 0.58LSB, and SNDR is 73.6dB. The chip occupies 15mm^2 in 0.18μm CMOS and dissipates 112mW.

25.5 A 12b 80MS/s Pipelined ADC with Bootstrapped Digital Calibraton

3:45 PM

C. Grace[1], P. Hurst[2], S. Lewis[2]
[1]Conexant Systems, Newport Beach, CA
[2]University of California, Davis, CA

A 12b 80MS/s pipelined ADC is calibrated for constant and signal-dependent gain errors as well as for slew-rate errors. With foreground calibration, peak SNDR is 72.6dB, and peak SFDR is 85.4dB. Using an on-chip microprocessor for calibration, the total power dissipation is 755mW from 2.5V, and the active area is 19.6mm^2 in a 0.25μm CMOS process.

25.6 An 80MHz 10b Pipeline ADC with Dynamic Range Doubling and Dynamic Reference Selection

4:15 PM

O. Stroeble, V. Dias, C. Schwoerer
Infineon, Munich, Germany

A 10b 80MHz pipeline ADC consumes 22mA at 1.5V and occupies a die area of 0.3mm^2 in a 0.13μm CMOS technology. The ADC is based on a conventional 1.5b pipeline architecture combined with dynamic-range-doubling and dynamic-reference-selection algorithms.

25.7 A 14b Linear-Capacitor Self-Trimming Pipelined ADC

4:45 PM

S-T. Ryu[1], S. Ray[1], B-S. Song[1], K-Y. Cho[2], K. Bacrania[3]
[1]University of California, La Jolla, CA
[2]KAIST, Daejon, Korea
[3]Intersil, Palm Bay, FL

Capacitor mismatch in a 1.5b/stage pipelined ADC is self-trimmed with a zero-forcing calibration loop based on ΔΣ polarity detection. Signal-subtracted analog PN error correlation shortens background calibration time by a factor of 10. The 4.2 x 3.8mm^2 chip in 0.18μ CMOS exhibits 1LSB INL at 14b, 84dB SFDR at 30MS/s, and consumes 350mW at 3V.

25.8 An Opamp with Common-Mode-Linearized Input Stage

5:00 PM

N. Carter
Analog Devices, Santa Clara, CA

Wideband large-signal distortion has been optimized by applying a common-mode linearization technique to the amplifier input stage. An operational amplifier has been fabricated in a 6GHz f_T dielectrically-isolated complementary bipolar process that achieves 1nV/√Hz voltage noise, better than 90dBc distortion for a $2V_{pp}$ 10MHz input signal, a 2GHz GBW, and 500μV V_{os}.

CONCLUSION 5:15 PM

OPTICAL AND FAST I/O

Chair: **Larry DeVito,** *Analog Devices, Wilmington, MA*
Associate Chair: **John Khoury,** *Vitesse Semiconductor, Somerset, NJ*

26.1 Single-Stage 378MHz 178kΩ Transimpedance Amplifier with Capacitively-Coupled Voltage Dividers

1:30 PM

C. Seidl, J. Knorr, H. Zimmermann
Technical University of Vienna, Vienna, Austria

A transimpedance amplifier with an integrated photodiode in a 0.6μm BiCMOS technology is described. A transimpedance of 178kΩ and a bandwidth of 378MHz for DVD applications are achieved with capacitively-coupled voltage dividers in the feedback path. An optical fiber receiver achieves a sensitivity of -30.4dBm at 1Gb/s.

26.2 A 3Gb/s Monolithic Photodiode and Pre-Amplifier in Standard 0.18μm CMOS

1:45 PM

S. Radovanovic, A-J. Annema, B. Nauta
University of Twente, Enschede, The Netherlands

A 3Gb/s optical detector with integrated photodiode and pre-amplifier for 850nm light is presented. The IC is implemented in standard 0.18μm CMOS. The data rate is achieved by using an inherently robust analog equalizer without sacrificing responsivity.

26.3 Burst-Mode Receiver for 1.25Gb/s Ethernet PON with AGC and Internally Created Reset Signal

2:00 PM

Q. Le[1], T-H. Yoo[2], S-G. Lee[1]
[1]Information and Communications University, Daejeon, Korea
[2]Electronics and Telecommunications Research Institute, Daejeon, Korea

A burst-mode receiver for 1.25Gb/s Ethernet passive optical network (PON) systems is implemented in 0.18μm CMOS technology. With AGC, the receiver achieves a sensitivity of -22dBm, overload of -3.5dBm and loud/soft ratio of 17.5dB. The receiver creates an internal reset signal, and all timing parameters exceed current standards.

26.4 A 40Gb/s CMOS Distributed Amplifier for Fiber-Optic Communication Systems

2:30 PM

H. Shigematsu[1], M. Sato[1], T. Hirose[1], F. Brewer[2], M. Rodwell[2]
[1]Fujitsu, Atsugi, Japan
[2]University of California, Santa Barbara, CA

A 0.18μm CMOS distributed amplifier with optimized source degeneration acheives a 4dB gain and 39GHz bandwidth within 1dB gain variation.

26.5 A 12dBm 320GHz GBW Distributed Amplifier in a 0.12μm SOI CMOS

2:45 PM

J. Kim, J-O. Plouchart, N. Zamdmer, R. Trzcinski, R. Groves, M. Sherony, Y. Tan, M. Talbi, J. Safran, L. Wagner
IBM, Hopewell Junction, NY

A 9-stage distributed amplifier achieves 11dB gain and 90GHz 3dB cut-off frequency equivalent to a 320GHz GBW. The measured 1dB output compression point is 12dBm at 20GHz, the OIP3 is 15.5dBm at 50GHz, and the noise figure is 5.5dB at 18GHz.

BREAK 3:00 PM

26.6 A 40Gb/s Amplifier and ESD Protection Circuit in 0.18μm CMOS Technology

3:15 PM

S. Galal, B. Razavi
University of California, Los Angeles, CA

A triple-resonant LC network increases the bandwidth of cascaded differential pairs by a factor of 2√3, yielding a 40Gb/s CMOS amplifier with a gain of 15dB and a power dissipation of 190mW from a 2.2V supply. An ESD protection circuit employs negative capacitance along with T-coils and pn junctions to operate at 40Gb/s while tolerating 700V.

26.7 A BiCMOS 10Gb/s Adaptive Cable Equalizer

3:45 PM

G. Zhang[1], P. Chaudhari[2], M. Green[1]
[1]University of California, Irvine, CA
[2]Stanford University, Stanford, CA

An adaptive cable equalizer for 10Gb/s broadband data using a SiGe BiCMOS process is presented. The circuit consists of a feed-forward equalizer that compensates for a copper cable length between 4 and 15 feet. Adaptation is performed by sensing the transition time of the equalizer output using a circuit based on the source-coupled node of a differential pair.

26.8 A 2GHz CMOS VGA with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet

4:15 PM

C-H. Wu, C-S. Liu, S-I. Liu
National Taiwan University, Taipei, Taiwan

A fully integrated 2GHz variable gain amplifier is implemented in a 0.18μm CMOS process to achieve 50dB linear-in-magnitude controlled-gain range for 10GBase-LX4 Ethernet. The measured dynamic range is 35dB from 9 to 495mVpp with BER less than 10^{-12}. The 0.7mm^2 chip dissipates 40mW.

26.9 Output Buffer Impedance Control and Noise Reduction Using a Speed-Locked Loop

4:30 PM

M. Bazes
Intel, Haifa, Israel

A speed-locked loop (SLL) controls output buffer drive strength in an Ethernet controller chip. The SLL automatically determines chip speed and adjusts the output buffer drive strength so that buffer impedance and switching noise remain within narrow limits over all process, voltage, and temperature conditions.

26.10 A PVT-Tolerant 0.18-600MHz Self-Calibrated Digital PLL in 90nm CMOS

4:45 PM

J. Lin, B. Haroun, T. Foo, J-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, J. Kirkpatrick
Texas Instruments, Dallas, TX

A digital PLL with logarithmic time digitizer, digitally-controlled oscillator, and start-up calibration achieves constant damping factor and fractional loop bandwidth over a 0.18 to 600MHz range of output frequencies and PVT conditions with output jitter less than 0.04 UIPP. The 0.18mm^2 chip is implemented in 90nm CMOS, operates over 0.7 to 2.4V power supply and consumes 1.7mW at 1V and 520MHz.

CONCLUSION 5:15 PM

SRAM

Chair: **Sreedhar Natarajan,** *MOSYS, Kanata, Canada*
Associate Chair: **Bruce Bateman,** *T-RAM, San Jose, CA*

27.1 Cosmic-Ray Immune Latch Circuit for 90nm Technology and Beyond

1:30 PM

Y. Arima, T. Yamashita, Y. Komatsu, T. Fujimoto, K. Ishibashi
STARC, Yokohama, Japan

A cosmic-ray immune latch circuit is presented. The storage node is separated into three electrodes, and the soft error on one node can be corrected by the other two even if there is a large and long-lasting influx of radiation-induced charges. The circuit is soft error free for 90nm and finer technologies.

27.2 A 300MHz, 25μA/Mb Leakage, On-Chip SRAM Module Featuring Process-Variation Immunity and Low-Leakage-Active Mode for Mobile Phone Application Processor

2:00 PM

M. Yamaoka[1], Y. Shinozaki[2], N. Maeda[3], Y. Shimazaki[3], K. Kato4, S. Shimada[4], K. Yanagisawa[4], K. Osada[1]
[1]Hitachi, Kokubunji, Japan
[2]Hitachi, Fukuoka, Japan
[3]SuperH, Kodaira, Japan
[4]Renesas Technology, Kodaira, Japan

An on-chip 1Mb SRAM that has three modes of operation for application processors is developed to reduce power consumption. It operates at 300MHz, with leakage of 25μA/Mb in the standby mode, and 50μA/Mb at the low-leakage-active mode.

27.3 A 0.13μm Triple-Vt 9MB Third Level On-Die Cache for the Itanium®2 Processor

2:30 PM

J. Chang, J. Shoemaker, M. Haque, M. Huang, K. Truong, M. Karim, S. Chiu, G. Leong, K. Desai, R. Goe, S. Kulkarni, A. Rao, D. Hannoun, S. Rusu
Intel, Santa Clara, CA

The 18-way set-associative, single-ported 9MB cache for the Itanium®2 Processor uses 210 identical 48kB sub-arrays with a 2.21μm² cell in a 0.13μm 6M technology. A staged mode ECC scheme avoids a latency increase in the L3 Tag. A high Vt implant improves the read stability and reduces the sub-threshold leakage.

BREAK 3:00 PM

27.4 A 0.7fJ/bit/search, 2.2ns Search-Time, Hybrid type TCAM Architecture

3:15 PM

S. Choi[1], K. Sohn[1], M-W. Lee[1], S. Kim[1], H-M. Choi[1], D. Kim[1], U-R. Cho[2], H-G. Byun[2], Y-S. Shin[2], H-J. Yoo[1]
[1]KAIST, Daejeon, Korea
[2]Samsung, Hwasung, Korea

A 2.2ns search-time, 0.7fJ/bit/search 0.1μm CMOS TCAM uses NOR cell for high-speed coarse search and NAND cell for low-power fine search. A hidden bank selection eliminates timing penalty for partial activation, match line repeater enhances the search speed and column decoding enables high memory density.

27.5 Architecture and Circuit Techniques for a Reconfigurable Memory Block

3:45 PM

K. Mai, R. Ho, E. Alon, D. Liu, Y. Kim, D. Patil, M. Horowitz
Stanford University, Stanford, CA

A 2KB reconfigurable SRAM block using self-timed, pulse-mode circuits capable of emulating a portion of a cache or a streaming FIFO is realized in a 1.8V 0.18μm CMOS process and operates at 1.1GHz (10FO4 cycle). The additional logic needed for reconfigurability consumes 26% of the total power and 32% of the total area.

27.6 Per-bit Sense Amplifier Scheme for 1GHz SRAM Macro in Sub-100nm CMOS Technology

4:15 PM

K. Takeda[1], Y. Hagihara[1], Y. Aimoto[2], M. Nomura[1], R. Uchida[1], Y. Nakazawa[1], Y. Hirota1, S. Yoshida[2], T. Saito[2]
[1]NEC, Sagamihara, Japan
[2]NEC, Kawasaki, Japan

A sensing circuit is developed in order to produce a 1GHz SRAM macro to be used in sub-100nm CMOS technology nodes. It employs a sense amplifier for each bit-line pair in high-speed operations. The amplifier's optimized composition consists of just ten transistors and helps to minimize area overhead.

27.7 A Fully Digital Circuit for a Minimum Distance Search Using an Asynchronous Bubble Shift Memory

4:30 PM

S. Nakahara, T. Kawata
Hitachi, Ome, Japan

The architecture described allows a fully digital circuit to search for the minimum Hamming distance. It compares favorably with prior approaches in its robustness and short design time. A concentration of asynchronous circuit techniques allows a 35ns search time of 62entry x 128b data with a 0.13μm 5M CMOS process.

27.8 A Differential Current-Mode Sensing Method for High-Noise-Immunity, Single-Ended Register Files

4:45 PM

N. Tzartzanis, W. Walker
Fujitsu, Sunnyvale, CA

A register file read-out method that relies on differential current-mode sensing while using single-ended bit lines is presented. This method improves noise immunity, access, and cycle time compared to dynamic approaches. A 34x64-bit, 10R/6W, write-through register file is implemented in 0.11μm, 1.2V CMOS with an access time of 1.07ns and dissipation of 133mW at 500MHz.

27.9 A 90nm Dual-Port SRAM with 2.04μm² 8T-Thin Cell Using Dynamically Controlled Column Bias Scheme

5:00 PM

K. Nii, Y. Tsukamoto, S. Imaoka, T. Yoshizawa, H. Makino
Renesas Technology, Itami, Japan

A high-density dual-port SRAM (DP-SRAM) with a 2.04μm² cell size is implemented in 90nm CMOS technology. A dynamically-controlled column-bias scheme is presented, which reduces the active power by 64% and the stand-by current by 93%.

CONCLUSION 5:15 PM

DEEP-SUBMICRON ANALOG AND RF CIRCUIT DESIGN

This Short Course is intended to provide both entry-level and experienced engineers with practical design approaches for implementation of analog and RF circuitry in deep-submicron CMOS and BiCMOS technologies. Course completion provides an overall perspective of the circuit-design issues and detailed design strategies for circuit building blocks in wired and wireless communication applications. Topics covered address the challenges faced by analog and RF designers in technologies with channel lengths of 90nm and below including the device models, design methodologies, and system-integration technologies.

For Registration, please use the ISSCC 2004 Registration Form on the Advance Program Centerfold. Sign-in is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00 AM.

The Short Course will be offered twice on Thursday, February 19.
The first session is scheduled for 8:00AM to 4:30PM.
The second session is scheduled for 10:00AM to 6:30PM.

CD of the Short Course & Relevant Papers: Short Course registrants will receive a CD-ROM at the Short Course. The CD-ROM includes: (1) The four Short Course presentations in PDF format for printing hard copies of the visuals, (2) Bibliographies of relevant papers for all four presentations, and (3) PDF copies of relevant background material, and important papers in the field (about 10-20 papers per presentation).

OUTLINE

Models for Deep-Submicron Analog/Mixed-Signal ICs
(8:00AM-9:30AM), (10:00AM-11:30AM)

Accurate models are critical for simulation of analog/mixed-signal ICs. Details of recent fundamental breakthroughs in MOSFET modeling are reviewed, and shown to overcome basic flaws that plague existing MOSFET models. An often-unappreciated show-stopper in the CMOS shrink-path is the increase in statistical variations, and the transition from correlated to uncorrelated (mismatch) variations being dominant. A framework with accurate techniques for modeling DSM statistical variations is presented.

Instructor: Colin McAndrew received the Ph.D. in Systems Design Engineering from the University of Waterloo in 1984, and the B.E. in Electrical Engineering from Monash University, Melbourne, Australia, in 1978. From 1987 to 1995 he was at AT&T Bell Laboratories, Allentown PA. Since 1995, he has been with Motorola, Tempe AZ, and is at present Director of Enabling Technology. His work is on compact and statistical modeling and characterization for circuit simulation.

Analog Circuit Design In Deep Submicron CMOS Processes
(10:00A-11:30A), (12:00P-1:30P)

This presentation reviews some challenges of deep-sub micron analog design. While digital circuits benefit greatly from the high tranconductance of short-channel MOS transistors, analog circuits are limited by lower voltage gains, higher gate capacitance, and even gate leakage. The low supply voltages of the core transistors often necessitate specialized design techniques. One solution is to use a combination of low voltage core transistors and higher voltage I/O transistors.

Instructor: Eric Soenen received the Ph.D. degree from Texas A&M University in 1992, and an MBA from the University of Texas in 2000. He joined Texas Instruments in 1991. He was Design Manager for Data Converters and Product Line Manager for Wireless Infrastructure RF. In 2002, he joined Barcelona Design, Newark, CA. He is presently Director of Analog Synthesis Engine Development. His research interests include synthesis of data converters and phase-locked loops.

Recent Developments in RF CMOS Transceivers
(1:00P-2:30P), (3:00P-4:30P)

This presentation describes new RF architectures and circuit techniques developed for high-performance wireless communications. Design techniques for zero-IF, low-IF, single-VCO heterodyne, and offset-PLL architectures are presented, and examples of the state-of-the-art for various wireless standards are reviewed. RF circuit topologies that alleviate architecture issues, and lend themselves to realization in CMOS are also described, and comparative studies of recently-reported transceiver designs, in the range of 1 to 5 GHz are used to illustrate issues and trade-offs.

Instructor: Behzad Razavi is Professor of Electrical Engineering at UCLA, where he conducts research on high-speed data communication circuits, wireless transceivers, phase-locking phenomena, and data converters. He is an IEEE Distinguished Lecturer, a Fellow of IEEE, and recipient of numerous awards at ISSCC, ESSCIRC, and CICC. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He has published six books in the area of analog and RF design, two of which have been translated to Chinese and Japanese.

Analog/RF Design in SiGe BiCMOS
(3:00P-4:30P), (5:00P-6:30P)

SiGe BiCMOS technology has established a strong presence in the high-performance analog/RF communications-IC market. The wide range of device options, along with their outstanding high-frequency performance, make the technology a natural choice for high-performance low-dc-power applications. This presentation will summarize the key design advantages of SiGe, and highlight some particular applications where the use of SiGe bipolar devices with their high linearity, high transconductance, and high breakdown voltage can lead to substantial improvements in performance and dc power. Particular attention will be paid to emerging wireless applications like 3G and 802.11a.

Instructor: Lawrence Larson received the B.S. and M.Eng. degrees in Electrical Engineering from Cornell University, and the PhD from UCLA in 1986. He was at Hughes Research Laboratories from 1980 to 1996, where he worked on the development of InP, GaAs, CMOS, SiGe and MEMs- based devices and circuits for communications. Since 1996, he has been a Professor at UCSD, where he is currently Director of the UCSD Center for Wireless Communications. He is the co-recipient of a number of awards for his work on high-speed microelectronics, has co-authored three books, published over 200 paper, and has 27 US patents.

F3: Analog Telecom ASIC & Circuit Concepts Forum: A/D D/A Building Blocks for Telecom Transceiver Applications

(Golden Gate A-B)

Chairman : **Jan Sevenhans,** *LEA ABC, Antwerpen, Belgium*
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David Robertson, Analog Devices, Wilmington, MA
Franz Dielacher, Infineon, Villach, Austria
Bram Nauta, University of Twente, Enschede, The Netherlands
Masayuki Katakura, Sony, Atsugi, Japan

This ISSCC 2004 Advanced Circuit Forum will dedicate a full day to the ying and the yang of microelectronics and telecom circuit design, the enablers of digital signal processing for an analog world:

Analog to-Digital and Digital to-Analog converters.
The stairway to the blue sky of telecom-transceiver performance is built on the state-of-the art bit rate and resolution of A/D and D/A converter IP-building-blocks to maximize the line length for DSL broadband modems, or the sensitivity of a cellular phone or a wireless LAN. In fact, the sampling rate and the resolution of the A/D and D/A determine much of the analog transceiver architecture, the order of the blocker and adjacent channel filters, or the smoothing and anti-alias filters. As well, the digital interpolator and decimator filters can be relaxed very often by simply choosing a faster or higher-resolution converter between the analog and the digital civilizations communicating via A/D and D/A converters. Clearly, the trade off is between performance and power consumption.

Finally, at the end of the afternoon, the speakers wil assemble in a panel format to field questions and comments from the audience.

Ideally, a lively discussion with this presentation on the state of the art in A/D & D/A building blocks for telecom transceiver applications.

Thursday, February 19th 8:30 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topics
8:00	Continental Breakfast
8:30	**Welcome and Introduction** Jan Sevenhans, LEA ABC, Antwerpen, Belgium
8:45	**25 years of A/D & D/A in Telecom** **Chang Zhong Yuan,** IDT-Newave Technology,Shanghai,China
9:30	**Impact of Jitter and Phase Noise on Converter Performance in Telecom** **Asad Abidi,** UCLA, CA
10:15	**A/D and D/A Converters for Broadband on DSL and Cable** **Jean-Philip Cornil,** Broadcom, Mechelen, Belgium
11:00	Break
11:15	**Challenges for Re-Use and Design Efficiency in A/D & D/A** **Carlos Leme,** Chipidea, Portugal
12:00	**A/D and D/A Converter Requirements and Implementation for W-CDMA Base Stations** **Manfred Punzenberger**, Infineon,Villach,Austria
12:45	Lunch
2:00	**Sigma-Delta A/D Converter Technology for Cellular Handsets** **Robert van Veldhoven,** Philips Einhoven, The Netherlands
2:45	**Pipelined A/D Convertors** **Steve Lewis,** UC Davis, CA
3:30	Break
3:45	**Panel Discussion**
5:00	Conclusion

F4: Microprocessor Circuit Design Forum: Managing Variability in Sub-100nm Designs

(Salon 10-15)

Chair: **Ron Preston** – Intel, Shrewsbury, MA

Committee:
Krste Asanovic, Massachusetts Institute of Technology, Cambridge, MA
William Bowhill, Intel, Shrewsbury, MA
Peter Kogge, University of Notre Dame, South Bend, IN
Georgios Konstadinidis, Sun Microsystems, Sunnyvale, CA
Nasser Kurd, Intel, Hillsboro, OR
Robert Rogenmoser, Broadcom, Santa Clara, CA
Hector Sanchez, Motorola, Austin TX
Simon Segars, ARM, Cambridge, England
James Warnock, IBM, Yorktown Heights, NY
Hoi-Jun Yoo, KAIST, Yusong, Korea

Variability, whether from process parameters or circuit activity, is a primary design consideration for designs in sub-100nm processes. Successful designers will require detailed knowledge of the specific variations that impact their designs, and will have to implement strategies to cope with these variations. In this Forum, the source and magnitude of circuit and parameter variations, along with their potential impact on designs in sub-100nm processes, will be reviewed. A number of techniques for coping with, and adapting a design for, variation such as statistical timing closure, adaptive circuit styles, and asynchronous design for variance tolerance, will be presented. The intended audience are circuit designers working in sub-100nm technologies, who need to understand how circuit and parameter variations will impact their designs, and strategies for coping with the impact.

The Forum will begin with two talks that will overview sources of variation and their impact on designs. In the first talk, David Frank from IBM will discuss the key sources of parameter variation, including systematic variation, chip-to-chip process variations, and parameter shifts that may occur during a chip's working lifetime, with a particular emphasis on understanding the impact to device threshold voltage caused by discrete-dopant fluctuations in the small geometries of sub-100nm processes. Samie Samaan of Intel will then discuss the impact of variations on designs in the last few process generations, and provide an outlook for the next few process generations, with a focus on the impact to timing margins.

Timing will be the focus of the next three talks. Chandu Visweswariah from IBM will describe a statistical approach to managing timing that can account for parameter variations. Tetsuya Higuchi from MIRAI/AIST will then outline an approach to adjusting chip timing post-fabrication, which has demonstrated the ability to lower power and improve frequency of a high-performance processor. The final timing talk will be from Steve Furber of the University of Manchester. Professor Furber will describe how asynchronous circuit techniques can be employed to reduce the impact of timing variations, whether they are caused by parameter variation, circuit switching behavior, or any other factor. This talk will also describe an asynchronous network-on-chip wiring fabric.

The final two talks will examine circuit design with variation as a key issue. Ray Heald of Sun Microsystems will describe the challenges of developing SRAM designs in high-performance microprocessor projects. With extremely small device geometries and low voltage levels, parameter variations, such as random dopant fluctuations, can have a significant impact, not only to timing, but to overall functionality of the design. In the final talk, Takayasu Sakurai from the University of Tokyo will describe adaptive circuit techniques such as body-biasing that can be used to help manage circuit variation.

Thursday, February 19th 8:30 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topic
8:00	Continental Breakfest
8:30	**Forum Introduction** **Ron Preston** – *Intel, Shrewsbury, MA*
9:00	**Parameter Variations in Sub-100nm CMOS Technology** **David J. Frank** – *IBM, Yorktown Heights, NY*
10:00	Break
10:15	**The Impact of Device Parameter Variations on the Frequency & Performance of Microprocessor Circuits** **Samie Samaan** – *Intel, Hillsboro, OR*
11:00	**Statistical Timing of Digital Integrated Circuits** **Chandu Visweswariah** – *IBM, Yorktown Heights, NY*
12:00	Lunch
1:00	**Post-Fabrication Adjustment with Genetic Algorithms** **Tetsuya Higuchi** – *MIRAI/AIST, Japan*
1:45	**Asynchronous Design for Tolerance to Timing Variability** **Steve Furber** – *The University of Manchester, UK*
2:45	Break
3:00	**Managing Variability in SRAM Designs** **Ray Heald** – *Sun Microsystems, Sunnyvale, CA*
3:45	**Adaptive Circuit Techniques for Managing Variations** **Takayasu Sakurai** – *University of Tokyo, Tokyo, Japan*
4:30	Open Forum Q&A *All speakers*
5:00	Conclusion

CONFERENCE REGISTRATION

Online regisration for ISSCC is the fastest, most convenient way to register, and will give you immediate confirmation of whether or not you have a place in the Tutorial, Short Course, and Forum sessions of your choice. If you register online, your registration is processed while you are online, and your written confirmation can be downloaded and printed for your record-keeping. If you register by fax or mail, you will not receive confirmation for several days. **Registration forms received without full payment will not be processed until payment is received at Event Solutions.**

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For those who wish to register by fax or mail, the Advance Registration Form can be found at the center of this booklet. Please read the explanations and instructions on the back of the form, carefully.

The deadline for receipt of Early Registration fees is **December 28, 2003. After December 28, 2003, and on or before January 20, 2004,** registrations will be processed only at the Late-Registration rates. **As of January 21, 2004, you must pay the onsite/highest registration fees.** Because of limited seating capacity in the meeting rooms and hotel fire regulations, onsite registration may be limited. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2004.

Full Conference Registration includes one copy each of the Digest of Technical Papers, the Visuals Supplement (mailed in March) and the ISSCC 2004 DVD (mailed in June). **Student registration does not include the Visuals Supplement or the ISSCC 2004 DVD.** All students must present their Student ID at the Conference Registration Desk to receive the student rate. Anyone registering at the IEEE Member rate must also provide his/her IEEE Membership number.

The Onsite and Advance Registration Desks at ISSCC 2004 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except presenting authors, must pick up their registration materials at these desks as soon as they arrive at the hotel. **The Presenting Author for each paper must go directly to Golden Gate C1 to register and to collect their materials.**

REGISTRATION HOURS:

Saturday, February 14	4:00 PM to 7:00 PM **(Tutorial and Forum Attendees Only)**
Sunday, February 15	6:30 AM to 1:30 PM **(Tutorial and Forum Attendees Only)** 4:00 PM to 8:00 PM
Monday, February 16	6:30 AM to 2:00 PM
Tuesday, February 17	8:00 AM to 2:00 PM
Wednesday, February 18	8:00 AM to 1:00 PM
Thursday, February 19	7:00 AM to 11:00 AM **(Short Course and Forum Attendees Only)**

NEXT ISSCC DATES AND LOCATION

ISSCC 2005 will be held February 7-9, 2005 at the San Francisco Marriott Hotel.

FURTHER INFORMATION

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ISSCC participants can make their hotel reservations online from the Conference website at **www.isscc.org** by clicking on the Hotel-Reservation link to the San Francisco Marriott. The special ISSCC group rates are $195/single, $215/double, $235/triple, and $255/quad. All online reservations require the use of a credit card and online reservations are confirmed immediately. We suggest that you **print the page containing your confirmation number and reservation details, and bring it with you** when you travel to ISSCC. Once made and confirmed, your online reservation can be changed by calling the Marriott at 1-800-228-9290 (toll free) or 415-896-1600, or by faxing your change to the Marriott at 415-442-0141.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet or on the conference website. **Be sure to fill in your correct email address and fax number, if you wish to receive a confirmation by email or fax.** In order to receive the special group rates you will need to enter the following Group Codes: SSCSSCA for a single/double; SSCSSCB for a triple, and SSCSSCC for a quad.

Hotel Reservations must be received at the San Francisco Marriott no later than January 20, 2004 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached and/or after January 20th, the group rate will no longer be available. After the 20th, reservation requests will be filled at the best available rate.

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Additional ISSCC publications can be purchased at the Conference Registration Desk. Prices are lower for purchases collected onsite than for those publications ordered after the Conference, that must be shipped to the purchaser for an additional fee.

TECHNICAL-BOOK DISPLAY

A number of technical publishers will have a collection of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite at a discounted rate. The book display is in the Golden Gate Hall, located one level above the ballroom, and technical sessions. The Book Display will be open on Monday from 12:00 Noon to 8:00 PM; on Tuesday from 10:00 AM to 8:00 PM; and on Wednesday from 10:00 AM to 5:00 PM.

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Reserve a space for this Tuesday, 17 February luncheon presentation. Contact Phyllis Buchta at p.buchta@ieee.org by February 6. Space is available on a first-come, first-served basis.

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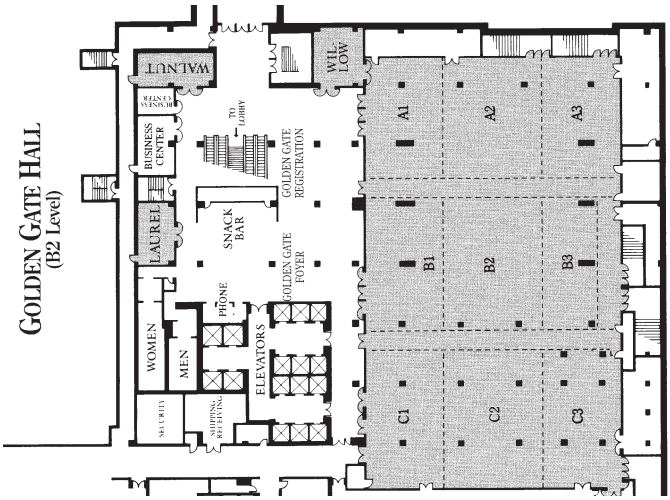
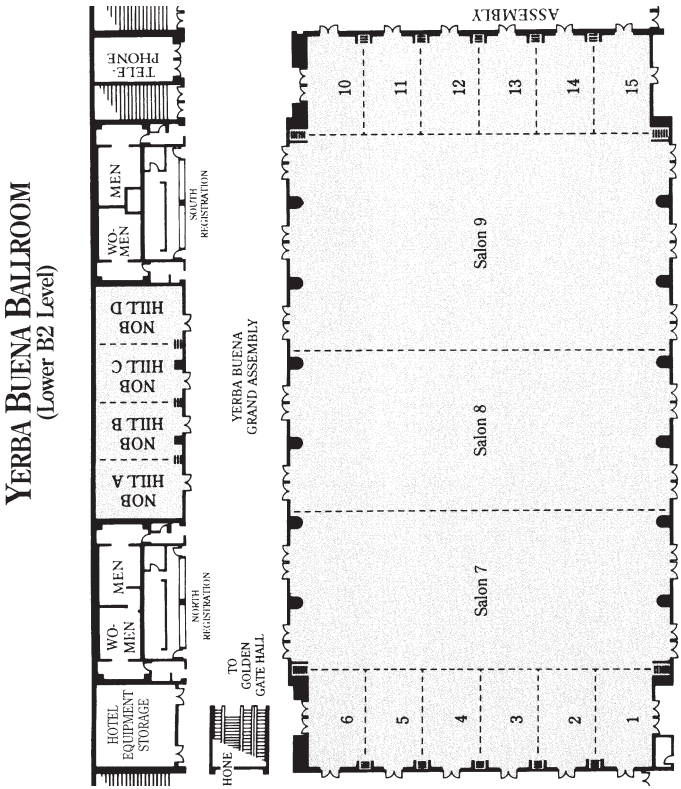
The Conference Book Display and Social Hour will be held in Golden Gate Hall. All Conference Technical Paper Sessions are in the Yerba Buena Ballroom. Layouts appear below:





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