IEEE SOLID-STATE CIRCUITS SOCIETY/IEEE SAN FRANCISCO SECTION, BAY AREA COUNCIL/UNIV. OF PA.

ADVANCE PROGRAM

2005 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 6, 7, 8, 9, 10

CONFERENCE THEME:

Entering the Nanoelectronic Integrated-Circuit Era

SAN FRANCISCO MARRIOTT HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY: 2 FORUMS: High-Frequency Clock Generation; Advanced DRAM; 8 TUTORIALS
3 SPECIAL-TOPIC SESSIONS: Powerline LAN; Processor Power Problems; 3D Integration

THURSDAY ALL-DAY: 3 FORUMS: Imager Characterization; Nanoscale Design; Automotive Circuits; SHORT COURSE: RF Circuits & Systems

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for the presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers, working at the cutting edge of IC design and application, to maintain technical currency and to network with leading experts.

CONFERENCE HIGHLIGHTS

On Sunday, February 6, the day before the official opening of the Conference, ISSCC 2005 offers:

- A choice of up to 3 of a total of 8 Tutorials
- Two ISSCC Advanced Solid-State Circuit Design Forums:
- GIRAFE (GHz Radio Front End) Advanced Solid-State Circuit Design Forum: "Clock and Frequency Generation for Wireless and Wireline Applications"
- Memory Circuit Design Forum: "Advanced Dynamic-Memory Design"

The 90-minute tutorials offer background information and a review of the current state-of-the-art in specific circuit-design topics. In the all-day Advanced Solid-State Circuit Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, three Special-Topic Evening Sessions addressing next-generation circuit-design challenges will be offered, starting at 7:30PM:

- Powerline LAN
- When Processors Hit the Power Wall
- 3D System-on-Package
- The Special-Topic Evening Sessions are open to all ISSCC attendees.

On Monday, February 7, a record ISSCC technical program of 233 papers in 6 parallel session, starts with 3 plenary talks: "Nanoelectronics for the Ubiquitous Information Society"; "Ambient Intelligence: Broad Dreams and Nanoscale Realities"; Innovation and Integration in the Nanoelectronics Era". A Social Hour, open to all ISSCC attendees, will follow the afternoon session. The Social Hour will feature posters from the winners of the 2003-04 and 2004-05 joint DAC-ISSCC student-design contest. Monday evening features two panel discussions and a Special-Topic Evening Session: Highlights of the Symposium on VLSI Technology, in which some of ISSCC-relevant papers from the Symposium are presented to intrigue and inspire ISSCC attendees.

On Tuesday, February 8, ISSCC 2005 offers morning and afternoon technical sessions, followed by a Social Hour, a Special-Topic Evening Session on Nanoscale SRAM and two panel discussions. Wednesday, February 9, features morning and afternoon technical sessions.

On Thursday, February 10, ISSCC 2005 offers a choice of four events:

- An ISSCC Short Course: "RF Circuit Design from Technology to Systems". Two sessions of the Short Course will be offered, with staggered starting times.
- An ISSCC Advanced Solid-State-Circuit-Design Forum "Automotive Technology and Circuits".
- An ISSCC Advanced Solid-State-Circuit-Design Forum on Microprocessor Design: "Robust Design Solutions for Nanoscale Circuits: From DFM through End-of-Life".
- An ISSCC Advanced Solid-State-Circuit-Design Forum: "Characterization of Solid-State Image Sensors".

Registration for the Thursday events is limited. Registration will be filled on a first-come first-served basis. Use of the ISSCC Web-registration site (www.isscc.org) is strongly encouraged. Web registrants will be provided with immediate confirmation on registration for Tutorials, Advanced Solid-State-Circuit-Design Forums, and the Short Course.

CONTENTS

TUTORIALS

T1: INTEGRATED POWER MANAGEMENT

As circuit-design power requirements never align well with the available power source, power management along with efficiency and cost are critical elements in all system designs. This tutorial provides an overview of dc/dc converter techniques (switched-inductor, switched-capacitor, linear-regulator, and compound architectures), and offers a discussion of the pros and cons for each. The characteristics of today's portable power sources, lithium-ion batteries being the most common, are also discussed. Finally, the focus is on circuit techniques which may be integrated into CMOS Systems-on-a-Chip when multiple supply voltages are required.

Instructor: Roy Kaller is Vice President of Engineering at SMSC in Phoenix, AZ where he is responsible for analog technology development and design automation. He joined SMSC as part of the company's acquisition of Gain Technology Corporation in June 2002. Prior to joining Gain Technology in 2000, he was the founder and director of National Semiconductor's Power Management design center in Grass Valley, CA. From 1992 until 1995, Roy was a design engineering manager for Silicon Systems, and he started his career at Burr-Brown Corporation in 1983 where he developed a broad range of products including precision op-amps, MUXes, DACs, and ADCs. Roy has been a member of ISSCC Analog Sub-committee since 2002, has published eight papers and holds one patent in analog integrated circuits and solid state chemistry. Roy earned his BSEE from the University of Arizona and is a graduate of the University's Arizona Executive Program.

T2: INTRODUCTION TO I/O DESIGN FOR DIGITAL SYSTEMS

This tutorial gives an introduction to digital I/O circuit design. Topics include essential transmission line theory, elements of transmitter and receiver design (boundary-scan blocks, up/down converters, line drivers and receivers, and ESD protection structures). In addition to more advanced topics such as differential I/O structures, on-chip termination, PVT compensation and clocking for I/O interfaces are discussed.

Instructor: Thucydides Xanthopoulos received his BS, MS, and PhD in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1992, 1995, and 1999, respectively. From 1999 to 2001 he was a consulting engineer with the Alpha Development Group, Compaq Computer in Shrewsbury, MA, where he designed the clock-generation and distribution network for the Alpha 21364 server processor (EV7). Since 2001, he has been a principal member of Technical Staff with Cavium Networks in Marlboro, MA, where he co-leads silicon implementation of security and network services processors and is primarily responsible for I/O, clocking, power distribution, and package design.

T3: RF MEMS: Devices, Circuits and Packaging

RF MEMS devices including micromechanical switches, resonators, 3D high-Q inductors and micromachined antennas can enable ultra-low-power wireless architectures in ultra-small microsystems. High-Q micro-mechanical resonators in the VHF and UHF range have become available, and wafer-level-packaged MEMS switches have demonstrated reliable operation for billions of cycles. This tutorial presents an introduction to RF MEMS devices, reviews the latest advances in the field, and discusses their manufacturing, performance and packaging.

Instructor: Farrokh Ayazi is an Assistant Professor in the School of ECE at Georgia Tech. He received his BSEE from the University of Tehran, in 1994, and MSEE and PhD degrees from the University of Michigan, in 1997 and 2000, respectively. His research interests are in the areas of micro-/nano-electromechanical resonators, RF MEMS, VLSI Analog IC's, MEMS inertial sensors and packaging. He is a 2004 recipient of the NSF CAREER Award, the 2004 Richard M. Bass Outstanding Teacher Award, and the Georgia Tech College of Engineering Cutting Edge Research Award for 2001-2002. He has served on the technical program committees of the IEEE ISSCC, MEMS, and Sensors conferences.

T4: PHASE-CHANGE MEMORY

Phase-change memory (PCM, also called OUM or PRAM), is an emerging non-volatile-memory technology that has the potential to improve the performance compared to Flash - write throughput (versus NOR), random read access time and throughput (versus NAND, direct write, bit granularity, endurance) - and to be scalable beyond Flash. The basic concepts of PCM, the memory cells, the electrical characteristics and the scaling perspective are reviewed. Key design aspects and challenges, related to the MOS-selected cell array as well as to the BJT-selected array, including examples and published results, are discussed.

Instructor: Giulio Casagrande graduated in Electronic Engineering in 1977 at the University of Padova, Italy. He joined ST Microelectronics, Milano, as a designer of EPROMs and EEPROMs and then he led the design and engineering team that developed the first generations of Flash memories in ST. He is presently Director of R&D of the Memory Products Group at ST Microelectronics, concentrating on advanced Flash design solutions for embedded applications, assessment and disruptive emerging memories, CAD and design methodology. He is a member of ISSCC Memory Sub-Committee.

T5: DSP CIRCUIT TECHNOLOGIES FOR THE NANOSCALE ERA

Some of the sub-65nm scaling challenges and new paradigm shifts in next-generation DSP architectures are discussed. Emerging trends in wireless and embedded DSP industry including special-purpose multimedia/communication accelerators, co-processor arrays, and reconfigurable DSP engines are reviewed. Energy-efficient arithmetic and logic circuit techniques, static/dynamic supply scaling, and multi-supply/multi-threshold design for switching and leakage energy reduction are described. Dedicated hardware accelerators and data-path building blocks for enabling high MOPS/W in specialized DSP tasks are presented. Many chip design examples and their results/trade-offs are be shown as part of this tutorial.

Instructor: Ram Krishnamurthy is a Senior Staff Research Engineer at Intel Corporation's Circuit Research Laboratories in Hillsboro, OR, where he leads the high-performance and low-voltage circuits research group. He holds 41 patents issued and published over 75 papers. He serves on the SRC ICSS task force and the ISSCC, CICC, and SoC program committees. Since 1999 he serves as an adjunct faculty member at Oregon State University, where he teaches VLSI system design. He received his PhD from Carnegie Mellon University in 1998

T6: NANOTECHNOLOGY 101

This tutorial provides the attendee with an introduction to the emerging opportunities in novel nanoscale devices and fabrication techniques with particular emphasis on the implications for circuit and system designers. Topics covered include: fundamentals of device physics and materials science at the nanoscale, the ITRS emerging research devices (memory & logic), nanotubes, nanowires, and nanoparticles, molecular devices, and nanofabrication techniques and their impact on device layout. An assessment of the level of maturity for the proposed devices will be given.

Instructor: H.-S. Philip Wong joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, in 1988. While at IBM Research, he was a Senior Manager having the responsibility of shaping and executing IBM's strategy on nanoscale science and technology and semiconductor technology. In September, 2004, he joined Stanford University as a Professor of Electrical Engineering.

T7: POLAR MODULATORS FOR LINEAR WIRELESS TRANSMITTERS

As spectral efficiency becomes increasingly important, most emerging wireless standards apply both amplitude and phase modulation and therefore require linear modulators. Polar modulators can produce more spectrally pure signals with higher power efficiency than traditional linear modulators. This tutorial provides an introduction to the concept of polar modulation and an in-depth look at some of the implementation challenges. The following topics are covered at both system and circuit levels:

(1) An overview of linear wireless transmitters
(2) Polar modulator implementation, including impairment mechanisms and limitations are detailed.
(3) Case studies of practical modulators for EDGE are treated

Instructor: Antonio Montalvo has been the director of Analog Devices Design Center in Raleigh, NC, since 2000. He is also an Adjunct Professor at North Carolina State University. He was with Ericsson from 1995 to 2000 where he led the RF IC group and with Advanced Micro Devices from 1987 to 1991 where he was involved with the design of Flash memories. He received a PhD from North Carolina State University in 1995, an MSEE from Columbia University in 1987 and a BS Physics from Loyola University in 1985.

T8: HIGH-SPEED ELECTRICAL INTERFACES: STANDARDS AND CIRCUITS

The physical-level standard specification space (including standards under development) and challenges in multi-gigabit range high-speed electrical interfaces area, such as XFI, CEI , XAUI, Fiber-Channel, SAS, SATA, etc. are reviewed. Jitter requirements, signal amplitude, impedance, S-parameter specifications and transmission channel representation, along with equalization techniques, are studied. Block diagrams and circuit solutions are also discussed. This tutorial helps to understand IC design parameters, their link to standard specifications, and current and future challenges in wireline design for multi-gigabit electrical interfaces.

Instructor: Yuriy M. Greshishchev, is a Technical Advisor on high-speed circuit design for wireline communications at PMC Sierra, Ottawa, Canada,. His design experience is in multi-gigabit rate CMOS, SiGe, III-V circuits for telecommunications and data communications applications area. He has been involved in XFI, fiber channel , SAS, RIO physical level standard technical groups. Yuriy is a member of ISSCC Technical Program Committee for five consecutive years. He presented an ISSCC Tutorial on "Front-end Circuit Design for Optical Communications" in 2001. He has co-authored two books and numerous technical papers on the area of high-speed communication circuit design and data converters. He received his PhD degree in Electrical and Computer Engineering from V.M. Glushkov Institute of Cybernetics, Microelectronics Division, Kiev, Ukraine, in 1984.

GIRAFE FORUM

F1 **Clock and Frequency Generation for Wireline and Wireless Apllications**

(Salon 9)

Organizer: **Rudolf Koch**, *Infineon, Munich, Germany*

Committee:
Franz Dielacher, *Infineon, Villach, Austria*
Trudy Stetzler, *Texas Instruments, Stafford, TX*
Charles Chien, *SST Communications, Santa Monica, CA*
John Long, *Delft University of Technology, Delft, The Netherlands*
Roger Minear, *Agere Systems, Wyomissing, PA*
Takehiko Nakao, *Toshiba, Kanagawa, Japan*
Tom Schiltz, *Linear Technology, Colorado Springs, CO*

The quality of the spectrum of clock generators has a crucial impact on the performance of communications systems. Different system concepts may yield widely disparate specifications for VCOs and PLLs even for the same application.

Trade-offs between contradictory requirements, such as low phase noise and wide bandwidth, are needed to fulfill and optimize system specifications.

The morning sessions of this forum deal with fundamental aspects of frequency generation. The first two speakers treat design criteria for clock generation for wireless and wireline systems. The modeling of noise sources in oscillator circuits is addressed by the next three presenters.

In the afternoon sessions, each of the three speakers discusses analysis and design of PLL frequency synthesizers, fractional-N frequency synthesizers, and spread-spectrum PLLs for communication applications.

Finally, at the end of the afternoon, the speakers will assemble in a panel format to field questions and comments from the audience.

Sunday, February 6th 8:00 AM

Forum Agenda:

Time	Topic
8:00	Continental Breakfast
8:30	***Welcome and Introduction*** **Rudolf Koch,** *Infineon, Munich, Germany*
08:35	***Formulating Design Criteria for Frequency Generation for Wireless Applications*** **Derek Shaeffer,** *Aspendos Communications, San Jose, CA*
09:05	***Formulating Design Criteria for Clock Generation for Wireline Applications*** **Takehiko Nakao,** *Toshiba, Kanagawa, Japan*
09:35	***Multiphase Ring Oscillators and Oscillator Phase Noise Modelling Techniques*** **Robert Renninger,** *Agere, Allentown, PA*
10:05	Break
10:35	***VCO Design and Phase Noise Modelling*** **Ali Hajimiri,** *California Institute of Technology, Pasadena, CA*
11:35	***Supply and Substrate Noise in VCOs*** **Jan Craninckx,** *IMEC, Leuven, Belgium*
12:05	Lunch
1:30	***System Analysis, Simulation, Design and Optimization of PLL Frequency Synthesizers for Communication Systems*** **Cicero Vaucher,** *Philips, Eindhoven, The Netherlands*
2:30	***Design, Simulation, and Bandwidth Extension Methods for Fractional-N Frequency Synthesis*** **Michael Perrott,** *Massachsetts Institute of Technology, Cambridge, MA*
3:30	Break
4:00	***Spread Spectrum PLLs; Direct Modulation with Wideband PLLs*** **Ivan Bietti,** *STMicroelectronics, Pavia, Italy*
5:00	Panel Discussion
5:30	Conclusion

MEMORY FORUM

F2: Advanced Dynamic Memory Design

(Salon 7)

Organizer/Chair: **Katsuyuki Sato,** *Elpida., Tokyo, Japan*
Committee: **Jinyong Chung,** *POSTECH, Pohang, Korea*
Young-Hyun Jun, *Samsung, HwaSung, Korea*
Terry Lee, *Micron Technology, Boise, ID*
John Barth, *IBM, Essex Junction, VT*
Martin Brox, *Infineon, Munich, Germany*
Takayuki Kawahara, *Hitachi, Tokyo, Japan*

DRAM is widely used not only as the main memory in PCs and servers, but also as the active memory in consumer products such as digital cameras, TVs, and mobile phones. Consequently, cost reduction is a paramount design consideration. Each new generation of DRAM has applied finer-pattern technology to cut costs. In this sense, new DRAM designs are leading-edge- technology-driven. This forum informs the audience about current DRAM technology and its associated circuit issues.

Jinyong Chung provides an overview of DRAM architecture, from basic cell operation to a chronological evolution of cell configuration. Cell leakage, soft errors related to alpha and neutron particles, and bit-line coupling are treated. Test-time-reduction methods to screen defective cells are described, and redundancy techniques to replace defective cells, rows or columns are developed. Size and voltage issues associated with further scaling are also discussed.

High-speed DRAM architecture and design is the focus of the second talk by Young-Hyun Jun. The key to high-speed operation is the internal clock-generation process in which DLLs and PLLs are vital. From basic circuit concepts to current practice, DLL and PLL design issues are discussed. The application of DLL and PLL techniques in graphics RAM and DDR2 are among the products illustrated. The new technologies needed to realize future high-speed DRAMs are presented.

The DRAM I/O interface is the subject of the talk by Terry Lee. Cost minimization, test-time reduction, the test of multiple devices in parallel, low-power multi-drop busses and upgradability are among the critical features needed in DRAM applications. This causes DRAM I/O to differ from data communications and backplane signaling. The theme of this presentation is the circuit and system design issues related to high-speed DRAM interfaces.

On-chip SRAM cache density is restricted by the limitations in SRAM size. High-performance embedded DRAM is aimed at applications employing on-chip cache. John Barth describes the technology of embedded DRAM to realize high speed and a wide internal bus with a minimum die penalty while suppressing noise. Structures for high-speed embedded DRAM testing are described, and design-for-test techniques are introduced.

Martin Brox focuses on DRAM for mobile applications including browsers, cameras, and video-conferencing. These all require high-density DRAMs. The talk treats the design of mobile RAM to meet the unique requirements necessitated by such applications.

Sunday, February 6th 8:00 AM

Takayuki Kawahara introduces the design of sub-1V DRAMs which play critical roles in reducing dissipation in MPU/SoC/SiP for power-aware systems. However, four major challenges need be faced to achieve this: reducing leakage currents; maintaining the signal charge of memory cells; reducing speed variations caused by deviations of threshold voltage, and reducing the cell size. He presents current advances to deal with these issues in sub-1V DRAMs, and solutions for nanoscale LSI system.

Tomoyuki Ishii introduces future challenges for DRAM technology in the nanoscale process generation. From an operational-stability point-of-view, DRAM has better scalability than SRAM. However, the standard 1T1C type DRAM has serious difficulties in maintaining adequate retention time and storage capacitance, as the process scales. Several non-1T1C approaches for scalable DRAM are introduced, along with new device structures. Investigation of a memory cell using only 10 electrons per bit is discussed.

Forum Agenda:

Time	Topics
8:00	Continental Breakfast
8:30	***Introduction & Updates*** **Jinyong Chung,** *POSTECH, Pohang, Korea*
9:15	***High-Speed DRAM Design*** **Young-Hyun Jun,** *Samsung, HwaSung, Korea*
10:15	Break
10:30	***DRAM I/O Interface*** **Terry Lee,** *Micron Technology, Boise, ID*
11:30	***High Performance Embedded DRAM and test structures*** **John Barth,** *IBM, Essex Junction, VT*
12:30	Lunch
1:15	***DRAM Design for Mobile Applications*** **Martin Brox,** *Infineon, Munich, Germany*
2:15	***Sub-1V DRAM Design*** **Takayuki Kawahara,** *Hitachi, Tokyo, Japan*
3:15	Break
3:30	**DRAM in Nanoscale Era** **Tomoyuki Ishii,** *Hitachi, Tokyo, Japan*
4:30	Conclusion

SPECIAL-TOPIC EVENING SESSIONS

SE1: Powerline LAN: Is There a Concrete Wall Dividing Wireless from Wireline?

(Salon 8)

Organizer: **Mark Ingels,** *STMicroelectronics Zaventem, Belgium*
Chair: **Michael Green,** *University of California, Irvine, CA*

From offices to coffee houses, wireless LANs have become ubiquitous within the United States. However, there are many situations where a wireless signal encounters attenuation within a building. For example concrete walls and ceilings are known to impede RF transmission. In such situations Power Line Communication (PLC) is emerging as an alternative technology for high-speed data communication within the home. This new technology can assist or even replace the wireless systems as needed. In this Special-Topic Evening session, the significance of PLC will be revealed. Infrastructural aspects that may affect the choice between wireline and wireless for the transmission of broadband data is addressed and the advantages and needs for powerline systems is demonstrated. The session gives an overview and comparison of various available and emerging PLC technologies and practical systems are presented.

Sunday, February 6th 7:30 PM

SE1: Powerline LAN: Is There a Concrete Wall Dividing Wireless from Wireline?

Time	Topics
7:30	***Broadband Powerline Multimedia Home Networking: Advantages and Challenges,*** **Haniph A. Latchman,** *University of Florida Gainesville, FL*
8:00	***OFDM for Powerline Communications*** **Jim Petranovich,** *Conexant Systems, San Diego, CA*
8:30	***Performance Analysis of a CDMA Chipset for InHouse Broadband Powerline Communications***, **Vincent Buchoux**, *LEA, Courbevoie, France*
9:00	***Remote Control via Powerline,*** **Claudio Cantoro,** *Dora, Milano, Italy*

SPECIAL-TOPIC EVENING SESSIONS

SE2: When Processors Hit the Power Wall (or "When the CPU hits the fan").

(Salon 7)

Organizer: **Sam Naffziger,** *Hewlett Packard, Fort Collins, CO*
CO - Organizer: **James Warnock,** *IBM, Yorktown Heights, NY*
CO - Organizer: **Herbert Knapp,** *Infineon, Munich, Germany*

Power consumption and heat removal have become first-order limiters to "Moore's Law" in regards to the growth of processor performance. This limitation has bubbled up from mobile devices to desktop systems and now even server processors are investing heavily in techniques that manage and reduce power consumption. The result is a fundamental shift in how circuit designers and architects attempt to achieve performance from each new design generation. No aspect of the processor design ecosystem goes untouched: silicon process technology, circuit design, computer architecture, packaging and cooling are all facing fundamental shifts in priorities and methods. The power consumption problem on leading edge processors and the possible technology directions in architecture, circuits and cooling are explored in this special-topics session. The first step to solving a problem is to understand it better by identifying it. So we begin by examing where the power is consumed on a leading edge processor and how it varies with time and workload. The next talk involves a look at one of the frontiers of VLSI design: the many opportunities present in creating "environmentally aware" chips that measure and react to their environment to optimize power, performance and other tradeoffs. Lastly two of the industries leading architects discuss the meaning of "low-power architecture", and some of the brightest opportunities for power efficiency. The session concludes with a look by one of the leading innovators in cooling technology at how waste heat that byproduct of computation can be removed efficiently.

Time	Topic
7:30 pm	***Spatially Resolved Imaging Of Microprocessor Power*** **Hendrik Hamann,** *IBM, Yorktown Heights, NY*
8:00 pm	***Adaptive Techniques for Managing Power Consumption*** **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*
8:30 pm	***Low-Power for High-Performance PC Compatible Processors*** **David R. Ditzel,** *Transmeta Corporation, Santa Clara, CA*
9:00 pm	***Power-Efficient Stream Architectures*** **William Dally,** *Stanford University and Stream Processors, Palo Alto, CA*
9:30 pm	***Advanced Cooling for High Performance VLSI*** **Ken Goodson,** *Stanford University, Palo Alto, CA*

SE3: Integration in the 3rd Dimension: Opportunities and Challenges

(Salon 9)

Organizer: **Larry Pileggi**, *Carnegie Mellon University, Pittsburgh, PA*
Chair: **Werner Weber,** *Infineon, Munich, Germany*

While it is apparent that integrating electronic systems beyond two dimensions can potentially provide great advantages, it is less obvious what the most promising approaches for such integration will be with future technologies. The papers in this session will describe and evaluate various opportunities and challenges for vertical integration of integrated electronic systems. Cost considerations are considered prominently, as well as the potential performance improvements that are realized. Various integration concepts are considered for integrated systems which include digital logic, analog circuits and sensors. The session begins with a cost-based argument for 2.5D integration based on stacking of traditional 2D integrated circuits. Results indicate a performance advantage as well due to the shortening of long interconnect wiring when integrating in 3D. A subsequent paper applies similar performance reasoning for "folding" ICs into multiple active layers to reduce the lateral dimensions. Exciting opportunities are further explored for expanding in the 3rd dimension via RF-MEMS components that are built directly on top of monolithic ICs. Then, the session closes with a description of how wafer-scale integration in the third dimension is used to construct antennas and other microwave components that would otherwise be challenging, if not impossible, for traditional monolithic design.

Time	Topic
7:30	***Exploring Cost and Performance Advantages of 2.5-D Integration*** **Wojciech Maly,** *Carnegie Mellon University, Pittsburgh, PA*
8:00	***3D Integration's Architectural and Circuit Design Opportunities*** **Wilfried Haensch,** *IBM, Yorktown Heights NY*
8:30	***Above IC & embedded RF MEMs platform for SoC Integration: Status and Prospect*** **Pascal Ancey,** *STMicroelectronics, Crolles Cedex, France*
9:00	***A Wafer Level Integration Technology for On-Wafer Antennas and Microwave Components*** **Hermann Schumacher,** *University of Ulm, Ulm, Germany*

SESSION 1 SALON 7-9

PLENARY SESSION - INVITED PAPERS

Chair: **Timothy Tredwell,** *Eastman Kodak, Rochester, NY*
ISSCC Executive-Committee Chair
Associate Chair: **Ian Young,** *Intel, Hillsboro, OR*
ISSCC Program-Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:30AM**

1.1 Nanoelectronics for the Ubiquitous Information Society

8:40AM

Daeje Chin, *Minister of Information and Communications, Korea*

Nanoelectronics will open up both new opportunities and new challenges. Meanwhile, it has been successfully used in mass production of gigabit memories, including Flash and DRAM, and in field-emission display (FED) with carbon nano-tubes. The technical challenge is to deal with process and device parameter variation, while the economic challenge is to reduce the high cost of fabrication. One way to overcome these technical and economic uncertainties is to organize a tight collaboration of the device industry with system and service industries, to distribute the risk, and to maximize the total social benefit. The “IT 839 Strategy” of the Korean Government is an example of such a program to enhance cooperation amongst service, system, and device industries, to speed up the use of nanoelectronics for the realization of a ubiquitous information society. In such a society, information technology (IT) enables everyone to enjoy daily life without awareness of IT itself. This is made possible by the "Invisible Silicon" that resides within almost everything in our society, to sense, analyze, and control ourselves and our environment. Nanoelectronics allows the mass production of such new silicon. RFID chips and sensor networks are examples of "Invisible Silicon", which will integrate nano-electro-mechanical systems and RF technology, as well as low-power and multimedia SoCs. These technologies will facilitate future IT, and change our world, just as fourth-generation mobile-phone developments are leading us to the ubiquitous information society.

ISSCC, SSCS, JSSCC, & IEEE AWARD PRESENTATIONS

9:30AM

BREAK 10:00 AM

1.2 Ambient Intelligence: Broad Dreams and Nanoscale Realities

10:15AM

Hugo De Man, *Senior Research Fellow, IMEC; Professor, Katholieke Universiteit Leuven, Belgium*

Ambient Intelligence (AmI) is a vision of a world in which people will be surrounded by networks of intelligent devices that are sensitive to, and adaptive to, their needs. This concept implies a consumer-oriented industry driven by software from the top, and enabled (and constrained) by nano-scale physics at the atomic level. **"more-Moore"** will be needed to deliver the Giga-ops computation and GHz communication capabilities required for stationary and wearable devices. But AmI also creates new challenges at the architectural and physical levels. To make AmI possible, AmI devices need two-orders-of-magnitude-lower power dissipation than

today's microprocessors, at one-twentieth of the cost. But these requirements conflict with the embedded programmability needed for personalization and adaptation to new services. We will focus on emerging techniques for bridging this gap between software-centric systems and power-efficient platform architectures for AmI devices.

A second challenge is to cope with the fact that nano-scale physical phenomena are in conflict with the traditional "nice and predictable" digital abstractions now used for complexity management. Techniques for coping with uncertainty and signal degradation, while achieving better-than-worst-case design, will be discussed.

Finally, one must realize that to facilitate AmI, **"more-than-Moore"** technology is required, for example, for the design of autonomous wireless sensor networks. Correspondingly, attention will be paid to novel combinations of technologies above and around CMOS, for the design of ultra-low-power, ultra-simple sensor motes for AmI.

1.3 Innovation and Integration in the Nanoelectronics Era
11:05AM

Sunlin Chou, *Senior Vice President and General Manager, Technology and Manufacturing Group, Intel, Hillsboro, OR*

Demand for electronics continues to grow as new products combine and enhance computing, communications, and digital capabilities. Hardware and software are evolving to enable new applications and usage modes, by offering features such as multitasking, parallel processing, mobility and wireless connectivity. Integration at both component and product platform levels, and efficient use of power, will become more important. These call for holistic solutions involving systems, circuits, processes, devices, and packaging. Many techniques to improve power efficiency have been developed and more will emerge. Silicon technology and scaling remain keys to progress, with transistors and circuit elements already at nanoscale dimensions. Innovation will accelerate as nanotechnology further renews and extends silicon technology. Skillful integration of new materials, processes, and device structures will be essential. Successful nanoelectronics companies will excel in innovation and integration, extend Moore's Law into and beyond the next decade, and drive the development of future growth opportunities.

SESSION 2 SALON 1-6

NON-VOLATILE MEMORY

Chair: **Yair Sofer,** *Saifun Semiconductors, Netanya, Israel*
Associate Chair: **Yukihito Oowaki,** *Toshiba, Kawasaki, Japan*

2.1 A 146mm² 8Gb NAND Flash Memory in 70nm CMOS

1:30 PM

T. Hara[1], K. Fukuda[1], K. Kanazawa[1], N. Shibata[1], K. Hosono[1], H. Maejima[1], M. Nakagawa[1], T. Abe[1], M. Kojima[1], M. Fujiu[1], Y. Takeuchi[1], K. Amemiya[1], M. Morooka[1], T. Kamei[2], H. Nasu[2], K. Kawano[2], C-M. Wang[3], K. Sakurai[1], N. Tokiwa[1], H. Waki[1], T. Maruyama[1], S. Yoshikawa[1], M. Higashitani[3], T. Pham[3]
[1]Toshiba, Yokohama, Japan
[2]SanDisk, Yokohama, Japan
[3]SanDisk, Sunnyvale, CA

A 146mm² 8Gb NAND flash memory with 4-level programmed cells is fabricated in a 70nm CMOS technology. A single-sided pad architecture and extended block-addressing scheme without redundancy is adopted for die size reduction. The programming throughput is 6MB/s and is comparable to binary flash memories.

2.2 An 8Gb Multi-Level NAND Flash Memory in a 63nm CMOS Process

2:00 PM

D-S. Byeon, S-S. Lee, Y-H. Lim, J-S. Park, W-K. Han, P-S. Kwak, D-H. Kim, D-H. Chae, S-H. Moon, S-J. Lee, H-C. Cho, J-W. Lee, J-S. Yang, Y-W. Park, D-W. Bae, J-D. Choi, S-H. Hur, K-D. Suh
Samsung, Hwasung, Korea

An 8Gb multi-level NAND flash memory is fabricated in a 63nm CMOS technology with shallow trench isolation. The cell and chip sizes are 0.02μm² and 133mm², respectively. Performance improves to 4.4MB/s by using the 2x program mode and by decreasing the cycle time from 50ns to 30ns. This also improves the read throughput to 23MB/s.

2.3 Enhanced Write Performance of a 64Mb Phase-Change RAM

2:30 PM

H-R. Oh, S. KANG, B. Cho, W. Cho, B-G. Choi, H. Kim, K-S. Kim, D-E. Kim, C-K. Kwak, H-G. Byun
Samsung, Hwasung, Korea

A 1.8V 64Mb Phase-Change RAM with improved write performance is fabricated in a 0.12μm CMOS technology. The improvement of RESET and SET distributions is based on cell current regulation and multiple step-down pulse generators. The read access time and SET-write time are 68ns and 180ns, respectively.

BREAK 3:00 PM

2.4 A 128Mb NOR Flash Memory with 3MB/s Program Time and Low-Power Write Using an In-Package Inductor Charge-Pump

3:15 PM

R. Sundaram, J. Javanifard, P. Walimbe, B. Pathak, R. Melcher, P. Wang, J. Tacata
Intel, Folsom, CA

Improved performance of flash memories requires programming more cells in parallel. This design uses an inductive pump to transfer the energy to a capacitor to achieve the needed voltage. The discrete inductor is bonded atop the die which also includes the control circuitry. With an inductive pump, the current saving in the program mode is 47.5mA compared to a capacitive pump.

2.5 A 125MHz Burst-Mode Flexible Read-While-Write 256Mb NOR Flash Memory

3:45 PM

C. Villa[1], D. Vimercati[1], S. Schippers[1], E. Confalonieri[1], M. Sforzin[1], S. Polizzi[2], M. La Placa[2], C. Lisi[1], A. Magnavacca[1], E. Bolandrina[1], A. Martinelli[1], V. Dima[1], A. Scavuzzo[2], B. Calandrino[2], N. Del Gatto[1], M. Scardaci[3], F. Mastroianni[1], M. Pisasale[3], A. Geraci[1], M. Gaibotti[1], M. Sali[1]
[1]STMicroelectronics, Agrate Brianza, Italy
[2]STMicroelectronics, Palermo, Italy
[3]STMicroelectronics, Catania, Italy

A 1.8V 256Mb 2b/cell NOR flash memory is designed in a 130nm technology. A fast gate-voltage-ramp constant-current-reading concept is implemented to obtain a robust read-while-write/erase function and 125MHz burst read frequency.

2.6 A 90nm 512Mb 166MHz Multi-Level Cell Flash with 1.5MB/sProgramming

4:15 PM

M. Taub[1], R. Bains[1], H. Castro[1], S. Eilert[1], R. Fackenthal[1], C. Haid[1], K. Parat[2], S. Peterson[1], A. Proescholdt[1], K. Ramamurthi[1], P. Ruby[1], M. Szwarc[1], D. Young[1]
[1]Intel, Foslom, CA
[2]Intel, Santa Clara, CA

A 2b/cell flash memory in 90nm triple-well CMOS technology achieves 1.5MB/s programming and 166MHz synchronous operation. The design features 2-row programming, optimized program control hardware, 3 transistor x-decoder with negative deselected rows and configurable output buffers. The die is 42.5mm^2 with a cell size of 0.076μm^2.

2.7 126mm^2 4Gb Multi-Level AG-AND Flash Memory with 10MB/s Programming Throughput

4:45 PM

H. Kurata[2], Y. Sasago[2], K. Otsuga[2], T. Arigane[2], T. Kawamura[2], T. Kobayashi[2], H. Kume[3], K. Homma[3], K. Kozakai[3], S. Noda[3], T. Ito[3], M. Shimizu[3], Y. Ikeda[3], O. Tsuchiya[3], K. Furusawa[3]
[1]Hitachi, Kokubunji, Japan
[2]Hitachi, Tokyo, Japan
[3]Renesas Technology, Tokyo, Japan

A 4Gb flash memory, fabricated in 90nm CMOS technology, results in a 126mm^2 chip size and a 0.0162μm^2/b cell size. Address and temperature compensation methods control the resistance of the inversion-layer local bit-line. Programming throughput of 10MB/s is achieved by using self-boosted charge injection scheme.

CONCLUSION 5:15 PM

SESSION 3 SALON 7

BACKPLANE TRANSCEIVERS

Chair: **Mehmet Soyuer,** *IBM, Yorktown Heights, NY*
Associate Chair: **Muneo Fukaishi,** *NEC, Kanagawa, Japan*

3.1 A 5Gb/s NRZ Transceiver with Adaptive Equalization for Backplane Transmission

1:30 PM

N. Krishnapura, M. Barazande-Pour, Q. Choudhry, J. Khoury, K. Lakshimikumar, A. Aggarwal
Vitesse Semiconductor, Somerset, NJ

The proposed 5Gb/s transceiver has a transmitter with 2-tap pre-emphasis and an adaptive receiver with 1-tap feedforward and 3-tap decision feedback equalization. The quad transceiver occupies 12mm^2 in 0.13µm CMOS, consumes 2.1W from 1.2V, and has a BER <10^{-15} over 4 pairs of 1-meter backplane trace with crosstalk.

3.2 A 6.4Gb/s CMOS SerDes Core with Feedforward and Decision-Feedback Equalization

2:00 PM

M. Sorna[1], T. Beukema[2], K. Selander[1], S. Zier[1], B. Ji[1], P. Murfet[3], J. Mason[3], W. Rhee[2], H. Ainspan[2], B. Parker[2]
[1]IBM, Hopewell Junction, NY
[2]IBM, Yorktown Heights, NY
[3]IBM, Hursley, United Kingdom

A 4.9 to 6.4Gb/s 2-level SerDes ASIC I/O core designed in 0.13µm CMOS uses a 4-tap FFE in the transmitter and a 5-tap DFE with receiver AGC. Error-free operation is achieved on channels with over 30dB loss at the half-baud rate. The TX/RX pair consumes 290mW from a 1.2V supply and uses a die area of 0.79mm^2.

3.3 A 0.6 to 9.6Gb/s Binary Backplane Transceiver Core in 0.13µm CMOS

2:30 PM

K. Krishna[1], D. Yokoyama-Martin[1], S. Wolfer[1], C. Jones[2], M. Loikkanen[1], J. Parker[1], R. Segelken[1], J. Sonntag[1], J. Stonick[1], S. Titus[3], D. Weinlader[1]
[1]Synopsys, Hillsboro, OR
[2]Stexar, Hillsboro, OR
[3]UNC, Chapel Hill, NC

A backplane transceiver core in 0.13µm dual-gate CMOS, operating at 0.6 to 9.6Gb/s with an area of 0.56mm^2 and dissipating 150mW at 6.25Gb/s, is presented. This core uses a unique adaptive receive equalization strategy, transmit pre-emphasis, and has extensive optional test features including a built-in BER tester and an on-chip receiver sampling scope.

BREAK 3:00PM

3.4 A Transmit Architecture with 4-Tap Feedforward Equalization for 6.25/12.5Gb/s Serial Backplane Communications

3:15 PM

P. Landman, K. Brouse, V. Gupta, S. Wu, R. Payne, U. Erdogan, R. Gu, A-L. Yee, B. Parthasarathy, S. Ramaswamy, B. Bhakta, W. Mohammed, J. Powers, Y. Xie, L. Wu, L. Dyson, K. Heragu, W. Lee
Texas Instruments, Dallas, TX

A transmit architecture with a programmable 4-tap feedforward equalizer for 6.25 to 12.5Gb/s serial communications through lossy channels is described. A 16:8-channel MUX/DEMUX chip fabricated in a 0.13μm 7M CMOS process, demonstrates a near-end jitter or 16ps and an equalized far-end jitter of 55ps at 6.25Gb/s over a 36" legacy backplane channel.

3.5 A 6.25Gb/s Binary Adaptive DFE with First Post-Cursor Tap Cancellation for Serial Backplane Communications

3:45 PM

R. Payne, B. Bhakta, S. Ramaswamy, S. Wu, J. Powers, B. Parthasarathy, P. Landman, U. Erdogan, A-L. Yee, R. Gu, L. Wu, Y. Xie, K. Brouse, W. Mohammed, K. Heragu, V. Gupta, L. Dyson, W. Lee
Texas Instruments, Dallas, TX

A 6.25Gb/s serial receiver with a 4-tap adaptive DFE is implemented in a 0.13μm 7LM CMOS process. Direct cancellation of the first post-cursor ISI is achieved, enabling recovery of a data eye fully closed from channel losses and crosstalk. A BER<10^{-15} is measured over legacy backplane channels.

3.6 12Gb/s Duobinary Signaling with x2 Oversampled Edge Equalization

4:15 PM

K. Yamaguchi[1], K. Sunaga[1], S. Kaeriyama[1]*, T. Nedachi[1], M. Takamiya[1], K. Nose[1], Y. Nakagawa[1], M. Sugawara[2], M. Fukaishi[1]*
[1]NEC, Sagamihara, Japan
[2]NEC, Santa Clara, CA

A backplane transceiver in 90nm CMOS that employs duobinary signaling over copper traces is described. To introduce duobinary signaling into data transfers on printed boards, three techniques are developed: 1) edge equalization for equalizer adaptation, 2) 2x oversampled transmitter equalizer for ISI control, and 3) 2b-transition-ensure encoding for clock recovery.

3.7 A 25Gb/s PAM4 Transmitter in 90nm CMOS SOI

4:45 PM

C. Menolfi[1], T. Toifl[1], R. Reutemann[2], M. Ruegg[2], P. Buchmann[1], M. Kossel[1], T. Morf[1], M. Schmatz
[1]IBM, Rueschlikon, Switzerland
[2]Miromico, Zurich, Switzerland

A 25Gb/s multi-level PAM4 transmitter intended for short-range chip-to-chip on-board interconnects is presented. A 4-tap FIR pre-emphasis filtering scheme is used to equalize channel loss and to improve eye opening. Fabricated in a low-k partially depleted 90nm SOI technology, it occupies 0.052mm² and draws 99.3mA from a 1V supply.

CONCLUSION 5:15 PM

SESSION 4 SALON 8

TD: MIXED-DOMAIN SYSTEMS

Chair: **Kerry Bernstein,** *IBM, Essex Junction, VT*
Associate Chair: **Siva Narendra,** *Intel, Hillsboro, OR*

4.1 Joining Ionics and Electronics: Semiconductor Chips with Ion Channels, Nerve Cells and Brain Tissue

1:30 PM

P. Fromherz
Max Planck Institute for Biochemistry, Munich, Germany

The microscopic interfacing of semiconductor devices and living neuronal systems is discussed. From the biological side, ion channels, nerve cells, and brain tissue are considered. Basic experimental studies are performed with capacitors and transistors of simple silicon chips. The approach is extended to a CMOS chip with 16000 transistor sensors.

4.2 An Analog Bionic Ear Processor with Zero-Crossing Detection

2:00 PM

R. Sarpeshkar, M. Baker, C. Salthouse, J-J. Sit, L. Turicchia, S. Zhak
Massachusetts Institute of Technology, Cambridge, MA

A 75dB 251μW analog speech processor is described that preserves the performance, robustness, and programmability needed for deaf patients at a reduced power consumption compared to that of implementations with A/D and DSP. It also provides zero-crossing outputs for stimulation strategies that use phase information to improve performance.

4.3 An IC/Microfluidic Hybrid Microsystem for 2D Magnetic Manipulation of Individual Biological Cells

2:30 PM

H. Lee[1], Y. Liu[1], E. Alsberg[2], D. Ingber[2], R. Westervelt[1], D. Ham[1]
[1]Harvard University, Cambridge, MA
[2]Harvard Medical School, Boston, MA

A microfluidic system is fabricated on top of an IC chip, suspending magnetic-bead-tagged biological cells in a biocompatible environment. The IC produces patterned magnetic fields using a microcoil array to manipulate individual bead-bound cells. The hybrid prototype manipulates bovine capillary endothelial cells with precise spatial control.

BREAK 3:00 PM

4.4 A VLSI Analog Computer/Math Co-Processor For A Digital Computer

3:15 PM

G. Cowan, R. Melville, Y. Tsividis
Columbia University, New York, NY

A single-chip VLSI analog computer having 80 integrators and 336 other programmable linear and nonlinear circuits is fabricated in a 0.25μm CMOS process. The chip can be used to accelerate a digital computer's numerical routines. The IC is 1cm^2 and consumes 300mW.

4.5 Towards Chip-Scale Atomic Clocks

3:45 PM

C. Nguyen[1], J. Kitching[2]
[1]DARPA, Arlington, VA, and University of Michigan, Ann Arbor, MI
[2]NIST, Boulder, CO

MEMS technology is used to shrink atomic clocks from their present-day table-top sizes down to only 1cm^3 while at the same time retaining timing stability on the order of 30ns over one hour. The power consumption of the system is less than 30mW.

4.6 Opportunities for Optics in Integrated Circuits Applications

4:15 PM

D. Miller, A. Bhatnagar, S. Palermo, A. Emami-Neyestanak, M. Horowitz
Stanford University, Stanford, CA

Optics potentially addresses two key problem in electronic chips and systems: interconnects and timing. Short optical pulses (e.g., picoseconds or shorter) offer particularly precise timing. Results are shown for optical and electrical four-phase clocking, with <1ps rms jitter for the optical case.

4.7 Processing of MEMS Gyroscopes on Top of CMOS ICs

4:45 PM

A. Witvrouw[1], A. Mehta[1], A. Verbist[1], B. Du Bois[1], S. Van Aerde[2], J. Ramos-Martos[3], J. Ceballos[3], A. Ragel[3], J. Mora[3], M. Lagos[3], A. Arias[3], J. Hinojosa[3], J. Spengler[4], C. Leinenbach[5], T. Fuchs[5], S. Kronmueller[6]
[1]IMEC, Leuven, Belgium
[2]ASM, Leuven, Belgium
[3]IMSE-CNM, Sevilla, Spain
[4]Philips Research, Boeblingen, Germany
[5]Bosch, Gerlingen-Schillerhoehe, Germany

Integrated 10μm thick poly-SiGe gyroscopes are processed on top of an 8" standard 0.35μm CMOS wafer with 5 metal levels by using an advanced plasma-enhanced chemical vapor deposition multi-layer technology. The gyroscopes are free-moving with Q-factors for the drive mode up to 10000 at the pressure of 0.8mTorr while the CMOS chip is fully functional.

CONCLUSION 5:15 PM

SESSION 5 SALON 9

WLAN TRANSCEIVERS

Chair: **Arya Behzad,** *Broadcom, San Diego, CA*
Associate Chair: **Mototsugu Hamada,** *Toshiba, Kawasaki, Japan*

5.1 An Auto-I/Q Calibrated CMOS Transceiver for 802.11g

1:30 PM

Y. Hsieh[1], W-Y. Hu[2], S-M. Lin[2], C-L. Chen[2], W-K. Li[2], S-J. Chen[1], D. Chen[3]
[1]National Taiwan University, Hsin-Chu, Taiwan
[2]Muchip, Hsin-Chu, Taiwan
[3]National Taiwan University, Taipei, Taiwan

The CMOS transceiver IC uses the super-heterodyne architecture to implement a 802.11g RF front-end with auto I/Q calibration function. 1° quadrature mismatch and 0.1dB gain mismatch can be achieved after the auto tuning in both the transmitter and receiver sides. Implemented in a 0.25μm CMOS process with 2.7V supply, the transceiver achieves a 5.1dB receive cascade NF and a 7dBm transmit output P_{1dB}.

5.2 An 802.11g WLAN SoC

2:00 PM

S. Mehta[1], D. Weber[1], M. Terrovitis[1], K. Onodera[1], M. Mack[1], B. Kaczynski[1], H. Samavati[1], S. Jen[1], W. Si[1], M. Lee[1], K. Singh[1], S. Mendis[1], P. Husted[1], N. Zhang[1], B. McFarland[1], D. Su[1], T. Meng[2], B. Wooley[2]
[1]Atheros Communications, Sunnyvale, CA
[2]Stanford University, Stanford, CA

A single-chip 802.11g-compliant WLAN radio that implements all RF, analog, and digital PHY and MAC functions is implemented in a 0.18μm CMOS technology. The IC transmits 4dBm EVM-compliant output power for a 64QAM OFDM signal. The overall receiver sensitivities are -95dBm and -73dBm for data rates of 6Mb/s and 54Mb/s, respectively.

5.3 A Fully Integrated SoC for 802.11b in 0.18μm CMOS

2:30 PM

H. Darabi, S. Khorram, Z. Zhou, T. Li, B. Marholev, J. Chiu, J. Castaneda, E. Chien, S. Anand, S. Wu, M. Pan, H. Kim, P. Littieri, B. Ibrahim, J. Rael, L. Tran, E. Geronaga, J. Trachewsky, A. Rofougaran
Broadcom, Irvine, CA

A 0.18μm CMOS 802.11b SoC integrated all the radio building blocks including the PA, the PLL loop filter, and the antenna switch, as well as the complete physical layer and the MAC sections. At 2.4GHz, it dissipates 165mW in the receive-mode and 360mW in the transmit-mode from a 1.8V supply. The receiver achieves a typical NF of 6dB, and –88dBm sensitivity at 11Mb/s rate. The transmitter delivers a nominal output power of 13dBm.

BREAK 3:00 PM

5.4 A Compact Dual-Band Direct-Conversion CMOS Transceiver for 802.11a/b/g WLAN

3:15 PM

Z. Xu[1], S. Jiang[1], Y. Wu[1], H-Y. Jian[1], G. Chu[1], K. Ku[1], P. Wang[1], N. Tran[1], Q. Gu[1], M-Z. Lai[1], C. Chien[1], M. Chang[1,2], P. Chow[1]
[1]SST Communications, Santa Monica, CA
[2]University of California, Los Angeles, CA

A dual-band direct-conversion RF transceiver for 802.11a/b/g WLAN is implemented in 0.18μm CMOS technology with 6mm² die size and 182mW power dissipation while transmitting 1dBm at 5GHz. The receiver achieves 5dB NF, -8dBm IIP3 (high LNA gain), 96dB total gain, and -31.4dB EVM. The transmitter achieves 1dBm and 2.5dBm linear output power at 5GHz and 2.4GHz, respectively, with an EVM less than -31dB.

5.5 A Low-Power Dual-band Triple-Mode WLAN CMOS Transceiver

3:45 PM

T. Maeda, T. Yamase, T. Tokairin, S. Hori, R. Walkington, K. Numata, N. Matsuno, K. Yanagisawa, N. Yoshida, H. Yano, Y. Takahashi, H. Hida
SNEC, Tsukuba, Japan

The 0.18μm CMOS direct-conversion dual-band triple-mode WLAN transceiver covers 2.4 to 2.5GHz and 4.9 to 5.95GHz and draws 78mA in the receive mode and 76mA in the transmit mode, from a 1.8V supply both at 2.4/5GHz. The system NF of 3.5/4.2dB, the sensitivity of -93/-94dBm for a 6Mb/s OFDM signal, and the EVM of 3.2/3.4% are obtained at 2.4/5.2GHz.

5.6 An SoC for Bidirectional Point-to-Multipoint Wireless Digital Audio Applications

4:15 PM

K. Kianush[1], J. Rapp[2], D. Westberg[2], J. van Valburg[3], P. Johansson[2], R. Ponnette[4], N. Philips[4]
[1]Catena, Delft, The Netherlands
[2]Catena, Kista, Sweden
[3]Catena, Eindhoven, The Netherlands
[4]Philips, Leuven, Belgium

A single-chip transceiver for wireless digital audio applications is realized in a 0.25μm BiCMOS process. To avoid the congested 2.4GHz band and to achieve better penetration through walls, 863 and 915MHz bands are adopted. The frame structure used in this design guarantees a low latency for streaming audio. Adaptive frequency hopping and antenna diversity ensure robust link management.

5.7 A Dual-Band Frequency Synthesizer for 802.11a/b/g with Fractional-Spur Averaging Technique

4:45 PM

S. Pellerano, S. Levantino, C. Samori, A. Lacaita
Politecnico di Milano, Milan, Italy

A 0.25μm BiCMOS spur-compensated fractional-N PLL is implemented in an 802.11a/b/g zero-IF transceiver. The synthesizer covers the 2.4 to 2.5GHz and the 5.1 to 5.9GHz bands with 0.5MHz and 5MHz resolution, respectively. The phase noise integrated from 10kHz to 10MHz is lower than 1.25° rms for any synthesized carrier. The power consumption is 39/59mW in 2.5/5GHz mode from 2.5V supply.

5.8 A Fully Integrated Transformer-Based Front-End Architecture for Wireless Transceivers

5:00 PM

I. Bhatti, R. Roufoogaran, J. Castaneda
Broadcom, Irvine, CA

A fully integrated transformer-based RF front-end architecture is presented that integrates matching, combining, and T/R switch functions on chip. The front-end is implemented in a 0.18μm CMOS Bluetooth transciever achieving -90dBm receiver sensitivity and 2dBm transmit power from a 1.8V supply.

CONCLUSION 5:15 PM

SESSION 6 SALON 10-15

HIGH-SPEED AND OVERSAMPLED DACs

Chair: **Robert Neff,** *Agilent Technologies, Palo Alto, CA*
Associate Chair: **Zhongyuan Chang,** *IDT-Newave Technology, Shanghai, China*

6.1 A 1.2GS/s 15b DAC for Precision Signal Generation

1:30 PM

R. Jewett, J. Liu, K. Poulton
Agilent Technologies, Palo Alto, CA

A 1.2GS/s 15b DAC achieves untrimmed SFDR of -70dBc to $f_s/4$ and -63dBc to Nyquist (with 10dB better results at 500MS/s). A per-element resampling scheme and dynamic element matching achieve DNL of 2LSBs. In RZ output mode, ACPR for a 20MHz band at 900MHz is 69dB. The chip uses 40GHz-f_T NPNs and is implemented in 0.35μm CMOS.

6.2 A 1.6GS/s 12b RTZ GaAs RF DAC for Multiple Nyquist Operation

2:00 PM

M-J. Choe, K-H. Baek, M. Teshome
Rockwell, Thousand Oaks, CA

RZ current switches are added to a current steering DAC for high-frequency wideband applications to achieve 800MHz bandwidth at 1st and 2nd Nyquist band without the need for a reverse sinc equalization filter. Implemented in a GaAs HBT process with 4.5μm² minimum emitter area, the DAC dissipates 1.2W at -5V with a 1.6GHz clock and 0dBm typical output power.

6.3 A 1.7GHz 3V Direct Digital Frequency Synthesizer with an On-chip DAC in 0.35μm SiGe BiCMOS

2:30 PM

K-H. Baek, E. Merlo, M-J. Choe, A. Yen, M. Sahrling
Rockwell, Thousand Oaks, CA

A single-chip direct digital frequency synthesizer with hardware efficient phase-to-amplitude mapping and an integrated DAC achieves over 50dB SFDR in full-Nyquist band at 1.7GHz clock frequency for synthesized output signals up to 850MHz. The IC is implemented in a 0.35μm SiGe BiCMOS process and occupies an area of 4.8×5.0mm². Power efficiency is 1.76mW/MHz at 3V.

BREAK 3:00 PM

6.4 A 12b 500MS/s DAC with >70dB SFDR up to 120MHz in 0.18μm CMOS

3:15 PM

K. Doris[1,2], *J. Briaire*[1], *D. Leenaerts*[1], *M. Vertregt*[1], *A. van Roermund*[2]
[1]Philips, Eindhoven, The Netherlands
[2]Technical University Eindhoven, Eindhoven, The Netherlands

A CMOS current steering 12b 500MS/s 216mW DAC without any additional circuitry to remove errors introduced during the conversion process has >70dB SFDR up to 120MHz above the Nyquist band. This is comparable to state-of-the-art performance requiring additional circuitry, and better than any design without additional circuitry.

6.5 A 350MHz Low-OSR ΔΣ Current-Steering DAC with Active Termination in 0.13μm CMOS

3:45 PM

M. Clara, W. Klatzer, A. Wiesbauer, D. Straeussnigg
Infineon, Villach, Austria

A time-interleaved architecture overcomes the dynamic performance limitations of standard DWA switching. Clocked at 350MHz, the DAC with active output buffer achieves a linearity of 76dB for a signal swing of 1.536V and an effective resolution of 11.9b in a bandwidth of 29.16MHz. It is fabricated in a standard 0.13μm CMOS process and consumes 62mW from a 1.5V supply.

6.6 Integrated Stereo ΔΣ Class D Amplifier

4:15 PM

E. Gaalaas[1], B. Liu[2], N. Nishimura[2]
[1]Analog Devices, Bedford, MA
[2]Analog Devices, Tokyo, Japan

A 2×40W (into 4Ω with a 20V supply) integrated stereo ΔΣ class D amplifier with 100dB SNR is realized in a 0.6μm CMOS process with DMOS transistors and buried zener diodes. Feedback from power stage outputs gives 0.001% THD and 65dB PSRR. The modulator clock rate is 6MHz, but dynamically adjusted quantizer hysteresis reduces the output data rate to 450kHz, helping achieve 88% efficiency.

6.7 A 22GS/s 6b DAC with Integrated Digital Ramp Generator

4:45 PM

P. Schvan[1], D. Pollex[1], T. Bellingrath[2]
[1]Nortel Networks, Ottawa, Canada
[2]Institut fuer Mikroelektronik Stuttgart, Germany

A 22GS/s 6b DAC is presented that includes a digital ramp pattern generator. The DAC core and ramp generator consume 2W and 1.2W respectively operating from 3.3V. The DAC produces a differential signal up to $1.3V_{pp}$. DNL<0.5LSB and INL<0.9LSB are measured. The highest glitch energy is 0.5pVs. Settling times are 70 and 40ps for full- and half-scale transitions, respectively.

6.8 A 2GHz Mean-Square Power Detector with Integrated Offset Chopper

5:00 PM

M. Kouwenhoven, A. van Staveren
National Semiconductor, Delft, The Netherlands

A 2GHz mean-square power detector with integrated chopper is presented. It typically achieves an offset reduction of 14.8dB compared to unchopped, untrimmed units and 12dB reduction of the offset variation over temperature (-40°C to +85°C) compared to laser-trimmed units. The chip is designed in a 0.35μm BiCMOS process, measures 1.5x1.5mm² and draws 8mA from a 2.7V supply.

CONCLUSION 5:15 PM

SESSION 7 NOB HILL

MULTIMEDIA PROCESSING

Chair: **Lee-Sup Kim,** *KAIST, Daejeon, Korea*
Associate Chair: **Masafumi Takahashi,** *Toshiba, Kawasaki, Japan*

7.1 A 1.3TOPS H.264/AVC Single-Chip Encoder for HDTV Applications

1:30 PM

Y-W. Huang[1], T-C. Chen[1], C-H. Tsai[1], C-Y. Chen[1], T-W. Chen[1], C-S. Chen[2], C-F. Shen[2], S-Y. Ma[3], T-C. Wang[4], B-Y. Hsieh[5], H-C. Fang[1], L-G. Chen[1]
[1]National Taiwan University, Taipei, Taiwan
[2]Chip Implementation Center, Hsin-Chu, Taiwan
[3]Vivotek, Taipei, Taiwan
[4]Chin Fong Machine Industrial, Chang Hua, Taiwan
[5]MediaTek, Hsin-Chu, Taiwan

An H.264/AVC encoder is implemented on a 31.72mm^2 die with 0.18μm CMOS technology. A four-stage macroblock pipelined architecture encodes 720p 30f/s HDTV videos in real time at 108MHz. The encoded video quality is competitive with reference software requiring 3.6TOPS on a general-purpose processor-based platform.

7.2 An 81MHz 1280x720Pixelsx30f/s MPEG-4 Video/Audio CODEC Processor

2:00 PM

H. Yamauchi, S. Okada, M. Suzuki, Y. Matsuo, Y. Ishii, T. Mori, T. Watanabe, Y. Matsushita
Sanyo Electric, Gifu, Japan

A high-definition MPEG-4 CODEC processor capable of encoding 720p images (1280x720 pixels 30f/s) at 81MHz is presented. The CODEC is implemented with only 390k gates and an 80kb SRAM. It is fabricated in a 0.13μm CMOS process on a 5.6mmx5.6mm die.

7.3 An H.264/MPEG-4 Audio/Visual CODEC LSI with Module-Wise Dynamic Voltage/Frequency Scaling

2:30 PM

T. Fujiyoshi, S. Shiratake, S. Nomura, T. Nishikawa, Y. Kitasho, H. Arakida, Y. Okuda, Y. Tsuboi, M. Hamada, H. Hara, T. Fujita, F. Hatori, T. Shimazawa, K. Yahagi, H. Takeda, M. Murakata, F. Minami, N. Kawabe, T. Kitahara, K. Seta, M. Takahashi, Y. Oowaki
Toshiba, Kawasaki, Japan

A single-chip H.264/MPEG-4 audio/visual LSI for mobile applications with a module-wise dynamic voltage/frequency scaling architecture is described. This LSI operates even during the voltage/frequency transition with no performance overhead by using a dynamic de-skewing system and an on-chip voltage regulator with slew-rate control. The IC consumes 90mW in decoding QVGA H.264 video at 15f/s and MPEG-4 AAC LC audio simultaneously.

BREAK 3:00 PM

7.4 A Streaming Processing Unit for a CELL Processor

3:15 PM

B. Flachs[1], S. Asano[2], S. Dhong[1], P. Hofstee[1], G. Gervais[1], R. Kim[1], T. Le[1], P. Liu[1], J. Leenstra[3], J. Liberty[1], B. Michael, S. Mueller[3], O. Takahashi[1], Y. Watanabe[2], A. Hatakeyama[4], H. Oh[1], N. Yano[2]
[1]IBM, Austin, TX
[2]Toshiba, Austin, TX
[3]IBM, Boeblingen, Germany
[4]Sony, Austin, TX

The design of a 4-way SIMD streaming data processor emphasizes achievable performance in area and power. Software controls data movement and instruction flow, and improves data bandwidth and pipeline utilization. The micro-architecture minimizes instruction latency and provides fine-grain clock control to reduce power.

7.5 A 600MIPS 120mW 70μA Leakage Triple-CPU Mobile Application Processor Chip

3:45 PM

S. Torii[1], S. Suzuki[2], H. Tomonaga[1], T. Tokue[2], J. Sakai[1], N. Suzuki[1], K. Murakami[2], T. Hiraga[2], K. Shigemoto[2], Y. Tatebe[2], E. Obuchi[2], N. Kayama[2], M. Edahiro[1], T. Kusano[2], N. Nishi[1]
[1]NEC, Sagamihara, Japan
[2]NEC, Kawasaki, Japan

A triple-CPU mobile application processor is developed on an 8.95mmx8.95mm die in a 0.13μm CMOS process. The IC integrates 3xARM926 cores, a DSP, several accelerators, as well as strong bus and memory interfaces. It consumes 120mW for digital TV, web browser, and 3D graphics, and 250mW@200MHz for 600MIPS with full processing.

7.6 90nm Low-Leakage SoC Design Techniques for Wireless Applications

4:15 PM

P. Royannez
Texas Instruments, Villeneuve Loubet, France

The new generation of multimedia-application processors requires a drastic leakage reduction to bring the standby current to 50μA. An efficient set of leakage reduction techniques, including power gating, memory retention, voltage scaling, and dual V_t, is employed on a 50M transistor, 80mm^2 IC, fabricated in a 90nm CMOS technology, resulting in a 40x leakage reduction.

7.7 A 100-Channel Analog CMOS Auditory Filter Bank for Speech Recognition

4:45 PM

E. Fragnière[1,2]
[1]Swiss Centre of Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland
[2]University of Applied Sciences, Fribourg, Switzerland

An ASIC emulates the inner ear as a bank of 100 exponentially distributed asymmetric band-pass filters that roll off at up to 450dB/dec and have individually tunable Q-factors. The output is encoded into an auditory-nerve-like pulsed format on a digital port. The chip is integrated in a 0.5μm process and consumes 2.6mW at 3.3V.

CONCLUSION 5:15 PM

DISCUSSION SESSIONS

E1: Mobile Imaging: Paradigm Shift or Technology Bubble?

(Salon 7)

Organizer: **Boyd Fowler,** *Agilent Technologies, Santa Clara, CA*
Moderator: **Jed Hurwitz,** *ST Microelectronics, Edinburgh, Scotland*

Since the 1960s telephone companies have tried to develop and market picture-phones without success. Today there are tens of millions of cell phones with imagers being sold worldwide. Will this prove to be another picture-phone failure or is it different this time? What is the application that will make mobile imaging successful? Will mobile imaging replace stand-alone digital cameras? If mobile imaging is here to stay, how does everyone in the value chain realize a profit?

Panelists:

Jinsung Choi, *LG Electronics, Seoul, Korea*
Minoru Etoh, *DoCoMo Communications, San Jose, CA*
Janne Haavisto, *Nokia, Tampere, Finland*
Jason Hartlove, *Agilent Technologies, Santa Clara, CA*
Tadakuni Narabu, *Sony, Kanagawa, Japan*
Stephen A. Noble, *Eastman Kodak, Rochester, NY*

E2: What Papers Will and Will Not Be at ISSCC2010?

(Salon 8)

Organizer: **Axel Thomsen,** *Silicon Laboratories, Austin, TX*
Moderator: **David Robertson,** *Analog Devices, Wilmington, MA*

The 1980s and 1990s witnessed great advances in analog integrated circuit design, particularly in CMOS technology. High-resolution circuits such as data converters and high-performance RF CMOS circuits were created. In the future as technology scaling results in sub-1V power supplies, is any transistor level circuit innovation possible or will all innovation be at the system level?

Panelists:

Randall Geiger, *Iowa State University, Durham Ames, IA*
Bang Won Lee, *ATLab, KyungGi-Do, Korea*
Dennis Monticelli, *National Semiconductor, Santa Clara, CA*
Don Shaver, *Texas Instruments, Dallas, TX*
Werner Weber, *Infineon, Munich, Germany*
Bill Redman-White, *Philips Semiconductors and Southampton University, Southhampton, United Kingdom*

SE4: Toward the Nanoscale Transistor - Highlights of 2004 Symposium on VLSI Technology

(Salon 9)

Organizer: **Takayuki Kawahara,** *Hitachi, Tokyo, Japan*
Chair: **Shin'ichiro Kimura,** *Hitachi, Tokyo, Japan*

In the nano-scale era, the advantages of bulk-CMOS technology diminish with transistor scaling. Among the difficulties encountered are the ON current limits, the inherent increase in OFF current due to leakage, and manufacturability. For Moore's Law to remain valid, these difficulties must be overcome. Fortunately, as indicated by leading researchers in their fields, new technologies are emerging that address these issues, and appear suitable for nanotechnology implementations.

The papers in this session have been carefully selected from the 2004 Symposium on VLSI Technology. The technologies discussed include: strained-channel technology, 5nm FinFETs, a hybrid technology using a bulk-Si-SOI combination, and a sub-10nm bulk-CMOS transistor. Demonstrated, are devices with 1 to 2mA ON currents with minimal OFF currents. The underlying concepts are revealed, as are the potential for application of each technology.

The intent in presenting this session is to provide to ISSCC attendees the concepts underlying prototype devices, so that circuit designers become better able to contribute to building a nano-scale world.

Time	Topic
8:00	***"An Enhanced 90nm High Performance Technology with Strong Performance Improvements from Stress and Mobility Increase through Simple Process Changes"*** **Rajesh B. Khamankar**, *Texas Instruments, Dallas, TX*
8:30	***"5nm-Gate Nanowire FinFET"*** **Fu-Liang Yang,** *Taiwan Semiconductor, Manufacturing Company, Hsin-Chu City, Taiwan*
9:00	***"A Simplified Hybrid Orientation Technology (SHOT) for High Performance CMOS"*** **Bruce Doris,** *IBM, Hopewell Junction, NY*
9:30	***"A hp22 nm Node Low Operating Power (LOP) Technology with Sub-10nm Gate-Length Planar Bulk CMOS Devices"*** **Nobuaki Yasutake,** *Toshiba, Kanagawa, Japan*

SESSION 8 SALON 1-6

CIRCUITS FOR HIGH-SPEED LINKS AND CLOCK-GENERATORS

Chair: **Hirotaka Tamura,** *Fujitsu, Kanagawa, Japan*
Associate Chair: **Sung Min Park,** *Ewha Womans University, Seoul, Korea*

8.1 Circuit Techniques for a 40Gb/s Transmitter in 0.13μm CMOS

8:30 AM

J. Kim[1], J-K. Kim[1], B-J. Lee[1], M-S. Hwang[1], H-R. Lee[1], S-H. Lee[2], N. Kim[2], D-K. Jeong[1], W. Kim[1]
[1]Seoul National University, Seoul, Korea
[2]Silicon Image, Sunnyvale, CA

Implemented in 0.13μm CMOS, the 40Gb/s transmitter uses shunt-and-double-series inductive peaking and negative feedback for bandwidth enhancement and pulsed latch-based dividers and retimers for timing closure. The 38.4Gb/s 2^{31}-1 PRBS transmitted eye has differential voltage swing of 549mV_{pp}, rise time of 14ps, and clock jitter of 0.65ps_{rms} and 4.9ps_{pp}.

8.2 40Gb/s 4:1 MUX/1:4 DEMUX in 90nm standard CMOS

9:00 AM

K. Kanda, D. Yamazaki, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, H. Onodera
Fujitsu, Kawasaki, Japan

A 1.2V 40Gb/s 4:1 MUX and 1:4 DEMUX are implemented in a in 90nm digital-compatible standard CMOS technology. The MUX and DEMUX operate from a 1.2V supply and draw 110mA and 52mA, respectively. Experimental results show a clear eye opening of 300mV_{pp} for the MUX and that of 540mV_{pp} for the DEMUX at 40Gb/s.

8.3 An 80GHz Travelling-Wave Amplifier in 90nm CMOS

9:30 AM

R-C. Liu[1], T-P. Wang[1], L-H. Lu[1], H. Wang[1], S-H Wang[2], C-P. Chao[2]
[1]National Taiwan University, Taipei, Taiwan
[2]TSMC, Hsin-Chu, Taiwan

A 6-stage travelling wave amplifier (TWA) implemented in a bulk 90nm CMOS technology is presented. By utilizing gate-line capacitive division and low-loss coplanar waveguides, the fabricated TWA exhibits 7.4dB gain with a 3dB bandwidth of 80GHz while maintaining input and output return losses better than 8dB from dc to 100GHz. A GBW of 190GHz is achieved.

BREAK 10:00 AM

8.4 A 1.8V Three-Stage 25GHz 3dB-BW Differential Non-Uniform Downsized Distributed Amplifier

10:15 AM

A. Yazdi, D. Lin, P. Heydari
University of California, Irvine, CA

A three-stage non-uniform downsized distributed amplifier is realized in a 0.18μm SiGe process, using CMOS transistors only. The amplifier achieves the differential forward gain of 7.8dB over a 25GHz bandwidth and an IIP3 of +4.7dBm. The 1.025x1.29mm^2 chip dissipates 54mW from a 1.8V supply.

8.5 A 1V 24GHz 17.5mW PLL in 0.18μm CMOS

10:45 AM

A. Ng, G. Leung, K-C. Kwok, L. Leung, H. Luong
Hong Kong University of Science and Technology, Hong Kong, China

A 1V 24GHz fully integrated PLL is designed in a 0.18μm using CMOS transistors only. CMOS process using a transformer-feedback VCO and a stacked frequency divider. The PLL measures an in-band phase noise of -106.3dBc/Hz at 100kHz offset and an out-of-band phase noise of -119.1dBc/Hz at 10MHz offset. It consumes 17.5mW from a 1V supply and occupying an area of 0.55mm^2.

8.6 Spread-Spectrum Clock Generator for Serial ATA using Fractional PLL controlled by ΔΣ Modulator with Level Shifter

11:15 AM

M. Kokubo[1], T. Kawamoto[1], T. Oshima[1], T. Noto[2], M. Suzuki[2], S. Suzuki[2], T. Hayasaka[2], T. Takahashi[2], J. Kasai[2]
[1]Hitachi, Kokubunji, Japan
[2]Renesas Technology, Kodaira, Japan

Implemented in a 0.15μm CMOS process, the spread-spectrum clock generator uses the fractional PLL controlled by a ΔΣ modulator. An adaptive level shifter is adopted for expanding the input range of the ΔΣ modulator. The 1.5GHz prototype achieves the peak spurious reduction level of 20.3dB and the random jitter of 8.1ps in 250-cycle averaging period.

8.7 A Low-Jitter 5000ppm Spread-Spectrum Clock Generator for Multi-Channel SATA Transceiver in 0.18μm CMOS

11:45 AM

H-R. Lee[1], O. Kim[2], G. Ahn[2], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea
[2]Silicon Image, Sunnyvale, CA

A low-jitter 5000ppm spread-spectrum clock generator is implemented in a 0.18μm CMOS process. By using 10 multi-phase clocks and a ΔΣ modulator with periodic input, the chip has a deterministic jitter of 25ps due to spread-spectrum clocking and an amount of spreading of 5000ppm.

CONCLUSION 12:15 AM

SESSION 9 SALON 7

SWITCHED-CAPACITOR ΔΣ MODULATORS

Chair: **Willy Sansen,** *Katholieke Universiteit Leuven, Belgium*
Associate Chair: **Andrea Baschirotto,** *University of Lecce, Italy*

9.1 A 0.6V 82dB ΔΣ Audio ADC Using Switched-RC Integrators

8:30 AM

G-C. Ahn[1], D-Y. Chang[1], M. Brown[1], N. Ozaki[2], H. Youra[2], K. Yamamura[2], K. Hamashita[2], K. Takasuka[2], G. Temes[1], U-K. Moon[1]
[1]Oregon State University, Corvallis, OR
[2]Asahi Kasei Microsystems, Atsugi, Japan

A 2-2 MASH ADC consumes 1mW from a 0.6V supply. It utilizes a local-feedback loop for large input range, and switched-RC integrators to achieve high linearity without clock boosting or bootstrapping. The prototype IC is fabricated in a 0.35μm CMOS process. It provides 82dB DR over the A-weighted audio band, and 103dB SFDR at -3dBFS input.

9.2 A Low-Power Multi-Bit ΔΣ Modulator in 90nm Digital CMOS without DEM

9:00 AM

J. Yu[1], F. Maloberti[2]
[1]Texas Instruments, Dallas, TX
[2]University of Texas, Richardson, TX

A 2nd-order 4b ΔΣ modulator uses 3- and 5-level DACs. Truncating the ADC output while shaping and cancelling the error enables the use of low-resolution DACs and avoids DEM. The prototype is implemented in a 90nm digital CMOS technology and uses 2.1mW from a 1.3V supply with a 40MHz clock. The SNDR is 52dB, 61dB and 72dB for an OSR of 10, 20 and 50, respectively.

9.3 A 66dB-DR 1.2V 1.2mW Single-Amplifier Double-Sampling 2nd-order ΔΣ ADC for WCDMA in 90nm CMOS

9:30 AM

J. Koh, G. Gomez, Y. Choi
Texas Instruments, Dallas, TX

A single-amplifier double-sampling 2nd-order ΔΣ ADC with 5-level quantization is implemented in 90nm CMOS. To alleviate the capacitor mismatch issues in double sampling techniques, a single capacitor method is introduced, achieving 63dB peak SNDR and 66dB DR in a 1.94MHz bandwidth while consuming 1.2mW from a 1.2V supply.

BREAK 10:00 AM

9.4 A 100dB SNR 2.5MS/s Output Data Rate ΔΣ ADC

10:15 AM

J. Gorbold[1], R. Maurino[1], R. Brewer[1], C. Hurrell[1], C. Lyden[2], M. Vickery[1]
[1]Analog Devices, Newbury, United Kingdom
[2]Analog Devices, Cork, Ireland

A multi-bit cascaded 2-2-0 ΔΣ modulator in 0.25μm CMOS attains 100dB SNR in a 1MHz signal bandwidth. The complete A/D converter includes an on-chip opamp for driving the large input capacitors dictated by kT/C noise, a reference buffer and a programmable decimation filter. The power consumption of the modulator including reference buffer is 475mW from a dual supply (2.5V and 5V).

9.5 An 80MHz 4× Oversampled Cascaded ΔΣ-Pipelined ADC with 75dB DR and 87dB SFDR

10:45 AM

A. Bosi[1], A. Panigada[1], G. Cesura[1], R. Castello[2]
[1]STMicroelectronics, Pavia, Italy
[2]University of Pavia, Pavia, Italy

A 2nd-order 4b ΔΣ modulator in cascade with a 9b pipeline clocked at 80MHz achieves 75dB DR, 74dB peak SNR and more than 87dB SFDR in a 10MHz bandwidth by means of background digital linearization and noise-cancellation algorithms. The 0.18μm CMOS chip consumes 240mW including reference generator, digital decimator and correction logic.

9.6 A 106dB SNR Hybrid Oversampling ADC for Digital Audio

11:15 AM

K. Nguyen, B. Adams, K. Sweetland, K. McLaughlin, H. Chen
[1]Analog Devices, Wilmington, MA

A ΔΣ ADC with a CT 1st stage is presented. A hybrid tuning circuit adjusts the RC time constant to compensate for process, supply, and sampling rate variations. The ISI of the feedback DAC is eliminated by an RTZ scheme applyied to the error current of the CT integrator. The ADC achieves 106dB SNR, -97dB THD+N, occupies 0.82mm^2 in a 0.35μm CMOS process and dissipates 18mW.

9.7 A 0.18μm102dB-SNR Mixed CT SC Audio-Band ΔΣ ADC

11:45 AM

P. Morrow[1], M. Chamarro[1], C. Lyden[2], P. Ventura[1], A. Abo[3], A. Matamura[4], M-D. Keane[1], R. O'Brien[1], N. McGuinness[1], P. Minogue[1], M. McGranaghan[1], J. Mansson[1], I. Ryan[1]
[1]Analog Devices, Limerick, Ireland
[2]Analog Devices, Cork, Ireland
[3]Analog Devices, San Jose, CA
[4]Analog Devices, Tokyo, Japan

A 2nd-order mixed CT SC ΔΣ modulator uses multi-bit feedback to reduce clock-jitter sensitivity. The chip is implemented in 0.18μm CMOS using 3.3V I/O devices and achieves 102dB SNR in a 20kHz bandwidth by using chopper stabilization to reduce flicker noise. The ADC core draws 11.3mA from a 3.3V supply and occupies 0.65mm^2.

CONCLUSION 12:15 PM

SESSION 10 SALON 8

MICROPROCESSORS AND SIGNAL PROCESSING

Chair: **Georgios Konstadinidis,** *Sun Microsystems, Sunnyvale, CA*
Associate Chair: **Sung Bae Park,** *Samsung, Yongin-City, Korea*

10.1 The Implementation of a 2-core Multi-Threaded Itanium® Family Processor

8:30 AM

S. Naffziger[1], T. Grutkowski[2], B. Stackhouse[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

The next generation in the Itanium® processor family, code named Montecito, is introduced. Implemented in a 90nm 7M process, the processor has two dual-threaded cores integrated with 26.5MB of cache. Of the total of 1.72B transistors, 64M are dedicated to logic and the rest to cache. With both cores operating at full speed, the chip consumes 100W.

10.2 The Design and Implementation of a First-Generation CELL Processor

9:00 AM

D. Pham[1], S.Asano[2],M. Bolliger[1], M. Day[1], H. Hofstee[1], C. Johns[1], J. Kahle[1], A. Kameyama[3], J. Keaty[1],Y. Masubuchi[2], M. Riley[1], D. Shippy[1], D. Stasiak[1], M.Wang[1], J. Warnock[1], S. Weitzel[1], D. Wendel[1], T. Yamazaki[1], K. Yazawa[2]
[1]IBM, Austin, TX
[2]Sony, Tokyo, Japan
[3]Toshiba, Austin, TX

A CELL Processor is a multi-core chip consisting of a 64b Power architecture processor, multiple streaming processors, a flexible IO interface, and a memory interface controller. This SoC is implemented in 90nm SOI technology. The chip is designed with a high degree of modularity and reuse to maximize the custom circuit content and achieve a high-frequency clock-rate.

10.3 Implementation of a 4th-Generation 1.8GHz Dual-Core SPARC V9 Microprocessor

9:30 AM

J. Hart, S. Choe, L. Cheng, C. Chou, A. Dixit, K. Ho, J. Hsu, K. Lee, J. Wu
SUN Microsystems, Sunnyvale, CA

This fourth-generation processor combines two enhanced third-generation cores using an advanced 90nm dual-V_t dual-gate-oxide technology. Hardware additions feature expanded caches and inclusion of a 2MB Level2 cache and a Level3 tag. The chip operates at 1.8GHz while dissipating <100W at 1.1V.

BREAK 10:00 AM

10.4 Creating the BlueGene/L Supercomputer from Low-Power SoC ASICs

10:15 AM

A. Bright[1], M. Ellavsky[2], A. Gara[1], R. Haring[1], R. Lembach[2], J. Marcella[2], V. Salapura[1]
[1]IBM, Yorktown Heights, NY
[2]IBM, Rochester, MN

An overview of the design aspects of the BlueGene/L chip, the heart of the BlueGene/L supercomputer, is presented. Following an SoC approach, processors, memory and communication subsystems are integrated into one low-power chip. The high-density system packaging of the BlueGene/L system provides better power and cost performance.

10.5 An SoC with 1.3Gtexels/s 3D Graphics Full Pipeline Engine for Consumer Applications

10:45 AM

D. Kim[1], K. Chung[1], C-H. Yu[1], C-H. Kim[1], I. Lee[1], J. Bae[1], Y-J. Kim[2], Y. Chung[2], S. Kim[2], Y-H. Park[2], N. Seong[2], J-A. Lee[2], J. Park[2], S. Oh[2], S-W. Jeong[2], L-S. Kim[1]
[1]KAIST, Daejeon, Korea
[2]Samsung, Giheung, Korea

A 3D graphics SoC whose performance is 33Mvertices/s and 1.3Gtexels/s is designed for consumer applications. The SoC integrates an ARM11 RISC processor, a dedicated 3D graphics full pipeline engine, and video composition IPs. The SoC contains 17.9M transistors in 50mm^2 area and is fabricated in a 0.13μm 7M CMOS process.

10.6 A 50Mvertices/s Graphics Processor with Fixed-Point Programmable Vertex Shader for Mobile Applications

11:15 AM

J-H. Sohn, J-H. Woo, M-W. Lee, H-J. Kim, R. Woo, H-J. Yoo
KAIST, Daejeon, Korea

A user-programmable mobile 3D graphics processor with a 32b RISC, a 128b fixed-point SIMD vertex shader and a rendering engine is implemented. A programmable frequency synthesizer controls the clock frequency continuously and adaptively for low power. The chip achieves 50Mvertices/s and 200Mtexels/s, dissipating 155mW in a 0.18μm 6M CMOS process.

10.7 A 51.2GOPS, 1.0GB/s-DMA Single-Chip Multi-Processor Integrating Quadruple 8-Way VLIW Processors

11:45 AM

T. Shiota, K-I. Kawasaki, Y. Kawabe, W. Shibamoto, A. Sato, T. Hashimoto, F. Hayakawa, S-I. Tago, H. Okano, Y. Nakamura, H. Miyake, A. Suga, H. Takahashi
Fujitsu, Kawasaki, Japan

A 51.2-GOPS chip multi-processor integrates four 8-way VLIW embedded processors with 1.0GB/s local-bus direct memory access. This IC completes MPEG2 MP@HL video-stream decoding at 68% of its processor capability without dedicated hardware. The 11.9mm×10.3mm chip is fabricated in a 90nm 9M CMOS process and consumes 5W at 533MHz.

10.8 XiSystem: a XiRisc-Based SoC with Reconfigurable IO Module

12:00 PM

A. Lodi[1], A. Cappelli[1], M. Bocchi[1], C. Mucci[1], M. Innocenti[1], C. De Bartolomeis[1], L. Ciccarelli[1], R. Giansante[1], F. Campi[2], M. Toma[2], R. Guerrieri[1]
[1]University of Bologna, Bologna, Italy
[2]STMicroelectronics, Agrate Brianza, Italy

XiSystem is an SoC comprised of a XiRisc reconfigurable processor and an eFPGA implementing reconfigurable IOs. This system-level reconfigurable platform implements high-perfomance application-specific SoCs. XiSystem is implemented in a 0.13μm CMOS technology in an area of 42mm^2 and consumes 300mW at 166MHz.

CONCLUSION 12:15 PM

SESSION 11 SALON 9

ULTRA WIDEBAND SOLUTIONS

Chair: **Ali Hajimiri,** *California Institute of Technology, Pasadena, CA*
Associate Chair: **Tom Schiltz,** *Linear Technology, Colorado Springs, CO*

11.1 An Interference-Robust Receive Chain for UWB Radio in SiGe BiCMOS

8:30 AM

J. Bergervoet[1], K. Harish[1], G. van der Weide[1], D. Leenaerts[1], R. van de Beek[1], H. Waite[2], Y. Zhang[2], S. Aggarwal[2], C. Razzell[2], R. Roovers[1]
[1]Philips, Eindhoven, The Netherlands
[2]Philips Semiconductors, San Jose, CA

A fully integrated receive chain for UWB radio in SiGe BiCMOS is presented. The packaged device includes a wideband LNA, a mixer, and an IF filter and has an overall NF of 7.5dB. The IIP3 of –3dBm and the accurately controlled and steep filter characteristic enables a robust co-existence with systems working in the 2.4 and 5GHz bands.

11.2 A SiGe BiCMOS 1ns Fast Hopping Frequency Synthesizer for UWB Radio

8:45 AM

D. Leenaerts[1], R. van de Beek[1], G. van der Weide[1], H. Waite[2], J. Bergervoet[1], K. Harish[1], Y. Zhang[2], C. Razzell[2], R. Roovers[1]
[1]Philips, Eindhoven, The Netherlands
[2]Philips Semiconductors, San Jose, CA

A fully integrated multi-tone generator based on 2 PLLs and a SSB mixer in 0.25µm SiGe BiCMOS achieves frequency hopping between 3.432, 3.960, and 4.488GHz within 1ns. Spurious tones are below –50dBc in the 5GHz and –45dBc in the 2.4GHz ISM bands. The power dissipation is 73mW from a 2.7V supply. The close-in phase noise is below –90dBc/Hz and out-of-band phase noise is below –100dBc/Hz at 1MHz offset.

11.3 A 7-Band 3 to 8GHz Frequency Synthesizer with 1ns Band-Switching Time in 0.18µm CMOS Technology

9:00 AM

J. Lee, D-W. Chiu
National Taiwan University, Taipei, Taiwan

A frequency synthesizer incorporates one single-sideband mixer to switch among 7 bands distributed from 3 to 8GHz with 1ns settling time. Fabricated in a 0.18µm CMOS technology, it achieves a sideband rejection of 37dB while consuming 48mW from a 2.2V supply.

11.4 A Semi-Dynamic Regenerative Frequency Divider for Mode-1 MB-OFDM UWB Hopping Carrier Generation

9:15 AM

C-C. Lin, C-K. Wang
National Taiwan University, Taipei, Taiwan

A semi-dynamic regenerative frequency divider for MB-OFDM UWB hopping carrier generation is presented. With the ratio of 7.5, it provides quadrature symmetric 528MHz deviation for direct frequency synthesis. Realized in 0.18µm CMOS, the chip occupies 0.8×0.85mm^2. The synthesizer achieves -20dBc image suppression while consuming 18mW from a 1.8V supply.

11.5 A 3.1 to 8.2GHz Direct Conversion Receiver for MB-OFDM UWB Communications

9:30 AM

A. Ismail[1,2], A. Abidi[2]
[1]Skyworks Solutions, Irvine, CA
[2]University of California, Los Angeles, CA

A direct conversion receiver for UWB applications operates in 3.1-8.2GHz and gives a NF of 3.3-4.1dB and a conversion gain of 52dB. The chip includes an RF receive chain and a 16GHz quadrature VCO to generate seven carrier frequencies from 3.4 to 7.9GHz. The circuit is fabricated in 0.18μm SiGe BiCMOS process and draws 88mA from a 2.7V supply.

BREAK 10:00 AM

11.6 A 1.4V 5GHz Four-Antenna Cartesian-Combining Receiver in 90nm CMOS for Beamforming and Spatial Diversity Applications

10:15 AM

J. Paramesh[1,2], R. Bishop[2], K. Soumyanath[2], D. Allstot[1]
[1]University of Washington, Seattle, WA
[2]Intel, Hillsboro, OR

A 90nm CMOS four-channel analog beam-forming receiver draws 140mW at 1.4V and achieves 6dB SNR improvement with 360° look-angle coverage and 20dB interference cancellation. Vector combinations of programmable gain elements eliminate the need for explicit phase shifters. The analog combining technique is also useful as a low-power range extender/interference canceller in conjunction with spatial-multiplexing MIMO.

11.7 A 24GHz Phased-Array Transmitter in 0.18μm CMOS

10:45 AM

A. Natarajan, A. Komijani, A. Hajimiri
California Institute of Technology, Pasadena, CA

A fully integrated 4-element phased-array transmitter at 24 GHz with on-chip PAs is implemented in a 0.18μm CMOS process. It has a beam-forming resolution of 10°, a peak-to-null ratio of 23dB, and isolation between paths of 28dB. Each CMOS PA can deliver up to +14dBm into a 50Ω load. The transmitter supports 500Mb/s QPSK signal and has a bandwidth in excess of 400MHz. The die size is 6.8mm×2.1mm and the complete 4-element transmitter including 4 on-chip PAs draws 788mA from a 2.5V supply.

11.8 A 3.1 to 5GHz CMOS DSSS UWB Transceiver for WPANs

11:15 AM

S. Iida[1], K. Tanaka[1], H. Suzuki[2], N. Yoshikawa[2], N. Shoji[2], B. Griffiths[3], D. Mellor[3], F. Hayden[3], I. Butler[3], J. Chatwin[3]
[1]Sony, Tokyo, Japan
[2]Sony, Atsugi, Japan
[3]Mixed Signal Systems, Scotts Valley

A DSSS UWB transceiver using the 3.1 to 5GHz band is implemented in 0.18μm CMOS and includes a programmable pulse shaping circuit in the transmitter, an LNA with a NF of 4dB and a 6th-order active LPFs with a bandwidth of 500MHz in the receiver. Die area of the transceiver is around 9mm^2, and the transceiver consumes 105mW in the transmit mode and 280mW in the receive mode from a 1.8V supply.

11.9 A 0.13μm CMOS UWB Transceiver

11:45 AM

B. Razavi[1], T. Aytur[2], H. Kang[2], C. Hsu[2], F. Yang[2], C. Lee[2], R. Yan[2]
[1]University of California, Los Angeles, CA
[2]Realtek, Irvine, CA

A direct-conversion UWB transceiver for Mode1 OFDM applications employs three resonant networks and three PLLs. Designed in a 0.13μm CMOS technology, the transceiver provides a total gain in the range of 69 to 73dB and a NF in the range of 5.5 to 8.4dB across three bands, and a TX P_{1dB} of -10dBm. The circuit consumes 105mW from a 1.5V supply.

CONCLUSION 12:15 PM

SESSION 12 SALON 10-15

OPTICAL COMMUNICATIONS

Chair: **Larry De Vito,** *Analog Devices, Wilmington, MA*
Associate Chair: **Yusuke Ohtomo,** *NTT, Kanagawa, Japan*

12.1 A 3V 10.7Gb/s Differential Laser Diode Driver with Active Back-Termination Output Stage

8:30 AM

S. Morley
Analog Devices, Limerick, Ireland

A 3V 10.7Gb/s differential laser diode driver fabricated on a 0.35μm SiGe bipolar process is presented. A feedback-amplifier output stage provides both differential and common-mode active back termination of the output transmission lines with 80mA maximum modulation current. Rise and fall times of 28ps are achieved, and typical power dissipation is 0.67W for I_{mod}=40mA.

12.2 A 20Gb/s VCSEL Driver with Pre-Emphasis and Regulated Output Impedance in 0.13μm CMOS

9:00 AM

D. Kucharski[1,2], Y. Kwark[1], D. Kuchta[1], D. Guckenberger[1,2], K. Kornegay[2], M. Tan[3], C-K. Lynn[3], A. Tandon[3]
[1]IBM, Yorktown Heights, NY
[2]Cornell University, Ithaca, NY
[3]Agilent Technologies, Palo Alto, CA

Two 20Gb/s optical transmitters are presented. They are a part of a 4×12 array intended for backplane data links. The drivers are fabricated in 0.13μm CMOS and include pre-emphasis and regulated output impedance. When coupled to 990nm VCSELs, they provide optical modulation amplitude of 0dBm and consume 70mW and 120mW.

12.3 A 0.5μm SiGe Pre-Equalizer for 10Gb/s Single-Mode Fiber Optic Links

9:30 AM

M. El Said[1], J. Sitch[2], M. Elmasry[1]
[1]University of Waterloo, Waterloo, Canada
[2]Nortel Networks, Ottawa, Canada

A 10-complex-tap T/2-spaced pre-equalizer, intended to equalize a 10Gb/s duobinary signal transmitted over 400km of standard single-mode fiber, is described. Fabricated in 47GHz f_T SiGe technology, it operates at clock frequencies up to 13GHz (limited by test equipment), occupies an area of 3.9x3.2mm^2, and dissipates 3W from a dual supply of 5V and 3.3V.

BREAK 10:00 AM

12.4 1.25Gb/s Burst-Mode Receiver ICs with Quick Response for PON Systems

10:15 AM

M. Nakamura, Y. Imai, Y. Umeda, J. Endo, Y. Akatsu
NTT, Atsugi, Japan

1.25Gb/s burst-mode receiver ICs for optical access networks are described. A quick-response receiver circuit with variable gain accommodates signal amplitute changes between bursts. The optical receiver that uses these ICs exhibits fast settling time of under 20UIs and sensitivity of -30dBm with DR of over 26dB using a PIN-PD.

12.5 A 10Gb/s Burst-Mode CDR IC in 0.13µm CMOS

10:45 AM

M. Nogawa[1], K. Nishimura[1], S. Kimura[2], T. Yoshida[2], T. Kawamura[1], M. Togashi[1], K. Kumozaki[2], Y. Ohtomo[1]
[1]NTT, Atsugi, Japan
[2]NTT, Chiba, Japan

A 10Gb/s burst-mode CDR IC that is eight times faster than previous burst-mode ICs is fabricated in a 0.13µm CMOS process. It amplifies an AC-coupled input burst by means of an edge detection technique, and extracts a clock within 5UIs with a gated oscillator. It consumes 1.2W from a 2.5V supply.

12.6 A 12.5Mb/s to 2.7Gb/s Continuous-Rate CDR with Automatic Frequency Acquisition and Data-Rate Readback

11:15 AM

D. Dalton[1], K. Chai[2], E. Evans[2], M. Ferriss[1], D. Hitchcox[2], P. Murray[1], S. Selvanayagam[2], P. Shepherd[2], L. DeVito[3]
[1]Analog Devices, Limerick, Ireland
[2]Analog Devices, Newbury, United Kingdom
[3]Analog Devices, Wilmington, MA

A continuous-rate CDR is presented that operates from 12.5Mb/s to 2.7Gb/s. The circuit automatically detects a change in input data rate, acquires the new frequency and reports the data rate to the user without the need for an external reference clock or any programming. In tracking mode, it uses a dual-loop DLL/PLL to exceed the SONET jitter specifications.

12.7 A 3.125Gb/s Limit Amplifier with 42dB Gain and 1µs Offset Compensation in 0.18µm CMOS

11:45 AM

E. Crain, M. Perrott
Massachusetts Institute of Technology, Cambridge, MA

An offset-compensation method uses a peak detector and multiple tap feedback to achieve 1000x improvement in settling time compared to prior art. Measurement results for a 3.125Gb/s limit amplifier with 42dB gain implemented in a 0.18µm CMOS process are presented.

12.8 A 21mW 2.5Gb/s 15KΩ Self-Compensated Differential Transimpedance Amplifier

12:00 PM

C-M. Tsai, L-R. Huang
Industrial Technology Research Institute, Hsin-Chu, Taiwan

A differential transimpedance amplifier combined with a positive feedback compensation circuit tolerates 1.5pF parasitic capacitance from ESD protection in 0.35µm SiGe BiCMOS. A 2.5Gb/s receiver demonstrates 15kΩ transcimpedance gain and DR from -3 to -23.5dBm while consuming 21mW from a 3V supply.

CONCLUSION 12:15 PM

SESSION 13 NOB HILL

SENSORS

Chair: **Euisik Yoon,** *KAIST, Daejeon, Korea*
Associate Chair: **Navakanta Bhat,** *IISc, Bangalore, India*

13.1 A CMOS Temperature Sensor with a 3σ Inaccuracy of ±0.1°C from -55°C to 125°C

8:30 AM

M. Pertijs, K. Makinwa, J. Huijsing
Delft University of Technology, Delft, The Netherlands

A smart temperature sensor is accurate to within ±0.1°C (3σ) over the full military temperature range of –55°C to 125°C. This 5× improvement is achieved using DEM, a current-gain independent PTAT bias circuit, and a low-offset ΔΣ ADC combining chopping and CDS. The sensor is fabricated in 0.7μm 2M1P CMOS with 4.5mm² area and draws 75μA.

13.2 A CMOS Rotary Encoder Based on Magnetic Pattern Analysis with a Resolution of 10b per Rotation

9:00 AM

S. Kawahito[1], T. Takahashi[2], Y. Nagano[2], K. Nakano[3]
[1]Shizuoka University, Hamamatsu, Japan
[2]NTN, Iwata, Japan

A single-chip CMOS magnetic rotary encoder system based on magnetic pattern analysis is presented. Magnetic sensor arrays are integrated with ADCs and DSP circuits and fabricated in a standard 0.25μm CMOS technology. The chip detects the rotation angle within an error of ±0.36 degrees (10b per rotation).

13.3 A Hall Sensor Analog Front-End for Current Measurement with Continuous Gain Calibration

9:30 AM

M. Pastre[1], M. Kayal[1], H. Blanchard[2]
[1]Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland
[2]LEM, Geneva, Switzerland

A fully integrated analog front-end for Hall sensors continuously calibrates the gain of the sensor and amplifier circuitry without interfering with normal operation. An integrated coil generates a modulated reference magnetic field measured by the sensor and combined with the external field. A better than 50ppm/°C gain drift is achieved.

BREAK 10:00 AM

13.4 A Microsystem for Trace Environmental Monitoring

10:15 AM

S. Martin[1], F. Gebara[1], B. Larivee[2], R. Brown[3]
[1]University of Michigan, Ann Arbor, MI
[2]Analog Devices, Boston, MA
[3]University of Utah, Salt Lake City, UT

Integrated microsensors with an analog front-end enable trace metal detection. The 36mm² device is fabricated in a 5V 0.5μm CMOS process with the sensor layers post processed and dissipates 15mW. A detection limit of 0.8ppb for lead is attained using two $3x10^{-6}cm^2$ electrodes.

13.5 A Fully-Integrated CMOS Hall Sensor with a 4.5μT, 3σ Offset Spread for Compass Applications

10:45 AM

J. van der Meer[1], F. Riedijk[1], E. van Kampen[1], K. Makinwa[2], J. Huijsing[2]
[1]Xensor Integration, Delfgauw, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands

A fully-integrated CMOS Hall sensor suitable for use in compass applications has a 3σ offset spread less than 4.5μT. After artificial aging it drifts less than 250nT. Using two such sensors, a fully integrated electronically calibrated compass with a stability of 0.5° is realized. The sensor has an analog PWM and a digital RS232/SPI/μwire interface.

13.6 A 0.8mA 50Hz 15b SNDR ΔΣ Closed-Loop 10g Accelerometer Using an 8th-Order Digital Compensator

11:15 AM

C. Condemine[1], N. Delorme[1], J. Soen[1], J. Durupt[1], J-P. Blanc[1], M. Belleville[1], A. Besancon-Voda[2]
[1]CEA - LETI, Grenoble, France
[2]Automatic Laboratory of Grenoble, St Martin d'Héres, France

A ΣΔ-based closed-loop ±10g accelerometer providing 88dB SNDR over a 50Hz bandwidth is fabricated in a 19.4mm² die using 0.35μm CMOS technology. A ΔΣ interface performs the readout, ADC and electrostatic actuation of the sensor, while an 8th-order digital compensator computes the actuation command.

13.7 A 200×160-Pixel CMOS Fingerprint Recognition SoC with Adaptable Column-Parallel Processors

11:45 AM

S-J. Kim, K-H. Lee, S-W. Han, E. Yoon
KAIST, Daejeon, Korea

A CMOS fingerprint recognition SoC with embedded column-parallel processors is optimized for 2D digital image processing. The processor employs self-configuration features for adaptive filter operations and the pixel includes a sensing block, ADC and frame memory without area penalty. The total image processing time is less than 360ms at 10MHz.

13.8 A CMOS Integrated Capacitive Fingerprint Sensor with a 32b Microcontroller

12:00 PM

S-M. Jung, J-M. Nam, D-H. Yang, M-K. Lee
Yonsei University, Seoul, Korea

The ASIC implementation of a capacitive fingerprint sensor SoC has an embedded 32b RISC microcontroller. The SoC also comprises a 160x192 array of cells with a sensor-detecting circuit. The test chip is fabricated in a 0.35μm 4M1P CMOS process with a die size of 12mmx12.7mm.

CONCLUSION 12:15 PM

SESSION 14 SALON 1-6

TD: LOW-POWER WIRELESS AND ADVANCED INTEGRATION

Chair: **Robert Mertens,** *IMEC, Leuven, Belgium*
Associate Chair: **Francis Jeung,** *Brand in Chip, San Jose, CA,*

14.1 A 950MHz Rectifier Circuit for Sensor Networks with 10m-Distance

1:30 PM

T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, S. Otaka
Toshiba, Kawasaki, Japan

A high-sensitivity rectifier is fabricated in a 0.3µm CMOS technology. The circuit can rectify an RF signal less than the NMOS threshold voltage by using a bias voltage between the gate and the drain terminals of a transistor. The IC achieves a 950MHz signal rectification over -14dBm corresponding to 10m-distance communication and recharges a 1.2V secondary battery.

14.2 A 1V 433MHz/868MHz 25kb/s FSK 2kb/s OOK RF transceiver SoC in Standard Digital 0.18µm CMOS

2:00 PM

V. Peiris[1], C. Arm[1], S. Bories[2], S. Cserveny[1], F. Giroud[1], P. Graber[2], S. Gyger[1], E. Le Roux[1], T. Melly[1], M. Moser[2], O. Nys[2], F. Pengg[1], P-D. Pfister[1], N. Raemy[1], A. Ribordy[1], P-F. Ruedi[1], D. Ruffieux[1], L. Sumanen[3], S. Todeschini[2], P. Volet[1]
[1]Swiss Centre of Electronics and Microtechnology, Neuchâtel, Switzerland
[2]Xemics, Neuchâtel, Switzerland
[3]Texas Instruments, Helsinki, Finland

A 1V wireless SoC embedding an RF transceiver, a sensor interface, a 6.4MHz RISC micro-controller with an 8k instruction SRAM and a power management unit is reported. The radio supports 25kb/s FSK and 2kb/s OOK modulations in the 433/868MHz bands. In the 433MHz band, the receiver draws 2.1mA while providing a sensitivity of -108dBm and the transmitter draws 27.6mA for an output power of 10.5dBm.

14.3 Nano-Wires for Room-Temperature-Operated Hybrid CMOS-NANO Integrated Circuits

2:30 PM

S. Ecoffey, V. Pott, M. Mazza, A. Schmid, Y. Leblebici, M. Declercq, A. Ionescu
Swiss Federal Institute of Technology, Lausanne, Switzerland

N-doped polysilicon gated-nanowires (poly-SiNW) are reported. The V-shape and hysteresis of their I-V characteristics are used to build analog and memory circuit cells. Integration of the poly-SiNWs in CMOS is demonstrated. Precise current-measurement application with 1pA resolution and negative differential resistor are reported. A nanoscale capacitor-less hysteresis memory cell using constant-current biased poly-SiNW is designed and experimentally validated.

14.4 A 3D-Integration Scheme Utilizing Wireless Interconnections for Implementing Hyper Brains

2:45 PM

A. Iwata, M. Sasaki, T. Kikkawa, S. Kameda, H. Ando[1], K. Kimoto, D. Arizono, H. Sunami
Hiroshima University, Higashi-Hiroshima, Japan

A 3D integration custom stack system utilizing a local wireless interconnect (LWI) and a global wireless interconnect (GWI) is proposed. The LWI transfers Gb/s pulses using resonant coupling of spiral inductors with low-power dissipation of several mW. The GWI transfers global clocks and data on a 20GHz signal using on-chip antennas.

BREAK 3:00 PM

14.5 A 195Gb/s 1.2W 3D-Stacked Inductive Inter-Chip Wireless Superconnect with Transmit Power Control Scheme

3:15 PM

N. Miura[1], D. Mizoguchi[1], M. Inoue[1], H. Tsuji[1], T. Sakurai[2], T. Kuroda[1]
[1]Keio University, Yokohama, Japan
[2]University of Tokyo, Tokyo, Japan

An inductively coupled wireless interface achieves aggregated data rate of 195Gb/s among 4 stacked chips in a package by arranging 195 transceivers in 50μm pitch with power dissipation of 1.2W. The transmit power is controlled in accordance to the communication distance to reduce both the power dissipation and the cross-talk of the system.

14.6 Substrate Integrity Beyond 1GHz

3:45 PM

M. Nagata[1], M. Fukazawa[1], N. Hamanishi[2], M. Shiochi[2], T. Iida[2], J. Watanabe[2], Y. Murasaka[3], A. Iwata[3]
[1]Kobe University, Kobe, Japan
[2]Toshiba, Kawasaki, Japan
[3]A-R-Tec, Higashi-Hiroshima, Japan

Substrate coupling in a 90nm CMOS technology is evaluated in a 1.2V standard-cell-based loop shift register. Measurement results show that frequency dependence of digital substrate coupling beyond 1GHz is a combination of reduced isolation in device-level coupling through MOSFETs and reduced large-signal circuit-level coupling to the substrate.

14.7 Design For Manufacturability in the Nanometer Era: System Implementation and Silicon Results

4:15 PM

A. Strojwas, J. Kibarian
PDF Solutions, San Jose, CA

A design for manufacturability method to create manufacturable-by-construction designs is presented. Silicon results show significant yield benefit compared to traditional methods.

14.8 A 20GHz CMOS RF Down-Converter with an On-Chip Antenna

4:45 PM

Y. Su, J-J. Lin, K. O
University of Florida, Gainesville, FL

Using a 20GHz down-converter fabricated in a 0.13μm CMOS process, this paper demonstrates the feasibility of a pair of ICs with on-chip antennas communicating over free space. The circuit achieves 9dB conversion gain and 6.6dB SSB NF while consuming 12.8mW from a 1.5V supply.

14.9 A Flexible 8b Asynchronous Microprocessor based on Low-Temperature Poly-Silicon TFT Technology

5:00 PM

N. Karaki, T. Nanmoto, H. Ebihara, S. Utsunomiya, S. Inoue, T. Shimoda
Seiko Epson, Fujimi-machi, Suwa-gun, Japan

A flexible 8b asynchronous microprocessor ACTII based on low-temperature poly-silicon TFT technology, surface-free technology by laser annealing and ablation (SUFTLA®), and asynchronous circuit design language, verilog+, is presented. The 32k-transistor microprocessor draws 180μA from a 5V supply. The power level is 30% of the synchronous counterpart.

CONCLUSION 5:15 PM

SESSION 15 SALON 7

ADCs, DC REFERENCES, AND CONVERTERS

Chair: **Klaas Bult,** *Broadcom, Bunnik, The Netherlands*
Associate Chair: **Venu Gopinathan,** *Texas Instruments, Dallas, TX*

15.1 A Split-ADC Architecture for Deterministic Digital Background Calibration of a 16b 1MS/s ADC

1:30 PM

J. McNeill[1], M. Coln[2], B. Larivee[2]
[1]Worcester Polytechnic Institute, Worcester, MA
[2]Analog Devices, Wilmington, MA

Self-calibration in fewer than 10,000 conversions is demonstrated in a 16b, 1MS/s algorithmic ADC. A split-ADC architecture enables continuous digital background calibration. The analog sub-system of the ADC is implemented in 0.25μm CMOS, consumes 105mW and has a die size of 1.2x1.4mm^2.

15.2 A 3.3mW 12MS/s 10b Pipelined ADC in 90nm Digital CMOS

2:00 PM

R. Wang[1], K. Martin[1], D. Johns[1], G. Burra[2]
[1]University of Toronto, Toronto, Canada
[2]Texas Instruments, Dallas, TX

A 10b pipelined ADC has been realized in a digital 90nm CMOS technology using techniques such as switched opamps and switched-input buffers. Measurements show that this ADC samples at 12 MS/s achieving a peak SNDR of 52.6dB using a 1.2V supply. It consumes 3.3mW and occupies 0.3mm^2 core area.

15.3 A 50MS/s (35mW) to 1kS/s (15μW) Power Scalable 10b Pipelined ADC with Minimal Bias Current Variation

2:30 PM

I. Ahmed, D. Johns
University of Toronto, Toronto, Canada

A new opamp with a short power-on time is used in a 10b 1.5b/stage power scalable pipelined ADC in 0.18μm CMOS. A current modulation technique is used so that as the power is varied from 15μW (at 1kS/s) to 35mW (at 50MS/s) the bias currents only increase by a factor of 50. The SNDR is 54 to 56dB for all sampling rates.

BREAK 3:00 PM

15.4 A 10b 125MS/s 40mW Pipelined ADC in 0.18μm CMOS

3:15 PM

M. Yoshioka, M. Kudo, K. Gotoh, Y. Watanabe
Fujitsu, Kawasaki, Japan

A 10b 125MS/s pipelined ADC uses a new front-end circuit and consumes 40mW from a 1.8V supply. The ADC is implemented in a 0.18μm CMOS process and has an active area of 1.1×0.6mm^2. Measured INL and DNL are within ±0.7LSB, and ±0.5LSB, respectively. Peak SNDR is 53.7dB with a 2MHz input.

15.5 A 30mW 8b 200MS/s Pipelined CMOS ADC Using a Switched-Opamp Technique

3:45 PM

H-C. Kim, D-K. Jeong, W. Kim
Seoul National University, Seoul,Korea

An 8b 200MS/s 2.8b-per-stage pipelined ADC is realized in a 0.18μm CMOS process. By using partially switched opamps, the ADC consumes 30mW from a 1.8V supply and occupies 0.15mm^2. The ADC achieves 47.3dB SNDR, 55.8dB SFDR, and 7.6 ENOB for a 90MHz input at 200MS/s.

15.6 A 0.5μA Precision CMOS Floating-Gate Analog Reference

4:15 PM

B. Ahuja, H. Vu, C. Laber, W. Owen
Intersil, Milpitas, CA

A precision voltage reference with a TC <1ppm/°C is implemented using a floating-gate technique in a 1.5μm CMOS process. The reference is factory programmed from 0.5 to 5V without trim circuits to 0.2mV accuracy. The chip shows long-term drift of 10ppm/(1khr)$^{0.2}$.

15.7 A SC DC-DC Converter with Pseudo-Continuous Output Regulation using a Three-Stage Switchable Opamp

4:45 PM

H. Lee, P. Mok
Hong Kong University of Science and Technology, Hong Kong, China

Pseudo-continuous control is developed for a regulated SC DC-DC converter using a three-stage switchable opamp. The alternate switching of gain stages enables continuous output regulation in all clock phases. The converter achieves an output ripple of 20mV and output recovery time of ~25μs for a load current of 50 to 150mA and switching frequency of 200 to 500kHz in 0.6μm CMOS.

CONCLUSION 5:15 PM

SESSION 16 SALON 8

CLOCK DISTRIBUTION AND POWER CONTROL

Chair: **Hoi-Jun Yoo,** *KAIST, Daejeon, Korea*
Associate Chair: **Souichi Miyata,** *Sharp, Nara, Japan*

16.1 Clock Distribution on a Dual-core Multi-threaded Itanium®-Family Processor

1:30 PM

E. Fetzer[1], P. Mahoney[2], B. Doyle[1], S. Naffziger[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

Clock distribution on the 90nm Itanium® processor is detailed. A region-based active de-skew system reduces the PVT sources of skew across the entire die during normal operation. Clock vernier devices inserted at each local clock buffer allow up to a 10% clock-cycle adjustment via firmware or scan. The system supports a constantly varying frequency and consumes <25W from PLL to latch while providing <10ps of skew across PVT.

16.2 A 90nm Variable-Frequency Clock System for a Power-Managed Itanium®-Family Processor

2:00 PM

T. Fischer[1], F. Anderson[2], B. Patella[1], S. Naffziger[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

A clock-generation system delivers fixed- and variable-frequency clocks for adaptive power control on a 1.7B-transistor dual-core CPU. Frequency synthesizers digitally divide a fixed-frequency PLL clock in 1/64th cycle steps using programmable voltage-frequency-converter loops. 1-cycle loop response tracks supply transients with adaptive modulation, improving CPU performance by over 10% compared to a fixed-frequency design.

16.3 Deterministic Inter-Core Synchronization with Periodically All-in-Phase Clocking for Low-Power Multi-Core SoCs

2:30 PM

K. Nose, A. Shibayama, H. Kodama, M. Mizuno, M. Edahiro, N. Nishi
NEC, Sagamihara, Japan

Periodically all-in-phase clocking (8-step frequency increments with a 4.5ns switching time) and deterministic synchronous bus wrappers (synchronized data transfer among different frequency cores) are developed for dynamic voltage- and frequency-scaling multi-core SoCs. A maximum of 60% power reduction in MPEG-4 decoding with 1.5 to 2X throughput increase are confirmed.

BREAK 3:00 PM

16.4 High-Tension Power Delivery: Operating 0.18μm CMOS Digital Logic at 5.4V

3:15 PM

S. Rajapandian, K. Shepard
Columbia University, New York, NY

A “high-tension” power-delivery system stacks CMOS logic domains to operate at multiples of the supply voltage without explicit downconverters. Experimental results are presented for a prototype system in a 0.18μm technology operating at 3.6V and 5.4V. Peak energy efficiencies as high as 93% are demonstrated at 3.6V.

16.5 Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS

3:45 PM

B. Calhoun, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

Local voltage dithering combined with sub-threshold operation permits ultra-dynamic voltage scaling from 1.1V to below 300mV for a 90nm CMOS adder test chip. Operating at 330mV, it provides minimum energy per cycle with 9-times less energy than ideal shutdown for reduced-rate scenarios. Measurements characterize the minimum energy point across temperature.

16.6 Sleep Transistor Circuits for Fine-Grained Power Switch-Off with Short Power-Down Times

4:15 PM

S. Henzler[1], T. Nirschl[1,2], S. Skiathitis[1,3], J. Berthold[2], J. Fischer[1], P. Teichmann[1], F. Bauer[1], G. Georgakos[2], D. Schmitt-Landsiedel[1]
[1]Technical University Munich, Munich, Germany
[2]Infineon Technologies, Munich, Germany
[3]IBM, Böblingen, Germany

Fine-grained sleep transistor circuits are demonstrated with 0.12μm 16b MAC. Standby power is reduced by a factor of 5500 at 85°C with speed reduction of 5%. Charge recycling reduces the minimum sleep time by 25%. Dynamic power dissipation decreases by 16% activating a fraction of the switch in slow mode. Double switching inhibits power-on glitches and reduces current spikes by 38% .

16.7 Power and Temperature Control on a 90nm Itanium®-Family Processor

4:45 PM

C. Poirier[1], R. McGowen[2], C. Bostak[1], S. Naffziger[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

This paper describes the embedded feedback and control system on a 90nm Itanium®-family processor, code-named Montecito, that maximizes performance while staying within a target power and temperature (PT) envelope. This system utilizes on-chip sensors and an embedded micro-controller to measure PT and modulate voltage and frequency to meet PT constraints.

CONCLUSION 5:15 PM

SESSION 17 SALON 9

RF CELLULAR ICs

Chair: **David Su,** *Atheros Communications, Sunnyvale, CA*
Associate Chair: **Charles Chien,** *SST Communications, Santa Monica, CA*

17.1 A 90nm CMOS Single-Chip GPS Receiver with 5dBm Out-of-Band IIP3 2dB NF

1:30 PM

D. Sahu, A. Das, Y. Darwhekar, S. Ganesan, G. Rajendran, R. Kumar, C. BG, A. Ghosh, A. Gaurav, K. T, A. Goyal, S. Bhagavatheeswaran, K. Mun Low, N. Yanduru, S. Venkatraman
Texas Instruments, Bangalore, India

A single-chip GPS receiver with a low-IF heterodyne RF front-end includes a LNA, image-reject IQ mixers, a passive poly-phase filter, and a fully integrated synthesizer. The IF-strip consists of a jammer-reject filter, a VGA, a $\Delta\Sigma$ ADC, and a digital IF-filter. The receiver dissipates 60mA at 1.4V and acheives a NF of 2dB and out-of-band IIP3 of 5dBm.

17.2 A Single-Chip Si-LDMOS Power Amplifier for GSM

2:00 PM

T. Shimizu, Y. Matsunaga, S. Sakurai, I. Yoshida, M. Hotta
Renesas Technology, Takasaki, Japan

A 0.23µm single-chip Si-LDMOS high-power amplifier with matching circuits and all control blocks for quad-band GSM handset phones is implemented in 2.1×2.45mm^2. The IC achieves maximum PAE of 54% at 36dBm output power and input VSWR of less than 1.6 over the GSM850/900 bands.

17.3 A 1.75GHz GSM/EDGE Polar Modulated CMOS RF Power Amplifier

2:15 PM

P. Reynaert, M. Steyaert
Katholieke Universiteit, Leuven, Belgium

A 0.18µm linearized CMOS power amplifier, based on polar modulation, is implemented in a 1.8x 3.6mm^2. The switching RF PA achieves an output power of 27dBm with a PAE of 34% and an input power of -3dBm. As an EDGE transmitter, the amplifier achieves an average output power of 23.8dBm, a PAE of 22%, an EVM-rms of 1.67%, and an ACPR of -56.7dBc.

17.4 A Loop-Bandwidth Calibration System for Fractional-N Synthesizer and $\Delta\Sigma$ PLL Transmitter

2:30 PM

Y. Akamine[1], M. Kawabe[1], K. Hori[1], T. Okazaki[2], N. Tolson[3], M. Kasahara[4], S. Tanaka[1]
[1]Hitachi, Kokubunji, Japan
[2]Hitachi, Ome, Japan
[3]Renesas Technology, Berkshire, United Kingdom
[4]Renesas Technology, Takasaki, Japan

A 0.25µm BiCMOS fractional-N PLL with loop-bandwidth calibration is implemented in 3.3x3.3mm^2. Using double-integration that integrates VCO output signal over the transient step response, the calibrated PLL achieves tuning accuracy of 2% with less than 2° rms phase error when used as a $\Delta\Sigma$-PLL transmitter for GSM.

BREAK 3:00 PM

17.5 All-Digital PLL and GSM/EDGE Transmitter in 90nm CMOS

3:15 PM

R. Staszewski, J. Wallberg, S. Rezeq, C-M. Hung, O. Eliezer, S. Vemulapalli, N. Barton, M-C. Lee, P. Cruise, C. Fernando, M. Entezari, R. Staszewski, K. Maggio, K. Muhammad, D. Leipold
Texas Instruments, Dallas, TX

A 1.2V 42mA all-digital PLL and polar transmitter for a single-chip GSM/EDGE transceiver is implemented in 90nm CMOS. It transmits GMSK with 0.5° rms phase error and achieves -165dBc/Hz phase noise at 20MHz offset, with 10μs settling time. A digitally controlled 6dBm class-E PA modulates the amplitude- and meets the EDGE spectral mask with 3.5% EVM.

17.6 A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18μm Standard CMOS

3:45 PM

O. Erdogan, R. Gupta, D. Yee, J. Rudell, J-S. Ko, R. Brockenbrough, S-O. Lee, E. Lei, J. Tham, H. Wu, C. Conroy, B. Kim
Berkana Wireless, Campbell, CA

A 0.18μm CMOS single-chip fully integrated quad-band GSM/GPRS transceiver is presented. The low-IF receive section achieves -110dBm sensitivity at the antenna and -15dBm IIP3. The offset-frequency PLL transmitter achieves 1.2° rms phase noise, -65dBc modulation mask at 400kHz, and -165dBc/Hz noise at 20MHz. The chip occupies 17mm^2 and dissipates 95mA/112mA in receive/transmit mode.

17.7 A CMOS Direct Down-Converter with 78dBm Minimum IIP2 for 3G Cell-Phones

4:15 PM

M. Brandolini, P. Rossi, D. Sanzogni, F. Svelto
Università di Pavia, Pavia, Italy

A 0.18μm CMOS direct down-converter achieves 78dBm IIP2, 10dBm IIP3, and 4nV/√Hz noise density while drawing 4mA from a 1.8V supply.

17.8 A 5th-Order Continuous-Time Harmonic-Rejection G_mC Filter with In-Situ Calibration for use in Transmitter Applications

4:30 PM

J. Rudell, O. Erdogan, D. Yee, R. Brockenbrough, C. Conroy, B. Kim
Berkana Wireless, Campbell, CA

A 0.18μm CMOS 5th-order harmonic-rejection G_mC filter is presented for use in offset PLL transmitter applications. Using an in-situ calibration scheme with a tuning accuracy of 2% and a maximum calibration time of 90μs, this filter tunes from 52 to 151MHz and draws 7mA from a 1.8V supply while achieving an IIP3 of 7dBV with an output noise floor of 9.3μV in a 30kHz BW.

17.9 A Fully Integrated Highly Linear Zero-IF CMOS Cellular CDMA Receiver

4:45 PM

N. Kim, V. Aparin, G. Brown, Y. Wu, A. Cicalini, S. Kwok, C. Persico
Qualcomm, San Diego, CA

A 0.25μm highly linear zero-IF CMOS receiver with integrated LNA, down-converter, baseband filter, and VCO supports US and Japanese CDMA applications. The receiver IC occupies 5.8mm^2 and draws 56mA at 2.5V.

CONCLUSION 5:15 PM

Sunday, February 6th	**ISSCC 2005 TUTORIALS**						
	8:00 AM	**T1:** Integrated Power Management **T2:** Introduction to I/O Design for Digital Systems **T3:** RF MEMS: Devices, Circuits and Packaging **T4:** Phase-Change Memory			**T5:** DSP Circuit Technologies for the Nanoscale Era **T6:** Nanotechnology **T7:** Polar modulators for linear wireless transmitters **T8:** High-Speed Electrical Interfaces: Standards And Circuits		
		GIRAFE FORUM			**MEMORY FORUM**		
	8:00 AM	**F1:** Clock and Frequency Generation for Wireline and Wireless Apllications (Salon 9)			**F2:** Advanced Dynamic Memory Design (Salon 7)		
		ISSCC 2005 SPECIAL-TOPIC EVENING SESSIONS					
	7:30 PM	**SE1:** Powerline LAN: Is There a Concrete Wall Dividing Wireless? (Salon 8)		**SE2:** When Processors Hit the Power Wall (or "When the CPU hits the fan") (Salon 7)		**SE3:** Integration in the 3rd Dimension:Opportunities and Challenges (Salon 9)	
Monday, February 7th	**ISSCC 2005 PAPER SESSIONS**						
	8:30 AM	**Session 1:** Plenary Session (Salons 7-9)					
	1:30 PM	**Session 2:** Non-Volatile Memory (Salon 1-6)	**Session 3:** Backplane Transceivers (Salon 7)	**Session 4:** TD: Mixed-Domain Systems (Salon 8)	**Session 5:** WLAN Transceivers (Salon 9)	**Session 6** High-Speed and Oversampled DACs (Salon 10-15)	**Session 7:** Multimedia Processing (NOB HILL)
	5:15 PM	Author Interviews; Social Hour; Poster Session (DAC Student Design Contest Winners) (Golden Gate Hall)					
		ISSCC 2005 DISCUSSION SESSIONS					
	8:00 PM	**E1:** Mobile Imaging: Paradigm Shift or Technology Bubble? (Salon 7)		**E2:** What Papers Will and Will Not Be at ISSCC2010? (Salon 8)		**SE4:** Toward the Nanoscale Transistor - Highlights of 2004 Symposium on VLSI Technology (Salon 9)	
Tuesday, February 8th	**ISSCC 2005 PAPER SESSIONS**						
	8:30 AM	**Session 8:** Circuits for High-Speed Links and CLK-Generators (Salon 1-6)	**Session 9:** Switched-Capacitor $\Delta\Sigma$ Modulators (Salon 7)	**Session 10:** Microprocessors and Signal Processing (Salon 8)	**Session 11:** Ultra Wideband Solutions (Salon 9)	**Session 12** Optical Communications (Salon 10-15)	**Session 13:** Sensors (NOB HILL)
		Session 14: TD: Low-Power Wireless		**Session 16:** Clock Distribution		**Session 18** High-Speed Interconnects	

		(Salon 1-6)	(Salon 7)	(Salon 8)			
	1:30 PM	**Session 14:** TD: Low-Power Wireless and Advanced Integration (Salon 1-6)	**Session 15:** ADC and DC Circuits (Salon 7)	**Session 16:** Clock Distribution and Power Control (Salon 8)	**Session 17**: RF Cellular Ics (Salon 9)	**Session 18** High-Speed Interconnects and Building Blocks (Salon 10-15)	**Session 19:** Imagers (NOB HILL)
	5:15 PM	Author Interviews; Social Hour; Poster Session (DAC Student Design Contest Winners) (Golden Gate Hall)					
		ISSCC 2005 DISCUSSION SESSIONS					
	8:00 PM	**SE5:** SRAM Design in the Nanoscale Era (Salon 9)		**E3:** RF MEMS: Fact or Stiction (Salon 8)		**E4:** Driving Miss Ubiquity: What applications will fill tomorrow's fabs? (Salon 7)	
Wednesday, February 9th		**ISSCC 2005 PAPER SESSIONS**					
	8:30 AM	**Session 20:** Processor Building Blocks (Salon 1-6)	**Session 21:** TD: RF Trends (Salon 7)	**Session 22:** PLL, DLL, and VCOs (Salon 8)	**Session 23:** Wireless Receivers for Consumer Electronics (Salon 9)	**Session 24:** Baseband Processing (Salon 10-15)	**Session 25:** Dynamic Memory (NOB HILL)
	1:30 PM	**Session 26:** Static Memory (Salon 1-6)	**Session 27:** Filters and Continuous-Time $\Delta\Sigma$ Converters (Salon 7)	**Session 28:** Clocking and I/O (Salon 8)	**Session 29:** RF Techniques (Salon 9)	**Session 30:** Displays and Biosensors (Salon 10-15)	**Session 31:** Mass Storage (NOB HILL) **Session 32:** TD: Advanced Array Structures (NOB HILL)
	5:15 PM	Author Interviews (South Grand Assembly)					
Thursday, February 10th		**ISSCC 2005 SHORT COURSE**					
	8:00 AM	RF Circuit Design from Technology to Systems					
		CIRCUIT DESIGN FORUM		**CIRCUIT DESIGN FORUM**		**ATAC FORUM**	
	8:00 AM	**F3:** Characterization of Solid-State Image Sensors		**F4:** Robust Design Solutions for Nanoscale Circuits: From DFM through End-of-Life		**F5:** ATAC: Automotive Technology and Circuits	

BOOK DISPLAY
Monday, February 6th, 12:00 PM - 8:00 PM (Golden Gate Hall)
Tuesday, February 7th, 10:00 AM - 8:00 PM (Golden Gate Hall)
Wednesday, February 8th, 10:00 AM - 5:00 PM (Golden Gate Hall)

SESSION 18 SALON 10-15

HIGH-SPEED INTERCONNECTS AND BUILDING BLOCKS

Chair: **Vadim Gutnik,** *Impinj, Newport Beach, CA*
Associate Chair: **Michael Green,** *University of California, Irvine. CA*

18.1 A 10Gb/s CMOS Adaptive Equalizer for Backplane Applications

1:30 PM

S. Gondi[1], J. Lee[2], B. Razavi[1]
[1]University of California, Los Angeles, CA
[2]National Taiwan University,Taepei, Taiwan,

An equalizer employs reverse scaling and dual-loop adaptation to achieve a binary data rate of 10Gb/s. Realized in 0.13μm CMOS technology, the circuit adapts to traces up to 30 inches on FR4 boards while consuming 25mW from a 1.2V supply.

18.2 A 7-Tap Transverse Analog FIR Filter in 0.12μm CMOS for Equalization of 10Gb/s Fiber-Optic Data Systems

2:00 PM

S. Reynolds, P. Pepeljugoski, J. Schaub, J. Tierno, D. Beisser
IBM, Yorktown Heights, NY

A 130mA 2.5V 7-tap analog FIR equalizer for 10Gb/s fiber-optic links is implemented in a 0.12μm CMOS process. The filter precedes the receiver CDR and recovers data signals distorted by multi-mode fiber dispersion over a 600m link to a BER $<10^{-12}$. Tap delays are implemented by a combination of passive and buffered LC transmission lines.

18.3 A 10 Gb/s Eye-Opening Monitor in 0.13μm CMOS

2:30 PM

B. Analui[1], A. Rylyakov[2], S. Rylov[2], A. Hajimiri[1]
[1]California Institute of Technology, Pasadena, CA
[2]IBM, Yorktown Heights, NY

An eye-opening monitor circuit in 0.13μm CMOS operates from 1 to 12.5Gb/s at 1.2V supply. It maps the input eye to a 2D error diagram with 68dB mask error dynamic range. Left and right half of the eye are monitored separately to capture asymmetric eyes. Tested input amplitude is from 50 to 400mV. The chip consumes 330mW and works at 10Gb/s with a supply voltage as low as 1V.

BREAK 3:00 PM

18.4 A 100mW 4x10Gb/s Transceiver in 80nm CMOS for High-Density Optical Interconnects

3:15 PM

C. Kromer[1], G. Sialm[1], C. Berger[2], T. Morf[2], F. Ellinger[1], M. Schmatz[2], D. Erni[1], G-L. Bona[2], H. Jäckel[1]
[1]Swiss Federal Institute of Technology, Zürich, Switzerland
[2]IBM, Rüschlikon, Switzerland

A quad-optical transceiver in 80nm CMOS transmits 10Gb/s/ channel over a multi-mode fiber at a BER of $<10^{-12}$. Each driver consumes 2mW from a 0.8V supply and a VCSEL requires 7mA from a 2.4V supply. The receiver excluding the output buffer consumes 6mW from a 1.1V supply per channel and features a transimpedance gain of 10.1kΩ.

18.5 A 0.25μm CMOS 3b 10GS/s Frequency Channelized Receiver for Serial-Links

3:45 PM

K. Lee, W. Namgoong
University of Southern California, Los Angeles, CA

A frequency channelized receiver that samples at an effective sampling frequency of 10GS/s with 3b resolution is fabricated in a 0.25μm CMOS process. The chip occupies 4mm^2 and consumes 1W at 2.5V supply. The functionality of the receiver is demonstrated by correctly reconstructing data from 10GS/s in a channel with significant ISI.

18.6 An RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access in Chip-to-Chip Communication

4:15 PM

J. Ko[1], J. Kim[1], Z. Xu[2], Q. Gu[1], C. Chien[1,2], M. Chang[1]
[1]University of California, Los Angeles, CA
[2]SST Communications, Los Angeles, CA

An RF/baseband FDMA-interconnect transceiver, implemented in 0.18μm CMOS, enables reconfigurability and multiple access for multi-I/Os on a shared bus. The RF/baseband transceiver achieves an aggregate data rate of 3Gb/s/pin (3.6Gb/s/pin) for bi-directional (uni-directional) signaling while dissipating 92mW and occupying 0.65mm^2.

18.7 A 40Gb/s 2.5V 2^7-1 PRBS Generator in SiGe Using a Low-Voltage Logic Family

4:45 PM

D. Kucharski, K. Kornegay
Cornell University, Ithaca, NY

A 40Gb/s PRBS generator with a sequence length of 2^7-1 is implemented in a SiGe BiCMOS process with f_T=120GHz. It consumes 550mW from a 2.5V supply. Low-voltage operation is achieved through the use of an alternative family of logic gates with reduced device stacking.

18.8 A 72Gb/s 2^{31}-1 PRBS Generator in SiGe BiCMOS Technology

5:00 PM

T. Dickson[1], E. Laskin[1], I. Khalid[2], R. Beerkens[2], J. Xie[2], B. Karajica[2], S. Voinigescu[1]
[1]University of Toronto, Toronto, Canada
[2]STMicroelectronics, Ottawa, Canada

A 2^{31}-1 72Gb/s PRBS generator is reported in a 0.13μm SiGe BiCMOS technology with 150GHz-f_T HBTs. Variable delays are introduced along the 36GHz clock path to increase timing margins. A true BiCMOS logic family using NMOS FETs in the clock path is employed throughout the circuit, which dissipates 9.28W from a 3.3V supply to provide a single-ended output swing of 300mV at 72Gb/s.

CONCLUSION 5:15 PM

SESSION 19 NOB HILL

IMAGERS

Chair: **Abbas El Gamal,** *Stanford University, Stanford, CA*
Associate Chair: **Hirofumi Sumi,** *Sony, Kanagawa, Japan*

19.1 A 1/4.5" 3.1M Pixel FT-CCD with 1.56μm Pixel Size for Mobile Applications

1:30 PM

M. Oda, T. Kaida, S. Izawa, T. Ogo, K. Itsumi, Y. Okada, K. Sasada
Sanyo Electric, Gifu, Japan

The frame-transfer CCD (FT-CCD) achieves a saturation signal voltage of 270mV and a sensitivity of 280mV/lx·s in full-resolution still mode. The sensor can also operate in a 30f/s VGA with a movie mode with saturation signal voltage of 1040mV and a sensitivity of 960mV/lx·s. A 9-phase vertical transfer technique reduces smear signals to -75dB.

19.2 A 2.0μm Pixel-Pitch MOS Image Sensor with an Amorphous Si Film Color Filter

2:00 PM

M. Kasano, Y. Inaba, M. Mori, S. Kasuga, T. Murata, T. Yamaguchi
Matsushita, Kyoto, Japan

A CMOS image sensor with an amorphous Si film color filter is implemented on a standard Si process. The color filter thickness is less than 100nm. The sensor achieves a 30% aperture ratio by a 1.5transistor/pixel architecture and a 0.15μm design rule.

19.3 A 19.5b DR CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters

2:15 PM

M. Mase[1], S. Kawahito[1], M. Sasaki[2], Y. Wakamori[3]
[1]Shizuoka University, Shizuoka, Japan
[2]Sendai National College of Technology, Miyagi, Japan
[3]Yamaha, Shizuoka, Japan

A CMOS image sensor with 117dB DR is demonstrated in a 0.25μm CMOS technology through merging of multiple exposures. A 12b cyclic ADC with integrated noise canceling is implemented in the column of the image sensor and achieves a DNL of +0.4/-0.8 LSB.

19.4 A 100dB DR CMOS Image Sensor Using a Lateral Overflow Integration Capacitor

2:30 PM

S. Sugawa[1], N. Akahane[1], S. Adachi[2], K. Mori[2], T. Ishiuchi[2], K. Mizobuchi[2]
[1]Tohoku University, Miyagi, Japan
[2]Texas Instruments, Ibaragi, Japan

The wide DR CMOS image sensor incorporates a lateral overflow capacitor in each pixel to integrate the overflow charges from the photodiode when it saturates. The 7.5×7.5μm^2 pixel, 1/3" VGA sensor fabricated in a 0.35μm 3M2P CMOS process achieves a 100dB dynamic range with no image lag, 0.15mV$_{rms}$ random noise and 0.15mV fixed pattern noise.

19.5 A Linear-Logarithmic CMOS Sensor with Offset Calibration Using an Injected Charge Signal

2:45 PM

K. Hara, H. Kubo, M. Kimura, F. Murao, S. Komori
Renesas Technology, Hyogo, Japan

A combined linear and logarithmic image sensor is implemented in a 0.35μm 1P3M technology. The pixel is 7.5x7.5μm^2 with a 37% fill factor and contains only 4 transistors. Offset calibration in the logarithmic region is realized by using electrical charge injection into the photodiode. The sensor achieves 120dB DR and the offset calibration reduces the FPN from 13mV to 5mV.

BREAK 3:00 PM

19.6 Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology

3:15 PM

V. Suntharalingam, R. Berger, J. Burns, C. Chen, C. Keast, J. Knecht, R. Lambert, K. Newcomb, D. O'Mara, D. Rathman, D. Shaver, A. Soares, C. Stevenson, B. Tyrrell, K. Warner, B. Wheeler, D. Yost, D. Young
MIT Lincoln Laboratories, Lexington, MA

A 1024x1024 integrated image sensor with 8μm pixels, is developed with 3D fabrication in 150mm wafer technology. Each pixel contains a 2μmx2μmx7.5μm 3D via to connect a deep depletion, 100% fill-factor photodiode layer to a fully depleted SOI CMOS readout circuit layer. Pixel operability exceeds 99.9%, and the detector has a dark current of <3nA/cm^2 and pixel responsivity of ~9μV/e at room temperature.

19.7 A Progressive 1920x1080 Imaging SoC for HDTV Cameras

3:45 PM

L. Kozlowski, G. Rossi, L. Blanquart, R. Marchesini, Y. Huang, G. Chow, J. Richardson
AltaSens, Thousand Oaks, CA

A 2/3" 5μmx5μm pixel HDTV imager in a 0.25μm CMOS process uses a tapered reset technique to suppress kT/C noise and supply 12b video with <15 e-read noise at 60, 72 and 90Hz frame rates. Peak S/N ratio at 90Hz(225MHz video rate; 2.7Gb/s at 12b/pixel) is 52dB at standard scene illumination. Random noise at 18dB gain is 8e-, independent of video frequency.

19.8 A High-Speed Profile Data Acquiring Image Sensor

4:15 PM

Y. Sugiyama, M. Takumi, H. Toyoda, N. Mukozaka, A. Ihori, T. Kurashina, Y. Nakamura, T. Tonbe, S. Mizuno
Hamamatsu Photonics, Shizuoka, Japan

A profile imager for high-speed automatic target tracking has the capability of executing both target-tracking control from a 512x512 image array of 20μmx20μm pixels and the acquisition of a sub-array, simultaneously. 128x128 partial images of an automobile license plate can be captured at 1620f/s. A 0.6μm 3M2P CMOS process is used to implement the 13.0mm×14.3mm imager.

19.9 Temporal Change Threshold Detection Imager

4:45 PM

U. Mallik, M. Clapp, E. Choi, G. Cauwenberghs, R. Etienne-Cummings
Johns Hopkins University, Baltimore, MD

A 90x90 active pixel sensor (APS) achieves 2% in-pixel change/motion detection at 30f/s consuming 4.2mW. The 6T 2C 25μmx25μm pixel in 0.5μm 2P3M CMOS provides intensity readout, detection of change events and polarities. Event address and APS value output are asynchronous, facilitating compression. The imager is intended for low-power low-bandwidth surveillance network applications.

19.10 A Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging

5:00 PM

C. Niclass, E. Charbon
Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland

An avalanche photodiode array uses single-photon counting to perform time-of-flight range-finding on a scene uniformly hit by 100ps 250mW uncollimated laser pulses. The 32x32 pixel sensor, fabricated in a 0.8μm CMOS process uses a microscanner package to enhance the effective resolution in the application to 64x64 pixels. The application achieves a measurement depth resolution of 1.3mm to a depth of 3.75m.

CONCLUSION 5:15 PM

SE5: SRAM Design in the Nanoscale Era

(Salon 9)

Organizer: **Sreedhar Natarajan,** *MoSys, Stittsville, Canada*
Chair: **Alexander Shubat,** *Virage Logic, Fremont, CA*

The geometries of SRAMs have shrunk substantially over the years. SRAMs have been the mainstream embedded memory for most applications (processors, graphics, etc.), although a new suite of replacements is being researched. In the sub-90nm era, SRAMs face a new set of issues that need to be addressed and solved in the areas of design, test and process. Twenty years ago, soft errors emerged as a problem for DRAMs, which store data in a single capacitor. This was not a concern for SRAMs. Soft error rates (SER) are caused when a neutron, alpha particle or some other ionizing particle strikes a solid-state memory and may degrade the stored data. As transistor geometries have shrunk, SER becomes a much bigger issue in SRAMs. Considering the incredibly high wafer cost, there is not much incentive for companies to spin multiple silicon shuttles and hence, have to ensure the design is equipped with Design for Testability (DFT) capabilities. Robust dynamic and static circuits and design margins are also key for proper functionality. Leakage is another critical concern for power-aware systems and innovative circuit techniques are required to address the standby leakage. The experienced speakers address leakage, DFT and SER issues in SRAMs.

Time	Topic
8:00	***SRAM Design in 90nm Era***, **Harold Pilo,** *IBM, Essex Junction, VT*
8:30	***Test Solutions to Improve SRAM Yield,*** **Yervant Zorian,** *Virage Logic, Fremont, CA*
9:00	***SER in SRAMs,*** **Robert Baumann,** *Texas Instruments, Dallas, TX*
9:30	***SRAM Leakage-Reduction Techniques,*** **Soon Moon Jung**, *Samsung, Yongin-City, Korea*

E3: RF MEMS: Fact or Stiction

(Salon 8)

Organizer: **Ken Cioffi,** *Discera, San Jose, CA*
Moderator: **Bob Puers,** *Katholieke Universiteit Leuven, Leuven Belgium*

RF MEMS components including switches, varactors, inductors, resonators, and filters have been proposed for use in RF systems. Can these components replace traditional technologies such as semiconductor switches, quartz crystals, and SAW resonators or will manufacturability/cost/performance issues keep them always on the horizon? Alternatively, will advanced circuit techniques make many of these components obsolete before they come to market or will RF MEMS play a key role in determining new circuit topologies?

Panelists:

Natalino Camilleri, *RF & Wireless Design Services, Cupertino, CA*
Dan Hyman, *XCom Wireless, Signal Hill, CA*
Bill Krenik, *Texas Instruments, Dallas, TX*
Clark T.-C. Nguyen, DARPA, *Arlington, VA* and University of Michigan, Ann Arbor, MI
Tomoki Uwano, *Matsushita, Osaka, Japan*
Benedetto Vigna, *ST Microelectronics, Milano, Italy*

E4: Driving Miss Ubiquity: What applications will fill tomorrow's fabs?

(Salon 7)

Organizer: **Toru Shimizu,** *Renesas Technology, Tokyo, Japan*
Moderator: **Robert Brodersen,** *University of California, Berkeley, CA*

The objective of this panel is to describe the applications that will drive the demand for advances in silicon technology and integrated circuit design. The panelist will debate the merits and universal appeal of several applications such as body area networks, smart dust, ambient intelligence, cell phones, RFID tags, and ubiquitous networks.

Panelists:

Gerard Beenker, *Philips, Eindhoven, The Netherlands*
Robert Glidden, *Impinj, Seattle, WA*
Bert Gyselinckx, *IMEC, Leuven, Belgium*
Ryo Imura, *Hitachi, Tokyo, Japan*
Hirotaka Nakano, *Osaka University, Osaka, Japan*
Kristofer S.J. Pister, *Dust Networks, Berkeley, CA*

SESSION 20 SALON 1-6

PROCESSOR BUILDING BLOCKS

Chair: **Atila Alvandpour,** *Linkoping University, Linkoping, Sweden*
Associate Chair: **Fumio Arakawa,** *Hitachi, Tokyo, Japan*

20.1 An 8GHz Floating Point Multiply

8:30 AM

W. Belluomini, D. Jamsek, A. Martin, C. McDowell, R. Montoye, T. Nguyen, H. Ngo, J. Sawada, I. Vo, R. Datta
IBM, Austin, TX

The implementation of the mantissa portion of a floating-point multiply (54x54b) is described. The 0.124mm^2 multiplier is implemented using limited switch dynamic logic and operates at speeds up to 8GHz in a 90nm SOI technology. The multiplier dissipates between 150mW and 1.8W as it scales between 2GHz and 8GHz.

20.2 A 110GOPS/W 16b Multiplier and Reconfigurable PLA Loop in 90nm CMOS

9:00 AM

S. Hsu, S. Mathew, M. Anders, B. Bloechel, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

A 16b 2's-complement multiplier with a reconfigurable PLA control block is fabricated in a 90nm dual-V$_t$ CMOS process and occupies 0.03mm^2. It performs 1GHz single-cycle operations and dissipates 9mW to deliver 110GOPS/W at 1.3V, and is frequency scalable to 1.5GHz at 1.95V. PMOS sleep transistors enable an ultra low standby-mode power of 75μW with wake-up time < 1 cycle.

20.3 A Double-Precision Multiplier with Fine-Grained Clock-Gating Support for a First-Generation CELL Processor

9:30 AM

J. Kuang[1], T. Buchholtz[2], S. Dance[2], J. Warnock[3], S. Storino[2], D. Wendel[4]
[1]IBM, Austin, TX
[2]IBM, Rochester, MN
[3]IBM, Yorktown Heights, NY
[4]IBM, Böblingen, Germany

A double-precision multiplier for a 90nm SOI CELL processor is presented. Dynamic Booth logic is designed for scalability and with noise, leakage, and pulse-width variation tolerance. Static partial-product compression is implemented with replicated bits for performance. The design supports fine-grained clock gating domains for active power reduction.

BREAK 10:00 AM

20.4 A Low-Leakage 2.5GHz Skewed CMOS 32b Adder for Nanometer CMOS Technologies

10:15 AM

K. von Arnim[1,2], P. Seegebrecht[2], R. Thewes[1], C. Pacha[1]
[1]Infineon Technologies, Munich, Germany
[2]Christian Albrecht University, Kiel, Germany

A 32b parallel prefix adder demonstrates leakage-current-reduction capabilities of skewed CMOS logic. Sub-100nA leakage currents and single-cycle activation from standby mode is achieved using multi-tox logic gates in 90nm CMOS technology. The data path contains improved sense amplifier-based flip-flops and skewed CMOS logic adapted latches.

20.5 The Multi-threaded Parity-Protected 128-Word Register Files on a Dual-Core Itanium®-Family Processor

10:45 AM

L. Wang[1], E. Fetzer[2], J. Jones[3]
[1]University of Connecticut, Storrs, Connecticut
[2]Hewlett Packard, Fort Collins, CO
[3]Intel, Fort Collins, CO

The dual-thread 18-port 128wx82b FPU register file, and the 22-port 128wx65b integer register file of the microprocessor is described. Parity embedded into each register provides soft error detection. The design integrates a charge-compensated thread switch and power-saving features to operate at 1.1V consuming 400mW at maximum frequency.

20.6 A 32b 64-Word 9-Read-Port/7-Write-Port Pseudo Dual-Bank Register File Using Copied Memory Cells for a Multi-Threaded Processor

11:15 AM

M. Sumita, Y. Ikeda
Matsushita, Kyoto, Japan

A method for copying memory cells to reduce the size of the register file for a multi-threaded processor is proposed. The number of transistors in the memory cell is reduced to 70% and the total bit and word lines is reduced to 63%. The register file is implemented in a 100nm CMOS process. The size of the register file is reduced to 62% of a conventional register file. The power consumption is reduced by 50%.

20.7 A 3Gb/s/ch Transceiver for RC-limited On-Chip Interconnects

11:45 AM

D. Schinkel[1], E. Mensink[1], E. Klumperink[1], E. van Tuijl[1,2], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands
[2]Philips, Eindhoven, The Netherlands

A bus-transceiver chip in 0.13μm CMOS uses 10mm uninterrupted differential interconnects of 0.8μm pitch (82MHz RC-limited bandwidth). The chip achieves 3Gb/s/ch using a pulse-width pre-emphasis technique in combination with resistive termination while twisted interconnects mitigate crosstalk. Power consumption is 6mW/ch at a 1.2V supply.

CONCLUSION 12:15 PM

SESSION 21 SALON 7

TD: RF TRENDS: ABOVE-IC INTEGRATION AND MM-WAVE

Chair: **Ernesto Perea,** *ST Microelectronics, Crolles, France*
Associate Chair: **Christian Enz,** *CSEM, Neuchatel, Switzerland*

21.1 Tunable RF and Analog Circuits Using On-Chip MEMS Passive Components

8:30 AM

G. Fedder, T. Mukherjee
Carnegie Mellon University, Pittsburgh, PA

Micromachining in RF foundry processes enhances inductor and capacitor quality factors, increases varactor tuning range, and supports creation of electromechanical mixer-filters that down-convert RF signals from GHz to MHz frequency band with built-in frequency selectivity. An on-chip parallel receiver architecture and circuit blocks incorporating these MEMS devices for low-power operation are presented.

21.2 Integration of High-Q BAW Resonators and Filters above IC

9:00 AM

M. Dubois[1], C. Billard[2], C. Muller[1], G. Parat[2], P. Vincent[2]
[1]Swiss Centre of Electronics and Microtechnology, Neuchâtel, Switzerland
[2]CEA - LETI, Grenoble, France

A double-lattice BAW filter with balanced input and output is designed with a center frequency of 2.14GHz. The filter is integrated directly above a 0.25µm BiCMOS RF IC. Insertion loss of -3dB and out-of-band rejection better than -50dB are achieved. An integrated LNA comprising two broadband amplifiers and one BAW filter is also presented.

21.3 A SiGe:C BiCMOS WCDMA Zero-IF RF Front-End Using an Above-IC BAW Filter

9:30 AM

J-F. Carpentier[1], A. Cathelin[1], C. Tilhac[1], P. Garcia[1], P. Persechini[1], P. Conti[2], P. Ancey[1], G. Bouche1, G. Caruyer[1], D. Belot[1], C. Arnaud[1], C. Billard[3], G. Parat[3], J-B. David[3], P. Vincent[3], M-A. Dubois[4], C. Enz[4]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Plan-les-Ouates, Switzerland
[3]CEA - LETI, Grenoble, France
[4]Swiss Centre of Electronics and Microtechnology, Neuchatel, Switzerland

The feasibility of a fully integrated RF front-end using an above-IC BAW integration technique is demonstrated for WCDMA applications. The circuit has a voltage gain of 31.3dB, a noise figure of 5.3dB, an in-band IIP3 of -8dBm and IIP2 of 38dBm, with a total power consumption of 36mW. The BAW filter area is 0.45mm^2 and the total circuit area including the BAW filter is 2.44mm^2.

21.4 A 450µW-RX 1.6mW-TX Super-Regenerative Transceiver for Wireless Sensor Networks

9:45 AM

B. Otis, Y-H. Chee, J. Rabaey
University of California, Berkeley, CA

A fully-integrated 2GHz super-regenerative transceiver is implemented in a 0.13µm CMOS process. The transmit and receive paths utilize BAW resonators, yielding a 450µW 1V RF front-end and a transmitter delivering 380µW with 23% efficiency. At 5kb/s, the receiver achieves a sensitivity of -100.5dBm for 10^{-3} BER.

BREAK 10:00 AM

21.5 Thin Film as Enabling Passive Integration Technology for RF SoC and SiP

10:15 AM

G. Carchon, X. Sun, G. Posada, D. Linten, E. Beyne
IMEC, Leuven, Belgium

Thin-film Cu/BCB technology with integrated inductors, resistors and capacitors is described for the realization of high-quality on-chip and in-package Si-based passive elements. Thin-film SiP and SoC inductor and transmission line performances are compared. A SiP 7GHz power splitter, a 50GHz BPF, and two 90nm CMOS VCOs operating at 5.8GHz and 15GHz with on-chip thin-film inductors are discussed.

21.6 A 60GHz Direct-Conversion CMOS Receiver

10:45 AM

B. Razavi
University of California, Los Angeles, CA

A direct-conversion receiver incorporates folded microstrip lines to create resonance at 60GHz in a common-gate LNA and active mixers. Realized in 0.13μm CMOS technology, it provides a voltage gain of 28dB with 12.5dB NF while consuming 9mW from a 1.2V supply.

21.7 A 70GHz Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology

11:15 AM

M-D. Tsai[1], H. Wang[1], J-F Kwan[2], C-S Chang[2],
[1]National Taiwan University, Taipei, Taiwan
[2]TSMC, Hsin-Chu, Taiwan

A broadband cascaded multi-stage distributed amplifier (CMSDA) is implemented in a standard 90nm CMOS technology. The 0.72mm^2 CMOS cascaded multi-stage distributed amplifier achieves better than 7dB gain with a bandwidth of 70GHz, 10dBm output power for 1dB compression at 30GHz, 9.3dBm IIP3 at 40GHz and 6.4dB average NF from 1 to 25GHz.

21.8 A 114GHz VCO in 0.13μm CMOS Technology

11:45 AM

P-C. Huang[1], M-D. Tsai[1], H. Wang[1], C-S Chang[2]
[1]National Taiwan University, Taipei, Taiwan
[2]TSMC, Hsin-Chu, Taiwan

A D-band (110 to 170GHz) CMOS VCO is presented. This push-push VCO implemented in standard 0.13μm CMOS technology has a 114GHz output signal with a phase noise of -107.6dBc/Hz at 10MHz offset and power consumption of 8.4mW from a 1.2V supply.

21.9 A Fully Integrated BiCMOS PLL for 60GHz Wireless Applications

12:00 PM

W. Winkler, J. Borngräber, B. Heinemann, F. Herzel
IHP, Frankfurt (Oder), Germany

An integrated PLL aimed at wireless transceivers in the unlicensed band from 59GHz to 64GHz is described. The PLL was fabricated in a SiGe:C BiCMOS technology with both f_T/f_{max}=200GHz. The measured PLL lock range is from 53.3GHz to 55.7GHz. It operates from a 3V supply except for a first divide-by-two stage which requires a 5V supply. Total power consumption is 895mW.

CONCLUSION 12:15 PM

SESSION 22 SALON 8

PLL, DLL, AND VCOs

Chair: **Roger Minear,** *Agere Systems, Wyomissing, PA*
Associate Chair: **Thomas Burger,** *Swiss Federal Institute of Technology, Zurich, Switzerland*

22.1 A 0.94ps-rms-Jitter 0.016mm² 2.5GHz Multi-Phase Generator PLL with 360° Digitally Programmable Phase Shift for 10Gb/s Serial Links

8:30 AM

T. Toifl[1], C. Menolfi[1], P. Buchmann[1], M. Kossel[1], T. Morf[1], M. Ruegg[2], R. Reutemann[2], M. Schmatz[1], J. Weiss[1]
[1]IBM, Rueschlikon, Switzerland
[2]Miromico, Zurich, Switzerland

A PLL generates 8 equidistant clock phases whose timing with respect to a reference clock can be simultaneously shifted in 3ps steps by a digital value. Each VCO phase is fed to a dedicated phase detector and the weighted dectector outputs are summed. Fabricated in 90nm SOI-CMOS technology, the PLL has a jitter of 0.94ps$_{rms}$ at 2.5GHz and consumes 20mW from a 0.9V supply.

22.2 A 15mW 3.125GHz PLL for Serial Backplane Transceivers in 0.13µm CMOS

9:00 AM

J. Parker[1], D. Weinlader[2], J. Sonntag[1]
[1]Synopsys, Hillsboro, OR
[2]Synopsys, Allentown, PA

A 3.125GHz PLL fabricated in a 0.13µm CMOS process in a area of 0.064mm² is described. The PLL uses an architecture optimized for low noise, low power and small die area. In steady-state operation, the PLL forces the up and down currents in the charge pump to match one another. The total measured jitter is 1.3ps rms when operating at 3.125GHz and the chip consumes 15mW.

22.3 A Low-Jitter Wideband Multi-Phase PLL

9:30 AM

M. Kossel, P. Buchmann, C. Menolfi, T. Morf, T. Toifl, M. Schmatz
IBM, Rueschlikon, Switzerland

A multi-phase PLL, implemented in 90nm SOI CMOS, covers a frequency range from 4.3 to 7.4GHz at a supply voltage of 1V. The ring-oscillator-based PLL shows an in-band phase noise of up to -113dBc/Hz at 1 MHz offset and a supply noise rejection of 0.23%delay/%supply due to the rigorous application of CML-type circuit topologies combined with replica biasing.

BREAK 10:00 AM

22.4 A 44GHz Differentially Tuned VCO with 4GHz Tuning Range in 0.12µm SOI CMOS

10:15 AM

J. Kim, J-O. Plouchart, N. Zamdmer, R. Trzcinski, K. Wu, B. Gross, M. Kim
IBM, Hopewell Junction, NY

A differentially tuned VCO is fully integrated in a standard microprocessor 0.12µm SOI CMOS. A phase noise of -101.8dBc/Hz at 1MHz offset is measured with 7.5mW at 1.5V. The VCO tuning range is 9.8% from 40GHz to 44GHz. The output power is up to -6dBm after a single-stage buffer amplifier with 6mW at 1.5V.

22.5 A Low-Phase-Noise 0.004ppm/Step DCXO with Guaranteed Monotonicity in 90nm CMOS

10:45 AM

J-C. Lin
Texas Instruments, Plano, TX

A 26MHz DCXO achieves phase noise of -140dBc/Hz at 1kHz, -152dBc/Hz at 10kHz offset, and supply pushing of 0.5ppm/V. Frequency tuning is done by a pre-distorted 14b MOS capacitor DAC. Monotonicity of ~0.004ppm/step across the entire 70ppm tuning range is guaranteed by a $\Delta\Sigma$ modulation scheme. The circuit occupies 0.18mm^2 in 90nm CMOS.

22.6 A Self-Biased PLL With Current-Mode Filter for Arbitrary Clock Generator

11:15 AM

G. Yan, C. Ren, Z. Guo, Q. Ouyang, Z. Chang
Integrated Device Technology, Shanghai, China

A self-biased PLL with current mode filter is designed to achieve a bandwidth that scales with reference clock and is independent of PVT and multiplication factor. It provides wide tuning range with a simple robust structure. The 0.2mm^2 chip is fabricated in 0.35μm CMOS. Running at 800MHz, the phase jitter is 72.7ps$_{pp}$ and the power consumption is 20mW.

22.7 An Ultra-Low-Power Fast-Lock-in Small-Jitter All-Digital DLL

11:45 AM

J-S. Wang, Y-M. Wang, C-H. Chen, Y-C. Liu
Chung-Cheng University, Chia-Yi, Taiwan

Using binary-weighted differential-delay cells and an asynchronous binary search circuit, the proposed 1.0V 0.25μm all-digital DLL achieves nearly 2 orders of magnitude reduction in power consumption, a 36% reduction in jitter, and a 33% reduction in locking cycles, compared to conventional fast-lock mixed-mode DLLs.

CONCLUSION 12:15 PM

SESSION 23 SALON 9

WIRELESS RECEIVERS FOR CONSUMER ELECTRONICS

Chair: **John R. Long,** *Delft University of Technology, Delft, The Netherlands*
Associate Chair: **Tony Montalvo,** *Analog Devices, Raleigh, NC*

23.1 A Direct-Conversion Receiver for DVB-H

8:30 AM

N. Kearney[1], P. Antoine[2], P. Bauser[3], B. Hugues[2], M. Buchholz[4], D. Carey[1], T. Cassagnes[2], T. Chan[1], S. Colomines[2], F. Hurley[1], D. Jobling[3], A. Murphy[1], J. Rock[1], D. Salle[2], C-T. Tu[3]
[1]Freescale Semiconductor, Cork, Ireland
[2]Freescale Semiconductor, Toulouse, France
[3]Freescale Semiconductor, Geneva, Switzerland
[4]Freescale Semiconductor, Munich, Germany

A 240mW direct-conversion DVB-H receiver in a 0.35μm BiCMOS process is presented. The receiver covers UHF bands IV and V, and exhibits a nominal 80dB gain, 8.5dB NF, and 8.5dBm IIP3. The IC includes an LNA, dual quadrature mixers, base-band filtering, three 4x VCOs, an integer PLL, and a reference oscillator.

23.2 UMTV: a Single Chip TV Receiver for PDAs, PCs and Cell-Phones

9:00 AM

H. Rumpt[1], D. Kasperkovitz[1], J. van der Tang[2], B. Nauta[3]
[1]ItoM, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands
[3]University of Twente, Enschede, The Netherlands

A zero-external-component TV receiver for portable platforms is realized in a mainstream 8GHz-f_T BiCMOS process. Die size is 5×5mm^2 and power dissipation is 50mA at 3V. The receiver includes a single tunable LNA (3mA) with less than 5dB NF from 40 to 900MHz. The programmable IF filters cover all analog and digital standards.

23.3 A 120nm CMOS DVB-T Tuner

9:30 AM

D. Saias, F. Montaudon, E. Andre, M. Bely, P. Busson, S. Dedieu, A. Dezzani, A. Moutard, G. Provins, E. Rouat, J. Roux, G. Wagner, F. Paillardet
STMicroelectronics, Crolles, France

A DVB-T tuner is integrated in 0.12μm CMOS. The 16mm^2 chip integrates a double conversion chain including PLL, VCOs, voltage regulators, and ADC. The receiver exhibits a 6.5dB NF, a VCO phase noise of -140dBc/Hz at 1MHz offset at 1.21GHz, and a 14b ADC. It is compatible for integration with a digital demodulator IP.

Break 10:00 AM

23.4 A CMOS TV Tuner/Demodulator IC with Digital Image Rejection

10:15 AM

C-H. Heng[1], M. Gupta[1], S-H. Lee[1], D. Kang[1], B-S. Song[2]
[1]Chrontel, San Diego, CA
[2]University of California, San Diego, CA

A single-chip TV tuner/demodulator IC using a low-IF dual-conversion architecture is implemented. It receives the NTSC/PAL/SECAM signals in the 48 to 860MHz frequency range without off-chip image filters, and performs channel selection, image rejection, and video/sound demodulation digitally. The 6x6mm^2 chip in 0.25μm CMOS with on-chip 75Ω cable driver consumes 1W from a 2.5V supply.

23.5 A Compact Triple-Band Eureka-147 RF Tuner with an FM Receiver

10:45 AM

G. Luff, S. Tuncer, N. Troop, C. Taylor, D. Eddowes
Frontier Silicon, Cambridge, United Kingdom

A 0.35μm SiGe BiCMOS single-chip RF tuner for DAB and DMB receives DAB signals in both L-Band and Band 3, and FM broadcast signals on Band 2. The chip contains a VCO, integer-N PLL, multi-band LNA with an AGC, quadrature mixer, IF filter, IF AGC amplifier and supply regulators. The 2.5mmx2.5mm die has a sensitivity of -100dBm in Band 3, is packaged in a 5mm×5mm QFN-32, and consumes 150mW from a 3V supply.

23.6 A 2.3GHz SiGe RF IC Front-End for Satellite Radio Applications

11:15 AM

R. Pelleriti[1], G. Cali`[1], R. Camden[2], P. De Vita[1], S. Geraci[1], A. Palleschi[1], M. Paparo[1], C. Schiro`[1], A. Bruno[1]
[1]STMicroelectronics, Catania, Italy
[2]XM Satellite Radio, Boca Raton

A 0.35μm SiGe BiCMOS double-conversion digital audio satellite radio receiver with on-chip RF and IF PLLs is presented. The 17mm^2 front-end has -97dBm input sensitivity, 3.5dB NF, -13dBm off-channel IIP3 at maximum RF gain and 12dBm at minimum RF gain, 35dB RF and 90dB IF gain range, with >30dB image rejection and 30dBm on-channel OIP3. The RF VCO features a phase noise of -107dBc/Hz at 100kHz offset.

23.7 A Single-Chip Receiver for Multi-User Low-Noise Block Down-Converters

11:45 AM

T. Copani[1], S. Smerzi[2], G. Girlando[2], G. Ferla[2], G. Palmisano[1]
[1]University of Catania, Catania, Italy
[2]STMicroelectronics, Catania, Italy

A 12GHz single-chip receiver for multi-user low-noise block down-converters is presented. The 3.3mmx2mm die is implemented in a 50GHz-f_T 0.8μm silicon bipolar technology and includes two down converter channels and a 10.2GHz local oscillator synthesizer. The receiver features a 7.8dB SSB NF, an output P_{1dB} of 5dBm with 32dB conversion gain and phase noise of –96dBc/Hz at 100kHz offset from the 10.2GHz carrier.

CONCLUSION 12:15 PM

SESSION 24 SALON 10-15

BASEBAND PROCESSING

Chair: **Albert Van der Werf,** *Philips Research, Eindhoven, The Netherlands*
Associate Chair: **Yiwan Wong,** *ASRTRI, Shatin, Hong Kong, China*

24.1 A 1.2V 6.7mW Impulse-Radio UWB Baseband Transceiver

8:30 AM

C-H. Yang, K-H. Chen, T-D. Chiueh
National Taiwan University, Taipei, Taiwan

A 2.7mm^2 CMOS baseband transceiver IC for impulse-radio UWB communication systems is implemented in a 0.18μm CMOS process. This chip provides up to 62.5Mb/s data transmission for short-range wireless communications while drawing 6.7mW from a 1.2V power supply.

24.2 A 480Mb/s LDPC-COFDM-Based UWB Baseband Transceiver

9:00 AM

H-Y. Liu, C-C. Lin, Y-W. Lin, C-C. Chung, K-L. Lin, W-C. Chang, L-H. Chen, H-C. Chang, C-Y. Lee
National Chiao Tung University, Hsin-Chu, Taiwan

A Low-Density Parity-Check (LDPC) Coded OFDM-based UWB baseband transceiver features a semi-regular LDPC CODEC, a parallel pipelined FFT, and a division-free channel equalizer. The chip is implemented in a standard 0.18μm CMOS process and achieves a 480Mb/s data rate with an energy consumption of 1.2nJ/b.

24.3 A 135Mb/s DVB-S2 Compliant CODEC Based on 64,800b LDPC and BCH Codes

9:30 AM

P. Urard[1], E. Yeo[2], L. Paumier[1], P. Georgelin[1], T. Michel[1], V. Lebars[1], E. Lantreibecq[1], B. Gupta[2]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Berkeley, CA

A CODEC fully compliant to DVB-52 broadcast standards is implemented in both 0.13μm 8M and 90nm 7M low-leakage CMOS technologies. The system includes encoders and decoders for both LDPC codes and serially concatenated BCH codes. This CODEC outperforms the DVB-S2 error performance requirements by up to 0.1dB. The 0.13μm design occupies 49.6mm^2 and operates at 200MHz, while the 90nm design occupies 15.8mm^2 and operates at 300MHz.

BREAK 10:00 AM

24.4 A Reprogrammable EDGE Baseband and Multimedia Handset SoC with 6Mb Embedded DRAM

10:15 AM

A. Cofler[1], D. Dutoit[1], F. Druilhe[1], M. Harrand[2]
[1]STMicroelectronics, Grenoble, France
[2]STMicroelectronics, Crolles, France

A 0.13μm 6M CMOS EDGE baseband and multimedia handset SoC features a 6Mb embedded-DRAM DSP instruction memory to allow dynamic upgrade of DSP software, such as applications downloaded from the network. Full-chip standby current is 690μA which gives 500h complete GSM/EDGE terminal autonomy when using a 800mAH battery.

24.5 A Multi-Standard DSL Central Office Modem SoC

10:45 AM

F. Chow, R. Price
Texas Instruments, San Jose, CA

The ADSL central office SoC supports 16 ADSL2+ modems, each running at 16Mb/s simultaneously and is configurable to satisfy multiple standards. The 107M-transistor SoC supports 12,475M C-programmable and configurable DSP accelerator MACs/s. The 145mm^2 chip is implemented in a 0.13μm 6M process and dissipates 2.7W at 494MHz.

24.6 A WLAN SoC for Video Applications Including Beam Forming and Maximum Ratio Combining

11:15 AM

W. McFarland, D. Breslin, J. Cho, W-J. Choi, P. Dua, J. Gilbert, P. Husted, J. Kuskin, M. Mack, S. Mendis, S. Ng, J. Smith, J. Thomson, Y-H. Wang, N. Zhang, X. Zhang
Atheros Communications, Sunnyvale, CA

A WLAN SoC for video applications handles 802.11a/b/g and supports PHY data rates to 108 Mb/s. The SoC implements two chain maximum ratio combining and beam-forming. Video features include a jitter removal system and MPEG-TS packet aggregation. Measured results on the 7.2mm×7.2mm IC using a 0.18μm CMOS process demonstrate throughput improvements in both RX and TX.

24.7 A 180Ms/s 162Mb/s Wideband Three-Channel Baseband and MAC Processor for 802.11a/b/g

11:45 AM

M. Bhardwaj[1], C. Briggs[1], A. Chandrakasan[2], C. Eldridge[1], J. Goodman[3], T. Nightingale[1], S. Sharma[1], G. Shih[1], D. Shoemaker[1], A. Sinha[1], R. Venkatesan[1], J. Winston[1], W. Zhou[1]
[1]Engim, Acton, MA
[2]Massachusetts Institute of Technology, Cambridge, MA
[3]Engim, Ottawa, Canada

A wideband wireless digital PHY/MAC chip processes 90MHz of bandwidth and integrates three fully asynchronous 802.11a/b/g compliant modems delivering a peak data rate of 162Mb/s. The 70.55mm^2 IC in 0.18μm CMOS technology features a near-far DR of 45dB for 54Mb/s signals, OFDM (CCK) transmit SNR of 68db (77dB) and a spectrum monitor with 1.4MHz resolution at 250kHz.

CONCLUSION 12:15 PM

SESSION 25 NOB HILL

DYNAMIC MEMORY

Chair: **Hideto Hidaka,** Renesas Technology, Itami, Japan
Associate Chair: **John Barth,** IBM, Essex Junction, VT

25.1 An 18.5ns 128Mb SOI DRAM with a Floating Body Cell

8:30 AM

T. Ohsawa, K. Fujita, K. Hatsuda, T. Higashi, M. Morikado, Y. Minami, T. Shino, H. Nakajima, K. Inoh, T. Hamamoto, S. Watanabe
Toshiba, Yokohama, Japan

A dynamic latch sense amplifier/bit line replenishes "1" cells with holes lost during word line cycles and reduces the refresh busy rate. A multi-averaging method of dummy cells over 128 pairs of "1s" and "0s" enhances the sense margin and contributes to the 18.5ns access time. The 25.7ns virtually static RAM (VSRAM) mode is realized by taking advantage of the cell's quasi non-destructive read-out.

25.2 A 322MHz Random-Cycle Embedded DRAM with High-Accuracy Sensing and Tuning

9:00 AM

M. Iida[1], N. Kuroda[1], H. Otsuka[1], M. Hirose[1], Y. Yamasaki[1], K. Ota[1], K. Shimakawa[1], T. Nakabayashi[1], H. Yamauchi[1], T. Sano[2], T. Gyohten[2], M. Maruta[2], F. Morishita[2], A. Yamazaki[2], K. Dosaka[2], M. Takeuchi[2], K. Arimoto[2]
[1]Matsushita, Nagaokakyo, Japan
[2]Renesas Technology, Itami, Japan

An embedded DRAM macro in a logic compatible 90nm CMOS process is designed with low-noise core architecture and high-accuracy post-fabrication tuning. With a 5fF/cell capacitance, a 61% improvement of sensing accuracy enables 322MHz random-cycle operation and reduces data retention power to 60μW.

25.3 A 400MHz Random-Cycle Dual-port Interleaved DRAM with Striped-Trench Capacitor

9:30 AM

M. Shirahama, Y. Agata, T. Kawasaki, R. Nishihara, W. Abe, N. Kuroda, H. Sadakata, T. Uchikoba, K. Takahashi, K. Egashira, S. Honda, M. Miura, S. Hashimoto, H. Kikukawa, H. Yamauchi
Matsushita, Nagaokakyo, Japan

A 400MHz random-cycle dual-port interleaved 1.5V DRAM macro with fully sense-signal-loss compensating technologies based on noise-element breakdowns, a striped trench capacitor cell and write-before-sensing by a decoded write-bus circuit technique. The IC is implemented in a 0.15μm CMOS logic process.

BREAK 10:00 AM

25.4 An AND-type Match-line Scheme for Energy-Efficient Content Addressable Memories

10:15 AM

J-S. Wang, H-Y. Li, C-C. Chen, C. Yeh
National Chung-Cheng University, Chia-Yi, Taiwan

An AND-type match-line scheme is fabricated in a 0.18μm 1.8V CMOS process. The 256×128b CAM achieves a faster search time and a 20% energy reduction compared with NOR designs. This AND-type circuit has a search time of 1.75ns with an energy of 0.57fJ/bit/search.

25.5 Concordant Memory Design Using Statistical Integration for the Billions-Transistor Era

10:45 AM

S. Akiyama[1], T. Sekiguchi[2], K. Kajigaya[3], S. Hanzawa[2], R. Takemura[2], T. Kawahara[2]
[1]Hitachi, Kokubunji, Japan
[2]Hitachi, Tokyo, Japan
[3]Elpida Memory, Sagamihara, Japan

Concordant memory design incorporates device fluctuation statistically into the SNR analysis in DRAM and represents failed bits in a chip. It assures 1.4V array operation of 100nm, 1Gb DRAM. Calculated and experimental results agree on the dependence of failed bit count on the array voltage.

25.6 An 800Mb/s/pin 2Gb DDR2 SDRAM Using an 80nm Triple Metal Technology

11:15 AM

K. Kyung, C. Kim, J. Lee, J. Kook, S. Seo, D. Kim, J. Kim, J. Sunwoo, H. Lee, C. Kim, B. Jeong, Y. Sohn, S. Hong, J. Lee, J. Yoo, S. Cho
Samsung, Hwasung, Korea

A 1.8V, 800Mb/s/pin, 2Gb DDR2 SDRAM is developed using an 80nm triple metal technology. With the triple metal technology, NMOS precharge I/O scheme and statistical analysis, DDR800 4-4-4 performance is achieved at 1.8V. For mass production, a high-speed clock using an on chip PLL and an address-pin-reduction mode are employed.

25.7 A 20GB/s 256Mb DRAM with an Inductorless Quadrature PLL and a Cascaded Pre-emphasis Transmitter

11:45 AM

K-H. Kim, Y-S. Sohn, C-K. Kim, D-J. Lee, G-S. Byun, H. Lee, J-H. Lee, J. Sunwoo, J-H. Choi, J-W. Chai, C. Kim, S-I. Cho
Samsung, Hwasung, Korea

A 20GB/s 1.8V 256Mb DRAM is designed and fabricated using an 80nm CMOS process. An inductorless tetrahedral oscillator generates inherent quadrant phases combined with a cascaded pre-emphasis transmitter to achieve a 10Gb/s/pin data rate.

CONCLUSION 12:15 PM

SESSION 26 SALON 1-6

STATIC MEMORY

Chair: **Alexander Shubat,** *Virage Logic, Fremont, CA*
Associate Chair: **Jinyong Chung,** *POSTECH, Pohang, Korea*

26.1 A 3GHz 70Mb SRAM in 65nm CMOS Technology with Intergrated Column-Based Dynamic Power Supply

1:30 PM

K. Zhang, U. Bhattacharya, Z. Chen, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, M. Bohr
Intel, Hillsboro, OR

A 70Mb SRAM chip is designed and fabricated in 65nm CMOS technology. A column-based dynamic multi-V_{CC} scheme is integrated into the design to improve cell read and write margins while reducing power consumption. The design operates at 3GHz with a 1.1V power supply.

26.2 A 256Mb Synchronous-Burst DDR SRAM with Hierarchical Bit-Line Architecture for Mobile Applications

2:00 PM

Y-H. Suh, H-Y. Nam, S-B. Kang, B-G. Choi, H-S. Mo, G-H Han, H-K. Shin,W-R. Jung, H. Lim, C-K. Kwak, H-G. Byun
Samsung, Hwasung, Korea

A 256Mb synchronous-burst DDR SRAM is designed using a hierarchical bit-line architecture. The chip is based on stacked single-crystal silicon TFT cells which provide area-effective switching between different levels of bit lines. A 280Mb/s data rate is achieved with an operating current of 17mA in a 61.1mm^2 IC implemented in an 80nm process.

26.3 A Read-Static-Noise-Margin-Free SRAM Cell for Low-V_{DD} and High-Speed Applications

2:30 PM

K. Takeda[1], Y. Hagihara[1], Y. Aimoto[2], M. Nomura[1], Y. Nakazawa[1], T. Ishii[2], H. Kobatake[2]
[1]NEC, Sagamihara, Japan
[2]NEC, Kawasaki, Japan

A read-static-noise-margin-free SRAM cell consists of seven transistors, several of which are low-V_t NMOS transistors used to achieve both low-V_{DD} and high-speed operation. A 64kb SRAM macro is fabricated in 90nm CMOS technology. Both a minimum V_{DD} of 440mV and a 20ns access time with a 0.5V supply are obtained.

26.4 Low-Power Embedded SRAM Modules with Expanded Margins for Writing

2:45 PM

M. Yamaoka[1], N. Maeda[2], Y. Shinozaki[3], Y. Shimazaki[2], K. Nii[4], S. Shimada[2], K. Yanagisawa[2], T. Kawahara[1]
[1]Hitachi, Kokubunji, Japan
[2]Renesas Technology, Tokyo, Japan
[3]Hitachi, Fukuoka, Japan
[4]Renesas Technology, Itami, Japan

A low-power embedded SRAM module implements a writing margin expansion for low-voltage operation, a write replica circuit for low-power operation and a low-leakage structure. The replica circuit reduces active power by 18%, and a 512kb module operates at 450MHz, has 7.8μA leakage in standby, and a minimum V_{DD} of 0.8V.

BREAK 3:00 PM

26.5 PVT-Aware Leakage Reduction for On-Die Caches with Improved Read Stability

3:15 PM

C. Kim[1], J-J. Kim[2], I-J. Chang[3], K. Roy[3]
[1]University of Minnesota, Minneapolis, MN
[2]IBM, Yorktown Heights, NY
[3]Purdue Unviersity, West Lafayette, IN

A run-time leakage reduction technique for SRAM caches considers architecture and behavior to achieve an optimal tradeoff between overhead energy and leakage savings. A 16kB SRAM shows a 94.2% cell leakage reduction with a 2% performance penalty. Fabricated in a 0.18µm 6M CMOS process, the 3.2mm×2.9mm die also shows 25% improvement in read stability.

26.6 0.3 to 1.5V Embedded SRAM with Device-Fluctuation-Tolerant Access-Control and Cosmic-Ray-Immune Hidden-ECC Scheme

3:45 PM

T. Suzuki, Y. Yamagami, I. Hatanaka, A. Shibayama, H. Akamatsu, H. Yamauchi
Matsushita, Nagaokakyo, Japan

A device-fluctuation-tolerant access-control scheme and a unique cosmic-ray-immune hidden-ECC scheme are implemented in a 32kb SRAM in a 0.13µm CMOS process. The SRAM operates at 0.3V at 6.8MHz under severe device fluctuations. Operation ranges from 30MHz at 0.4V to 960MHz at 1.5V. The hidden-ECC reduces access-timing and the calculated soft-error-rate is reduced by 3.6×10^{-10} per Mb.

26.7 A 4.8GHz Fully Pipelined Embedded SRAM in the Streaming Processor of a CELL Processor

4:15 PM

T. Asano[1], T. Nakazato[2], S. Dhong[3], A. Kawasumi[2], J. Silberman[4], O. Takahashi[3], M. White[3], H. Yoshihara[5]
[1]IBM, Yasu, Japan
[2]Toshiba, Austin, TX
[3]IBM, Austin, TX
[4]IBM, Yorktown Heights, NY
[5]Sony, Austin, TX

A 6-stage fully pipelined embedded SRAM is implemented in a 90nm SOI technology. The array uses a conventional 6-transistor memory cell and sense amplifier to achieve the cycle time while minimizing the impact of device variation. A sum-addressed pre-decoder allows partial activation for power savings.

26.8 The Asynchronous 24MB On-Chip Level-3 Cache for a Dual-Core Itanium®-Family Processor

4:45 PM

J. Wuu[1], D. Weiss[1], C. Morganti[2], M. Dreesen[1]
[1]Hewlett Packard, Fort Collins, CO
[2]Intel, Fort Collins, CO

The 24MB level-3 cache on a dual-core Itanium® processor has more than 1.47G transistors. The cache uses an asynchronous design to reduce latency and power, and it includes other power saving and reliability improvement features. The 5-cycle array operates above 2GHz at 0.8V and 85°C while consuming less than 4.2W.

CONCLUSION 5:15 PM

SESSION 27 SALON 7

FILTERS AND CONTINUOUS-TIME ΔΣ CONVERTERS

Chair: **Raf Roovers,** *Philips Research, Eindoven, The Netherlands*
Associate Chair: **Bill Redman-White,** *Philips Semiconductors, Southampton, United Kingdom*

27.1 A 3mW 74dB SNR 2MHz CT ΔΣ ADC with a Tracking-ADC-Quantizer in 0.13μm CMOS

1:30 PM

L. Doerrer
Infineon, Villach, Austria

A 3rd-order CT multibit ΔΣ ADC for wireless applications is implemented in 0.13μm CMOS. Instead of using a 4b flash quantizer, a tracking ADC composed of 3 comparators with interpolation is used to reduce the power consumption. Over a bandwidth of 2MHz the SNR is 74dB. The ADC consumes 3mW from a 1.5V supply when clocked at 104MHz.

27.2 A 1.2V 3.5mW ΔΣ Modulator with a Passive Current Summing Network and a Variable Gain Function

2:00 PM

T. Nagai, H. Satou, H. Yamazaki, Y. Watanabe
Fujitsu, Kawasaki, Japan

A 1.2V 3.5mW CT ΔΣ modulator with a mixer for a mobile digital TV receiver is implemented in 0.11μm CMOS. A current summing network composed of passive elements is used in the loop filter feedforward path, contributing to the low power consumption. A 78dB total DR is achieved by varying the DAC output power with the input signal power.

27.3 A 4th-order 86dB CT ΔΣ ADC with Two Amplifiers in 90nm CMOS

2:30 PM

R. Hezar[1], A. Das[2], G. Gomez[1], R. Byrd[1], B. Haroun[1]
[1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Bangalore, India

A 4th-order 1b CT ΔΣ converter using a two-amplifier loop and a 267MHz sampling frequency is implemented in 90nm CMOS. A double-loop architecture couples passive poles with a reduced number of active blocks to improve area and power while achieving 86dB peak SNR over a 600kHz band.

BREAK 3:00 PM

27.4 A Low-Noise Low-Voltage CT ΔΣ Modulator with Digital Compensation of Excess Loop Delay

3:15 PM

P. Fontaine, A. Mohieldin, A. Bellaouar
Texas Instruments, Dallas, TX

The implementation of a 3rd-order 50MS/s CT ΔΣ modulator with 5 levels of quantization, for a CDMA2k receiver, is presented. Its 9nVrms/√Hz input referred noise produces 80dB of DR in a 600kHz BW for signals as low as 70mVrms. It draws 4mA from a single 1.5V supply, uses a 90nm CMOS process and occupies 0.25mm^2.

27.5 A 4.7mW 89.5dB DR CT Complex ΔΣ ADC with Built-In LPF

3:30 PM

F. Muñoz[1], K. Philips[2], A. Torralba[1]
[1]Universidad de Sevilla, Sevilla, Spain
[2]Philips Research, Eindhoven, The Netherlands

A CT complex ΔΣ ADC with built-in LPF is presented. A modified feedback topology is used to improve robustness to interferers near $f_s/2$ or f_s. Adding programmable gain control, the 0.18μm CMOS ADC achieves 89.5dB DR in a 1MHz BW, consuming 4.7mW from a 1.8V supply.

27.6 A 43mW CT Complex ΔΣ ADC with 23MHz of Signal Bandwidth and 68.8dB SNDR

3:45 PM

N. Yaghini, D. Johns
University of Toronto, Toronto, Canada

A low-power wide-BW CT complex ΔΣ ADC suitable for a low-IF receiver is fabricated in a 0.18μm CMOS process and consumes 42.6mW from a 1.8V supply. The IC achieves 68.8dB SNDR and a DR of 72.5dB over a 23.0MHz band centered around 11.5MHz.

27.7 Dynamically Power-Optimized Channel-Select Filter for Zero-IF GSM

4:15 PM

M. Ozgun[1], Y. Tsividis[1], G. Burra[2]
[1]Columbia University, New York, NY
[2]Texas Instruments, Dallas, TX

A 1.2V channel-select filter is implemented in a 0.18μm digital CMOS process for a zero-IF GSM system. The filter includes a coarse AGC system with dynamic impedance scaling and dynamic biasing to optimize power consumption, which is scaled down in 5 steps from 2.6mW to 0.45mW per channel without introducing transients due to the changes. The area per channel is $1.2mm^2$.

27.8 A 0.5V Filter with PLL-Based Tuning in 0.18μm CMOS

4:45 PM

S. Chatterjee, Y. Tsividis, P. Kinget
Columbia University, New York, NY

Design techniques that allow analog circuit operation with supply voltages as low as 0.5V are presented. A fully integrated 135kHz 5th-order elliptic LPF, including automatic bias circuits and an on-chip PLL for tuning, is implemented with standard devices in a 0.18μm CMOS process. The $1mm^2$ chip has a measured DR of 57dB and draws 2.2mA from the 0.5V supply.

CONCLUSION 5:15 PM

SESSION 28 SALON 8

CLOCKING AND I/O

Chair: **Dennis Fischette**, *AMD, Sunnyvale, CA*
Associate Chair: **Hennu Tenhunen**, *Royal Institute of Technology, Stockholm, Sweden*

28.1 A Sub-10ps Multi-Phase Sampling System Using Redundancy

1:30 PM

L-M. Lee, C-K. Yang
University of California, Los Angeles, CA

The feasibility of sampling with clock phases spaced by a bin size of <10ps for a multi-channel system in a 0.18μm CMOS technology is demonstrated. The phase spacing is limited only by uncorrelated thermal noise in the system. Redundancy is introduced in addition to interpolators and offset compensation to reduce static errors to 1.5ps.

28.2 Programmable On-Chip Picosecond Jitter-Measurement Circuit without a Reference-Clock Input

2:00 PM

M. Ishida[1], K. Ichiyama[1], T. Yamaguchi[1], M. Soma[2], M. Suda[3], T. Okayasu[3], D. Watanabe[3], K. Yamamoto[3]
[1]Advantest Laboratories, Sendai, Japan
[2]University of Washington, Seattle, WA
[3]Advantest Laboratories, Meiwa, Japan

An on-chip jitter measurement circuit in 0.18μm CMOS is demonstrated, using a combination of a programmable delay line, interleaving PFDs, and programmable charge pumps. The method does not require a reference clock. Interleaving PFDs minimizes bias errors. Measurement linearity is 3.5μV/ps with an error of $1.03ps_{rms}$ for a 2GHz clock.

28.3 A Chip-Package Hybrid DLL and Clock Distribution Network for Low-Jitter Clock Delivery

2:15 PM

D. Chung[1], C. Ryu[1], H. Kim[1], C. Lee[2], J. Kim[2], J. Kim[2], J. Yu[2], K. Bae[2], S. Lee[2], H. Yoo[1], J. Kim[1]
[1]KAIST, Daejeon, Korea
[2]Amkor Technology, Seoul, Korea

A chip-package hybrid DLL and clock distribution network provides low-jitter clock signals by utilizing seperate supply connections and lossless package layer interconnections instead of on-chip global wires. The hybrid scheme has $78ps_{pp}$ jitter and under 240mV digital noise at 500MHz, while a conventional scheme has a $172ps_{p-p}$ jitter under the same conditions.

28.4 A CMOS DLL-Based 120MHz to1.8GHz Clock Generator for Dynamic Frequency Scaling

2:30 PM

J-H. Kim, Y-H. Kwak, S-R. Yoon, M-Y. Kim, S-W. Kim, C. Kim
Korea University, Seoul, Korea

A DLL-based clock generator for dynamic frequency scaling is fabricated in a 0.35μm CMOS technology. It generates clock signals ranging from 120MHz to 1.8GHz. The frequency can be dynamically changed. If the clock generator scales its output frequency dynamically by programming with the same last bit, it takes only one clock cycle to lock. The proposed clock generator has a jitter of $\pm 6.6ps_{pp}$ at 1.3GHz.

28.5 1.1 to 1.6GHz Distributed Differential Oscillator Global Clock Network

2:45 PM

S. Chan[1], K. Shepard[1], P. Restle[2]
[1]Columbia University, New York, NY
[2]IBM, Yorktown Heights, N.Y.

A distributed differential oscillator global clock network using on-chip spiral inductors is designed in a 0.18μm 1.8V CMOS technology. The 2mmx2mm resonant clock network has a tank Q of 4.3, achieves more than an order of magnitude less jitter than a conventional non-resonant tree-driven-grid global clock network, and uses almost three times less power.

BREAK 3:00 PM

28.6 A 3Gb/s 8b Single-Ended Transceiver for 4-Drop DRAM Interface with Digital Calibration of Equalization Skew andOffset Coefficients

3:15 PM

S-J. Bae, H-J. Chi, H-R. Kim, H-J. Park
Pohang University of Science and Technology, Pohang, Korea

A 3Gb/s/pin 8b parallel 4-drop single-ended DRAM transceiver is implemented in a 0.25μm CMOS process. Digital calibrations are performed for equalization and compensation of data skew and offset voltage. A continuosly active on-die termination is used to reduce reflections. A phase detector is proposed for the digital DLL to achieve the S/H time of 10ps.

28.7 3Gb/s AC-Coupled Chip-to-chip Communication using a Low-Swing Pulse Receiver

3:45 PM

L. Luo, J. Wilson, S. Mick, J. Xu, P. Franzon, L. Zhang
North Carolina State University, Raleigh, NC

A 3Gb/s 60mV low-swing pulse receiver is presented for AC-coupled interconnect (ACCI). Using this receiver, we demonstrate without errors, chip-to-chip communication through an ACCI channel with 150fF coupling capacitors, across 15cm FR4 micro-strip line. A test chip is fabricated in 0.18μm CMOS technology and the TX and RX dissipate 15mW per I/O at 3Gb/s.

28.8 Mixed-Voltage I/O Buffer with Dynamic Gate-Bias Circuit to Achieve 3xVDD Input Tolerance by Using 1xVDD Devices and Single VDD Supply

4:15 PM

M-D. Ker, S-L. Chen
National Chiao-Tung University, Hsin-Chu, Taiwan

This work presents a mixed-voltage I/O buffer realized with $1xV_{DD}$ devices and single V_{DD} power supply to receive $3xV_{DD}$ input signals without suffering gate-oxide reliability problems. The proposed I/O buffer is verified in a 0.13μm 1V CMOS process. This technique can be extended to receive $4xV_{DD}$, $5xV_{DD}$, and even $6xV_{DD}$ input signals.

28.9 Clocking and Circuit Design for a Parallel I/O on a First-Generation CELL Processor

4:45 PM

K. Chang[1], S. Pamarti[1], K. Kaviani[1], E. Alon[1,2], X. Shi[1], T. Chin[1], J. Shen[1], G. Yip[1], C. Madden[1], R. Schmitt[1], C. Yuan[1], F. Assaderaghi[1], M. Horowitz[1,2]
[1]Rambus, Los Altos, CA
[2]Stanford University, Stanford, CA

A parallel I/O is integrated on a first-generation CELL processor in 90nm SOI CMOS. A clock-tracking architecture suppresses reference jitter to achieve 6.4Gb/s/link operation at 21.6mW/Gb/s. SOI effects on analog circuits, in particular high-speed receivers, are addressed to achieve a receiver sensitivity of ±12mV at 6.4Gb/s with BER $<10^{-14}$ measured using 7b PRBS data.

CONCLUSION 5:15 PM

SESSION 29 SALON 9

RF TECHNIQUES

Chair: **Mario Paparo,** *STMicroelectronics, Catania, Italy*
Associate Chair: **Qiuting Huang,** *ETH, Zurich, Switzerland*

29.1 A 21 to 26GHz SiGe Bipolar PA MMIC

1:30 PM

T. Cheung[1], J. Long[2], D. Harame[3]
[1]University of Toronto, Toronto, Canada
[2]Delft University of Technology, Delft, The Netherlands
[3]IBM, Essex Junction, VT

A 3-stage 21 to 26GHz SiGe PA with 21dBm output power is presented. Small-signal gain is approximately 20dB and reverse isolation is <-30dB. PAE at 24GHz is >12.5%. On-chip transformers are extensively used to efficiently couple common-base stages and I/O to source and load, respectively. The 2.45×2.45mm^2 chip is fabricated in a 0.18μm SiGe BiCMOS process (f_T=100GHz) and draws 450mA from a 1.8V supply.

29.2 Direct-Digital RF Modulator IC in 0.13μm CMOS for Wide-Band Multi-Radio Applications

2:00 PM

P. Eloranta, P. Seppinen
Nokia, Helsinki, Finland

An IQ-modulator constructed using direct digital-to-RF converters for wide-band multi-radio applications achieves better than -43dBc of LO-leakage and -47dBc of image rejection. The signal-level dependent maximum power consumption is 60.5mW with a -10dBm WCDMA signal. The modulator occupies 0.7mm^2 of silicon area in a standard 1.2V 0.13μm CMOS process.

29.3 Low-Power g_m-Boosted LNA and VCO Circuits in 0.18μm CMOS

2:30 PM

X. Li, S. Shekhar, D. Allstot
University of Washington, Seattle, WA

A 5.8GHz fully integrated common-gate LNA uses a g_m-boosting technique and draws 1.9mA from a 1.8V supply with 9.4dB gain, 7.6dBm IIP3, and 2.5dB NF. A Colpitts differential VCO (QVCO) employs a similar method and draws 3.6mA (4.3mA) from a 2V supply. Phase noises at 50kHz and 1MHz offset frequencies are -97dBc/Hz (-104Bc/Hz) and -128 dBc/Hz (-127dBc/Hz), respectively.

29.4 A 0.75 to 2.2GHz Continuously Tunable Quadrature VCO

2:45 PM

D. Guermandi, P. Tortori, E. Franchi, A. Gnudi
University of Bologna, Bologna, Italy

The ±20% tuning range of a fully-integrated quadrature LC-VCO is extended to ±50%. The quadrature VCO is inserted in a loop with an SSB mixer and two frequency dividers that add 100×100μm^2 area in a 0.13μm CMOS process and draw 10mA from a 1.2V supply. Quadrature error is <2° and phase noise <-120dBc/Hz at 1MHz offset.

BREAK 3:00 PM

29.5 A 32GHz Quadrature LC-VCO in 0.25μm SiGe BiCMOS Technology

3:15 PM

W. Chan[1], H. Veenstra[2], J. Long[3]
[1]Delft University of Technology, Singapore
[2]Philips, Eindhoven, The Netherlands
[3]Delft University of Technology, Delft, The Netherlands

A 32GHz quadrature VCO achieves over 45dB of image rejection in a 70GHz-f_T SiGe process. Each VCO stage uses a new negative resistance topology to realize >330Ω of negative resistance with <4fF parasitic capacitance. The coupled VCO has a measured tuning range of 30.6 to 32.6GHz, phase noise of -97dBc/Hz at 1MHz offset and occupies 0.7×0.5mm^2.

29.6 A 1mW Current-Reuse CMOS Differential LC-VCO with Low Phase Noise

3:30 PM

Y. Seok-Ju, S. So-Bong, L. Sang-Gug
Imformation and Communications University, Daejeon, Korea

An LC-VCO with half of the power dissipation of a that of the conventional topology is presented. The LC-VCO replaces one of the NMOSFET of the conventional differential LC-VCO with a PMOSFET. The operational principles and design guidelines of the proposed topology are reported. The proposed LC-VCO is implemented in a 0.18μm CMOS technology for 2GHz applications and measured show phase noise is -103dBc/Hz at 100KHz offset while dissipating 1mW from a 1.25V supply.

29.7 I/Q Mismatch Compensation in a 90nm Low-IF CMOS Receiver

3:45 PM

I. Elahi[1], K. Muhammad[1], P. Balsara[2]
[1]Texas Instruments, Dallas, TX
[2]University of Texas, Richardson, TX

An I/Q mismatch compensation circuit for a low-IF GSM receiver implemented in a 90nm CMOS process is presented. A single-tap adaptive decorrelation technique is used with L_1-norm inverse power measurement and gear-shifting circuits. An image rejection ratio in excess of 50dB is achieved allowing the receiver to use IF frequencies higher than half of the channel bandwidth.

29.8 A Noise Cancellation Technique in Active RF-CMOS Mixers

4:00 PM

H. Darabi, J. Chiu
Broadcom, Irvine, CA

Based on the physical understanding of noise mechanisms in active mixers, a noise cancellation technique to reduce the flicker-noise contribution of the switches in a Gilbert-type mixer is presented. A prototype double-balanced mixer in 0.13μm CMOS is fabricated as a proof of concept. The circuit achieves a flicker-noise corner almost an order-of-magnitude lower than that of a standard implementation without compromising the linearity, gain, or power consumption.

29.9 A WLAN Direct Up-Conversion Mixer with Automatic Image Rejection Calibration

4:15 PM

J. Craninckx, B. Debaillie, B. Côme, S. Donnay
IMEC, Leuven, Belgium

A direct upconverter for 5 to 6GHz WLAN is presented that includes circuitry for automatic output spectrum calibration. For calibration, the RF signal is down-converted by reusing the up-conversion mixers, making the up- and down-conversion errors correlated. The transmit errors are determined based on only low-frequency measurements. The realized mixer achieves >40dB image rejection.

29.10 A 17mW 0.66mm² Direct-Conversion Receiver for 1Mb/s Cable Replacement

4:45 PM

S. Verma, J. Xu, M. Hamada, T. Lee
Stanford University, Stanford, CA

A very low-cost WPAN receiver implemented in 0.25μm CMOS technology consumes 17mW from a 1.8V supply and occupies an area of 0.66mm². A new coding scheme permits the integration of a HPF to mitigate DC-offset and 1/f noise. A linear front-end eliminates the external band-preselect filter.

CONCLUSION 5:15 PM

SESSION 30 SALON 10-15

DISPLAYS AND BIOSENSORS

Co-Chair: **Tiemin Zhao,** *Reflectivity, Sunnyvale, CA*
Co-Chair: **Roland Thewes,** *Infineon, Munich, Ge*rmany

30.1 A CMOS-Based Microdisplay with Calibrated Backplane

1:30 PM

A. Chen, A. Akinwande, H-S. Lee
Massachusetts Institute of Technology, Cambridge, MA

A 360x200 microdisplay backplane is implemented in a standard CMOS process. It includes silicon light emitters for use in conjunction with image intensifiers, and is also compatible with organic LED technology. The integrated display driver includes column-parallel DACs with self-calibration techniques to improve precision while minimizing area. The IC is fabricated in 0.18μm 5M1P CMOS process and is 80mm^2.

30.2 A Panel-Sized TFT-LCD Scan Driver

2:00 PM

D. Sasaki, O. Ishibashi, T. Toba, S. Noda, J. Yanase, H. Takaoka, Y. Sato, Y. Kamon, H. Tsuchi, H. Okumura, H. Kanoh, H. Hayama
NEC, Sagamihara, Japan

Panel-sized drivers are LSIs with lengths nearly equal to the width/height of LCDs. They have equal outputs to scan/column lines and do not need tapes or PCBs for assembly. These SOI devices employ CMOS TFTs on a glass substrate. Including the floating body effect, a 189mm-long scan driver with 768 outputs for TFT-LCDs is fabricated successfully.

30.3 An LCD Column Driver Using a Switched Capacitor DAC

2:30 PM

M. Bell
National Semiconductor, Phoenix, AZ

LCD column drivers have traditionally used non-linear R-string style DAC's. This paper describes an architecture that uses 768 linear charge redistribution 10/12b DACs to implement a 384-output column driver. Each DAC performs its conversion in less than 15μs and draws less than 2.5μA. This architecture allows 10b independent color control in a 17mm^2 die for the LCD television market.

BREAK 3:00 PM

30.4 A Three-Dimensional Neural Recording Microsystem with Implantable Data Compression Circuitry

3:15 PM

R. Olsson III[1,2], K. Wise[2]
[1]Sandia National Laboratories, Albuquerque, NM
[2]University of Michigan, Ann Arbor, MI

A 256-site microsystem comprises 4 neural recording arrays with integrated amplification and multiplexing circuitry and an implantable spike detection ASIC. The spike detector compresses the amount of neural data by 92%, increasing the total number of channels recorded wirelessly from 25 to 312. The implantable circuitry consumes 5.4mW at 3V.

30.5 A Battery-Powered 8-Channel Wireless FM IC for Biopotential Recording Applications

3:45 PM

P. Mohseni, K. Najafi
University of Michigan, Ann Arbor, MI

An 8-channel microsystem for transmission of 7 input biopotentials using wireless FM in the band of 94 to 98MHz requires only 3 off-chip components. The 4.84mm^2 IC is fabricated using a 1.5μm 2P2M CMOS process, dissipates ~2.05mW at 3V, and wirelessly reconstructs an 800μV neural spike over a distance of ~13cm with an I/O correlation coefficient of ~96%.

30.6 A Wireless Biosensing Chip for DNA Detection

4:15 PM

Y. Yazawa[1], T. Oonishi1, K. Watanabe[1], R. Nemoto[1], M. Kamahori[1], T. Hasebe[1], Y. Akamatsu[2]
[1]Hitachi, Kokubunji, Japan
[2]Hitachi, Takasaki, Japan

A wireless sensing chip for biological assay is fully operational in a sample solution. The IC monolithically integrates a biological sensor, an RF communication circuit, and a coupling coil on a 2.5mmx2.5mm chip in 0.35μm CMOS technology. A detection of single nucleotide polymorphism (SNP) in DNA is successfully carried out by the chip.

30.7 A Programmable Electrochemical Biosensor Array in 0.18μm Standard CMOS

4:45 PM

A. Hassibi, T. Lee
Stanford University, Stanford, CA

A 10×5 electrochemical biosensor array is designed and fabricated in standard 0.18μm CMOS. Each pixel occupies 160μm×120μm and contains a programmable sensor capable of performing differential impedance spectroscopy, amperometric analysis, and field-effect sensing for molecular biology applications.

CONCLUSION 5:15 PM

MASS STORAGE

Chair: **David Parlour,** *Xilinx, San Jose, CA*
Associate Chair: **Ram Krishnamurthy,** *Intel, Hillsboro, OR*

31.1 A CMOS 1x to16x Speed DVD Write Channel IC

1:30 PM

Y. Konno[1], K. Tomioka[1], Y. Aiba[1], K. Yamazoe[1], B-S. Song[2]
[1]Asahi Kasei Microsystems, Atsugi, Japan
[2]University of California, San Diego, CA

The optical recording write pulse sequence is generated by using 20-phase VCO clock edges, phase-locked to the 26 to 420MHz input-channel clock frequencies. Pulse width and delay are programmable with 120±40ps timing resolution at 16x speed. Fabricated in 0.35μm CMOS, the chip occupies 3.5x3.3mm^2 and consumes 294mW at 3.3V.

31.2 DLL-Based Clock Recovery In a PRML Channel

2:00 PM

P. Wang, Y-Y. Lin, M-T. Yang, J-B. Yang, H. Hsieh, Y. Cheng, C-Y. Cheng, H-W. Kao, J-S. Pan
MediaTek, Hsin-Chu, Taiwan

A DLL-based clock recovery circuit is designed to eliminate drawbacks of the VCO while maintaining the advantages of a PLL for frequency multiplication and jitter filtering. This design demonstrates that the tracking jitter is 1/20 of that of a PLL for a 1024 times frequency multiplication. The circuits are verified with PRML detectors for BD/DVD at channel bit rates of 264/478Mb/s.

31.3 A CMOS Multi-Format Read/Write SoC for 7x Blu-ray/16x DVD/56xCD

2:30 PM

P-H. Liu, J-S. Pan,Y. Cheng, W-Y. Wu, C-Y. Chen, J-B. Yang, M-T. Yang, H-J. Hsieh, P-Y. Wang, M-Y. Chao, L-L. Lin, J-H. Shieh, C-N. Chen, H-W. Kao, Y-Y. Lin, C-N. Chiu, H-C. Chen, S-C. Hu, S-F. Tsai, C-C. Hsu, C-C. Mao, C-C. Chen
MediaTek, Hsin-Chu, Taiwan

An SoC for high-speed read and write functions is designed for multi-formats of 7xBD/16xDVD/56xCD at channel bit rates of 462/418/242Mb/s. The data is detected by a PRML detector. The ECC CODEC for all formats is integrated as a single RS-CODEC. The SoC is implemented as a 30mm^2 die in a 0.18μm 1P6M CMOS process and consumes 1.0/0.9/0.7W in 7xBD/16xDVD/56xCD playback modes.

BREAK 3:00 PM

TD: ADVANCED ARRAY STRUCTURES

Chair: **Eugenio Cantatore,** *Philips Research, Eindhoven, The Netherlands*
Associate Chair: **Koji Kotani,** *Tohoku University, Sendai, Japan*

32.1 Memory Technologies in the Nano-Era: Challenges and Opportunities

3:15 PM

K. Kim, G. Jeong
Samsung, Yongin, Korea

As we move into the nano-era, there are growing concerns about the future of conventional memories due to their increasing technical complexity, fabrication cost, and scalability issues. In this paper, technical challenges and recent breakthroughs in conventional memories, and the future directions of memory development including new types of memories are introduced and discussed.

32.2 A Flexible 240x320-Pixel Display with Integrated Row Drivers Manufactured in Organic Electronics

3:45 PM

P. van Lieshout, E. van Veenendaal, L. Schrijnemakers, G. Gelinck, F. Touwslager, H. Huitema
Philips, Eindhoven, The Netherlands

Rollable electrophoretic displays with an active-matrix backplane are an emerging application of organic electronics. Integrating row shift registers on the display backplane reduces the number of interconnects and the footprint. Stand-alone shift registers using organic electronics on a flexible substrate are designed, realized, and characterized. The circuit contains 240 stages and has over 4000 transistors. Furthermore, a 240-stage shift register is integrated with a QVGA active-matrix display.

32.3 A Sheet-Type Scanner Based on a 3D-Stacked Organic-Transistor Circuit Using Double Word-Line and Bit-Line Structure

4:15 PM

H. Kawaguchi, S. Iba Y. Kato, T. Sekitani, T. Someya, T. Sakurai
University of Tokyo, Tokyo, Japan

Double word-line and bit-line structure in an organic FET-based sheet-type scanner is described. This structure reduces the line delay by a factor of 5, and the power by a factor of 7. To realize the structure in a pixel array, 3D stacked organic FETs are manufactured. The active leakage is reduced by a dynamic serially connected decoder.

CONCLUSION 4:45 PM

SHORT COURSE

RF CIRCUIT DESIGN FROM TECHNOLOGY TO SYSTEMS

This Short Course is intended to provide both entry level and experienced engineers with practical approaches to the design of RF circuitry in CMOS and BiCMOS technologies. Completing the course provides the attendee with an overall perspective of the technology considerations, circuit design issues and detailed design strategies for circuit building blocks for wired and wireless communication applications. Topics covered address the challenges faced by RF designers in current and future technologies with an emphasis on the detailed circuit design approaches and methodologies for RF integration.

For Registration, please use the ISSCC 2005 Registration Form on the Advance Program Centerfold. Sign-in is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00 AM.

The Short Course will be offered two times on Thursday, February 10.
The first session is scheduled for 8:00AM to 4:30PM.
The second session is scheduled for 10:00AM to 6:30PM.

CD of the Short Course & Relevant Papers: Short Course registrants will receive a CD-ROM at the Short Course. The CD-ROM includes: (1) The four Short Course presentations in PDF format for printing hard copies of the slides, (2) Bibliographies of relevant papers for all four presentations, and (3) PDF copies of relevant background material and important papers in the field (about 10-20 papers per presentation).

OUTLINE

Technology Options for RF-ICs (8:00A-9:30A), (10:00A-11:30A)

The focus of this presentation is to review the various technology options for RF integrated circuits; CMOS versus BiCMOS, MIM capacitors, varactors, inductors, switches, triple well isolation, ESD protection and packages.

Instructor: S. Simon Wong received the MS and PhD degrees from the University of California at Berkeley. He worked at National Semiconductor, Hewlett Packard Laboratories, and Cornell University. In 1988, he joined Stanford University where he is now a Professor of Electrical Engineering. His research group focuses on understanding and overcoming the limitations of circuit performance imposed by device, interconnection and on-chip components. He is a Fellow of the IEEE.

Wireless IC Building Blocks in CMOS/BiCMOS (10:00A-11:30A), (12:00P-1:30P)

The design of wireless RF IC building blocks, such as low-noise amplifiers (LNA), up and down-converting mixers and VCOs are described in this lecture. Both low-voltage/low-current and high-performance aspects of RF design are treated. The limitations and advantages of on-chip passive components in RF circuits - important to VCOs and low-voltage circuits among others - are included. Modelling, optimization and physical layout of passives for different circuit applications are described. Design examples in both CMOS and BiCMOS for single-chip (e.g., Bluetooth, 802.11x) and multi-standard transceivers are presented.

Instructor: John Long received the MEng and PhD degrees in Electronics from Carleton University in 1992 and 1996, respectively. He worked for 10 years at Bell-Northern Research on Gb/s fiber systems, and for 5 years at the University of Toronto. He joined Delft University of Technology in 2002 as Chair of the Electronics Research Laboratory, and currently serves on the ISSCC, ESSCIRC, BCTM, and European Microwave conference committees. His current research interests include: low-power transceiver circuitry for broadband and highly integrated radios, and electronics for high-speed data communications systems.

Effects of Substrate on the RF Performance of Silicon Integrated Circuits
(1:00P-2:30P), (3:00P-4:30P)

Silicon-based technologies use substrates with resistivities ranging between 0.01 and ~20Ω-cm. This relatively low substrate resistivity, if not properly engineered, can significantly degrade characteristics of transistors, inductors, capacitors, interconnects as well as the performance of LNAs, VCOs, mixers, transmit/receive switches, and power amplifiers. In general, the degradation can be minimized by making the substrate resistance either very small or very large. For silicon integrated circuits, it is more practical to lower the substrate resistances. However, lowering the substrate resistances can degrade amplifier stability, and increase unwanted noise and signal coupling. The underlying mechanisms for these are presented. With the increase of operating frequencies of RFCMOS circuits, integration of antennas has become a realistic option. The effects of substrate on on-chip antenna performance are also described.

Instructor: Kenneth O received his S.B, S.M, and Ph.D. degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology. From 1989 to 1994, he worked at Analog Devices developing CMOS, bipolar, and BiCMOS processes for RF and mixed signal applications. He is currently a professor at the University of Florida, Gainesville. His research group is developing circuits and components operating between 1 and 100GHz using silicon IC technologies. He was the general chair of the 2001 IEEE Bipolar/BiCMOS Circuits and Technology Meeting. He has authored and co-authored approximately 100 publications and holds five patents.

Front-End Design for Wireless Systems
(3:00P-4:30P), (5:00P-6:30P)

Design techniques relevant to RF front-ends and transceivers for wireless applications are discussed in the course. Considerations such as noise and linearity performance, dynamic range, matching and parasitic self-induced noise in these circuits are addressed. The discussion includes techniques applicable to traditional narrow-band and recently emerging broad-band wireless systems, such as Ultra Wideband. A comparison of design issues and trade-offs for the two types of systems is also presented.

Instructor: Ranjit Gharpurey is an Assistant Professor in the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor. His primary research interests are in the areas of high-frequency and high-speed circuit design and parasitic noise sources in integrated circuits with emphasis on RFIC design for wireless applications. He received his Ph. D. from the University of California at Berkeley in 1995 and his B. Tech from the Indian Institute of Technology, Kharagpur.

CIRCUIT DESIGN FORUM

F3: Characterization of Solid-State Image Sensors

(NOB HILL)

Organizer/ Chair : Albert Theuwissen, DALSA, Eindhoven, The Netherlands
Committee : **Dan McGrath,** Eastman Kodak, Rochester, NY**,**
Jed Hurwitz, ST Microelectronics, Edinburgh, UK,
Hirofumi Sumi, Sony, Tokyo, Japan,
Boyd Fowler, Agilent, Palo Alto, CA.

Solid-state image sensors are complex devices, something that is especially apparent when it comes to the issue of thorough characterization. With the introduction of the CMOS image sensors, about a decade ago, this evaluation and testing became even more complicated because the CMOS image sensors do have an increased functionality on-chip. This is in contrast to the CCD imagers which are limited to the analog pixel matrix in combination with a simple output amplifier on-chip. In the case of the CCD circuit any additional functionality is located off-chip.

For CMOS imagers, the analog circuitry and digital circuitry are integrated on the same imaging chip, with photons as the input signal and processed digital bits as the output. Where full-functional testing of the component is needed, the evaluation and testing discipline encompasses optical, analog circuit and digital circuit testing.

In many cases the image sensors are fabricated in CMOS processes that are in some way tweaked to result in a better imaging performances. The optimization of these CMOS processes involves semiconductor physics, semiconductors processing and characterization know-how. All these different parameters need to be characterized throughout the fabrication process.

Taken all together, the quality and performance of CCD and CMOS image sensors rely on a very extensive, multi-disciplinary characterization activity. It is the intention of this forum to give an in-depth overview of the issues in the different parts of the image sensor evaluation. Each talk of the forum addresses the characterization of a single discipline within the field of solid-state imaging : optics, device physics, electrical circuitry, design for testability, semiconductor technology, sensitivity and standardization of testing. The organizing committee has invited key-specialists in each of these fields to speak at this forum.

Thursday, February 10th 8:00 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topics
8:00	Breakfast
8:30	**Welcome and Overview** **Albert Theuwissen**, DALSA, Eindhoven, The Netherlands
8:45	**Optics** **Nobukazu Teranishi**, Matsushita, Kyoto, Japan
9:35	**Device Physics** **Dave Sackett**, Eastman Kodak, Rochester, NY
10:25	Break
10:40	D**esign For Testability** **Bjornar Hernes**, Nordic Semiconductor, , Norway
11:30	**Electronic Circuits** **Lindsay Grant**, ST Microelectronics, Edinburgh, UK
12:20	Lunch
1:20	**Technology** **Shou-Gwo Wuu**, TSMC, Hsin-Chu, Taiwan,
2:10	**ISO Sensitivity** **Rick Baer**, Agilent, Palo Alto, CA
3:00	Break
3:15	**Standardization** **Hirofumi Sumi,** Sony, Tokyo, Japan
4:05	**Panel discussion** All speakers and all committee members
4:50	Conclusion

F4: Robust Design Solutions for Nanoscale Circuits: From DFM through End-of-Life

(Salon 7)

Organizers/Chair: **Norman Rohrer,** IBM, Essex Junction, VT
Committee:
Atila Alvandpour, Linkoping University, Linkoping, Sweden
Fumio Arakawa, Hitachi, Tokyo, Japan
Bill Bowhill, Intel, Hudson, MA
Harry Fair, AMD, Boxborough, MA
Georgios Konstadinidis, Sun Micro., Sunnyvale, CA
Nasser Kurd, Intel, Hillsboro, OR
Margaret Martonosi, Princeton University, Princeton, NJ
Shannon Morton, Icera, Wiltshire, UK
Ron Preston, Intel, Hudson, MA
Alice Wang, Texas Instruments, Dallas, TX
C. K. Ken Yang, University of California, Los Angeles, CA

65nm and 90nm technologies are putting the squeeze on CMOS circuit design. From DFM (birth) through reliability (end-of-life), the need for improved modeling and design margin continues to expand. For example, the voltage range is limited at the upper end for hot electron effects and gate oxide reliability, while the lower voltages are limited by functionality and SRAM stability. This forum will address DFM, reliability, design tools, design styles and architecture so your circuit may "live happily ever after".

Design for manufacturability (DFM) is a requirement for lithography. Clive Bittlestone will address the issues and methods of analysis of OPC data. Ron Bolam will provide the nanoscale reliability mechanisms and trends for hot-electron effect, NBTI, gate oxide reliability and electromigration pertinent to circuit design.

Jack Pippin will focus on the tools and techniques of circuit analysis required to optimize circuits within the reliability constraints. David Greenhill will show which circuit design styles are the most robust across the life of the circuit. Hyun-Geun Byun will focus on SRAM reliability and methods to cover SER and low voltage stability. Included with the SRAM discussion will be a new cell and the methods of testing.

High speed I/O design issues include the use of logic devices and increasing demand for higher data rates. Gerry Talbot will present solutions and methods for analysis for 65nm technologies. Hisashige Ando will present architectures which are tolerant to failures-in-time in SRAM and logical functions.

Join us for a full day of expert analysis and presentation.

Thursday, February 10th 8:00 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:30	**Welcome and Overview** **Norman Rohrer**, IBM, Essex Junction, VT
8:45	**Modelling DFM** **Clive Bittlestone,** Texas Instruments, Dallas, TX
9:35	**VLSI Reliability Mechanisms - Considerations for Circuit Design** **Ron Bolam**, IBM, Essex Junction, VT
10:25	Coffee Break
10:40	**Optimization Techniques for Robust Design** **Jack Pippin,** Intel, Hillsboro, OR
11:30	**Robust Circuit Designs, Flawed Circuit Designs** **David Greenhill,** Sun Microsystems, Sunnyvale, CA
12:20	Lunch
1:20	**Robust SRAM Design** **Hyun-Geun Byun,** Samsung, HwaSung-City, Korea
2:10	**Multi-Gb/s I/O Design Challenges in 65nm and Beyond** **Gerry Talbot,** AMD, Boxborough, MA
3:00	Coffee Break
3:15	**Tolerant Architectures** **Hisashige Ando**, Hitachi, Kawasaki, Japan
4:05	Q&A and Conclusion

ATAC FORUM

F5: ATAC: Automotive Technology and Circuits

(Salon 8)

Organizers/Chair: **Herman Casier,** AMI Semiconductor, Oudenaarde, Belgium
Wolfgang Pribyl, CONPRI, Graz, Austria

Committee: **Larry De Vito,** Analog Devices, Wilmington, MA
Muneo Fukaishi, NEC, Kanagawa, Japan
Franz Dielacher, Infineon, Villach, Austria
Dieter Draxelmayr, Infineon, Villach, Austria
Masayuki Katakura, SONY, Kanagawa, Japan
David Robertson, Analog Devices, Wilmington, MA

While the automotive market has long been driven by innovations and improvements of the mechanical, hydraulic and pneumatic systems of the car, this situation has changed and the majority of innovations in cars are actually driven by electronics. Electronics will become even more pervasive for the foreseeable future with a shift from separate electronic modules, to fully interconnected intelligent systems e.g. X-by-wire.

This evolution, together with the growing use of high-performance sensors requires increasingly complex and accurate electronic hardware and software in the car. At the same time, the stringent safety requirements are further tightened and the harsh automotive environment demands are further increased.

This Forum discusses the evolution in automotive high voltage and high power technologies, complex system developments and robust circuit design.

In the first paper, a comprehensive overview of automotive electronic systems and market trends will be given. The paper will demonstrate the key elements needed for this evolution/revolution of automotive electronics.

The second and third papers will discuss semiconductor technologies for automotive applications from the viewpoints of the car manufacturer and the semiconductor industry.

In the fourth and fifth papers, complex system design issues and trade-offs for in-vehicle image processing will be discussed. The use of such image processing and secure data communication in the harsh automotive environment are important for driver assistance systems and therefore will get high attention.

The sixth, seventh and eight papers will focus on robust circuit design aspects for a Local Interconnect Network (LIN) transceiver, for current and future lighting systems in the car and for integrated magnetic field and surface micro machined pressure sensors.

At the end of the afternoon, all speakers will assemble in a panel format for an open discussion with the audience on the challenges in all aspects of automotive electronics.

Thursday, February 10th 8:00 AM

This all-day forum encourages open interchange in a closed forum. Attendance is limited and pre-registration is required. Coffee breaks and lunch will be provided to allow a chance for participants to mingle and discuss the issues.

Forum Agenda:

Time	Topic
08:00	Continental Breakfast
08:30	**Welcome and Introduction** **Herman Casier**, AMIS, Oudenaarde, Belgium
08:40	**Automotive Systems and Markets** **Patrick Leteinturier,** Infineon, Munich, Germany
09:20	**Semiconductor Technologies Support New Generation Hybrid Car** **Masayuki Hattori**, Toyota, Japan
10:00	**SMARTMOS, the Ultimate Power, Analog, Mixed Signal Technology for Automotive Applications** **Hak-Yam Tsoi**, Freescale
10:40	Break
11:00	**In Vehicle Image Processing LSI for Driver Assistant Systems** **Shorin Koy**, NEC, Japan
11:40	**Overview and Challenges of Data Communication in the Vehicle** **Stefan Poledna**, TTTech, Vienna, Austria
12:20	Lunch
01:40	**A LIN transceiver, a case study of automotive design** **Koen Appeltans**, AMIS, Oudenaarde, Belgium
02:20	**Future Lighting Systems for Vehicles** **Gunther Leising**, Lumitech, Austria
03:00	**Smart Sensors for Automotive Applications** **Dirk Hammerschmidt**, Infineon, Villach, Austria
03:40	Break
04:00	**Panel Discussion**
05:00	Conclusion

INFORMATION

CONFERENCE REGISTRATION

ISSCC offers online registration. This is the fastest, most convenient way to register and will give you immediate confirmation of whether or not you have a place in the Tutorial and Short Course sessions of your choice, as well as in any of the five Forums offered. If you register online using a credit card, your registration is processed while you are online, and your written confirmation can be downloaded and printed for your recordkeeping. If you register by fax or mail, you will not receive confirmation for several days. **Registration forms received without full payment will not be processed until payment is received at Event Solutions.**

To register online, go to the ISSCC website at www.isscc.org/isscc or go directly to the registration website at www.yesevents.com/isscc/index.asp. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to **"ISSCC 2005"**. Payments by credit card will appear on your monthly statement as a charge from ISSCC.

For those who wish to register by fax or mail, the Advance Registration Form can be found at the center of this booklet. Please read the explanations and instructions on the back of the form carefully.

The deadline for receipt of Early Registration fees is **December 24, 2004. After December 24, 2004 and on or before January 11, 2005**, registrations will be processed only at the Late Registration rates. **As of January 11, 2005 you must pay the onsite/highest registration fees**. Because of limited seating capacity in the meeting rooms and hotel fire regulations, onsite registration may be limited. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2005.

Full conference registration includes one copy each of the Digest of Technical Papers in both hard copy and on CD, the Visuals Supplement (mailed in March) and the ISSCC 2005 DVD that includes the Digest and Visuals (mailed in May). **Student registration does not include the Visuals Supplement or the ISSCC 2005 DVD.** All students must present their Student ID at the Conference Registration Desk to receive the student rate. Anyone registering at the IEEE Member rate must also provide his/her IEEE Membership number. Those individuals who are members of both IEEE and SSCS will also receive a complimentary copy of the SSCS Digital Archive DVD set for years through 2004.

The On-site and Advance Registration Desks at ISSCC 2005 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except presenting authors, must pick up their registration materials at these desks as soon as they arrive at the hotel. **The Presenting Author for each paper must go directly to Golden Gate A3 to register and to collect his/her materials.**

REGISTRATION HOURS:

Saturday,	February 5	4:00 PM to 7:00 PM **(Tutorial and Forum Attendees Only)**
Sunday,	February 6	6:30 AM to 1:30 PM **(Tutorial and Forum Attendees Only)** 4:00 PM to 8:00 PM
Monday,	February 7	6:30 AM to 3:00 PM
Tuesday,	February 8	8:00 AM to 3:00 PM
Wednesday,	February 9	8:00 AM to 12:00 Noon
Thursday,	February 10	7:00 AM to 1:00 PM **(Short Course and Forum Attendees Only)**

INFORMATION

NEXT ISSCC DATES AND LOCATION

ISSCC 2006 will be held on February 5-9, 2006 at the San Francisco Marriott Hotel.

FURTHER INFORMATION

Please visit the ISSCC website at www.isscc.org
To be placed on the Conference Mailing List, please contact the Conference Office, c/o Courtesy Associates,

2025 M Street, N.W., Suite 800,
Washington, DC 20036
Email: ISSCC2005@courtesyassoc.com
Fax: 202-973-8722

HOTEL RESERVATIONS

ISSCC participants are urged to make their hotel reservations online. To do this, go to the conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott. In order to receive the special group rates you will need to enter the following Group Codes: IEIIEIA for a single; IEIIEIB for a double; IEIIEIC for a triple; or IEIIEID for a quad. The special ISSCC group rates are $199/single; $219/double; $239/triple; and $259/quad. The dates of your reservation must fall within the period of February 4-10, 2005. All online reservations require the use of a credit card. Online reservations are confirmed immediately, while you are online. We suggest that you print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. Once made and confirmed, your online reservation can be changed by calling the Marriott at 1-800-228-9290 (toll free) or 415-896-1600, or by faxing your change to the Marriott at 415-442-0141.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet. Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax.

Reservations must be received at the San Francisco Marriott no later than January 11, 2005 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached and/or after January 11th, the group rate will no longer be available. After the 11th, reservation requests will be filled at the best available rate.

IMPORTANT NOTICE FOR ALL 2005 ISSCC PARTICPANTS: It is vitally important that all 2005 ISSCC participants who do not live within driving distance of San Francisco make their hotel room reservations at the San Francisco Marriott, which is the conference hotel and location of all technical sessions and all other conference activities. The room rates have been negotiated based upon our need to use all available meeting space in the hotel. If we do not fill our negotiated room block, the ISSCC must pay huge fees for using all of the space. This will then result in unnecessary and unpopular increases in registration fees for ISSCCC in future years. Please support the Executive Committee in their attempt to keep your ISSCC registration fees reasonable. Book your room at the San Francisco Marriott hotel for ISSCC 2005.

CONFERENCE PUBLICATIONS

Additional ISSCC 2005 publications can be purchased at the Conference Registration Desk. Prices are lower for purchases collected onsite than for those publications ordered after the Conference that must be shipped to the purchaser for an additional fee. **Following ISSCC 2005, please order publications directly from the publisher, issccorders@s3digitalpub.com**.

TECHNICAL BOOK DISPLAY AND DAC STUDENT POSTERS

A number of technical publishers will have a collection of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The book display is in the Golden Gate Hall, located one level above the ballroom and technical sessions. The Book Display will be open on Monday from 12:00Noon - 8:00PM; on Tuesday from 10:00AM to 8:00PM; and on Wednesday from 10:00AM to 5:00PM.

The DAC Student Poster Contest winners for 2004 and 2005 will also display their winning papers in this area during the book display hours. Author Interviews will be held here as well, on Monday and Tuesday. Please note that the Author Interviews will move to the South Grand Assembly on Wednesday.

INFORMATION

SSCS DIGITAL-ARCHIVE DVD SET

All ISSCC registrants who are members of the IEEE Solid-State Circuits Society will receive a complementary SSCS Digital-Archive DVD Set. The two-DVD set contains the IEEE Journal of Solid-State Circuits (1966-2004), the conference records of the ISSCC (1955-2004), and the Symposium on VLSI Circuits (1988-2004). In addition, new for this year, the Digital-Archive DVD set will contain the conference records of the Custom Integrated Circuits Conference (1988-2004) and the European Solid-State Circuits Conference (1997-2004).

- To add SSCS membership while renewing IEEE membership, go to www.ieee.org/renew
- To add SSCS membership after renewing IEEE membership, go to www.ieee.org/addservices
- To join IEEE and SSCS, go to www.ieee.org/join

Check-off boxes are provided on the registration form to order additional copies of the Digital-Archive DVD.

CD OF THE ISSCC DIGEST, AND DVD OF THE DIGEST AND SLIDE SUPPLEMENT

New for this year, Conference attendees will receive a complementary CD of the ISSCC 2005 Digest of Technical Papers, in addition to the printed Digest, at the Conference. This CD will allow easy access to an electronic version of the technical papers. In addition, all Conference attendees (except student registrants) will receive by mail a complementary DVD containing the ISSCC 2005 Digest of Technical Papers, and the ISSCC 2005 Visuals Supplement. This DVD will be mailed in May, 2005.

ISSCC 2004 and 2005 SHORT-COURSE DVDs

A DVD of the ISSCC 2004 Short Course, "Deep-Submicron Analog and RF Circuit Design", and a DVD of the ISSCC 2005 Short Course, "RF CMOS Circuits" will be available for purchase at the Conference. These DVDs contain an audio recording of the original presentation, synchronized with the slides, along with written textual transcript. In addition, the DVD's will contain a pdf of the presentations suitable for printing, along with pdfs of key reference material. Check-off boxes are provided on the registration form to purchase the DVDs; They will not be available for purchase after the Conference.

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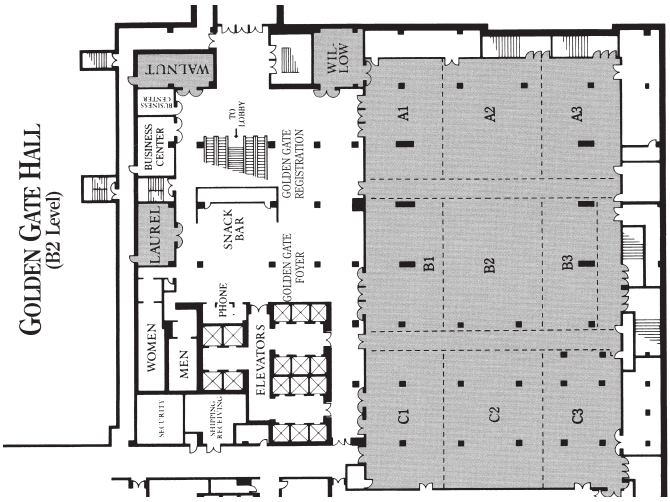

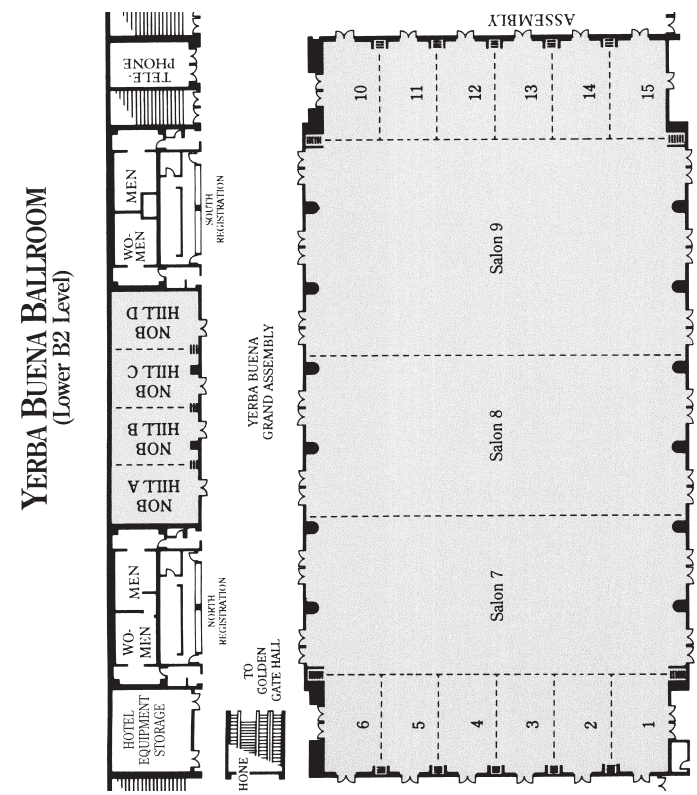

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