

ADVANCE PROGRAM



2006
IEEE

INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY
5, 6, 7, 8, 9

CONFERENCE THEME:

**Multimedia
for a Mobile World**

SAN FRANCISCO
MARRIOTT HOTEL

SUNDAY ALL-DAY: 3 FORUMS: Wireless CMOS Transceivers; Embedded SRAM; Circuits for Emerging Technologies; 9 TUTORIALS
3 SPECIAL-TOPIC SESSIONS: What Drives Displays?; Power-Aware Signal Processing; Analog Scaling
THURSDAY ALL-DAY: 3 FORUMS: Color Imaging; High-Speed Interconnect; MultiCore Challenges; SHORTCOURSE: A-to-D Converters

**5-DAY
PROGRAM**

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE HIGHLIGHTS

On Sunday, February 5, the day before the official opening of the Conference, ISSCC 2006 offers:

- A choice of up to 4 of a total of 9 Tutorials
- Three ISSCC Advanced-Circuit-Design Forums:
- GIRAFE (GHz Radio Front Ends) Forum:
“Advanced Wireless-CMOS-Transceiver Design”
- Memory-Circuit-Design Forum:
“Embedded SRAM Design”
- Technology-Directions Forum:
“Circuit Design in Emerging Technologies”

The 90-minute tutorials offer background information and a review of the current state-of-the-art in specific circuit-design topics. Scheduling is organized to allow an attendee to participate in 4 tutorials, two in the morning, and two in the afternoon. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in their technical field.

On Sunday evening, three Special-Topic Evening Sessions addressing next-generation circuit-design challenges will be offered starting at 7:30PM:

- What is Driving Displays?
- Power-Aware Signal Processing
- Analog scaling
- The Special-Topic Evening Sessions are open to all ISSCC attendees.

On Monday, February 6, ISSCC 2006 offers three plenary papers followed by six parallel technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will feature posters from the winners of the 2005-06 joint DAC-ISSCC student-design contest and the 2005 Asia Solid-State Circuits Conference student-design contest. Monday evening features a panel discussion “Is the Digital Designer Dead”, and three Special-Topic Evening Sessions:

- Emerging and Disruptive Memory Technologies
- CMOS RF Design in 90nm and Beyond
- Highlights of A-SSCC 2005 and the 2005 Symposium on VLSI Technology

On Tuesday, February 7, ISSCC 2006 offers morning and afternoon technical sessions, followed by a Social Hour, a Special-Topic Evening Session “Sensors on the Move”, and two panel discussions. Wednesday, February 9 features morning and afternoon technical sessions.

On Thursday, February 8, ISSCC 2006 offers a choice of four events:

- An ISSCC Short Course: “Analog-to-Digital Converters”. Two sessions of the Short Course will be offered, with staggered starting times.
- Three ISSCC Advanced-Circuit-Design Forums:
 - An ISSCC Advanced-Circuit-Design Forum:
“High-Speed Interconnect”
 - Microprocessor Forum: “Multicore Architectures:
Design and Implementation Challenges”
 - Image Sensor Forum: “Color Imaging”

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-registration site (www.isscc.org) is **strongly** encouraged. You will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

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TUTORIALS

T1: Introduction to Fractional- N Phase-Locked Loops

This tutorial begins with a brief review of integer- N PLLs, and then, presents a detailed explanation of the additional ideas and issues associated with the extension to fractional- N PLLs for frequency synthesis. Topics include a self-contained explanation of the relevant aspects of $\Delta\Sigma$ modulation, an extension of the well-known integer- N PLL linearized model to fractional- N PLLs, the non-ideal effects of particular concern in fractional- N PLLs such as charge-pump nonlinearities and data-dependent divider delays, and techniques for wideband in-loop digital modulation of the VCO. Case studies of example circuits and applications are presented to illustrate the main concepts.

Instructor: Ian Galton received his Sc.B. from Brown University, in 1984, and his M.S. and Ph.D. from the California Institute of Technology, in 1989 and 1992, respectively, all in electrical engineering. Since 1996, he has been a professor of electrical engineering at the University of California, San Diego, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996, he was with UC Irvine, the NASA Jet Propulsion Laboratory, Acuson, and Mead Data Central. His research involves the invention, analysis, and integrated-circuit implementation of critical communication-system building blocks, such as data converters, frequency synthesizers, and clock-recovery systems. In addition to his academic research, he regularly consults at several semiconductor companies, and teaches industry-oriented short courses on the design of mixed-signal integrated circuits. He has served as a member of a corporate Board of Directors, as a member of several corporate Technical Advisory Boards, and as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.

T2: Data-Converter Interfaces: The Analog and Digital Ins and Outs

Many of the critical performance characteristics of Data Converters are determined by their input and output circuitry. This tutorial will provide a high-level overview of how different architectural and circuit choices impact the analog, digital, reference, and clock interfaces, in today's A/D and D/A converter designs, and how this ultimately may limit the converter's performance under different application conditions.

Instructor: David Robertson is a Product-Line Director of the High-Speed-Converter Group at Analog Devices. He received his B.A. and B.E. degrees from Dartmouth College, in 1984 and 1985, respectively, and since 1985 has worked at Analog Devices on a wide variety of D/A and A/D converters on complementary bipolar, BiCMOS, and CMOS processes. Dave currently holds 14 patents on converter and mixed-signal circuits, has participated in two "outstanding-panel" ISSCC evening panel sessions, and was co-author of the paper that received the IEEE Journal of Solid-State Circuits 1997 Best Paper Award.

T3: Introduction to Statistical Variation and Techniques for Design Optimization

Variability is a reality in nanometer semiconductor processes. This tutorial will cover the sources of systematic and random variations of transistors and their surrounding interconnects. Included in the variability discussion will be within-chip variability, across-wafer variability, across-device variability, and device mismatch. The resulting impact upon an individual circuit's functionality and timing will be explored. Analytical approaches will be shown for examining the variability's impact upon leakage power, dynamic power, and circuit functionality of static and dynamic circuits, SRAM arrays, and PLLs. Techniques will include Monte-Carlo analysis, vector analysis, and statistical timing analysis.

Instructor: Norman Rohrer is a Distinguished Engineer in the PowerPC-Microprocessor Group within the System-and-Technology Group of IBM, located in Essex Junction, VT. Norman received his Bachelor's Degree in physics and mathematics from Manchester College, North Manchester, IN, in 1987. He received his Master's Degree and Doctor of Philosophy degree in electrical engineering from Ohio State University, Columbus, OH, in 1990 and 1992, respectively. Norman has been a lead designer on PowerPC 750 and 970 products for Apple's G3 and G5 chips, and Nintendo's GameCube. His interests lie in the area of high-speed circuit optimization for future technologies. Norman holds 18 patents, and is a co-author of two books titled "*High-Speed CMOS Circuit-Design Styles*", and "*SOI Circuit-Design Concepts*".

T4: Introduction to CMOS Bio-Sensors: Electrical Specifications, CMOS Processing, Circuit and System Design

Silicon-based bio-sensors and actuators have attracted much attention for a number of years — particularly if equipped with on-chip intelligence, i.e., CMOS circuitry. On the other hand, although there are a number of promising developments in this area, most of them focus, so far, on niche applications, but, commercialization of a number of approaches is still ongoing. It is thus sometimes difficult to distinguish whether a CMOS chip in this area is a "Me-too" demonstrator, competitive to other non-electronic technologies, or indeed provides a unique selling-point worthy of further development.

This talk will present an overview of the current status of CMOS approaches for in-vitro applications in life sciences and biotechnology, such as drug screening and medical diagnosis. Starting with a review of the operating principles and applications of the related sensors and actuators, required CMOS-processing extensions are considered, electrical specifications and related circuit requirements are derived, concrete circuit designs purpose are presented, and advantages and drawbacks compared to existing non-CMOS-based techniques (if available) are discussed. Chips and data presented in the literature considered to provide examples illustrating the above-mentioned issues.

Instructor: Roland Thewes received his Dipl.-Ing. and Dr.-Ing. in Electrical Engineering from the University of Dortmund, Germany, in 1990 and 1995, respectively. Since 1994, he has been with the Research Laboratories of Siemens and Infineon, where he was active in the design of non-volatile memories and in the field of reliability and yield of analog CMOS circuits. From 1997 to 1999, he managed projects in the fields of design-for-manufacturability, reliability, analog-device performance, and analog-circuit design. Since 2000, he has been responsible for the Laboratory on Mixed-Signal Circuits in Corporate Research of Infineon Technologies, and for the development of CMOS-based biosensors. He lectures at the University of Ulm, and serves as a member of the technical program committees of ESSDERC, IEDM, and ISSCC.

TUTORIALS

T5: Multi-Level Cell Design for Flash Memory

Flash Memory with multi-level cells was first reported at ISSCC in 1995. Since then, it has become commercially available in high volume from many semiconductor manufacturers. Multi-level design achieves the storage of more than two analog levels in a flash memory cell. If four analog levels are stored in a single flash cell, two bits of information can be programmed into the cell. This essentially reduces the cell area by half relative to single-bit storage, and can approach the same cost savings (from a memory-array perspective) as a change in one lithography generation. This tutorial explores some of the basic Multi-Level-Cell design techniques for Flash Memory, and will include:

- Basic concepts of multi-level analog storage relative to single-bit-per-cell storage
- The need for precise charge placement and precise charge sensing of floating-gate memory cells
- Circuit design and chip-architectural techniques to achieve multi-level analog storage of more than one bit per cell

Instructor: Mark Bauer is currently Senior Principal Engineer at Intel Corporation in Folsom, California, where he is responsible for advanced circuit design and Flash-memory technology development. He received his BSEE in Electrical Engineering in 1985 from the University of California at Davis. Upon graduation, Mark joined Intel's Memory Components Division, working on EPROM design. He started working on Flash-memory design in 1992, and was responsible for circuit-design and technology development for the first Intel StrataFlash™ memory. He has served on the ISSCC memory sub-committee since 1999. He has authored several technical papers, one of which won the Lewis Winner Award for Outstanding Paper at ISSCC (1995). He holds more than 20 patents in the field of Non-Volatile Memory.

T6: Cellular-Phone Applications Trends and DSP Technology

As the cellular phone spreads worldwide, its applications are rapidly expanding and becoming more and more attractive. These applications are based on digital-signal processing, for which high performance with low power consumption is required. From performance, cost, and power-consumption points of view, this tutorial will focus on multimedia applications and the related DSP technologies needed on the cellular phone, including;

- Multimedia applications
- Video- and audio-processing algorithms
- Multimedia DSP architectures
- Low-power circuit designs

Instructor: Masafumi Takahashi is currently a Chief Specialist at Toshiba Corporation Semiconductor in Kawasaki, Japan, where he is involved in the development of multimedia SoCs for mobile applications, focusing on audio-visual processing architectures and low-power circuit techniques. He joined Toshiba Corporation in 1987, where he was engaged in research on multiprocessor architectures until 1996. He has been a member of the ISSCC Signal Processing Sub-Committee since 2004. He received his ME from the University of Tsukuba, Japan in 1987.

T7: 3D Integration

Limitations to continued CMOS scaling are motivating interest in technologies which improve performance by reducing latency and increasing bandwidth. Such a development is in 3D chip technologies which come in many flavors and styles, but are receiving lots of attention lately, as a means of extending power-performance in high-end systems. Designing for three dimensions, however, forces us to look at formerly-two-dimensional integration issues, quite differently. A number of commercial offerings and research programs suggest ways of addressing these challenges. This tutorial will survey present development directions in 3D, and introduce some of the opportunities this exciting new technology creates.

Instructor: Kerry Bernstein is a Senior Technical Staff Member at the IBM T.J. Watson Research Center, Yorktown Hts, NY. He is currently responsible for future-product-technology definition, performance, and application. Kerry received his B.S in electrical engineering from Washington University in St.Louis, and joined IBM in 1978. He holds 50 US Patents, and is a co-author of 3 college textbooks and multiple papers on high-speed and low-power CMOS. His interests are in the area of high-performance low-power advanced circuit technologies. He is a staff instructor at RUNN/Marine Biological Laboratories, Woods Hole, MA.

T8: Millimeter-Wave ICs in Silicon

There is a plethora of emerging applications at high-microwave and millimeter-wave frequencies (e.g., at 24GHz, 60GHz, and 77GHz) that offer new opportunities and challenges for silicon implementation. This tutorial covers circuit design for some of these emerging applications, such as gigabit wireless Ethernet (GWE), and automotive radar. We will discuss some of the primary issues for integrated millimeter-wave circuits, and some of the circuit and system techniques that can be applied at such high frequencies, with a focus on distributed circuits and multiple-antenna-array approaches, and their resulting system improvements.

Instructor: Ali Hajimiri received his B.S. in electronics engineering from the Sharif University of Technology, and his M.S. and Ph.D. in electrical engineering from Stanford University, Stanford, CA. He has been with Philips Semiconductors, Sun Microsystems, and Lucent Technologies (Bell Labs) in Murray Hill. In 1998, he joined the faculty of the California Institute of Technology, Pasadena, where he is an Associate Professor of Electrical Engineering, and the director of the Microelectronics Laboratory. Ali holds several U.S. and European patents. He is an Associate Editor of the JSSC, and a member of the Technical Program Committee of the ISSCC. Ali was selected as one of the top-100 innovators (TR100) in 2004.

T9: Signal Integrity for High-Speed Circuit Designers

Signal integrity issues will be explained for beginning high-speed circuit designers. This tutorial will cover the operation principles of transmission lines on FR4 PCB, SPICE parameters for passive elements, signaling methods, compensation methods for channel loss, SPICE simulation examples using IBIS models, and power-integrity issues.

Instructor: Hong-June Park is a Professor at the POSTECH (Pohang University of Science and Technology) in Pohang, Korea. He is involved in the design of high-speed CMOS interface circuits and the signal-integrity issues associated with 2 to 5Gb/s DRAM interfaces. He received his PhD in Electrical Engineering from the University of California at Berkeley, in 1989.

GIRAFE FORUM

F1: Advanced Wireless CMOS Transceivers

Organizer: Rudolf Koch, *Infineon Technologies, Germany*

Committee: Ken Cioffi, *Discera, San Jose, CA*
Kari Halonen, *Helsinki University of Technology, Finland*
Tony Montalvo, *Analog Devices, Raleigh, NC*
Chris Rudell, *Intel, Santa Clara, CA*
Trudy Stetzler, *Texas Instruments, Stafford, TX*
David Su, *Atheros, Santa Clara, CA*
Francesco Svelto, *University of Pavia, Italy*

Wireless-transceiver integration has made dramatic progress in the last decade. GSM phones – single-band voice-only – started with a component count around 400, employing half a dozen or more chips in different technologies for signal processing alone. Today, we see two-chip and even single-chip implementations for wireless LAN or Bluetooth on the market. Cellular phones today routinely cover 3 or 4 bands, and support not only voice but also higher data rates. Increasingly, cameras, MP3 players, outlook support, etc. are added to the basic phone functionality. Whereas two-chip solutions and BiCMOS technologies for the RF frontend are still standard for cellular phones, the first plain CMOS transceivers are available on the market, and even single-chip CMOS solutions are being sampled.

The next challenge will be low-cost phones for emerging countries on one side, and multiband multistandard terminals on the other. Quad-band GSM/EDGE, together with UMTS, CDMA for phone functionality, FM-radio, digital radio, digital TV for entertainment, Bluetooth and WLAN for connectivity, GPS for localization and navigation and location-based services, and, finally, a megapixel camera, iPod functionality, games, and so on, will all be available in a future high-end phone.

Form-factor, battery-life and production-cost requirements can only be solved by further-increasing levels of integration, and by re-use and re-configurability of the hardware. How will the mass of components (filters, switches, LNAs, PAs) in the RF frontend be reduced? Will a software-defined radio be superior to hardware-centric implementations for so many standards? Where is the break-even point?

The morning presentation will address state-of-the-art architectures and design of wireless transceivers. After a short introduction and overview by the organizer, the second speaker, **Chris Rudell**, will discuss wireless standards and their impact on architectural choices. The next two speakers will look into these architectures in more detail. **Tony Montalvo** will show the latest advances in highly-integrated transmitters, e.g. linear I/Q modulators, polar concepts, etc. Then, **Bill McFarlane** will examine receiver architectures, and take a close look at the latest trends, such as multiple antennas and dynamic channel-bandwidth assignment. Finally, **Aarno Pärssinen** will address the problems arising from the rapidly-changing landscape of multi-standard transceivers, and discuss design methodologies supporting quick adaptation to new standards and requirements.

The afternoon presentations will primarily be dedicated to cellular applications. The first two, by **Andre Hanke** and **Bogdan Staszewski**, will look into their companies single-chip CMOS GSM transceivers, the first one integrating a proven standalone transceiver into a single-chip phone, and the second one pursuing digitally-oriented concepts. Finally, **Asad Abidi** will talk about one of the latest visions in this domain, namely, the software (-defined) radio.

The forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and to share their views.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of wireless CMOS transceivers.

Forum Agenda

<u>Time</u>	<u>Topics</u>
8:00	Breakfast
8:30	Welcome and Introduction <i>Rudolf Koch, Infineon Technologies, Munich, Germany</i>
9:00	Cellular and Short-Range Standards, Key Challenges, and their Impact on Architecture <i>Chris Rudell, Intel, Santa Clara, CA</i>
9:30	Highly-Integrated Linear Transmitters <i>Tony Montalvo, Analog Devices, Raleigh, NC</i>
10:30	Break
11:00	Receivers for Traditional, MIMO, and Dynamic-Bandwidth Radio Systems <i>Bill McFarland, Atheros, Santa Clara, CA</i>
12:00	System Design for Multi-Standard Radios <i>Aarno Pärssinen, Nokia, Helsinki, Finland</i>
12:45	Lunch
2:15	Transceiver Integration into a Single-Chip Cellular Phone <i>Andre Hanke, Infineon Technologies, Munich, Germany</i>
3:00	Digital RF Processor (DRP) for Cellular Phones <i>Bogdan Staszewski, Texas Instruments, Dallas, TX</i>
3:45	Break
4:15	Software-Defined Radio <i>Asad Abidi, University of California, Los Angeles, CA</i>
5:00	Panel Discussion
5:30	Conclusion

CIRCUIT DESIGN FORUM

F2: Embedded-SRAM Design

Organizer: **Hiroyuki Yamauchi**, *Fukuoka Institute of Technology, Fukuoka, Japan*

Chair: **Don Weiss**, *Intel, Fort Collins, CO*

Committee: **Bruce Bateman**, *T-RAM, San Jose, CA*
Jinyong Chung, *POSTECH, Pohang, Korea*
Kevin Zhang, *Intel, Hillsboro, OR*

Static Random-Access Memory (SRAM) is a dominant memory technology for embedded CMOS-memory applications. Classic 6T SRAM cells can be implemented in most logic-optimized CMOS processes, with few or no additional process steps, and provides a wide range of design flexibilities. Such memory arrays may be optimized for performance (latency and cycle time), functionality (multi-port, multi-bank), and density. Power has become a common limiting factor for embedded applications, from high-performance designs, where power-efficiency is very important, to mobile applications, where battery life is most critical. This forum will cover both ends of the power spectrum, scaling issues with sub-100nm designs, and advances in the test of highly-embedded arrays. Finally, this forum will look out on the horizon for promising new embedded-memory technologies.

Many high-performance VLSI applications, such as microprocessors, demand more and more on-die SRAM memory. Meeting the requirements in both performance and power consumption for such large on-die SRAMs has become increasingly challenging as technology scaling continues. **Kevin Zhang** will start the forum with some key architecture options/optimizations in large on-die cache-memory designs, and then discuss various circuit-design techniques for achieving high performance. Analysis-and-design tradeoffs for critical circuits will be presented. The design styles for multi-port memory (register files) will also be discussed as it becomes more important in many applications. Some state-of-the-art design techniques for lowering both dynamic and static power consumption, while retaining the high-performance goal, will also be discussed in detail.

At the other end of the power spectrum, mobile applications are driving SRAM-array design to extremely low power and very low voltages. **Masanao Yamaoka** will describe advanced low-voltage design techniques and the extra-power-reduction design techniques that are required for low active power. The low-leakage design techniques required for low stand-by power will also be presented. Finally, these techniques, as applied to some mobile processors, are presented.

Memories require extensive testing to ensure chip quality, since the vast majority of chip area is occupied by memory. **R. Dean Adams** will begin by describing how test-pattern selection requires a thorough understanding of the memory design to determine where defects can exist, and how they effect electrical operation. Multi-port designs can introduce even-more possible interactions and opportunities for defects to occur. Redundancy calculation is a significant part of testing to raise memory yield and therefore overall chip manufacturability. All of the needed testing must be accomplished via on-chip logic in the form of a memory built-in self-test (BIST). The BIST applies test patterns to the memory and analyzes the resulting read data. Further design-for-testability (DFT) techniques are utilized to check margins for memory timing and sense-amplifier signal values. All of these DFT factors must be utilized to enable thorough testing of memories.

As device channel lengths shrink down to tens of nanometers, SRAM designs meet new issues and challenges that require changes in the way designs are done.

Takayuki Kawahara will reexamine these scaling issues, their impact on cell operation and stability, and design for manufacturability within these new constraints. A new design methodology will be presented. Moreover, soft-error issues, especially those from cosmic rays and those associated with some new kinds of SRAM cells are discussed.

As high-performance multi-core processors are developed along with higher frequencies, SRAM designs must cope with high junction temperatures, fast random-cycle times and high bandwidth, as well as higher-density requirements. In order to meet these requirements, aggressive shrinking, 3D stacking, and other new memory technologies are being developed. **Hyun-Geun Byun** will address attractive alternatives to conventional 6T SRAM with solutions such as: Pseudo SRAMs, 3D-SRAM, amongst others. In particular, UtRAM, CellularRAM, FCRAM or Cosmo-RAM for mobile applications and BEDD3 for cache memory, will be discussed.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of embedded SRAM design.

Forum Agenda

<u>Time</u>	<u>Topic</u>
8:00	Breakfast
8:30	Introduction
8:40	High-Performance Power-Aware SRAM Design Kevin Zhang , <i>Intel, Hillsboro, OR</i>
9:45	Low-Power Low-Voltage SRAM Design for Battery Operation Masanao Yamaoka , <i>Hitachi, Tokyo, Japan</i>
10:50	Break
11:10	Design for Testability (DFT) R. Dean Adams , <i>Magma Design Automation, St. George, VT</i>
12:15	Lunch
1:00	Stability/Reliability/Manufacturability Factors in SRAM Design Takayuki Kawahara , <i>Hitachi, Tokyo, Japan</i>
2:05	Break
2:15	Alternatives to 6T SRAM Hyun-Geun Byun , <i>Samsung, HwaSung-City, Korea</i>
3:20	Panel Discussion
4:00	Conclusion

CIRCUIT DESIGN FORUM

F3: Circuit Design in Emerging Technologies

Organizer:	Eugenio Cantatore , <i>Philips, Eindhoven, The Netherlands</i>
Co-Organizer:	Kerry Bernstein , <i>IBM, Essex Junction, VT</i>
Committee:	Anantha Chandrakasan , <i>MIT, Cambridge, MA</i> Glenn Gulak , <i>University of Toronto, Toronto, Canada</i> Koji Kotani , <i>Tohoku University, Sendai, Japan</i> Siva Narendra , <i>Tyfone, Portland, OR</i> Larry Pileggi , <i>Carnegie Mellon University, Pittsburgh, PA</i> Werner Weber , <i>Infineon Technologies, Munich, Germany</i> C.K. Ken Yang , <i>University of California, Los Angeles, CA</i>

The development of the impressive new device technologies we see today is fuelled by a threefold need:

First, CMOS technology requires innovative device architectures and manufacturing approaches to meet the goals of the scaling roadmap.

Secondly, as it becomes more pervasive, electronics needs to evolve alternate forms of mainstream CMOS. These alternatives enable a wealth of emerging applications that traditional CMOS, due to intrinsic limitations, cannot serve. Examples include: large-area and flexible displays, low-cost identification tags, or even spoilage sensors to be embedded in packages.

Finally, limitations to extending the scaling roadmap motivate exploration of innovative ways to improve performance and cost-per-function. Completely new devices and manufacturing technologies potentially achieve much more than simple scaling.

For designers, these developments translate into the challenge to work with new materials, new devices, and innovative fabrication processes. Designers with the ability to combine creativity and novel technologies will lead the development of electronics in the coming era.

This Advanced-Circuit Forum on "Circuit Design in Emerging Technologies" is intended to offer designers an accurate overview of up-to-date design with novel devices, through the words of leading experts in these emerging fields.

The first two presentations address design of CMOS regular fabrics and multigate MOSFETs, of value in the short- and mid-term roadmap. The third and fourth presentations describe both novel (organic-transistor) and mature (Si-TFT) technologies which target applications different than those handled by standard CMOS. The last three presentations describe exciting "end-of-the-roadmap" technologies: Carbon nanotubes and nanowires (for both digital and analog applications) and Spintronics.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of circuit design in emerging technologies.

Forum Agenda

<u>Time</u>	<u>Topic</u>
8:00	Breakfast
8:30	Welcome and Overview Eugenio Cantatore , <i>Philips, Eindhoven, The Netherlands</i>
8:40	Regular Fabrics for Nano-Scaled CMOS Technologies Larry Pileggi , <i>Carnegie Mellon University, Pittsburgh, PA</i>
9:30	Multigate MOSFET Design Gerhard Knoblinger , <i>Infineon Technologies, Villach, Austria</i>
10:20	Break
10:40	Design with Organic TFTs Eugenio Cantatore , <i>Philips, Eindhoven, The Netherlands</i>
11:30	Technology Trends and Design with Silicon TFTs Tatsuya Shimoda , <i>Seiko-Epson, Nagano-ken, Japan</i>
12:20	Lunch
1:20	Digital Circuits Using Carbon Nanotubes: Modeling, Design, and Architectures Ali Keshavarzi , <i>Intel, Hillsboro, OR</i>
2:10	Analog-Circuit Design with 1D Electronic Devices Donhee Ham and Xiaofeng Li , <i>Harvard University, Cambridge, MA</i>
3:00	Break
3:20	Spintronics: Past, Present, and Future Stuart Parkin , <i>IBM Almaden Research Center, San Jose, CA</i>
4:10	Panel discussion
5:00	Conclusion

SPECIAL-TOPIC EVENING SESSIONS

SE1: What is Driving Displays?

Organizer: **Jed Hurwitz**, *Gigle Semiconductor, Edinburgh, United Kingdom*

Chair: **Marshall Bell**, *National Semiconductor, Pheonix, AZ*

The display business is a multi-billion-dollar market, with a wide range of solutions and technologies ranging from the low-power display on your cell phone to an HDTV home cinema the size of your living room, to even a virtual display. There are many different core technologies used for the generation and modulation of light, each with different merits and challenges. This session will introduce some of these technologies and, more importantly for the ISSCC community, the role of the associated microelectronics that is an integral part of each application.

The speakers in this Special-Topic Evening Session come from various backgrounds, and bring a collective experience of more than 50 years in the display industry. **Myunghye Lee** will talk about the driver IC technologies for TFT displays, **Arokia Nathan** will talk about flat-panel active-matrix Organic-LED technology, **Mary Lou Jepsen** will talk about liquid-crystal-on-silicon (LCOS) microdisplays for projection, and **Ian Underwood** will introduce Polymer-LED microdisplays for near-to-eye applications. This cross-section of technologies, challenges, and solutions, should serve to introduce an attendee not just to the core display technologies and the current state-of-the-art in the display arena, but should stimulate new thoughts on the opportunities for silicon providers to serve this growing market.

Come and be illuminated!

<u>Time</u>	<u>Topics</u>
7:30	TFT-Driver IC Design: What are the Challenges? , Myunghye Lee , <i>Samsung, Korea</i>
8:00	AMOLED Displays and Driving Schemes , Arokia Nathan , <i>University of Waterloo, Ontario, Canada</i>
8:30	Analog Silicon For Digital Television and Other Oxymorons , Mary Lou Jepsen , <i>MIT, Cambridge, MA</i>
9:00	CMOS Active-Matrix Backplane Design for Microdisplays , Ian Underwood , <i>MicroEmissive Displays, Edinburgh, United Kingdom</i>

SE2: Power-Aware Signal Processing**Organizer:** **Rajeevan Amirtharajah**, *University of California, Davis, CA***Chair:** **Wanda Gass**, *Texas Instruments, Dallas, TX*

Implementing the vision of “ubiquitous multimedia applications for a mobile world” will require incorporating power-awareness at all levels of portable-device design. Power-aware digital signal processing (DSP) will be a major component for next-generation portable multimedia platforms such as cellular phones beyond 3G, handheld gaming devices, MP3 players, digital cameras, and mobile television. This Special-Topic Evening Session on Power-Aware Signal Processing will describe novel circuit, architecture, CAD, and algorithmic techniques for linking system power consumption to signal-processing performance, user requirements, and power availability from batteries or energy harvesting from the environment. This session will provide presentations on a variety of approaches to implementing power-awareness, including the use of variable-precision arithmetic structures, reconfigurable architectures, power-optimized libraries, dynamically-scalable supply voltages, and variable-clocking strategies. These approaches will be described in a variety of application contexts, including wireless sensor nodes, digital still cameras, and portable multimedia devices. The first presentation in the session describes an energy-scalable computational array which targets mechanical-vibration energy-harvesting applications. The second presentation extends reconfigurable architectures to implement power-awareness for multimedia applications, focusing on video. Digital still-camera design is the topic of the third presentation, which addresses the challenges to delivering high computation throughput within a limited power budget at all levels of the system hierarchy. The final presentation develops image-processing techniques which can enable ambient intelligence.

<u>Time</u>	<u>Topics</u>
7:30	<i>An Energy-Scalable Computational Array for Sensor Signal Processing,</i> Rajeevan Amirtharajah , <i>University of California, Davis, CA</i>
8:00	<i>Power-Aware Multimedia,</i> Liang-Gee Chen , <i>National Taiwan University, Taipei, Taiwan</i>
8:30	<i>Power Management for Digital Still Cameras,</i> Clay Dunsmore , <i>Texas Instruments, Dallas, TX</i>
9:00	<i>Wireless Smart Vision for Ambient Intelligence,</i> Richard Kleihorst , <i>Philips, Eindhoven, The Netherlands</i>

SPECIAL-TOPIC EVENING SESSIONS

SE3: Analog Scaling

Organizer: **Andrea Baschirotto**, *University of Lecce, Lecce, Italy*

Chair: **Robert Neff**, *Agilent Labs, Palo Alto, CA*

According to ITRS, technology scaling provides a robust roadmap for digital circuits, while analog circuits strongly suffer from this trend. This disparity is becoming a crucial bottleneck in the realization of any SoC in a scaled technology which merges high-density digital parts with high-performance analog interfaces. This results from the fact that scaled technologies reduce the supply voltage, and this limits analog performance both in qualitative (is it possible to operate from a low voltage?) and quantitative (if it is possible to operate, what performance is achievable?) terms. In fact, the reduced voltage and the modified analog performance of scaled-technology devices imply a lower output swing and a reduced dynamic range for analog circuits. And this is more and more critical in advanced signal-processing systems, which require large dynamic range at low supply voltage. Analog designers have then to face challenging trade-offs between supply headroom, device matching, gain, and accuracy, etc.

This Special-Topic Evening Session is organized in three presentations that deal with these critical issues, giving an overview of the present situation and a forecast of the future. Each presentation will deal with one of the following open questions:

- How will the new scaled-technologies affect the power consumption of an analog system?
- Which analog topologies will be feasible in scaled technologies?
- Which level of performance will be possible in scaled technologies?

Each presentation will analyze the scalability of different blocks in analog signal-processing units, such as gain stages, filters, ADCs, etc.

<u>Time</u>	<u>Topics</u>
7:30	<i>The Effects of Technology Scaling on Power Dissipation in Analog CMOS Circuits,</i> Klaas Bult, <i>Broadcom, Bunnik, The Netherlands</i>
8:10	<i>Analog-Circuit Solutions in Scaled Technologies,</i> Andrea Baschiroto, <i>University of Lecce, Lecce, Italy</i>
8:50	<i>Delta-Sigma Converters in Scaled CMOS Technologies,</i> Willy Sansen, <i>KU Leuven, Leuven, Belgium</i>

SESSION 1

PLENARY SESSION - INVITED PAPERS

- Chair:** Timothy Tredwell, Eastman Kodak, Rochester, NY
ISSCC Executive-Committee Chair
- Associate Chair:** Jan Sevenhans, AMI Semiconductor,
Vilvoorde, Belgium
ISSCC Program-Committee Chair

FORMAL OPENING OF THE CONFERENCE 8:30AM

1.1 Where CMOS is Going: Trendy Hype vs. Real Technology 8:40 AM

Tze-Chiang (T.C.) Chen *IBM Fellow, VP of Science and Technology,
T.J. Watson Research Center, Yorktown Heights, NY*

The development of silicon technology has been, and will continue to be, driven by system needs. Traditionally, these needs have been satisfied by the increase in transistor density and performance, as suggested by 'Moore's Law' and guided by CMOS scaling theory. As the silicon industry moves towards the 45nm node and beyond, the two most important challenges cited are the growing standby power dissipation and the increasing variability in device characteristics. These complaints are cited as the reason Moore's Law is "broken", or why CMOS scaling is coming to an end. Actually, these effects are the embodiments of CMOS technology's approach to atomistic and quantum-mechanical physics boundaries. However, the infusion of new materials and device structures will extend the development lifetime of silicon CMOS by at least ten years. Cooperative circuit/technology co-design, and architectures developed concurrently with these new device innovations will provide a comprehensive solution to the challenges of deep submicron CMOS.

ISSCC, SSSC, JSSCC, & IEEE AWARD PRESENTATIONS 9:30 AM

BREAK 10:00 AM

1.2 ICs for Mobile Multimedia Communications 10:15AM

Hermann Eul, *Member of the Management Board,
Infineon Technologies, Munich, Germany*

The seemingly never-ending advancement of silicon technology has resulted in the emergence of mobile broadband communication systems for voice, data and video transmission with good connectivity and proper quality-of-service. Devices are being fabricated using processes managed at atomic levels, while IC design involves detailed systems engineering, including the incorporation of application content. Data-rate and mobility tradeoffs and different standards like 2G, 3G, Bluetooth, WLAN, GPS and digital-video broadcasting, are leading to multimode requirements and topics such as the coexistence of different technologies must be solved. Beyond all of that, secure data transfer using security checks like encryption is most important for the networked world.

All of these various topics are, finally, the reason for the appearance of challenging architectural requirements, such as architectural re-configurability and programmability, motivated by the growing importance of multimode and multistandard solutions. While parameters such as data-rate and algorithmic- and

circuit-complexity have changed approximately exponentially with time, there has not been much improvement in the battery capacity. For this reason key considerations for mobile products are energy management and power reduction. In this context, the introduction of platform concepts, including analog and RF at the most practical cost, power-levels and form-factors, are key requirements for system-on-chip and system-in-package solutions for current and future mobile multimedia terminals.

This talk will explore current multi-million-transistor ICs with multi-billion operations per second of signal processing, along with analog and RF capabilities for mobile multimedia communications. It will also consider special requirements on wafer processes such as leakage and analog and RF capabilities, and will look at how R&D engineers bridge the world of system-level design, silicon and software. Of course, new challenges going forward will be considered and explored.

1.3 The Future of Computing for Real-Time Entertainment

11:05AM

Ken Kutaragi, *President and CEO of SONY Computer Entertainment, Tokyo, Japan*

There are two elements in real-timeliness that a human being can intuitively sense. One is the continuity of motion that a human being can cognitively feel to be natural, and the other is response time between action and reaction. Correspondingly, of the applications that have advanced the concept of real-time computing is computer entertainment systems which originally started as computer games. Real-timeliness of computer entertainment systems must be quick enough to match the speed of the response time of the player. Lack of both processing power and data-transfer rate in achieving this level of real-timeliness using general-purpose microprocessors have motivated the development of a new breed of more-powerful processors built on a new architecture.

In computer entertainment systems, since the hardware is normally fixed for several years, once its specifications are determined, there is an inclination to seek the most-advanced technology within the future roadmap, typically that of three years ahead, and one generation ahead in the semiconductor-fabrication process. As a consequence, a system must start off by utilizing large-size chipsets at launch, but, during its life cycle, it goes through two generations of semiconductor fabrication processes for downsizing, as well as progressive integration of chips to reduce manufacturing costs, and to enable mass production. Today, more than 40 million computer entertainment systems are shipped in a year, and are becoming a strong leading power in spearheading advancement in semiconductor technology and in creating demand.

In the future of real-time computing, massive assembly of "Parallel computing over the network" to execute vast amounts of computation, and "Vision System" that recognize the real world, in real-time, from a vast number of sensors over the network, will lead the next era in real-time computing.

SESSION 2

BIOMEDICAL SYSTEMS

Chair: K. D. Wise, University of Michigan, Ann Arbor, MI

Associate Chair: Euisik Yoon, University of Minnesota, Minneapolis, MN

2.1 A 24×16 CMOS-Based Chronocoulometric DNA Microarray

1:30 PM

M. Augustyniak^{1,2}, C. Paulus³, R. Brederlow¹, N. Persike⁴, G. Hartwick¹, D. Schmitt-Landsiedel¹, R. Thewes¹

¹Infineon Technologies, Munich, Germany

²Technical University Munich, Munich, Germany

³Siemens, Munich, Germany

⁴Friz Biochem, Munich, Germany

An array of 24×16 electrochemical sensors for detecting bio-molecules uses gold sensor electrodes added to a 0.5µm CMOS process. Detection is based on time-resolved measurement of charge (Chronocoulometry). A differential measurement technique uses a replica electrode and fast integration to suppress background offset signals.

2.2 Fully Electronic CMOS DNA Detection Array based on Capacitance Measurement with On-Chip Analog-to-Digital Conversion

2:00 PM

C. Stagni degli Esposti¹, C. Guiducci¹, C. Paulus², M. Schienlé², M. Augustyniak³, G. Zuccheri¹, B. Samorì¹, L. Benini¹, B. Riccò¹, R. Thewes³

¹University of Bologna, Bologna, Italy

²Siemens, Munich, Germany

³Infineon Technologies, Munich, Germany

An 8×16 array of sensing micro-sites employs a fully-electrical label-free technique for DNA recognition using capacitance measurement and is fabricated in 0.5µm CMOS with added noble metal. Repeatability and parallel detection capability have been demonstrated. The DNA-chip is suitable for low-cost, fully-integrated point-of-care applications.

2.3 A 32-Site 4-Channel Cochlear Electrode Array

2:30 PM

P. Bhatti, S. Lee, K. Wise

University of Michigan, Ann Arbor, MI

A thin-film cochlear electrode array has been developed to improve pitch perception and reduce insertion damage. A silicon-parylene substrate supports 32 IrO sites on 250µm centers along with circuitry for current generation and position sensing. Interfacing over eight leads at ±3V, stimulus pulses cover ±500µA with 8b resolution and a minimum pulse width of 4µs.

Break 3:00 PM

2.4 A 0.1mm² Digitally Programmable Nerve Stimulation Pad Cell with High-Voltage Capability for a Retinal Implant

3:15 PM

M. Ortmanns¹, N. Unger¹, A. Rocke¹, M. Gehrke², H-J. Tiedtke²

¹sciworx, Hannover, Germany

²IIP Technologies, Bonn, Germany

A 0.1mm² autonomous and digitally programmable nerve stimulation pad cell in 0.35μm HVCMOS is used in a 232-electrode retinal implant. It provides greater than ±15V swing at the electrode in order to supply suitable stimulation currents into large electrode impedances. Customized ESD protection is used on all electrodes. Charge balancing is applied to prevent electrolysis.

2.5 Minimally Invasive Retinal Prosthesis

3:45 PM

L. Theogarajan¹, J. Wyatt¹, J. Rizzo^{2,3}, B. Drohan³, M. Markova¹, S. Kelly³, G. Swider², M. Raf⁴, D. Shire⁵, M. Gingerich², J. Lowenstein², B. Yomtov^{1,2}

¹MIT, Cambridge, MA

²MEEI, Boston, MA

³VA, Boston, MA

⁴University of California, Irvine, CA

⁵Cornell University, Ithaca, NY

A wireless retinal implant with a low-power area-efficient stimulator chip features an ASK demodulator, single-ended-to-differential converter, low-power DLL and programmable current drivers. The chip dissipates 1.3mW from ±2.5V at a data rate of 100kb/s. The chip is powered and driven through a wireless inductive link separated by 15mm.

2.6 A 60μW 60nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems

4:15 PM

R. Yazicioglu^{1,2}, P. Merken¹, R. Puers², C. Van Hoof^{1,2}

¹IMEC, Leuven, Belgium

²Katholieke Universiteit, Leuven, Belgium

A biopotential readout front-end can be configured to extract EEG, ECG, and EMG signals and draws 20μA from 3V. AC coupling of chopped amplifiers results in an input-referred noise of 60nV/√Hz and CMRR of 120dB at 1kHz. The immunity of the CMRR to electrode offset voltages is improved with an active input stage and 110dB CMRR is achieved at 100Hz with 50mV electrode offset.

2.7 A 1V 2.3μW Biomedical Signal Acquisition IC

4:45 PM

H. Wu, Y. Xu

National University of Singapore, Singapore

A 1V 2.3μW biomedical signal acquisition IC is fabricated in a 0.35μm CMOS process. It consists of an LNA and an 11b ADC. The OTA achieves an optimum trade-off between noise and power consumption with rail-to-rail output. A pseudo-S/H circuit is incorporated in the OTA. The modified successive-approximation ADC allows rail-to-rail inputs.

Conclusion

5:15 PM

SESSION 3

OVERSAMPLING ADCS

Chair: Raf Roovers, Philips, Eindhoven, The Netherlands

Associate Chair: Zhongyuan Chang, IDT-Newave Technology, Shanghai, China

3.1 A 14b 20mW 640MHz CMOS CT $\Delta\Sigma$ ADC with 20MHz Signal Bandwidth and 12b ENOB

1:30 PM

G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, E. Romani, A. Melodia, V. Mellini

Xignal Technologies, Unterhaching, Germany

A 3rd-order single-loop CT $\Delta\Sigma$ modulator with a 4b internal quantizer operating at 640MHz achieves 76dB SNR, -78dB THD, and 74dB SINAD in a 20MHz signal bandwidth with an OSR of 16. The modulator operates between 20 to 40MS/s output data rate and dissipates 20mW from a 1.2V supply at 40MS/s. The degradation of stability due to excess loop delay is solved with a quantizer feedback architecture.

3.2 A 375mW Quadrature Bandpass $\Delta\Sigma$ ADC with 90dB DR and 8.5MHz BW at 44MHz

2:00 PM

R. Schreier¹, N. Abaskharoun¹, H. Shibata², I. Mehr¹, S. Rose¹, D. Paterson¹

¹Analog Devices, Wilmington, MA; ²Analog Devices, Tokyo, Japan

A CT quadrature bandpass ADC is designed for a multi-standard television receiver. When clocked at 264MHz, the ADC achieves 90dB of total DR over an 8.5MHz BW centered at 44MHz. The 4th-order 4b ADC uses a modified feedforward topology and includes 12dB of AGC. The 2.5mm² chip consumes 375mW in a 0.18 μ m CMOS process.

3.3 A 118dB DR CT IF-to-Baseband $\Delta\Sigma$ Modulator for AM/FM/IBOC Radio Receivers

2:30 PM

P. Silva¹, L. Breems², K. Makinwa¹, R. Roovers², J. Huijsing¹

¹Delft University of Technology, Delft, The Netherlands

²Philips, Eindhoven, The Netherlands

A 1b 5th-order complex CT $\Delta\Sigma$ modulator with integrated IF mixer for AM/FM/IBOC car radio receivers is presented. The 118dB DR in AM mode enables the realization of the receiver without a VGA and an external AM channel filter. It is fabricated in a 0.18 μ m CMOS process and consumes 210mW from a 1.8V supply.

Break 3:00 PM

3.4 A 14mW Multi-bit $\Delta\Sigma$ Modulator with 82dB SNR and 86dB DR for ADSL2+

3:15 PM

S. Kwon¹, F. Maloberti²

¹University of Texas at Dallas, Richardson, TX

²University of Pavia, Pavia, Italy

Analog and digital feedforward swing-reduction techniques optimize the power consumption of this 2nd-order $\Delta\Sigma$ modulator. The 0.18 μ m CMOS prototype uses 2 telescopic OTAs and 2 ADCs requiring 10 comparators. The technique makes the modulator equivalent to a 4b architecture. The OSR is 33 and the clock frequency is 144MHz.

3.5 A 5.4mW 2-Channel Time-Interleaved Multi-bit $\Delta\Sigma$ Modulator with 80dB SNR and 85dB DR for ADSL**3:45 PM***K-S. Lee¹, S. Kwon¹, F. Malobert^f*¹University of Texas at Dallas, Richardson, TX²University of Pavia, Pavia, Italy

A 2nd-order $\Delta\Sigma$ modulator that obtains low power consumption by 2-channel time-interleaving is described. The main channel requires 2 opamps whereas the second channel does not use any active elements. This structure is robust to channel mismatches and uses a simple clocking scheme. The circuit is integrated in a 0.18 μm CMOS process and occupies an active area of 1.1mm².

3.6 A 0.5V 74dB SNDR 25kHz CT $\Delta\Sigma$ Modulator with Return-to-Open DAC**4:15 PM***K-P. Pun¹, S. Chatterjee², P. Kinge^f*¹Chinese University of Hong Kong, Hong Kong, China²Columbia University, New York, NY

A 0.5V 3rd-order 1b fully differential CT $\Delta\Sigma$ modulator in a 0.18 μm CMOS process is presented. A special return-to-open DAC, a body-input gate-clocked comparator, and body-input OTAs for the active-RC loop filter enable the ultra-low voltage operation. The 0.6mm² chip consumes 370 μW and achieves a peak SNDR of 74dB in a 25kHz BW.

3.7 A 0.9V $\Delta\Sigma$ Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique**4:45 PM***J. Goes¹, B. Vaz², R. Monteiro², N. Paulino¹*¹Universidade Nova de Lisboa, Monte da Caparica, Portugal²Acacia Semiconductor, Caparica, Portugal

A 2nd-order $\Delta\Sigma$ ADC implemented in 0.18 μm CMOS occupies 0.06mm² and dissipates 0.2mW from a 0.9V supply. It achieves 80dB SNDR and 83dB DR over a 10kHz BW employing a single-phase technique to reach such performance. An amplifier-sharing scheme is proposed to improve power and area efficiency.

3.8 A 80/100MS/s 76.3/70.1dB SNDR $\Delta\Sigma$ ADC for Digital TV Receivers**5:00 PM***Y. Fujimoto, Y. Kanazawa, P. Lo Re, M. Miyamoto*

SHARP, Nara, Japan

A 4th-order SC $\Delta\Sigma$ modulator with a 4b quantizer is designed for a low-power direct-conversion receiver SoC for Japanese ISDB-T and European DVB-T. It achieves a 76.3/70.1dB SNDR over a 3.2/4MHz bandwidth with a clock frequency of 80/100MHz. The 1.7mm² chip, fabricated in a 0.18 μm CMOS process draws 13.2/19.1mA from a 1.8V supply. It has a FOM of 0.7/1.64pJ/conversion.

Conclusion**5:15 PM**

SESSION 4

GIGABIT TRANSCEIVERS

Chair: Yuri Greshishchev, PMC-Sierra, Kanata, Canada

Associate Chair: Hirotaka Tamura, Fujitsu Laboratories, Japan

4.1 A 10Gb/s 5-Tap-DFE/4-Tap-FFE Transceiver in 90nm CMOS

1:30 PM

M. Meghelli, S. Rylov, J. Bulzacchelli, W. Rhee, A. Rylyakov, H. Ainspan, B. Parker, M. Beakes, A. Chung, T. Beukema, P. Pepeljugoski, L. Shan, Y. Kwark, S. Gowda, D. Friedman
IBM, Yorktown Heights, NY

A 90nm CMOS 10Gb/s SerDes for chip-to-chip communications over backplanes is presented. To mitigate channel impairments, the RX uses a 5-tap DFE and the TX a 4-tap FIR filter. The IC equalization abilities are evaluated using different type of channels. The power consumption of one (TX, RX) pair and one PLL is 300mW for 1.2V_{pp} differential TX output swing.

4.2 A Serial-Link Transceiver with Transition Equalization

2:00 PM

K. Wong, C-K. Yang
University of California, Los Angeles, CA

Two transition-equalization techniques are proposed. A pulse-overlapping half-symbol tap FIR transmitter is able to equalize a 120-inch 40dB attenuation FR4 with BER of $<10^{-13}$ at 3.7Gb/s. A DFE with transition ISI cancellation performs better than traditional DFE and achieves a BER of $<10^{-12}$ at 3.6Gb/s with 80-inch FR4

4.3 A Quad 6Gb/s Multi-rate CMOS Transceiver with TX Rise/Fall-Time Control

2:30 PM

Y. Moon, G. Ahn, H. Choi, N. Kim, D. Shim
Silicon Image, Sunnyvale, CA

A multi-rate transceiver incorporating TX slew control with $>2x$ range, PLL with $<0.5x$ LF area using capacitance multiplication, and $-SSCG$ having 11.7dB peak reduction is designed in 0.13 μ m CMOS. Occupying 2.33mm² with TX operable up to 8.5Gb/s, the quad transceiver consumes 386mW from 1.2V supply and has a BER $<10^{-14}$ at 6Gb/s over an 8m cable with 22dB loss.

Break 3:00 PM

4.4 A 12.5Gb/s Single-Chip Transceiver for UTP Cable in 0.13 μ m CMOS

3:15 PM

M. Callicotte, J. Little, H. Takatori, K. Dyer
Keyeye Communications, Sacramento, CA

The demand for multi-Gb transceivers over copper medium is rapidly increasing. While this function is currently accomplished by fiber-optic transceivers, their high cost and difficult installation makes other possible alternatives attractive. A 0.13 μ m CMOS solution consuming 3.8W at a maximum data-rate of 12.5Gb/s is presented.

4.5 A 100mW 9.6Gb/s Transceiver in 90nm CMOS for Next-Generation Memory Interfaces**3:45 PM***E. Prete, D. Scheideler, A. Sanders*
Infineon, Munich, Germany

An architecture for next-generation memory interface is demonstrated using 90nm bulk silicon to provide a 2-tap emphasized TX with <19ps jitter at 9.6Gb/s. The circuit uses a programmable PLL to track jitter up to 200MHz. The transceiver consumes 100mW from a 1V supply.

4.6 A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS**4:15 PM***B. Casper, J. Jaussi, F. O'Mahony, M. Mansuri, K. Canagasaby, J. Kennedy, E. Yeung, R. Mooney*
Intel, Hillsboro, OR

A forwarded clock I/O link in 90nm CMOS is capable of passing data at 20Gb/s over 7-inches of FR4 with 2 sockets and packages at a power dissipation of less than 12mW/Gb/s. Passive distribution and AC coupling of the forwarded clock are used to achieve 820fs_{rms} of sample-time uncertainty. Nyquist rate channel losses in excess of -15dB are compensated using a combination of 4-tap transmit equalization and receiver continuous-time equalization.

4.7 A 20Gb/s Adaptive Equalizer in 0.13μm CMOS Technology**4:45 PM***J. Lee*
National Taiwan University, Taipei, Taiwan

An adaptive equalizer incorporates a spectrum-balancing technique to achieve high speed and low power obviating the need for slicers. Fabricated in 0.13μm CMOS, this circuit achieves a 20Gb/s data rate with 14ps peak-to-peak jitter and consumes 60mW from a 1.5V supply.

4.8 An 8Gb/s Transformer-Boosted Transmitter with >V_{DD} Swing**5:00 PM***J. Kim, H. Hatamkhani, C-K. Yang*
University of California, Los Angeles, CA

An 8Gb/s serial-link transmitter that achieves >V_{DD} signal swing without stressing the voltage tolerance of the transistors is presented. The high-frequency signal is boosted to large swings above the supply rail through multiple transformer coupling. The design is implemented in 1.2V 0.13μm CMOS technology. The prototype TX achieves 1.42V_{pp} output swing with 1.16V on-chip V_{DD} and draws 136mA. The S₁₁ is less than -10dB for frequencies <4GHz.

Conclusion**5:15 PM**

SESSION 5

PROCESSORS

Chair: Héctor Sánchez, Freescale Semiconductor, Austin, TX

Associate Chair: Georgios Konstantinidis, Sun Microsystems, Sunnyvale, CA

5.1 A Power-Efficient High-Throughput 32-Thread SPARC Processor

1:30 PM

A. Leon, J. Shin, K. Tam, W. Bryg, F. Schumacher, P. Kongetira, D. Weisner

Sun Microsystems, Sunnyvale, CA

The first generation of Niagara SPARC processors implements a power-efficient multi-threading architecture to achieve high throughput with minimum hardware complexity. The design combines eight 4-threaded 64b cores, a high-bandwidth crossbar, a shared 3MB L2 Cache and four DDR2 DRAM interfaces. The 90nm 378mm² die consumes 63W at 1.2GHz. Memory design techniques to support the high bandwidth are also discussed.

5.2 A 16-Core RISC Microprocessor with Network Extensions

2:00 PM

V. Yalala, D. Brasili, D. Carlson, A. Hughes, A. Jain, T. Kiszely, K. Kodandapani, A. Varadharajan, T. Xanthopoulos

Cavium Networks, Marlboro, MA

A multi-core RISC processor is integrated with a number of security engines and network function accelerators creating a high-performance power-efficient SoC. It contains 180M transistors, dissipates 25W at 600MHz and is fabricated in a 1.2V 0.13μm CMOS process with 9 layers of copper interconnect using FSG dielectric and C4 bumps.

5.3 A Dual-Core Multi-Threaded Xeon™ Processor with 16MB L3 Cache

2:30 PM

S. Rusu, S. Tam, H. Muljono, D. Ayers, J. Chang

Intel, Santa Clara, CA

A dual-core 64b Xeon™ MP processor is implemented in a 65nm 8M process. The 435mm² die has 1.328B transistors. Each core has two threads and a unified 1MB L2 cache. The 16MB unified, 16-way set-associative L3 cache implements both sleep and shut-off leakage reduction modes.

Break 3:00 PM

5.4 A 2.6GHz Dual-Core 64b x86 Microprocessor with DDR2 Memory Support

3:15 PM

M. Golden¹, S. Arekapudi¹, G. Dabney², M. Haertel¹, S. Hale¹, L. Herlinger², Y. Kirn², K. McGrath¹, V. Palisetti¹, M. Singl²

¹Advanced Micro Devices, Sunnyvale, CA

²Advanced Micro Devices, Austin, TX

A microprocessor featuring 2 Hammer cores and an on-chip DDR2 memory controller implements Pacifica architectural support for virtualization. It is fabricated in a 90nm triple-V_t partially-depleted SOI process with 9 layers of copper interconnect. The chip achieves a clock frequency of 2.6GHz at 1.35V while dissipating 95W.

5.5 A 64b CPU Pair: Dual- and Single-Processor Chips**3:45 PM**

E. Cohen¹, N. Rohrer¹, P. Sardon¹, M. Canada¹, C. Lichtenau², M. Ringler², P. Kartschok¹, R. Floyd¹, J. Heaslip¹, M. Ross¹, T. Pflueger², R. Hilgendorf², P. McCormick¹, G. Salem¹, J. Connor¹, S. Geissler¹, D. Thygesen¹, R. Tabet¹

¹IBM, Essex Junction, VT; ²IBM, Böblingen, Germany; ³IBM, Austin, TX

Two Power™-architecture 64b microprocessor chips are fabricated in 90nm dual strained-silicon SOI technology. The dual-processor chip has split clock domains and power planes, 1MB L2 cache per core and a shared processor interconnect bus. The single-processor chip shares the dual's basic core and cache design.

5.6 High-Speed Interconnect for a Multiprocessor Server Using Over 1Tb/s Crossbar**4:15 PM**

J. Yamada, H. Adachi, Y. Mori, S. Okada, H. Ando
Fujitsu, Kawasaki, Japan

A 170GB/s crossbar for a multiprocessor server is realized with 10 LSIs. High density and low power are achieved with a 1.333Gb/s single-ended signal transmission, a driver using pre-emphasis, and a receiver using a data-synchronous scheme. The total bandwidth of the address crossbar LSI is 1.23Tb/s with 704 drivers and 352 receivers.

5.7 A 9GHz 65nm Intel Pentium®4 Processor Integer Execution Core**4:45 PM**

S. Wijeratne, N. Siddaiah, S. Mathew, M. Anders, R. Krishnamurthy, J. Anderson, S. Hwang, M. Ernest, M. Nardin
Intel, Hillsboro, OR

In a 4th-generation 65nm Intel Pentium®4 processor, the previously low voltage swing, 2x microprocessor frequency, AGU and ALUs are replaced with domino-logic-based architectures optimized for low latency, 2x frequency, and lower power. These redesigned AGU/ALUs reduce normalized dynamic power by 50% over the previous generation, and together with the similarly optimized integer register file, enable a 9GHz 64b integer execution core at 1.3V and 70°C.

Conclusion**5:15 PM**

SESSION 6

UWB

Chair: Masaru Kokubo, Hitachi, San Francisco, CA
Associate Chair: Mark Ingels, IMEC, Leuven, Belgium

6.1 A 16mA UWB 3-to-5GHz 20MPulses/s Quadrature Analog Correlation Receiver in 0.18 μ m CMOS

1:30 PM

J.. Ryckaert¹, M. Badaroglu¹, V. De Heyn¹, G. Van der Plas¹, P. Nuzzo², A. Bashcirotto³, S. D'Amico³, C. Desset¹, H. Suys¹, M. Libois¹, B. Van Poucke¹, P. Wambacq¹, B. Gyselinckx¹

¹IMEC, Leuven, Belgium

²University of Pisa, Pisa, Italy

³University of Lecce, Lecce, Italy

A 3-to-5GHz quadrature analog correlation RX for UWB impulse radio draws 16mA at 20MPulses/s, making it suitable for low-power low-data-rate applications. The RX is fully integrated in a CMOS 0.18 μ m process and comprises an LNA, quadrature LO generation and mixers, baseband filtering, an integrator, timing circuitry, and an ADC.

6.2 A CMOS Carrier-less UWB Transceiver for WPAN Applications

2:00 PM

Y. Zheng¹, Y. Tong^{1,2}, C. W. Ang^{1,2}, Y-P. Xu², W. G. Yeoh¹, F. Lin¹, R. Singh¹

¹Institute of Microelectronics, Singapore, Singapore

²National University of Singapore, Singapore, Singapore

A carrier-less impulse-based UWB transceiver (TRX) chipset is presented. The TRX employs high-order pulse transmission with analog pulse-position modulation. Realized in a 0.18 μ m CMOS process, the TRX achieves a NF in the range of 7.7 to 8.1dB, an IIP3 of -12.3dBm, and a sensitivity of -80 to -72dBm. It consumes 76mW and 81mW from a 1.8V supply in transmit and receive modes, respectively.

6.3 A Dual-Antenna Phased-Array UWB Transceiver in 0.18 μ m CMOS

2:30 PM

S. Lo, I. Sever, S-P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, T. Nguyen

Tzero Technologies, Sunnyvale, CA

A dual-antenna UWB transceiver in 0.18 μ m CMOS for mode-1 OFDM applications employs the techniques of antenna diversity and integrated RF selectivity. The packaged device achieves an overall NF of 6.3dB, an IIP3 of -3.3dBm, a TX P_{1dB} of 3.1dBm, and an EVM of -27.2dB for 480Mb/s. The transmit output spectrum is compliant with the FCC mask for UWB without any external BPF.

Break 3:00 PM

6.4 A 1.1V 3.1-to-9.5GHz MB-OFDM UWB Transceiver in 90nm CMOS

3:15 PM

A. Tanaka, H. Okada, H. Kodama, H. Ishikawa

NEC, Sagamihara, Japan

A 3.1-to-9.5GHz UWB transceiver is implemented in 90nm CMOS technology. It includes a 12-band synthesizer and wideband TX/RX chains operating from a 1.1V supply. The transceiver provides a TX OIP3 of 7.2 to 8.6dBm, an RX gain of 58 to 64dB, and a NF of 6.3 to 7.8dB across 12 bands.

6.5 A WiMedia/MBOA-Compliant CMOS RF Transceiver for UWB**3:45 PM**

C. Sandner¹, S. Derksen¹, D. Draxelmayer¹, S. EK¹, V. Filimor², G. Leach³, S. Marsili¹, D. Matveev¹, K. Mertens¹, F. Michl¹, H. Paul², M. Punzenberger¹, C. Reindl¹, R. Salerno¹, M. Tiebou², A. Wiesbauer¹, I. Winter³, Z. Zhang¹

¹Infineon, Villach, Austria; ²Infineon, Munich, Germany

³Riverbeck, Swindon, United Kingdom

A fully integrated WiMedia/MBOA-compliant RF transceiver for UWB data communication in the 3 to 5GHz band is presented. It is designed in a 0.13 μ m standard CMOS process with 1.5V single supply voltage. The NF is between 3.6 and 4.1dB over all 3 bands. On the TX side, the P_{1dB} is 5dBm supporting an EVM of -28dB and up to -4dBm output power. A single-PLL LO generation is included.

6.6 A Fully Integrated UWB PHY in 0.13 μ m CMOS**4:15 PM**

T. Aytur¹, H-C. Kang², R. Mahadevappa¹, M. Altintas¹, S. ten Brink¹, T. Diep¹, C-C. Hsu¹, F. Shi¹, F-R. Yang¹, C-C. Lee², R-H. Yan¹, B. Razavi³

¹Realtek, Irvine, CA; ²Realtek, Hsinchu, Taiwan

³University of California, Los Angeles, CA

A direct-conversion RF transceiver and digital PHY are integrated in a single 0.13 μ m digital CMOS chip. Designed for UWB OFDM operation as proposed by the WiMedia Alliance, the device supports both fixed and frequency-hopped modes in the band of 3.1 to 4.8GHz. The RF transceiver draws 100mA in receive mode and 70mA in transmit mode, and the complete chip occupies 17mm².

6.7 A 14-band Frequency Synthesizer for MB-OFDM UWB Application**4:45 PM**

C-F. Liang¹, S-I. Liu¹, Y-H. Cher², T-Y. Yang², G-K. Ma²

¹National Taiwan University, Taipei, Taiwan

²Industrial Technology Research Institute, Hsinchu, Taiwan

A 14-band frequency synthesizer for UWB application is realized in a 0.18 μ m CMOS process. It uses two PLLs and three mixers. The unwanted spurs due to frequency mixing are at least 35dB lower than the output carriers by using a quadrature divide-by-3 circuit and a 2-stage single-sideband mixer. The core circuit area is 1.5mm² and the power consumption is 160mW.

6.8 A sub-1mm² Dynamically Tuned CMOS MB-OFDM 3-to-8GHz UWB Receiver Front-End**5:00 PM**

M. Ranjan, L. Larson

University of California, San Diego, CA

A 3-to-8GHz heterodyne receiver front end for MB-OFDM UWB systems consisting of an LNA, a mixer, and an on-chip IF BPF is presented. Designed in 0.18 μ m CMOS, it uses no on-chip inductors or any off-chip components. Measured NF is 5.5dB, IIP2 is 33dBm, and the chip draws 19.5mA from a 2.3V supply.

Conclusion**5:15 PM**

SESSION 7

NONVOLATILE MEMORY

Chair: Giulio Casagrande, STMicroelectronics, Milan, Italy
Associate Chair: Yukihiro Oowaki, Toshiba, Japan

7.1 A 4b/cell NROM 1Gb Data-Storage Memory 1:30 PM

Y. Polansky¹, A. Lavan¹, R. Sahar¹, O. Dadashev¹, Y. Betser¹, G. Coher¹, E. Maayan¹, B. Eitan¹, F-L. Ni², Y-H-J. Ku², C-Y. Lu², T-C. Tingchen², C-Y. Lia², C-H. Chang², C-K. Chen², W-C. Ho²

¹Saifun Semiconductors, Netanya, Israel; ²Macronix, Hsinchu, Taiwan

A 4b/cell 1Gb data Flash based on a low-cost NROM process technology is achieved. The design includes a two-phase programming algorithm for supporting a fast and accurate threshold-voltage control. The read scheme incorporates a simple error-detection mechanism combined with an accurate drain-side sensing circuit with a built-in offset cancellation.

7.2 A 64Mb Chain FeRAM with Quad-BL Architecture and 200MB/s Burst Mode 2:00 PM

K. Hoya, D. Takashima, S. Shiratake, R. Ogiwara, T. Miyakawa, H. Shiga, S. Doumae, S. Ohtsuki, Y. Kumura, S. Shuto, T. Ozaki, K. Yamakawa, I. Kunishima, A. Nitayama, S. Fujii

Toshiba, Yokohama, Japan

A 64Mb chain FeRAM implemented in 0.13 μ m 3M CMOS technology is described. A quad-BL architecture reduces the die area by 6.5% and realizes 87.5mm² die with an effective cell-size of 0.7191 μ m² while eliminating BL-BL coupling noise. A high-speed ECC circuit and cell data write-back scheme achieves read/write cycle time of 60ns and 200MB/s burst.

7.3 Signal-Margin-Screening for Multi-Mb MRAM 2:30 PM

H. Hönigschmid¹, P. Beer¹, A. Bette¹, R. Dittrich¹, F. Gardić², D. Gogf², S. Lammers¹, J. Schmid¹, L. Altimime², S. Bournat², G. Müller²

¹Infineon Technologies, Munich, Germany

²Altis Semiconductor, Corbeil Essonnes, France

As MRAM technology is maturing, the need for developing a strategy to identify and replace marginal bits during read/write operation becomes necessary. The methodology and circuit techniques for read/write signal-margin screening implemented in a 0.18 μ m 16Mb MRAM design, are described. The methodology leads to increased read/write signal margins resulting in fully functional dice by applying a wafer-level screen test including half select disturb pattern.

Break 3:00 PM

7.4 A 16Mb MRAM with FORK Wiring Scheme and Burst Modes 3:15 PM

Y. Iwata¹, K. Tsuchida¹, T. Inaba¹, Y. Shimizu¹, R. Takizawa¹, Y. Ueda¹, T. Sugibayashi¹, Y. Asao¹, K. Kajiyama¹, K. Hosotani¹, S. Ikagawa², T. Kai², M. Nakayama², S. Tahara², H. Yoda³

¹Toshiba, Yokohama, Japan; ²NEC, Sagamihara, Japan

³Toshiba, Kawasaki, Japan

A 16Mb MRAM based on 0.13 μ m CMOS and 0.24 μ m MRAM process achieves a 34ns asynchronous access and 100MHz synchronous operation, compatible with pseudo-SRAM for mobile applications. By implementation of FORK wiring scheme, the cell efficiency is raised to 39.9% and the disturb robustness of half-selection state is improved.

7.5 A 0.1 μ m 1.8V 256Mb 66MHz Synchronous Burst PRAM**3:45 PM**

S. Kang, W. Cho, B-H. Cho, K-J. Lee, C-S. Lee, H-R. Oh, B-G. Choi, Q. Wang, H-J. Kim, M-H. Park, Y-H. Ro, S. Kim, D-E. Kim, K-S. Cho, C-D. Ha, Y. Kim, K-S. Kim, C-R. Hwang, C-K. Kwak, H-G. Byun, Y. Shin
Samsung, Hwasung-City, Korea

A 256Mb PRAM featuring synchronous burst read operation is developed. Using a charge-pump system, write performance is characterized at 1.8V supply. Measured initial read access time and burst-read access time are 62ns and 10ns, respectively. The maximum write throughput is 3.3MB/s.

7.6 A 4Gb 2b/cell NAND Flash Memory with Embedded 5b BCH ECC for 36MB/s System Read Throughput**4:15 PM**

R. Micheloni¹, R. Ravasio¹, A. Marelli¹, E. Alice², V. Altieri¹, A. Bovino², L. Crippa¹, E. Di Martino², L. D'Onofrio², A. Gambardella², E. Grillea², G. Guerra², D. Kim³, C. Missiroli¹, I. Motta¹, A. Prisco², G. Ragone¹, M. Romano², M. Sangalli¹, P. Saur², M. Scotti¹, S. Wor³

¹STMicroelectronics, Agrate Brianza, Italy

²STMicroelectronics, Arzano, Italy

³Hynix Semiconductor, Icheon, Korea

A 4Gb 2b/cell NAND Flash memory designed in a 90nm CMOS technology incorporates a 25MHz BCH ECC architecture, correcting up to 5 errors over a flexible data field (1B to 2102B). Two alternative Chien circuits are used depending on the number of errors (1 to 5) thus minimizing latency time. ECC area overhead is less than 1%.

7.7 A 56nm CMOS 99mm² 8Gb Multi-level NAND Flash Memory with 10MB/s Program Throughput**4:45 PM**

K. Takeuchi¹, Y. Kameda¹, S. Fujimura¹, H. Otake¹, K. Hosono¹, H. Shiga¹, Y. Watanabe¹, T. Futatsuyama¹, Y. Shindo¹, M. Kojima¹, M. Iwai¹, M. Shirakawa¹, M. Ichige¹, K. Hatakeyama¹, S. Tanaka¹, T. Kamef¹, J-Y. Fu², A. Cernea³, Y. Li², M. Higashitan¹, G. Hemink², S. Sato², K. Oowada², S-C. Lee³, N. Hayashida², J. Wan², J. Lutz³, S. Tsao³, M. Mofidi³, K. Sakurai¹, N. Tokiwa¹, H. Waki¹, Y. Nozawa¹, K. Kanazawa¹, S. Ohshima¹

¹Toshiba, Yokohama, Japan; ²SanDisk, Yokohama, Japan

³SanDisk, Sunnyvale, CA

Fabricated in 56nm CMOS technology, an 8Gb multi-level NAND Flash memory occupies 98.8mm², with a memory cell size of 0.0075 μ m²/b. The 10MB/s programming and 93ms block copy are also realized by introducing 8kB page, noise-cancellation circuits, external page copy and the dual V_{DD} scheme enabling efficient use of 1MB blocks.

Conclusion**5:15 PM**

DISCUSSION SESSION

E1: Is the Digital-Circuit Designer Dead?

Organizer: Shannon Morton, *Icera, Bristol, United Kingdom*
Moderator: Dennis Fischette, *AMD, Sunnyvale, CA*

Technology-scaling trends have often been said to prophesize the death of dynamic logic, the perennial foundation for exciting circuit design. Conversely, CAD tools have long sought to improve their capabilities with the most fundamental logic family: static logic. What, then, is the role of the digital designer in light of these compressive forces? Does life truly still exist in dynamic and cascode logic, etc.? Are those who design such structures fooling themselves about the future? Will new technologies provide scope for the evolution of the digital species? Is it beyond the scope of CAD tools to generate sufficiently fast/low-power circuits? Or, is the digital circuit designer dead?

Panelists:

Jon Beecroft, *Quadrics, Bristol, United Kingdom*
David Money Harris, *Harvey Mudd College, Claremont, CA*
Mark Horowitz, *Stanford University, Stanford, CA*
Robert Montoye, *IBM, Austin, TX*
Gary C. Moyer, *Intel, Hudson, MA*
Mike Seningen, *Intrinsity, Austin, TX*
Kazuo Yano, *Hitachi, Tokyo, Japan*

SE4: Emerging & Disruptive Memory Technologies**Organizer/Chair:** Sreedhar Natarajan, *Emerging Memory Technologies, Kanata, Canada*

This Special-Topic Evening Session is organized to give the audience an overview of some of the emerging and disruptive memory technologies for use at 65nm and below. Many new technologies are being researched and only a few of them will materialize at the end. Most of these new innovative and futuristic technologies are going to be very application-specific, and may (or may not suit) the wider market segment.

The first presentation of the session will discuss the SOI-based twincell technology which is a viable alternative to its counterparts, and has immense performance and power advantages. The next presentation will highlight the thyristor RAM which is an emerging memory technology that is gaining rapid momentum in the industry, with major advancements being made in cell manufacturability, while showing a lot of market potential. Many of the new technologies lack scalability, and are difficult to integrate due to the need for complex process steps. To overcome these difficulties, a highly-scalable resistance-change memory using solid electrolytes will be discussed in detail. The final presentation will outline the technologies required to take the industry to the terabit level of storage capacity, and compete with Nand Flash.

<u>Time</u>	<u>Topics</u>
8:00	<i>SOI TwinCell RAM Technology,</i> Kazutami Arimoto, <i>Renesas, Osaka, Japan</i>
8:30	<i>Thyristor RAM: An Evolving and Disruptive Memory Technology,</i> Bruce Bateman, <i>T-RAM, San Jose, CA</i>
9:00	<i>Small Hard-Disk Drives versus Solid-State Storage,</i> Barry Stipe, <i>Hitachi, San Jose, CA</i>
9:30	<i>Highly-Scalable Resistance-Change Memory Using Solid Electrolytes,</i> Michael N. Kozicki, <i>AxonTechnologies, Scottsdale, AZ</i> <i>Arizona State University, Tempe, AZ</i>

DISCUSSION SESSIONS

SE5: CMOS RF Design at 90nm and Beyond

Organizer: David Su, *Atheros Communications, Santa Clara, CA*

Chair: Tony Montalvo, *Analog Devices, Raleigh, NC*

The scaling of CMOS analog and RF circuits traditionally lags that of digital design by one or two technology nodes. For instance, the majority of today's RF CMOS products are still in 0.13 to 0.18 μ m CMOS technology. However, the increasing integration level for systems-on-a-chip will lead RF designers, willingly or unwillingly, to follow their digital counterparts to 90nm and beyond.

Several 90nm CMOS RF publications have already appeared at recent ISSCC Conferences. The trend should continue with designs at 65nm, and, dare we say, 45nm and beyond. What are the features of these scaled technologies and their impact on RF design? Can we truly exploit scaling advantages for RF circuits? Does it make sense to simply port existing RF designs, or is it desirable (or even necessary) to use a completely different architecture? Does the presence of RF on the same chip as the DSP slow the migration? In addition to the technical challenges of these scaled technologies, the associated economic issues are equally daunting. The projected staggering costs and long fabrication cycle times can create project-management nightmares. What do we do with millions of transistors on a chip? How do we justify a multi-million-dollar mask cost? In short, how do we succeed in RF design at 90nm and beyond ?

In this Special-Topic Evening Session, experts from academia and industry will describe some of the challenges that face RF designers as they embrace the inevitable prediction of Moore's Law. The speakers will address the advantages and obstacles that await RF designers as they migrate to the next scaled-technology node. In particular, they will address the technology-characteristics, modeling issues, circuit-design challenges, and an actual case study. This session promises to be enlightening and educational!

<u>Time</u>	<u>Topics</u>
8:00	<i>Technology-Property Exploration for Analog/RF Design at 90nm and Beyond,</i> Maarten Vertregt, Philips, Eindhoven, The Netherlands
8:30	<i>RF Modeling Challenges for Deep-Submicron CMOS,</i> Sally Liu, TSMC, Hsin-chu, Taiwan
9:00	<i>RF Design Challenges in Deep-Submicron CMOS,</i> Behzad Razavi, University of California, Los Angeles, CA
9:30	<i>Case Study of Single-Chip Integration for Wireless,</i> Bill Krenik, Texas Instruments, Dallas, TX

SE6: Highlights of A-SSCC 2005 and the 2005 Symposium on VLSI Technology

Co-Organizers: Takayasu Sakurai, *University of Tokyo, Tokyo, Japan*
 Ian Young, *Intel, Hillsboro, OR*
 Takayuki Kawahara, *Hitachi, Tokyo, Japan*

Chair: Yoshiaki Hagiwara, *Sony, Tokyo, Japan*

A-SSCC is the international forum for advances in solid-state circuit design held in Asia, and fully supported by the IEEE Solid-State Circuits Society. This conference was newly initiated in Hsinchu, Taiwan, in 2005. Amongst the papers presented following a very rigorous selection process, three papers, one from each of Korea, Taiwan, and China, are to be presented at ISSCC this year. The topics of the three papers are diverse, representing the balanced growth of LSI design in Asia. The presentation topics are: a high-speed serial links using DLL-based clock-edge modulation with 270Mb/s operation using 3.12mW from a 1.2V supply in 0.18 μ m CMOS, a low-power analog-digital mixed-mode low-power IC architecture for use inside a wireless endoscopic capsule, and a differential-cascade distributed amplifier with pass bandwidth of 100MHz to 25.5GHz using 0.18 μ m CMOS.

On the other hand, the Symposium on VLSI Technology celebrated its twenty-fifth anniversary in 2005, in Kyoto, Japan. The organizers of this conference have afforded a unique opportunity for engineers and scientists to share the entire VLSI spectrum by pairing the Symposium on VLSI Technology with the Symposium on VLSI Circuits. From the large collection of papers on new concepts and breakthroughs in VLSI devices and processes, three papers concerning advanced transistor technology have been selected for presentation at ISSCC this year. These describe the application of strained-Si directly on insulator to achieve high performance within a strict power budget, a 65nm-node HfSiON dielectric and body-biasing scheme with I_{on} of 510 μ A/ μ m and $I_{standby}$ of 23pA/ μ m, and an 8Å high-performing ultra-thin n-channel transistor with TaN-gated HfO₂ with on-current of 815 μ A/ μ m and off-current of 0.1 μ A/ μ m.

Time Topics

- 8:00 ***A 3mW 270Mb/s Clock-Edge-Modulated Serial Link for Mobile Applications***
 Won-Jun Choe, *Seoul National University, Seoul, Korea*
- 8:20 ***A Low-Power Digital IC Design for Use Inside a Wireless-Endoscopy Capsule,***
 Xiang Xie, *Tsinghua University, Beijing, China*
- 8:40 ***A 0.1 to 25.5GHz Differential-Cascade Distributed Amplifier in 0.18 μ m CMOS***
 Chihun Lee, *National Taiwan University, Taipei, Taiwan*
- 9:00 ***Super-Critical Strained-Si Directly On Insulator (SC-SSOI) CMOS Based on High-Performance PD-SOI Technology,***
 Aaron Voon-Yew Thean, *Freescale Semiconductor, Austin, TX*
- 9:20 ***Ultra-Low Standby Power (U-LSTP) 65nm-node CMOS Technology Utilizing HfSiON Dielectric and a Body-Biasing Scheme,***
 Naohiko Kimizuka, *NEC Kanagawa, Japan*
- 9:40 ***High-Performing 8Å EOT HfO₂ / TaN Low-Thermal-Budget n-channel FETs with Solid-Phase Epitaxially Regrown (SPER) Junctions,***
 Lars-Åke Ragnarsson, *IMEC, Leuven, Belgium*

SESSION 8

DRAM AND TCAM

Chair: Terry Lee, Micron Technology, Boise, ID
Associate Chair: Young-Hyun Jun, Hwasung-City, Korea

8.1 An 8Gb/s/pin 9.6ns Row-Cycle 288Mb Deca-Data Rate SDRAM with an I/O Error-Detection Scheme

8:30 AM

K-H. Kim, U. Kang, H-J. Chung, D-H. Park, W-S. Kim, Y-C. Jang, M. Park, H. Lee, J-Y. Kim, J. Sunwoo, H-W. Park, H-K. Kim, S-J. Chung, J-K. Kim, H-S. Kim, K-W. Kwon, Y-T. Lee, J-S. Choi, C. Kim
Samsung, Hwasung-City, Gyeonggi-Do, Korea

A 288Mb deca-data rate SDRAM with an I/O error-detection scheme is developed. Deca-data rate is proposed to include CRC for the higher data-rate beyond 5Gb/s/pin using a conventional DRAM process. Several techniques, including an area-efficient cell array consisting of two $6F^2$ cells are adopted to enhance the core cycle speed. Measurement results show that the chip has a peak bandwidth of 6.4GB/s and row-cycle time (t_{RC}) of 9.6ns with a 1.6V supply.

8.2 A 2Gb/s/pin 512Mb Graphics DRAM with Noise-Reduction Techniques

9:00 AM

M. Brox¹, H. Fibranz¹, M. Kuzmenka¹, F. Lu¹, S. Manr², M. Markert¹, U. Möller¹, M. Plan¹, P. Schmölz¹, P. Schrögmeier¹, A. Täuber¹, B. Weber¹, P. Mayer¹, W. Spirk¹, H. Steffens¹, J. Weller¹

¹Infineon, Munich, Germany

²Infineon, Cary, NC

A 512Mb DRAM operates up to a data-rate of 2Gb/s/pin. It employs an averaging pad-driver design which reduces simultaneous switching noise to one third of a conventional design. Resistive damping elements eliminate the level degradation of the receivers caused by an oscillation of the on-chip ground. A technique for cancelling line-to-line coupling noise is also described.

8.3 A 2.5Gb/s/pin 256Mb GDDR3 SDRAM with Series Pipelined CAS Latency Control and Dual-Loop Digital DLL

9:30 AM

D. Lee, H. Lee, K. Kwean, Y. Choi, H. Moon, S. Kwack, S. Kang, K. Kim, Y. Kim, Y. Choi, J. Kih

Hynix Semiconductor, Icheon, Korea

A series pipelined CAS latency control with voltage-controlled delay line that extends maximum data rate to 2.5Gb/s/pin at 1.7V, is presented. Other schemes applied in the DLL are dual loop control that increases power noise immunity and LPDCC that achieves low power consumption. All these schemes are implemented in a 8Mx32 device using a 0.10 μ m DRAM process.

8.4 An 8.4ns Column-Access 1.3Gb/s/pin DDR3 SDRAM with an 8:4 Multiplexed Data-Transfer Scheme

10:00 AM

H. Fujisawa¹, S. Kubouchi², K. Kuroki¹, N. Nishioka¹, Y. Riho¹, H. Noda¹, I. Fujii², H. Yokoi², R. Takishita², T. Ito², H. Tanaka², M. Nakamura¹

¹Elpida Memory, Sagamihara, Japan

²Hitachi, Kokubunji, Japan

The column access time of a 512Mb DDR3 SDRAM implemented in a 90nm dual-gate CMOS process is reduced by 2.9ns to 8.4ns through an 8:4 multiplexed data-transfer scheme that enables the use of shielded I/O lines. A dual-clock additive latency counter enables a 30% reduction in cycle time from 1.7 to 1.2ns. By combining these with a multiple on-die-termination merged output driver, 1.3Gb/s/pin operation at 1.36V and a column latency of 6 (CL6) is achieved.

Break 10:30 AM

8.5 A 65nm Low-Power Embedded DRAM with Extended Data-Retention Sleep Mode

10:45 AM

T. Nagai, M. Wada, H. Iwai, M. Kaku, A. Suzuki, T. Takai, N. Itoga, T. Miyazaki, H. Takenaka, T. Hojo, S. Miyano

Toshiba, Kawasaki, Japan

An extended data retention (EDR) sleep mode with ECC and MT-CMOS is proposed for embedded DRAM power reduction. In sleep mode, the retention time improves by 8 times and the leakage current is reduced to 13% of the normal operation mode. Since ECC scrubbing operates only in the EDR sleep mode, read/write performance is not degraded. A 65nm low-power embedded DRAM macro featuring 400MHz operation and 0.39mW of data-retention power is realized.

8.6 TCAM for IP-Address Lookup Using Tree-Style AND-type Match Lines and Segmented Search Lines

11:15 AM

J-S. Wang, C-C. Wang, C. Yeh

National Chung Cheng University, ChiaYi, Taiwan

Tree-style AND-type match-line and segmented search-line schemes cooperatively improve TCAM speed and energy efficiency for applications like IP-address lookup in a network router. Fabricated in a 0.13 μ m process, the TCAM achieves 1.10ns search time with 0.348fJ/b/search.

8.7 A Storage- and Power-Efficient Range-Matching TCAM for Packet Classification

11:45 AM

Y-D. Kim, H-S. Ahn, J-Y. Park, S. Kim, D-K. Jeong

Seoul National University, Seoul, Korea

A range-matching TCAM using the proposed range-matching cell increases storage efficiency by up to 2.5 times compared to a conventional TCAM. In addition, charge recycling with the proposed static TCAM cell can reduce the search-line power. The 512 \times 144b prototype chip, fabricated in a 1.2V 0.13 μ m CMOS process, achieves a 4.8ns search time at 0.59fJ/b/search.

Conclusion 12:15 AM

DISPLAY DRIVERS

Chair: Oh-Kyong Kwon, Hanyang University, Seoul, Korea
Associate Chair: Tieman Zhao, Reflectivity, Sunnyvale, CA

9.1 A 250 μ W 0.042mm² 2MS/s 9b DAC for Liquid Crystal Display Drivers
8:30 AM

I. Knausz¹, R. Bowmar²

¹National Semiconductor, Pittsford, NY

²Rochester Institute of Technology, Rochester, NY

The architecture and design methods are presented for implementing N-bit DACs optimized for small-format LCD column drivers. Individual 9b DACs in a 12-channel QVGA display system occupies a die area of 0.042mm². It represents a composite DAC performance of better than 0.60pJ/b/mm².

9.2 A Current Driver IC Using a S/H for QVGA Full-Color Active-Matrix Organic LED Mobile Displays
9:00 AM

J-H. Baek, J-H. Lee, H-S. Pae, C-J. Lee, J-S. Kim, M. Lee, J-T. Kim, C-S. Choi, H-K. Kim, T-J. Kim, H-K. Chung

Samsung, Yongin-City, Korea

A current driver with 720 outputs for active-matrix organic LEDs uses a current-copier scheme to produce 64 gray levels with maximum 2% error from 10nA to 10 μ A on a 19.2x17.8mm² die.

9.3 Panel-Sized TFT-LCD Column Driver
9:30 AM

O. Ishibashi, M. Iriguchi, K. Kimura, J. Ishii, D. Sasaki, H. Imai, H. Tsuchi, H. Hayama

NEC, Sagamihara, Japan

Panel-sized TFT-LCD column drivers have been fabricated on a glass substrate with TFT CMOS and low-resistivity copper-plated interconnections. These operate with a 16.25MHz internal clock, have 6b DACs, 6b accuracy with either 3072 or 1536 outputs, and use an offset-controlled amplifier. The operation of 15 inch XGA LCDs is demonstrated using panel-sized column drivers.

Break 10:00 AM

MM-WAVE AND BEYOND

Chair: Ali Hajimiri, California Institute of Technology, Pasadena, CA
Associate Chair: Hiroyuki Sakai, Matsushita Electric, Osaka, Japan

10.1 A 77GHz 4-Element Phased-Array Receiver with On-Chip Dipole Antennas in Silicon 10:15 AM

A. Babakhani, X. Guan, A. Hajimiri

California Institute of Technology, Pasadena, CA

On-chip antennas are used in a fully integrated phased-array receiver at 77GHz. The complete down-conversion, power-combining, and phase-generation functions are integrated in silicon with no external mm-wave electrical connections. Each of the 4 receiver elements has 41dB of gain with a NF of 8dB with a system BW of 3GHz.

10.2 A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon 10:45 AM

A. Natarajan, A. Komijani, A. Hajimiri

California Institute of Technology, Pasadena, CA

A fully integrated 77GHz 4-element phased-array transmitter in 0.12 μ m SiGe BiCMOS based on a continuous local phase shifting approach is presented. Each element generates +10.1dBm output power at 77GHz and has 34dB gain from baseband to RF with a bandwidth of 2.2GHz. The chip demonstrates successful beam-steering at 77GHz.

10.3 A 60GHz Receiver and Transmitter Chipset for Broadband Communications in Silicon 11:15 AM

B. Floyd, S. Reynolds, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes

IBM Research, Yorktown Heights, NY

An integrated SiGe superheterodyne RX/TX pair capable of Gb/s data rates in the 60GHz band is described. The 6dB NF RX includes an image-reject LNA, a multistage down-converter with on-chip IF filters, a frequency tripler, a PLL, and baseband outputs. The 10 to 12dBm P_{1dB} TX achieves 10% PAE in the final stage. It includes a PA, image-reject driver, multistage up-converter with on-chip filters, tripler, and PLL.

10.4 A 60GHz Transmitter with Integrated Antenna in 0.18 μ m SiGe BiCMOS Technology 11:45 AM

C-H. Wang¹, Y-H. Cho¹, C-S. Lin¹, H. Wang¹, C-H. Chen¹, D-C. Niu², J. Yeh², C-Y. Lee³, J. Cherr³

¹National Taiwan University, Taipei, Taiwan

²Chung-Shan Institute of Science and Technology, Tao-Yuan, Taiwan

³TSMC, Hsin-Chu, Taiwan

A 60GHz SiGe HBT transmitter IC with integrated antenna in a standard-bulk 0.18 μ m SiGe BiCMOS process is reported. This chip is composed of a VCO, a sub-harmonic mixer, a PA, and a tapered-slot antenna, all with differential designs. The measured results show 15.8dBm output power and 20.2dB conversion gain with 281mW dc power consumption.

10.5 A 10b 10GHz Digitally Controlled LC Oscillator in 65nm CMOS 12:00 PM

N. Da Dal¹, C. Kropf¹, M. Burian¹, T. Hartig¹, H. Euf²

¹Infineon, Villach, Austria

²Infineon, Munich, Germany

A digitally controlled LC oscillator (DCO) is integrated in a digital 65nm CMOS technology. The frequency can be fine tuned with 10b from 9.87 to 10.92GHz (10%) with a frequency step of 1.03MHz/LSB. The DCO draws 3.0mA from a 1.1V supply and achieves a phase noise of -102dBc/Hz at 1MHz offset (FOM=-177.2dBc/Hz).

Conclusion

12:15 PM

SESSION 11

RF BUILDING BLOCKS AND PLLs

Chair: Bram Nauta, University of Twente, Enschede, The Netherlands

Associate Chair: Marc Tiebout, Infineon, Munich, Germany

11.1 An 18mW 90-to-770MHz Synthesizer with Agile Auto-Tuning for Digital TV Tuners

8:30 AM

M. Marutani, H. Anbutsu, M. Kondo, N. Shirai, H. Yamazaki, Y. Watanabe
Fujitsu, Kawasaki, Japan

An 18mW 90-to-770MHz I/Q synthesizer is fabricated in a 1.2V 0.11 μ m CMOS process. The architecture is optimized to achieve low power and wide tuning range. A divide-by-3.5 7b VCO with an agile auto-tuning block is included. Phase noise is <-100 dBc/Hz at 100kHz offset.

11.2 A 2.3GHz LC-Tank CMOS VCO with Optimal Phase Noise Performance

9:00 AM

P. Andreani¹, A. Fard²

¹Technical University of Denmark, Lyngby, Denmark

²Mälardalen University, Västerås, Sweden

The phase-noise theory and design of a differential CMOS LC-tank VCO with double switch pair is presented. A formula for the minimum achievable phase noise in the $1/f^2$ region is derived. The 2.15 to 2.35GHz 0.3 μ m CMOS VCO has a phase noise of -143.9dBc/Hz at 3MHz offset and draws 4mA from a 2.5V supply.

11.3 A Phase-Noise Reduction Technique for Quadrature LC-VCO with Phase-to-Amplitude Noise Conversion

9:30 AM

C-W. Yao, A. Willson

University of California, Los Angeles, CA

A phase-noise reduction technique for quadrature VCOs reduces and shapes the transistor thermal noise injected into the system, and also provides a phase-to-amplitude noise conversion mechanism to further reduce phase noise. Two experimental designs provide 17% and 1% tuning ranges centered at 5.1GHz and 5.3GHz with phase noise of -132.6dBc/Hz and -134.4dBc/Hz at a 1MHz offset, respectively.

11.4 A 1V 17GHz 5mW CMOS QVCO Based on Transformer Coupling

9:45 AM

W. Ng, H. Luong

The Hong Kong University of Science and Technology, Hong Kong, China

A 1V 17GHz 5mW QVCO is designed using transformer coupling for high frequency, low voltage and low phase noise. Implemented in 0.18 μ m CMOS, the 0.37mm² chip achieves a tuning range of 16.5% at 17GHz, a phase noise of -110dBc/Hz at 1MHz offset while using 5mA from a 1V supply, resulting in a FOM of 187.6dB.

Break 10:00 AM

11.5 A 5GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications

10:15 AM

J-H. Zhan, T. Stewart

Intel, Hillsboro, OR

A 5GHz broadband LNA achieves 25dB gain, 2dB NF, -14dBm IIP3 and -13dB S11 while drawing 15.5mA from a 2.7V supply. The circuit is fabricated in an RF-enhanced 90nm CMOS technology. The active die area is 0.025mm².

11.6 A 3 to 5GHz CMOS UWB LNA with Input Matching Using Miller Effect**10:30 AM***H.-J. Lee¹, D. Ha¹, S. Chof²*¹Virginia Institute of Technology, Blacksburg, VA²Electronics and Telecommunications Research Institute, Daejeon, Korea

A UWB CMOS LNA uses the Miller effect with one additional inductor to achieve a broadband input match. The LNA has a power gain >15dB, $S_{11} < -10.5$ dB, $S_{22} < -13.1$ dB and $NF < 2.3$ dB over the 3 to 5GHz range. It is fabricated in 0.18 μ m CMOS and draws 6.4mA from a 1.8V supply.

11.7 A Fast-Settling PLL Frequency Synthesizer with Direct Frequency Presetting**10:45 AM***X. Kuang, N. Wu*

Chinese Academy of Sciences, Beijing, China

A PLL frequency synthesizer with frequency presetting is implemented in a 0.35 μ m CMOS process and occupies 0.4mm². The output frequency is between 560 and 820MHz, the supply is 3.3V, the measured settling time is <10 μ s and the phase noise is -85dBc/Hz at 10kHz offset. The synthesizer can automatically compensate for frequency variation with temperature.

11.8 An Electrical Funnel: a Broadband Signal Combining Method**11:15 AM***E. Afshari¹, H. Bhat², X. Li³, A. Hajimiri¹*¹California Institute of Technology, Pasadena, CA²Columbia University, New York, NY³Harvard University, Cambridge, MA

A non-uniform 2D propagation medium is compatible with modern IC processes and is used to produce a 4-to-1 broadband power combiner called an electrical funnel. The combiner is used in a wideband power amplifier in a 0.13 μ m SiGe BiCMOS process and yields 125mW peak output power at 85GHz with a 24GHz 3dB bandwidth.

11.9 A Single-Chip CMOS Power Amplifier for 2.4 GHz WLAN**11:45 AM***J. Kang¹, A. Hajimiri², B. Kim¹*¹Pohang University of Science and Technology, Pohang, Korea²California Institute of Technology, Pasadena, CA

A single-chip linear CMOS PA for OFDM WLAN applications adopts a fully differential topology with transformer-type output matching and operates from a 3.3V supply. All of the components, including the input balun and output transformer, are integrated on a single 0.18 μ m CMOS die and no off-chip component is required.

11.10 A UMTS-Compliant Fully Digitally Controlled Oscillator with 100MHz Fine Tuning Range in 0.13 μ m CMOS**12:00 PM***T. Pittorino¹, Y. Cherf², V. Neubauer³, T. Mayer¹, L. Maurel³*¹University of Linz, Linz, Austria²Linz Center of Mechatronics, Linz, Austria³Danube Integrated Circuit Engineering, Linz, Austria

A 0.13 μ m CMOS fully digitally controlled oscillator is presented. Running at 2GHz, it draws 3.2mA from a 2.5V supply and has a phase noise of -118dBc/Hz at 1MHz offset, as required for UMTS oscillators. A tuning range from 3.45 to 4.45GHz is achieved by using binary-weighted and thermometer-coded switchable capacitors, which allow a maximum frequency step of 200kHz.

Conclusion**12:15 PM**

SESSION 12

NYQUIST ADCs

Chair: Venu Gopinathan, Texas Instruments, Bangalore, India
Associate Chair: Aaron Buchwald, Mobius Semiconductor, Irvine, CA

12.1 A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step

8:30 AM

G. Geelen, E. Paulus, D. Simanjuntak, H. Pastoor, R. Verlinden
Philips, Eindhoven, The Netherlands

A 10b pipelined ADC with programmable speed and power achieves a power efficiency of 0.5pJ/conversion-step for sampling frequencies between 25 and 100MHz. Measurements show an ENOB of 9.3b, ERBW exceeding 100MHz, and THD<-65dB with a supply voltage of 1.2V. Chip area is 0.3mm² in a 90nm digital CMOS process.

12.2 A 10b 50MS/s Pipelined ADC with Opamp Current Reuse

9:00 AM

S-T. Ryu¹, B-S. Song¹, K. Bacrania²
¹University of California, San Diego, La Jolla, CA
²Conexant, Palm Bay, FL

Power-saving techniques such as opamp current reuse and capacitive level shift reduce the power consumption of a 10b pipelined ADC to 220μW/MHz. A 50MS/s prototype in 0.18μm CMOS consumes 18mW (11mW for analog) at 1.8V and occupies 1.1×1.3mm². The measured ENOB of the ADC is 9.2b (8.8b) for a 1MHz (20MHz) input.

12.3 A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS

9:30 AM

Y. Shimizu, S. Murayama, K. Kudoh, H. Yatsuda, A. Ogawa
Sony, Nagasaki, Japan

A 12b 40MS/s 2-step subranging ADC is realized in a 90nm digital CMOS process. It uses a 7b coarse quantizer with a high-gain offset-canceling positive-feedback amplifier. ENOB is 10.2b at a 0.7V supply and 11.0b at a 1.0V supply. The ADC consumes 30mW at 40MS/s.

Break 10:00 AM

12.4 Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies

10:15 AM

T. Sepke¹, J. Fiorenza¹, C. Sodin¹, P. Holloway², H-S. Lee¹
¹MIT, Cambridge, MA; ²National Semiconductor, Salem, NH

A comparator-based switched-capacitor (CBSC) design method for sampled-data systems utilizes topologies similar to traditional opamp-based methods but relies on the detection of the virtual ground using a comparator instead of forcing it with feedback. A prototype 10b CBSC 1.5b/stage pipelined ADC is implemented in a 0.18μm CMOS process. The converter operates at 8MHz and consumes 2.5mW.

12.5 A 25 μ W 100kS/s 12b ADC for Wireless Micro-Sensor Applications **10:45 AM***N. Verma, A. Chandrakasan*

Massachusetts Institute of Technology, Cambridge, MA

A 0.18 μ m CMOS 12b 100kS/s successive approximation ADC is presented. The entire ADC consumes 25 μ W from a 1V supply and achieves an SNDR of 65dB. Its sampling rate can be scaled, yielding linear power savings. Efficiency of the comparator is increased by an offset compensating latch, while noise performance and common-mode rejection are improved by a modified capacitor network.

12.6 A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13 μ m CMOS **11:15 AM***P. Bogner¹, F. Kuttner¹, C. Kropf¹, T. Hartig¹, M. Burian¹, H. Euf²*¹Infineon, Villach, Austria; ²Infineon, Munich, Germany

A 14b multi-bit-per-stage pipelined ADC is implemented in a 0.13 μ m digital CMOS process. The gain and matching errors of the analog circuitry are compensated by a digital calibration scheme that allows the usage of a low-gain op-amp. A low power consumption has been reached by introducing a charge compensation scheme.

12.7 A 15mW 0.2mm² 10b 50MS/s ADC with Wide Input Range **11:45 AM***H-C. Choi, J-H. Kim, S-M. Yoo, K-J. Lee, T-H. Oh, M-J. Seo, J-W. Kim*

Samsung, Yongin-City, Korea

A 10b 50MS/s pipelined ADC, implemented in a 0.13 μ m CMOS process, consumes of 15mW and occupies an active die area of 0.2mm². In the prototype ADC, a high-to-low analog level-shifting SHA is proposed to deal with a wide input range of 2V_{pp} differential. A PVT-insensitive bias generator is employed for low voltage operation. The measured DNL and INL are ± 0.17 LSB and ± 0.16 LSB, respectively.

12.8 A 13b Linear 40MS/s Pipelined ADC with Self-Configured Capacitor Matching **12:00 PM***S. Ray, B-S. Song*

University of California, San Diego, La Jolla, CA

Using statistical matching properties of capacitor arrays, a pipelined ADC self-configures the MDAC capacitor array for best matching from many trial combinations. A 0.18 μ m CMOS prototype achieves 13b linearity and over 80dB SFDR at 43MS/s. The chip consumes 268mW from a 1.8V supply and occupies 3.6mm².

Conclusion**12:15 PM**

SESSION 13

OPTICAL COMMUNICATION

Chair: Larry DeVito, Analog Devices, Wilmington, MA
Associate Chair: Sung Min Park, Ewha Womans University, Korea

13.1 A 9.95 to 11.1Gb/s XFP Transceiver in 0.13 μ m CMOS

8:30 AM

J. Kenney¹, D. Dalton², M. Eskiyerli³, E. Evans⁴, B. Hilton⁵, D. Hitchcox⁴, T. Kwok², D. Mulcahy⁵, C. McQuilkin⁵, V. Reddy⁴, S. Selvanayagam⁴, P. Shepherd⁴, W. Titus⁴, L. DeVito⁵

¹Analog Devices, Somerset, NJ

²Analog Devices, Limerick, Ireland

³Cambridge Silicon Radio, Cambridge, United Kingdom

⁴Analog Devices, Newbury, United Kingdom

⁵Analog Devices, Wilmington, MA

A 9.95 to 11.1Gb/s transceiver in 0.13 μ m CMOS for XFP modules is presented. The CDR uses a dual-loop DLL/PLL to exceed SONET jitter specifications. A half-rate binary phase detector with a 2:1 serializer implements full-rate I/O. Dispersion jitter from 9.5 inches of FR4 is equalized resulting in random jitter(rms) under 4mUI. Power consumption is 800mW.

13.2 An MLSE Receiver for Electronic-Dispersion Compensation of OC-192 Fiber Links

9:00 AM

H-M. Bae¹, J. Ashbrook¹, J. Park¹, N. Shanbhag², A. Singer², S. Chopra²

¹Intersymbol Communications, Champaign, IL

²University of Illinois, Urbana-Champaign, IL

A 9.953 to 12.5Gb/s MLSE receiver consisting of an AFE IC in a 0.18 μ m 3.3V $f_t=75$ GHz, and a digital IC in a 0.13 μ m 1.2V CMOS is presented. The AFE IC features a 7.5GHz 40dB VGA, a 4b 12.5GS/s ADC, a dispersion-tolerant clock-recovery unit, and a 1:8 DEMUX. The digital IC implements an 8-parallel, delayed recursion MLSE architecture and a non-linear channel estimator. The 4.5W receiver meets the SONET jitter specifications with 2200ps/nm of dispersion at BER=10⁻⁴.

13.3 A Monolithic Low-Bandwidth Jitter-Cleaning PLL with Hitless Switching for SONET/SDH Clock Generation

9:30 AM

D. Wei¹, Y. Huang¹, B. Garlepp², J. Heir¹

¹Silicon Laboratories, Austin, TX

²Rambus, Los Altos, CA

A single-chip jitter-cleaning PLL with hitless switching is presented. By utilizing the mostly-digital phase build-out technique, the steady-state output phase step after switching is bounded within 200ps.. At the loop bandwidth of 800Hz, the maximum output phase transient slope is <4.5ns/ms. The jitter generation is 0.8ps in the OC48 band and 0.4ps in OC192 band. The 16.32mm² chip is fabricated in a 0.25 μ m standard CMOS process and consumes 350mW at 3.3V.

Break 10:00 AM

13.4 A 24mW 1.25Gb/s 13k Transimpedance Amplifier Using Active Compensation

10:15 AM

C-M. Tsai¹, L-R. Huang²

¹National Chiao Tung University, Hsinchu, Taiwan

²Industrial Technology Research Institute, Hsinchu, Taiwan

A transimpedance amplifier using active compensation is demonstrated to achieve 3x bandwidth enhancement in a 0.35 μ m CMOS technology. At a BER of 10⁻¹², the measured dynamic range is -29.5 to 0dBm at 1.25Gb/s. The differential transimpedance gain is adjustable from 500 to 13k . The IC consumes 24mW from a 3V supply.

13.5 11Gb/s Monolithically Integrated Silicon Optical Receiver for 850nm Wavelength**10:30 AM***R. Swoboda¹, H. Zimmermann²*¹A3PICs, Vienna, Austria²Vienna University of Technology, Vienna, Austria

A monolithically integrated optical receiver is realized in a modified silicon 0.5 μ m BiCMOS process with $f_T=25$ GHz that contains a pin photodiode. At a wavelength of 850nm, a BER of 10^{-9} , a PRBS of $2^{31}-1$, the receiver has sensitivities of -10.8dBm, -10.1dBm, and -8.9dBm for data rates of 8Gb/s, 10Gb/s, and 11Gb/s, respectively.

13.6 A 10Gb/s Burst-Mode/Continuous-Mode Laser Driver with Current-Mode Extinction-Ratio Compensation Circuit**10:45 AM***D-U. Li, C-M. Tsai*

Industrial Technology Research Institute, Hsinchu, Taiwan

A burst/continuous-mode laser driver for 10Gb/s Ethernet PONs is implemented in a 0.18 μ m CMOS process. With a dual-loop current-mode control circuit, the driver automatically compensates the extinction ratio of the laser output. Under burst-mode operation, the laser turn on/off time is <3ns.

13.7 A 10Gb/s Photonic Modulator and WDM MUX/DEMUX Integrated with Electronics in 0.13 μ m SOI CMOS**11:15 AM***A. Huang, G. Li, Y. Liang, S. Mirsaidi, A. Narasimha, T. Pinguet, C. Gunn*

Luxtera, Carlsbad, CA

Monolithic integration of both photonic and electronic components operating at 10Gb/s in a 0.13 μ m SOI CMOS process for PowerPC processors is presented. A modulator uses free carrier plasma dispersion in a reverse-biased PIN optical phase shifter in a Mach-Zender interferometer. An AWG demultiplexer uses a forward-biased PIN phase shifter to compensate the optical path length improving the channel separation.

13.8 An Integrated VCSEL Driver for 10Gb Ethernet in 0.13 μ m CMOS**11:45 AM***S. Rabii, P. Chau, J. Dao, A. Feldman, H-J. Liaw, M. Loinaz, M. Luschas, A. Salleh, S. Sheth, S. Sidiropoulos, D. Stark, S. Verma*

Aeluros, Mountain View, CA

A 10.3Gb/s VCSEL driver is integrated with a complete Ethernet transceiver in a standard 0.13 μ m CMOS process. When driving a VCSEL differentially, the resulting optical eye exceeds the 10Gb/s Ethernet mask by 35%. Intended for short-reach applications, the driver dissipates 85mW from 1.2V and occupies 0.15mm².

13.9 A 10Gb/s Burst-Mode Adaptive Gain Select Limiting Amplifier in 0.13 μ m CMOS**12:00 PM***M. Nogawa¹, Y. Ohtomo¹, S. Kimura², K. Nishimura¹, T. Kawamura¹, M. Togashi¹*¹NTT, Atsugi, Japan²NTT, Chiba, Japan

A 10Gb/s burst-mode limiting amplifier is developed in a 0.13 μ m CMOS process. An adaptive gain-selection technique achieves a settling time of 0.8ns and a wide input dynamic range of 28dB, which is five-times wider than that of previous work at 10Gb/s.

Conclusion**12:15 PM**

SESSION 14

BASEBAND AND CHANNEL PROCESSING

Chair: K. Lawrence Loh, MediaTek, Hsinchu City, Taiwan

Associate Chair: Steffen Paul, Infineon, Munich, Germany

14.1 A 90nm CMOS Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380MHz ARM9 Core and Mixed-Signal Extensions

8:30 AM

T. Lüftner¹, J. Berthold¹, C. Pacha¹, G. Georgakos¹, G. Sauzon¹, O. Hömke¹, J. Beshena², P. Mahrla¹, K. Just¹, P. Hober¹, S. Henzler³, D. Schmitt-Landsiedel⁴, A. Yakovleff⁵, A. Klein¹, R. Knight⁵, P. Acharya¹, A. Bonnardot¹, M. Sauer¹

¹Infineon, Munich, Germany; ²Infineon, Xian, China

³Technical University of Munich, Munich, Germany

⁴Infineon, Sophia-Antipolis, France; ⁵Infineon, Bristol, United Kingdom

A 43.56mm² GSM/EDGE baseband processor in 90nm triple-well CMOS has multimedia and mixed-signal extensions, including a 16b HiFi audio front end. The ARM9 core with thin-gate devices reaches 380MHz operation at 470μW/MHz. Frequency and voltage scaling reduce active power in slow mode by 40% and there are nine independent power domains.

14.2 All-Digital Spread Spectrum Clock Generator for EMI Reduction

9:00 AM

S. Damphousse, K. Ouici, A. Rizki, M. Mallinson

ESS Technology, Kelowna, Canada

An all-digital spread spectrum clock generator is presented. A digital delay matrix (DDM) is used to adjust the delay on a clock, modulating the output and producing an up or down spread. The DDM delay is no longer than one period of the clock. Measured peak clock power reduction is greater than 13dB. The circuit occupies 0.06mm² in a 0.15μm CMOS process and consumes 7.1mW.

14.3 A 630MHz Direct Digital Frequency Synthesizer with 90dB SFDR in 0.25μm CMOS

9:30 AM

D. De Caro, N. Petra, A. Strollo

University of Naples, Naples, Italy

Multipartite table methods are used in the implementation of a direct digital frequency synthesizer. Two quadrature 13b outputs are produced with a SFDR >90dB and a frequency resolution of 0.15Hz at a 630MHz clock frequency. The 0.25μm CMOS chip occupies 0.063mm² and dissipates 76mW from a 2.5V supply at 630MHz.

14.4 A 380MHz 150mW Direct Digital Synthesizer/Mixer in 0.25μm CMOS

9:45 AM

D. De Caro, N. Petra, A. Strollo

University of Naples, Naples, Italy

A direct digital frequency synthesizer/mixer IC processes two 12b quadrature inputs by providing two quadrature 13b outputs with a SFDR greater than 90dB and a frequency resolution of 0.088Hz at 380MHz clock frequency. The IC has an area of 0.22mm² in 0.25μm CMOS and dissipates 150mW at 380MHz with a supply of 2.5V. At 1.8V, the power dissipation is 53mW at 270MHz.

Break 10:00 AM

14.5 A DSSS UWB Digital PHY/MAC Transceiver for Wireless Ad-Hoc Mesh Networks with Distributed Control**10:15 AM**

A. Koyama, H. Iwami, Y. Mizoguchi, S. Tashiro, F. Nishiyama, T. Yamagata, Y. Hashimoto, M. Takada, K. Watanabe, J. Iwasaki, M. Suzuki
Sony, Tokyo, Japan

A DSSS UWB digital PHY/MAC transceiver with distributed control has been developed. This chip provides fast acquisition within 8 μ s and \pm 7.5cm ranging accuracy, as well as distributed wireless access control of up to 64 terminals and a power save control function. Die area is 12.2mm² in a 0.13 μ m CMOS process. The maximum power dissipation of the core is 181mW at 1.2V.

14.6 A 1.8V 250mW COFDM Baseband Receiver for DVB-T/H Applications**10:45 AM**

L-F. Chen, Y. Chen, L-C. Chien, Y-H. Ma, C-H. Lee, Y-W. Lin, C-C. Lin, H-Y. Liu, T-Y. Hsu, C-Y. Lee
National Chiao Tung University, Hsinchu, Taiwan

A DVB-T/H baseband receiver with multi-stage power control, 2D linear channel equalizer, synchronizer, 2/4/8k-point FFT, and Viterbi/RS decoder is implemented in 0.18 μ m CMOS. At the highest data rate of 31.67Mb/s, it overcomes 70Hz Doppler frequency and consumes 250mW with a die size of 6.9 \times 5.8mm².

14.7 A 0.13 μ m CMOS SoC for All-Format Blue and Red Laser DVD Front-End Digital Signal Processing**11:15 AM**

M. Bathaee, H. Ghezelayagh, D. Nicolae, W. Heng, O. Fratu, R. Pop, G. Dilimot, V. Feies, P. Agache, R. Ruscu, M. Lorgulescu, W. Lin, M. Lei, J. Gang, D. Hui, W. Tao
Atmel, San Jose, CA

This paper presents an all-format DVD SoC front-end DSP capable of 550Mb/s for HD-DVD, Blu-ray disc and DVD/CD red laser rewritable standards. This chip includes an analog front-end, PRML read channel, disc controller, servo system and dual processor. The analog blocks contain 640k transistors, and the digital blocks consist of 2.3M gates with a die area of 62mm².

14.8 Fully Integrated CMOS SoC for 56/18/16xS Multi-format CD/DVD Applications with On-Chip 4-LVDS Channel WSG and 1.5Gb/s SATA PHY**11:45 AM**

J-S. Pan, A. Ho, T-H. Hsu, H-C. Chen, B-Y. Hsieh, H-C. Chen, Y-C. Liu, M-H. Lin, C-C. Hsiao, W-H. Tu, C-H. Chu, L. Huang, R. Lee, C. Liu, C-Y. Lin, C-L. Wu, C-M. Chang, J-W. Chen, C-H. Chou, S-P. Chen, B. Liu, H-S. Hsu, K-H. Chao, S-H. Chou, C-P. Ma, Y. Cheng, S-N. Tsai, J-N. Yang, S. Chien, K-H. Hsieh, K-J. Chang, Y-S. Weng, M-S. Tsai, H-C. Peng
MediaTek, Hsin-Chu City, Taiwan

Multi-format CD/DVD SoC, integrating an RF/AFE and a 1.5Gb/s SATA PHY, is presented. It supports a 471Mb/s 18x DVD. A partial parity mode reduces SDRAM bandwidth and a power control mode minimizes the system clock rate. The 0.18 μ m CMOS SoC has 10M transistors, occupies 5.4 \times 5.1mm², and consumes 772mW during a 16x DVD read.

Conclusion**12:15 PM**

SESSION 15

ORGANIC DEVICES AND CIRCUITS

Chair: Bill Bidermann, BK Associates, Los Gatos, CA

Associate Chair: Koji Kotani, Tohoku University, Sendai, Japan

15.1 Printable Electronics for Polymer RFID Applications

8:30 AM

M. Böhm¹, W. Fix¹, W. Glauer²

¹PolyIC, Erlangen, Germany; ²LRS - Univ. Erlangen-Nbg., Erlangen, Germany

An organic RF identification transponder operating at a carrier frequency of 13.56MHz is presented in a proof of concept IC with no ID. The rectifier and the digital integrated modulation circuit are based on organic p-type semiconducting material with a total transponder area of 4cm². The operational distance is 0 to 4.75cm while the clock frequency is 120Hz.

15.2 A 13.56MHz RFID System based on Organic Transponders

9:00 AM

E. Cantatore¹, T. Geuns¹, A. Gruijthuijsen¹, G. Gelinck¹, S. Drews², D. de Leeuw¹

¹Philips, Eindhoven, The Netherlands

²Philips, Hamburg, Germany

RFID tags using organic transistors are described: Two 8b tags carrying different codes, energized and read out at 13.56MHz, the defacto standard for item-level ID, have been tested and demonstrated to enable multiple-object identification for the first time; A 64b tag, the most complex organic transponder reported to date, operates at 125kHz and employs 1938 transistors.

15.3 Printed Electronic Nose Vapor Sensors for Consumer Product Monitoring

9:30 AM

V. Subramanian, J. Lee, V. Liu, S. Molesa

University of California, Berkeley, Berkeley, CA

Embedded sensors based on printed organic semiconductors are attractive for use in product content monitoring due to their low cost. Arraying multiple sensor elements in a bridge topology yields signatures that achieve high specificity using non-specific elements. The output signal is amplified and digitized to detect numerous analytes with up to 10ppm sensitivity. A wine-spoilage application is demonstrated.

Break 10:00 AM

15.4 An Organic FET SRAM for Braille Sheet Display with Back Gate to Increase Static Noise Margin

10:15 AM

M. Takamiya¹, T. Sekitani¹, Y. Kato¹, H. Kawaguchi², T. Someya¹, T. Sakurai¹

¹University of Tokyo, Tokyo, Japan; ²Kobe University, Kobe, Japan

Organic FETs (OFETs) are integrated with actuators and a Braille sheet display is demonstrated. A back-gated OFET SRAM and the circuit technology for the Braille sheet display to enhance speed, yield and lifetime are presented along with essential elements for future large-area electronics made with OFETs.

15.5 Analog Signal Processing with Organic FETs**10:45 AM***N. Gay¹, W.-J. Fischer¹, M. Halik², H. Klauk², U. Zschieschang², G. Schmid²*¹Dresden University of Technology, Dresden, Germany²Infineon Technologies, Erlangen, Germany

Regular and differential amplifiers as well as differential-to-single-ended circuits based on organic FETs (OFETs) are demonstrated. A numerical OFET model suitable for analog design is developed. Unity-gain bandwidths in excess of 1.4kHz and dc-gains of 10dB are achieved.

15.6 Flexible and Glass RFIC for Cryptographic Security Applications**11:15 AM***Y. Kurokawa¹, T. Ikeda¹, H. Dembo¹, S. Iwata¹, K. Ohshima¹, J. Ishii¹, T. Tsurume¹, A. Isobe¹, S. Saito¹, K. Dairiki¹, N. Kusumoto¹, Y. Shionoiri¹, T. Atsumi¹, M. Fujita¹, H. Kobayashi¹, H. Takashina², Y. Yamashita², S. Yamazaki¹*¹Semiconductor Energy Laboratory, Kanagawa, Japan²TDK, Chiba, Japan

A flexible RFID composed of an 8b CPU as well as RF circuitry for cryptographic security applications has been developed utilizes a flexible (plastic) LSI technology by means of a glass LSI peeling and transferring technology. The CPU supports a 3.39MHz clock and contains 26k transistors, 2kB ROM, 64b SRAM and a controller with 11k transistors.

15.7 A 2 V Organic Complementary Inverter**11:45 AM***S. De Vusser^{1,2}, S. Steudel^{1,2}, K. Myny¹, J. Genoe¹, P. Heremans^{1,2}*¹IMEC, Leuven, Belgium²Katholieke Universiteit, Leuven, Belgium

A complementary organic thin-film transistor technology uses pentacene and F₁₆CuPc as the p-type and n-type materials, respectively. The semiconductors are patterned by vacuum deposition through an integrated shadow mask, while tilting the substrate. Organic complementary inverters are realized that display an almost ideal inverter curve at a supply voltage of 2V, showing a gain of 14 and a noise margin of 0.65V.

15.8 CMOS-on-Plastic Technology using Sequential Laterally Solidified Silicon Thin-Film Transistors**12:00 PM***M. Kane¹, L. Goodman¹, A. Firester¹, P. van der Wilf², A. Limanov², J. Inf²*¹Sarnoff, Princeton, NJ²Columbia University, New York, NY

CMOS circuits are directly fabricated on plastic substrates using a process with a maximum temperature of 300°C. NMOS transistors with 2µm channel lengths have unity-gain frequencies greater than 250MHz, and CMOS ring oscillators operate at 100MHz with a 15V supply.

Conclusion**12:15 PM**

SESSION 16

MEMS & SENSORS

Chair: Farrokh Ayazi, Georgia Institute of Technology, Atlanta, GA
Associate Chair: Hirofumi Sumi, Sony, Kanagawa, Japan

16.1 A 4.5mW Closed-Loop $\Delta\Sigma$ Micro-gravity CMOS-SOI Accelerometer

1:30 PM

B. Vakili Amini, R. Abdolvand, F. Ayazi
Georgia Institute of Technology, Atlanta, GA

A force-rebalanced high-order $\Delta\Sigma$ micro-g accelerometer has been fabricated in CMOS-SOI. The measured acceleration resolution is $4\mu\text{g}/\sqrt{\text{Hz}}$, which is equivalent to a capacitive resolution of 2aF with a dynamic range of 95dB at 20Hz (resolution BW=3Hz). Measured sensitivity is 5pF/g (gain of 30V/g). The IC consumes 4.5mW from a 3V supply and uses 2.25mm².

16.2 A Programmable MEMS FSK Transmitter

2:00 PM

W-T. Hsu¹, A. Brown¹, K. Cioffi²
¹Discera, Ann Arbor, MI
²Discera, San Jose, CA

An FSK transmitter is modulated by changing the polarization voltage of a micromechanical resonator. The transmitter frequency can be programmed from 2 to 437MHz with 1ppm accuracy. The transmitter has 6X greater frequency deviation than quartz-based FSK modulators, 20kb/s data rate, and total 8ppm frequency variation from -40 to 85°C.

16.3 A Self-Resonant MEMS-based Electrostatic Field Sensor with 4V/m/ $\sqrt{\text{Hz}}$ Sensitivity

2:30 PM

T. Denison^{1,2}, J. Kuang², J. Shafran^{3,4}, M. Judy², K. Lundberg^{4,5}
¹Medtronic, Fridley, MN
²Analog Devices, Cambridge, MA
³Analog Devices, San Jose, CA
⁴MIT, Cambridge, MA
⁵Keeling Flight Hardware, Weston, MA

An electric-field sensor is presented for applications such as xerography. The sensor architecture combines a vibrating MEMS structure with synchronous detection-based electronics. Prototyped in a MEMS process, the noise floor is 4.0V/m/ $\sqrt{\text{Hz}}$ and the INL is 20V/m over a range of +/-700kV/m, an order-of-magnitude improvement over existing MEMS devices.

16.4 A CMOS Interface for a Gas-Sensor Array with a 0.5% Linearity over the 500k Ω -to-1G Ω Range and $\pm 2.5^\circ\text{C}$ Temperature Control Accuracy

2:45 PM

M. Malfatti¹, D. Stoppa¹, A. Simoni¹, L. Lorenzelli¹, A. Adami¹, A. Baschirotto²
¹Center for Scientific and Technological Research, Trento, Italy
²University of Lecce, Lecce, Italy

The interface IC includes 8 read-out channels and 2 closed-loop temperature control circuits, is fabricated in 0.35 μm 2P4M CMOS and dissipates 27mW from a 3.3V supply. The read-out structure, based on a controlled oscillator, achieves a 0.5% linearity and a SNR>48dB over the 500k Ω -to-1G Ω sensor resistance range with a 114dB DR. The temperature control systems maintain a 100°C gradient in the range 100 to 400°C with $\pm 2.5^\circ\text{C}$ accuracy.

Break 3:00 PM

16.5 A CMOS Temperature-to-Frequency Converter with $\pm 0.5^\circ\text{C}$ (3σ) Inaccuracy from -40 to 105°C **3:15 PM***K. Makinwa, M. Snoeij*

Delft University of Technology, Delft, The Netherlands

A temperature-to-frequency converter implemented in a standard CMOS process only requires a low-cost batch calibration. Its output frequency is determined by the process-independent (but temperature-dependent) thermal diffusivity of bulk silicon. The converter's inaccuracy is less than $\pm 0.5^\circ\text{C}$ (3σ) over the extended industrial temperature range from -40 to 105°C .

16.6 An Integrated Magnetic Sensor with Two Continuous-Time $\Delta\Sigma$ Converters and Stress Compensation**3:45 PM***M. Motz, U. Ausserlechner, W. Scherr, B. Schaffer*

Infineon, Villach, Austria

A linear 4kHz Hall sensor in $0.6\mu\text{m}$ BiCMOS has digital 3rd-order temperature compensation, a DR of 90dB and an offset of $50\mu\text{T}$. It uses a chopped 3rd-order multibit CT- $\Delta\Sigma$ ADC including an up/down counter loop and bandgap-based compensation for stability and accuracy. Digital compensation of sensitivity drift caused by package-induced stress is provided.

16.7 A 200dB Dynamic Range Iris-less CMOS Image Sensor with Lateral Overflow Integration Capacitor using Hybrid Voltage and Current Readout Operation**4:15 PM***N. Akahane¹, R. Ryzaki¹, S. Adachi², K. Mizobuchi², S. Sugawa¹*¹Tohoku University, Sendai, Japan²Texas Instruments, Miho, Japan

A $2.6\times 2.6\text{mm}^2$ image sensor fabricated in $0.35\mu\text{m}$ 2P3M CMOS contains 64×64 pixels with $20\times 20\mu\text{m}^2$ pixel size and has an extended dynamic range of over 200dB. This DR is equivalent to the incident light ranging from about 10^{-2} to 10^8 lx with the lens iris fixed.

16.8 A Back-Illuminated High-Sensitivity Small-Pixel Color CMOS Image Sensor with Flexible Layout of Metal Wiring**4:45 PM***S. Iwabuchi, Y. Maruyama, Y. Ohgishi, M. Muramatsu, N. Karasawa, T. Hirayama*

Sony, Atsugi-shi, Japan

A 1.3Mpixel color image sensor with a back-illuminated configuration and $3.45\mu\text{m}$ square pixels is fabricated in $0.25\mu\text{m}$ 1P3M CMOS. Its sensitivity at a wavelength of 550nm is 34% better than that of a conventional device, and it falls by only 15% when the light is incident at an angle of 20 degrees. Flexibility in metal wiring layout improves device characteristics such as saturation output.

16.9 Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers**5:00 PM***B. Aull, J. Burns, C. Chen, B. Felton, H. Hanson, C. Keast, J. Knecht, A. Loomis, M. Renzi, A. Soares, V. Suntharalingam, K. Warner, D. Wolfson, D. Yost, D. Young*

MIT Lincoln Laboratory, Lexington, MA

A 64×64 laser-radar (ladar) detector array with $50\mu\text{m}$ pixel size measures the arrival times of single photons using Geiger-mode avalanche photodiodes (APD). A 3-tier structure with active devices on each tier is used with 227 transistors, six 3D vias and an APD in each pixel. A 9b pseudorandom counter in the pixel measures time. Initial imagery shows 2ns time quantization.

Conclusion**5:15 PM**

SESSION 17

RFID AND RF DIRECTIONS

Chair: Vadim Gutnik, Impinj, Newport Beach, CA
Associate Chair: Hiroyuki Mizuno, Hitachi, Tokyo, Japan

17.1 An SOI-Based 7.5 μ m-Thick 0.15 \times 0.15mm² RFID Chip

1:30 PM

M. Usami¹, A. Sato¹, H. Tanabe¹, T. Iwamatsu², S. Maegawa², Y. Ohji¹
¹Hitachi, Tokyo, Japan
²Renesas Technology, Hyogo, Japan

A 0.15 \times 0.15mm² RFID chip containing a 128b ROM is fabricated in a 0.18 μ m 4M SOI CMOS technology. It achieves 480mm read range with a 2.45GHz carrier for a reader output power of 300mW. The chip is thinned precisely by using an SOI buried oxide layer structure as an etch stop. An RFID antenna is connected to the chip by using a double-surface electrode.

17.2 A Passive UHF RFID Tag LSI with 36.6% Efficiency CMOS-Only Rectifier and Current-Mode Demodulator in 0.35 μ m FeRAM Technology

2:00 PM

H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, K. Gotoh
Fujitsu, Kawasaki, Japan

A passive UHF RFID tag LSI in 0.35 μ m CMOS with 2kb FeRAM enables the 2.9-times higher 32b read-and-write throughput over an EEPROM-based tag. A CMOS full-wave rectifier improves the power efficiency from 16.6% up to 36.6% by lossless internal V_{in} cancellation and mirror stack architecture. A current-mode ASK demodulator converts the 15% power modulation into linear current signal over a 27dB dynamic range of the incoming power.

17.3 A 3.4Mb/s RFID Front-end for Proximity Applications Based on a Delta-modulator

2:30 PM

B. Gomez, G. Masson, P. Villard, G. Robert, F. Dehmas, J. Reverdy
CEA-LETI, Grenoble, France

A 13.56MHz RFID front-end uses multi-level signaling to achieve 3.4Mb/s operation. The circuit is built around a delta-modulator loop which ensures demodulation and ADC functions as well as supply-voltage regulation. The circuits, fabricated in a 6M 0.18 μ m 1.8V digital CMOS process in an area of <0.5mm².

Break 3:00 PM

17.4 A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss, and Noise Reduction

3:15 PM

D. Huang, W. Hant, N-Y. Wang, T. Ku, Q. Gu, R. Wong, F. Chang
University of California, Los Angeles, CA

An on-chip resonator with artificial dielectric in place of the LC tank yields reduced metal/substrate losses, higher resonator Q and a $\lambda/4$ length reduction of 4.7 times. The VCO uses 90nm CMOS, with 0.015mm² area, consumes 1.9mW and has a measured phase noise of -100dBc/Hz at 1MHz offset. The FOM is -193dBc/Hz.

17.5 A 5.4GHz 0.35 μ m BiCMOS FBAR Resonator Oscillator in Above-IC technology**3:45 PM***M. Aissi¹, E. Tournier¹, M-A. Dubois², G. Paraf³, R. Planat¹*¹LAAS-CNRS, Toulouse, France²CSEM, Neuchâtel, Switzerland³CEA-LETI, Grenoble, France

A 5.4GHz 0.35 μ m BiCMOS SiGe FBAR oscillator is presented. The FBAR resonator is directly integrated above the silicon IC, thus eliminating the bond wires and associated parasitics of the classical FBAR oscillators. The oscillator achieves a phase noise of -117.7dBc/Hz at 100kHz offset from 5.46GHz carrier frequency while the oscillator core draws 1.7mA from 2.7V.

17.6 Dielectrically Transduced Single-Ended to Differential MEMS Filter**4:00 PM***D. Weinstein, H. Chandralalim, L. Cheow, S. Bhawe*

Cornell University, Ithaca, NY

A single-ended input to balanced output 425MHz mechanically coupled electromechanical filter is presented. This technology provides 1MHz channel select filtering while eliminating the need for RF switches and baluns in front-end transceivers. The filter achieves 8dB insertion loss with -50dB stop-band rejection and -48dB common-mode suppression.

17.7 A Low-Power 2.4GHz CMOS Receiver Front-End Using BAW Resonators**4:15 PM***J. Chabloz, C. Müller, F. Pengg, A. Pezous, C. Enz, M-A. Dubois*

CSEM, Neuchâtel, Switzerland

A low-power 2.4GHz heterodyne receiver front-end is integrated in 0.18 μ m CMOS using BAW solidly mounted resonators. The resonators with Qs of up to 580, provide both impedance matching and selectivity. An image rejection of up to 50dB, a NF of 11dB and IIP3 of -16.1dBm with a power dissipation of 1.8mW are demonstrated.

17.8 A Miniature V-Band 3-Stage Cascode LNA in 0.13 μ m CMOS**4:45 PM***C-M. Lo, C-S. Lin, H. Wang*

National Taiwan University, Taipei, Taiwan

A miniature V-Band (50 to 75GHz) 3-stage cascode CMOS LNA implemented in 0.13 μ m bulk CMOS technology exhibits better than 20dB measured gain from 51 to 57.5GHz in 0.46mm² die size. The minimum NF is 7.1dB at 56.8GHz. The P_{1dB} is -22dBm, the IIP3 is -12dBm, and the total current is 33mA.

Conclusion**5:00 PM**

SESSION 18

CLOCK AND DATA RECOVERY

Chair: Roger Minear, Wyomissing, PA

Associate Chair: Bob Payne, Texas Instruments, Dallas, TX

18.1 A 25Gb/s CDR in 80nm CMOS for High-Density Interconnects

1:30 PM

C. Kromer¹, G. Sialm¹, C. Menolfi², M. Schmatz², F. Ellinger¹, H. Jäckel¹

¹ETH Zürich, Zürich, Switzerland

²IBM Research, Rüschlikon, Switzerland

A CDR for source-synchronous high-density link applications receives 25Gb/s at a BER of $<10^{-12}$. The CDR is a first-order bang-bang topology employing a phase interpolator, linear half-rate phase detector, an analog filter followed by a limiter and a digital loop filter. The core CDR circuit occupies 0.09mm^2 and consumes 98mW from a 1.1V supply.

18.2 A 2.5Gb/s Multi-rate 0.25 μm CMOS CDR Utilizing a Hybrid Analog/Digital Loop Filter

2:00 PM

M. Perrot¹, Y. Huang², R. Baird³, B. Garlepp⁴, L. Zhang², J. Heir²

¹MIT, Cambridge, MA

²Silicon Laboratories, Austin, TX

³Montana State University, Bozeman, MT

⁴Rambus, Los Altos, CA

A CDR comprises a Hogge detector and a 1st-order $\Delta\Sigma$ ADC, and uses a hybrid analog/digital loop filter to enhance integration and allow bandwidth tuning over a wide range of data rates from 155Mb/s to 2.7Gb/s. The CDR exceeds SONET performance at relevant data rates and generates 1.2ps_{rms} jitter at 2.5Gb/s.

18.3 A 0.03mm² 9mW Wide-Range Duty-Cycle-Correcting False-Lock-Free DLL with Fully Balanced Charge-Pump for DDR Interface

2:30 PM

Y. Tokunaga¹, S. Sakiyama¹, S. Doshō¹, Y. Doi¹, M. Hattori²

¹Matsushita, Moriguchi, Japan

²Panasonic Semiconductor Systems and Technology Co., Ltd.

A duty-cycle-correcting false-lock-free DLL for DDR interface is proposed. A fully balanced charge-pump equalizes the charge and discharge pulses of the phase detector to reduce update noise. The DLL achieved 49% to 51% duty-cycle output from a 30% to 70% duty-cycle input clock operating from 20 to 300MHz, consumes 9mW from a 2 to 4V supply, and occupies 0.03mm^2 in a $0.30\mu\text{m}$ CMOS process.

Break 3:00 PM

18.4 Improving CDR Performance via Estimation

3:15 PM

H. Lee¹, A. Bansal¹, Y. Frans², J. Zerbé², S. Sidiropoulos³, M. Horowitz¹

¹Stanford University, Stanford, CA

²Rambus, Los Altos, CA

³Aeluros, Mountain View, CA

A dual-loop CDR can be viewed as a simple phase-estimator. Different estimators can be built by changing the phase DAC control logic. Three different $0.13\mu\text{m}$ estimators for a 3Gb/s serial link are presented. These estimators address dual-loop CDR limitations including lock time, frequency range, and jitter tolerance in non-mesochronous systems.

18.5 A 3.2Gb/s Semi-Blind-Oversampling CDR**3:45 PM***M. van Ierssel¹, A. Sheikholeslami¹, H. Tamura², W. Walker³*¹University of Toronto, Toronto, Canada²Fujitsu, Kawasaki, Japan³Fujitsu, Sunnyvale, CA

A hybrid CDR increases jitter tolerance of a phase-tracking CDR by a factor of 32 at low frequencies, while maintaining the high-frequency jitter tolerance of a 5× blind-oversampling CDR. Measurements on a 0.11μm CMOS test chip at 2.4Gb/s confirm a 200UI_{pp} jitter tolerance at 200kHz. At 2.4Gb/s, the chip consumes 180mW from a 1.2V supply.

18.6 Data Recovery and Retiming for 4.8Gb/s Fully Buffered DIMM Serial Links**4:15 PM***H. Partovi¹, W. Walthes², L. Ravezzi¹, P. Lindt², S. Chokkalingam¹, K. Gopalakrishnan¹, A. Blum²,**O. Schumacher², C. Andreottf², M. Bruenner², B. Celli-Urban², D. Friebe², I. Koref², M. Verbeck², U. Lange²*¹Infineon, San Jose, CA²Infineon, Munich, Germany

Data recovery and retiming of 4.8Gb/s fully buffered DIMM serial links are described. A 2.4GHz retiming FIFO with an integrated insertion MUX is used to minimize the thru-latency. Fabricated in a 0.13μm 1.5V CMOS technology, the chip occupies 9.2×4.5mm². Using wide-band CML techniques, the input sensitivity with a minimum eye-opening of 0.35UI, is better than 50mV_{p-p} at a BER of 10⁻¹².

18.7 A 10Gb/s CMOS CDR and DEMUX IC with a Quarter-Rate Linear Phase Detector**4:45 PM***S. Byun, J. Lee, J. Shim, K. Kim, H-K. Yu*

Electronics and Telecommunications Research Institute, Daejeon, Korea

A 10Gb/s CDR and DEMUX IC in a 0.13μm CMOS consumes 100mA from a 1.2V core supply and 205mA from a 2.5V I/O supply including 18 LVDS drivers. The CDR system uses a quarter-rate linear phase detector and a 4-phase 2.5GHz LC-QVCO to achieve a BER of <10⁻¹⁵ and a jitter tolerance of 0.5UI_{pp} exceeding the OC-192 standard.

18.8 A 20Gb/s Embedded Clock Transceiver in 90nm CMOS**5:00 PM***J. Jauss¹, B. Casper¹, M. Mansuri¹, F. O'Mahony¹, K. Canagasaby², J. Kennedy¹, R. Mooney¹*¹Intel, Hillsboro, OR²Intel, Santa Clara, CA

A 20Gb/s embedded clock transceiver in 90nm CMOS is described. The RX front-end is 4-way interleaved with a LC-VCO-based CDR. The random jitter of the recovered clock is 1.44ps_{rms}. Data transfer rates of 20Gb/s across a 2-inch link and 14.4Gb/s across a 22-inch backplane link are achieved. At 20Gb/s, the transceiver dissipates 15.9mW/Gb/s.

Conclusion**5:15 PM**

Sunday, February 5th		ISSCC 2006 TUTORIALS	
8:00 AM	T1: Introduction to Fractional-N Phase-Locked Loops T2: Data-Converter Interfaces: The Analog and Digital Ins and Outs T3: Introduction to Statistical Variation and Techniques for Design Optimization T4: Introduction to CMOS Bio-Sensors: Electrical Specifications, CMOS Processing, Circuit and System Design	T5: Multi-Level Cell Design for Flash Memory T6: Cellular-Phone Applications Trends and DSP Technology T7: 3D Integration T8: Millimeter-Wave ICs in Silicon T9: Signal Integrity for High-Speed Circuit Designers	
GIRAFE FORUM		CIRCUIT DESIGN FORUM	
8:00 AM	F1: Advanced Wireless CMOS Transceivers	F2: Embedded-SRAM Design	F3: Circuit Design in Emerging Technologies
ISSCC 2006 SPECIAL- TOPIC EVENING SESSIONS			
7:30 PM	SE1: What is Driving Displays?	SE2: Power-Aware Signal Processing	SE3: Analog Scaling
Monday, February 6th			
8:30 AM	Session 1: Plenary Session		
1:30 PM	Session 2: Biomedical Systems	Session 3: Oversampling ADCs	Session 4: Gigabit Transceivers
5:15 PM	Author Interviews; Social Hour; Poster Session (DAC Student Design Contest Winners)	Session 5: Processors	Session 6: UWB
ISSCC 2006 DISCUSSION SESSIONS			
8:00 PM	E1: Is the Digital-Circuit Designer Dead?	SE4: Emerging & Disruptive Memory Technologies	SE5: CMOS RF Design at 90nm and Beyond
SE6: Highlights of A-SSCC 2005 and the 2005 Symposium on VLSI Technology			
Tuesday, February 7th			
8:30 AM	Session 8: DRAM and TCAM	Session 9: Displays Drivers	Session 10: MM-Wave and Beyond
1:30 PM	Session 16: MEMS and Sensors	Session 17: RFID and RF Directions	Session 18: Clock and Data Recovery
5:15 PM	Author Interviews; Social Hour; Poster Session (DAC Student Design Contest Winners)	Session 11: RF Building Blocks and PLLs	Session 12: Nyquist ADCs
ISSCC 2006 PAPER SESSIONS			
8:00 PM	E2: Present (and Future) Classic Circuits with less than 25 Transistors	Session 19: Analog Techniques	Session 20: WLAN/WPAN
ISSCC 2006 DISCUSSION SESSIONS			
8:00 PM	E3: What is Next to be Off-Shored, IC Design Jobs or IC Design Futures?	SE7: Sensors on the Move	Session 14: Baseband and Channel Processing
Session 15: Organic Devices and Circuits			
Wednesday, February 8th			
8:30 AM	Session 22: Low-Power Multimedia	Session 23: Technical and Architecture Directions	Session 24: High-Performance Digital Circuits
1:30 PM	Session 26: Static Memory	Session 29: Power Management and Distribution	Session 30: Silicon for Biology
5:15 PM	Author Interviews	Session 31: Very High-Speed ADCs and DACs	Session 32: PLLs, VCOs, and Dividers
ISSCC 2006 SHORT COURSE			
8:00 AM	Analog-to-Digital Converters		
CIRCUIT DESIGN FORUM			
8:00 AM	F4: Color Imaging	ATAC FORUM	
F5: ATAC: High-Speed Interconnect			
BOOK DISPLAY			
Monday, February 6th, 12:00 PM - 6:00 PM			
Tuesday, February 6th, 10:00 AM - 6:00 PM			
Wednesday, February 7th, 10:00 AM - 3:00 PM			
F6: Multi-Core Architectures: Designs, and Implementation Challenges			
CIRCUIT DESIGN FORUM			
Session 25: RF/IF Circuits			
Session 26: Cellular Building Blocks and SOCs			
Session 27: Image Sensors			
Session 28: Wireline Building Blocks			
Session 33: Mobile TV			
Session 34: SRAM			

SESSION 19

ANALOG TECHNIQUES

Chair: Axel Thomsen, Silicon Laboratories, Austin, TX
Associate Chair: Doug Smith, SMSC, Austin, TX

19.1 A 240W Monolithic Class-D Audio Amplifier Output Stage

1:30 PM

F. Nyboe^{1,2}, C. Kaya³, L. Risbo¹, P. Andrean²

¹Texas Instruments, Lyngby, Denmark

²Ørsted*DTU, Lyngby, Denmark

³Texas Instruments, Dallas, TX

A single-channel class-D audio amplifier output stage outputs 240W unclipped into 4Ω. 0.1% open-loop THD+N allows using the device in a fully-digital audio signal path with no feedback. The output current capability is ±18A and the part is fabricated in a 0.4μm/1.8μm high-voltage BiCMOS process. Over-current sensing protects the output from short circuits.

19.2 Frequency Compensation of an SOI Bipolar-CMOS-DMOS Car Audio PA

2:00 PM

R. van der Zee¹, R. van Heeswijk²

¹University of Twente, Enschede, The Netherlands

²Philips, Nijmegen, The Netherlands

A car audio PA uses a frequency-compensation scheme that avoids large compensation capacitors while retaining the bandwidth and stable load range of nested Miller compensation. The THD is 0.005% at 1kHz and 10W output power. The SNR is 108dB and the amplifier is stable for any passive load up to 50nF. The PA is fabricated in a 1μm SOI bipolar-CMOS-DMOS process.

19.3 A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR

2:30 PM

T. Ido¹, S. Ishizuka¹, L. Risbo², F. Aoyagi¹, T. Hamasaki¹

¹Texas Instruments, Kanagawa, Japan

²Texas Instruments, Lyngby, Denmark

A digital input controller for audio class-D amplifiers is presented. The controller utilizes specially configured integrated DAC and power stage feedback loop to suppress distortion components coming from power-stage switching with digital input capability. The class-D amplifier system with the controller and an existing power stage achieves 113dB DR, 0.0018% THD+N with 10W output power, and 0.004% THD+N with 100W output power into 4Ω load.

19.4 A CMOS LDO with Inherent Stability

2:45 PM

C-L. Chen, H-I. Pan

National Taiwan University, Taipei, Taiwan

A pole-zero pair-cancellation scheme stabilizes a CMOS LDO regulator with any load capacitance. A series of pole-zero pairs are generated by appropriately splitting the pass transistor into several unequal devices in parallel. Data from an LDO regulator with $V_o=2.5V$ and $I_{o,max}=150mA$ and fabricated in a 0.5μm CMOS technology, verify the inherent system stability.

19.5 A 4.1mW 79dB DR 4th-order Source-Follower-Based Continuous-Time Filter for WLAN Receivers

3:15 PM

*S. D'Amico¹, M. Contà², A. Baschiroto¹*¹University of Lecce, Lecce, Italy²RFDomus, Irvine, CA

Using a composite source-follower with positive feedback to synthesize complex poles, a single-branch CMOS biquad achieves large linearity at low overdrive voltage, saving power. In 0.18 μ m CMOS with a 1.8V supply, a 4th-order 10MHz filter for WLAN applications achieves 17.5dBm IIP3 and -40dB HD3 for a 600mV_{pp,diff} input signal amplitude. A 24 μ V_{rms} noise gives a 79dB DR while drawing 2.25mA from 1.8V.

19.6 A Micropower Chopper-Stabilized Operational Amplifier Using an SC Notch Filter with Synchronous Integration Inside the CT Signal Path

3:45 PM

R. Burt, J. Zhang

Texas Instruments, Tucson, AZ

A micropower chopper-stabilized opamp uses an SC notch filter with synchronous integration inside the CT signal path to eliminate chopping noise. Characteristics include rail-to-rail I/O, 15 μ A supply current at 1.8 to 5.5V, 2 μ V offset, 55nV/ \sqrt Hz noise, 350kHz GBW, and a chopping frequency of 125kHz. The Die area is 0.7mm² using 0.6 μ m CMOS.

19.7 A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18 μ m SiGe Process

4:15 PM

*S. Abedinpour¹, B. Bakaloglu², S. Kiaei²*¹Freescale Semiconductor, Tempe, AZ²Arizona State University, Tempe, AZ

A fully integrated 0.18 μ m SiGe synchronous buck DC/DC converter with an on-chip LC output filter supporting a maximum output current of 200mA and efficiency of 64% is presented. The converter utilizes a 10 μ m-thick electroplated copper layer for integrated inductors and gate capacitors. High switching frequency of 45MHz, multi-phase interleaved operation, and fast hysteretic control reduces the filter inductor and capacitor sizes by two orders of magnitude enabling a fully integrated converter.

19.8 A CMOS-Control Rectifier for Discontinuous-Conduction Mode Switching DC-DC Converters

4:45 PM

T. Man, M. Chan, P. Mok

Hong Kong University of Science and Technology, Hong Kong, China

A sub-1V boost converter with a CMOS-control rectifier enables adaptive dead-time control and mV-range forward-voltage drop. This converter can operate with <0.9V input and deliver 2.5V and 250mW output with 85% efficiency and is intended for single-cell battery-powered mobile systems.

Conclusion

5:00 PM

SESSION 20

WLAN/WPAN

Chair: Arya Behzad, Broadcom, San Diego, CA

Associate Chair: Jan Craninckx, IMEC, Leuven, Belgium

20.1 A 5GHz 108Mb/s 2x2 MIMO Transceiver with Fully Integrated 16dBm PAs in 90nm CMOS

1:30 PM

Y. Palaskas¹, A. Ravi¹, S. Pellerano¹, B. Carlton¹, M. Elmala¹, R. Bishop¹, G. Banerjee¹, R. Nicholls¹, S. Ling², S. Taylor¹, K. Soumyanath¹

¹Intel, Hillsboro, OR

²Intel, Folsom, CA

A 5GHz 2x2 MIMO transceiver in 90nm CMOS supports spatial multiplexing and diversity, achieving 54/108Mb/s with -75/-63dBm sensitivity for an AWGN/25ns-Rayleigh channel, respectively. Each RX draws 120mA from a 1.4V supply. Each 3.3V 5GHz PA delivers +16/+13dBm average power with -25/-27dB EVM in 1x1/2x2 modes, respectively. The system-in-package including microstrip front-end matching on a flip-chip package occupies a die area of 18mm².

20.2 An 802.11a/b/g SoC for Embedded WLAN Applications

2:00 PM

L. Nathawad¹, D. Weber², S. Abdollah², P. Chen¹, S. Enam³, B. Kaczynski⁴, A. Kheirkhahi¹, M. Lee², S. Limotyakis¹, K. Onoder², K. Vleugels⁴, M. Zargar¹, B. Wooley⁵

¹Atheros Communications, Irvine, CA

²Atheros Communications, Santa Clara, CA

³Jaalaa, San Diego, CA

⁴H-Stream Wireless, Los Altos, CA

⁵Stanford University, Stanford, CA

An 802.11a/b/g wireless LAN SoC for low-power embedded applications is implemented in a 0.18 μ m CMOS technology. The IC integrates the RF transceiver, digital PHY and MAC, CPU and host interface. For 64QAM OFDM, the 5GHz/2.4GHz TX EVM is -27.4dB/-27.5dB at an output power of -5.2dBm/-3.5dBm. Overall 5GHz/2.4GHz RX sensitivity is -73dBm/-76dBm at 54Mb/s.

20.3 A Wireless Transceiver with Integrated Data Converters for 802.11a/b/g Access Points

2:30 PM

T. Montalvo¹, C. Angeli¹, D. McLaurin¹, C. Peterser², E. Foglemar², J. Bruntilius², P. Brown², E. Yetis², J. Bray², M. Kessler³, B. Tenbroek⁴

¹Analog Devices, Raleigh, NC

²Analog Devices, San Diego, CA

³Analog Devices, Wilmington, MA

⁴Analog Devices, Kent, United Kingdom

A transceiver for 802.11a/b/g access points supports MRC diversity resulting in a 3dB static sensitivity improvement over a single-receiver implementation. A closed-loop transmit power control scheme achieves 0.5dB accuracy. Receive ADCs and transmit DACs are included, allowing autonomous AGC and transmit power control loops and an all-digital modem/MAC IC. The 25mm² IC is fabricated in a 0.18 μ m CMOS process and achieves 3.9dB/4.5dB (low-band/high-band) receive NF and less than -35dB transmit EVM.

Break

3:00 PM

20.4 A Highly Linear Direct-Conversion Transmit Mixer Transconductance Stage with Local Oscillation Feedthrough and I/Q Imbalance Cancellation Scheme **3:15 PM**

C. Lee¹, A. Behzad¹, D. Ojo¹, M. Kappes², S. Au¹, M-A. Par³, K. Carter³, S. Tian¹

¹Broadcom, San Diego, CA

²IQ-Analog, San Diego, CA

³Broadcom, Irvine, CA

A linear transconductance stage with process insensitive gain control and gain insensitive output offset current is proposed. A calibration scheme to remove the LO feedthrough (LOFT) and I/Q imbalance is also introduced. The prototype achieves 3rd-order IMD suppression better than 52dBc, LOFT suppression better than 32dBc, and image rejection better than 46dBc for all gain settings. The transmit chain achieves an 802.11a EVM of < -40dB.

20.5 An Ultra-Low-Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 130nm CMOS with 400mV Supply and an Integrated Passive RX Front-end **3:30 PM**

B. Cook, A. Berny, A. Molnar, S. Lanzisera, K. Pister

University of California, Berkeley, CA

A 2.4GHz RF transceiver in 130nm CMOS for sensor networks is presented. The transceiver operates from 400mV to accommodate a single solar cell power supply. The RX dissipates 200 to 750 μ W and achieves a 6.7dB NF and a -6.2dBm IIP3 at 330 μ W. At 300 μ W output power, the PA is 44% efficient and the overall TX is 30% efficient.

20.6 A Fully Integrated 2.4GHz IEEE 802.15.4 compliant Transceiver for ZigBee Applications **3:45 PM**

W. Kluge, L. Dathe, H. Roller, M. Lange, M. Taenzer, T. Ferchland, F. Poegel, D. Eggert

Atmel Germany, Dresden, Germany

A 0.18 μ m CMOS low-IF transceiver with integrated baseband processing according to IEEE 802.15.4 is described. The 5.77mm² die draws 14.7mA (RX) and 15.7mA (TX) while achieving -102dBm RX sensitivity and 3dBm TX power. The differential input 2.4mA RX RF-frontend provides 5.7dB system noise figure.

20.7 A 10.8mA Single-Chip Transceiver for 430MHz Narrowband Systems in 0.15 μ m CMOS **4:15 PM**

G. Hayashi¹, A. Sawada¹, T. Morie¹, K. Matsuyama¹, R. Kim¹, S. Yoshida¹, A. Matsumoto¹, K. Hijikata, K. Matsukawa¹, Y. Tamura², J. Ogawa², T. Takita²

¹Matsushita, Osaka, Japan, ²Matsushita, Kyoto, Japan

A low-power single-chip transceiver for 430MHz narrowband systems is implemented in a 0.15 μ m CMOS process. The chip integrates all the radio blocks including filters, a demodulator, and a microcontroller. The receive current of 10.8mA and the sensitivity of -120dBm at 1% BER are achieved in 2FSK operating at 2.4kb/s. The transceiver complies with the ARIB STD-T67.

20.8 A Fully Integrated Auto-Calibrated Super-Regenerative Receiver **4:45 PM**

J-Y. Chen, M. Flynn, J. Hayes

University of Michigan, Ann Arbor, MI

A fully integrated super-regenerative receiver in 0.13 μ m CMOS with on-chip quench generation is described. Auto-calibration improves the selectivity of a Q-enhanced filter and the sensitivity of super-regeneration. The prototype consumes 2.8mW, or 5.6nJ per received bit, at 500kb/s, and has a turn-on time of 83.6 μ s, a channel spacing of 10MHz, and a sensitivity of -90dBm.

Conclusion **5:00 PM**

SESSION 21

ADVANCED CLOCKING, LOGIC AND SIGNALING TECHNIQUES

Chair: Thucydides Xanthopoulos, Cavium Networks, Marlboro, MA

Associate Chair: Sohichi Miyata, SHARP, Osaka, Japan

21.1 Free-Running Ring Frequency Synthesizer

1:30 PM

D. Allen, A. Carley

TimeLab, Andover, MA

A digital processor uses a single free-running ring oscillator to synthesize multiple clocks without analog circuits or feedback loops. Fabricated in 0.18 μ m technology, the 4mm² die integrates 6 independent spread-spectrum synthesizers with <0.1ps period resolution. The synthesizers operate from 3 to 400MHz with a jitter <85ps, meeting PCI-Xclock-jitter requirements.

21.2 Clock Generation and Distribution of a Dual-Core Xeon™ Processor with 16MB L3 Cache

2:00 PM

S. Tam, J. Leung, R. Limaye, S. Choy, S. Vora, M. Adachi

Intel, Santa Clara, CA

The clock generation and hybrid clock distribution for a dual-core Xeon™ processor with 16MB L3 cache are designed for <11ps global clock skew in a 435mm² die. The cache and control sections contain 2 primary clock domains and 11 clock spines. A pipelined de-skew logic tolerant to inter-domain clock uncertainties manages the core and cache/control data communication.

21.3 A 5GHz Duty-Cycle Correcting Clock Distribution Network for the POWER6 Microprocessor

2:30 PM

M. Thomson¹, P. Restle¹, N. James²

¹IBM, Yorktown Heights, NY

²IBM, Austin, TX

Microprocessor global clock distribution networks use long buffered wires where reflections can be significant. Using accurate transmission-line models and optimization, these reflection effects can be exploited to improve clock-distribution characteristics. The clock distribution network of the POWER6 microprocessor is designed to run at frequencies exceeding 5GHz using only inverters and transmission lines and is capable of on-the-fly duty-cycle correction.

Break 3:00 PM

21.4 A Receiver with Start-up Initialization and Programmable Delays for Wireless Clock Distribution**3:15 PM**

X. Guo, R. Li, D-J. Yang, K. O
University of Florida, Gainesville, FL

A receiver for wireless clock distribution runs at 2.25GHz with 5ps_{pp} jitter. The clock is distributed as a sine wave at 8 times the actual clock frequency to mitigate dispersion. The receiver includes an initialization circuit and a frequency divider with 16 quantized programmable delays for skew reduction.

21.5 A 1.1GHz Charge-Recovery Logic**3:45 PM**

V. Sathe, J-Y. Chueh, M.. Papaefthymiou
University of Michigan, Ann Arbor, MI

A GHz-class dynamic charge-recovery logic is implemented with an on-chip clock generator and integrated inductor in a 0.13 μ m CMOS process. The chip operation is verified at clock frequencies up to 1.3GHz. At its natural frequency, the design recovers 60% of total circuit energy every cycle.

21.6 A 3.5 GHz Rotary-Traveling-Wave-Oscillator Clocked Dynamic Logic Family in 0.25 μ m CMOS**4:15 PM**

J. Wood, T. Edwards, C. Ziesler
Multigig, Scotts Valley, CA

Initial silicon results for a 3.5GHz dynamic logic family in 0.25 μ m SOI are presented. The chip is clocked with a rotary-traveling-wave oscillator, demonstrating per-gate dissipation of 100fJ per operation.

21.7 Distributed Loss Compensation for Low-latency On-chip Interconnects**4:45 PM**

A. Jose, K. Shepard
Columbia University, New York, NY

The use of distributed loss compensation for on-chip interconnects is discussed. Results are presented for a 14mm 3Gb/s on-chip link in 0.18 μ m CMOS with a measured latency of 12.1ps/mm and an energy dissipation of 2pJ/b with a BER<10⁻¹⁴. A 3 \times improvement in power consumption and a 1.5 \times improvement in latency over an optimally-repeated RC line is demonstrated.

Conclusion**5:15 PM**

DISCUSSION SESSIONS

E2: Present (and Future) Classic Circuits with Less than 25 Transistors

Organizer: JoAnn Close, *Analog Devices, San Jose, CA*

Moderator: Bill Redman-White, *Philips Semiconductors and Southampton University, United Kingdom*

Some circuits are easily forgotten, like cheap wines, but others are instantly classic vintage. These are the sound choices of the past and present, and will be brought to the table for years to come. We ask some connoisseurs to choose their pick of circuits with fewer than 25 transistors from the last 20 years, those which best illustrate continued and undiminished creativity in the field of “tiny” circuit design.

Panelists:

Klaas Bult, *Broadcom, Bunnik, The Netherlands*

Bob Dobkin, *Linear Technology, Milpitas, CA*

Barrie Gilbert, *Analog Devices, Beaverton, OR*

Tom Lee, *Stanford University, Stanford, CA*

Takahiro Miki, *Renesas Technology, Hyogo, Japan*

Yannis Tsividis, *Columbia University, New York, NY*

E3: What is Next to be Off-Shored, IC Design Jobs or IC Design Futures?

Organizer: Hui Pan, *Broadcom, Irvine, CA*

Moderator: John Stonick, *Synopsys, Hillsboro, OR*

The off-shoring of chip manufacturing has brought about profound changes in the semiconductor industry – affordable foundry services and a boom in the fabless integrated-circuit (IC) design business. Now, comes the next step: moving IC design offshore. Will this lead to another boom in the semiconductor industry that features a new “design-less” business model; or does design-less simply mean jobless for those presently employed in the industry? This panel, which comprises renowned off-shoring experts and industrial managers, will discuss the roadmap and impacts, in hope of shedding light on how IC designers can cope with the trend toward more off-shoring.

Panelists:

Clair Brown, *University of California, Berkeley, CA*

Marco Corsi, *Texas Instruments, Dallas, TX*

Brian Fuller, *EE Times, San Francisco, CA*

Ron Hira, *Rochester Institute of Technology, Rochester, NY*

Jurgen Knorr, *Dubai Silicon Oasis, Dubai, UAE*

Bill Yang Liu, *Analog Devices, Shanghai, China*

Daniel J. Radack, *DARPA, Arlington, VA*

DISCUSSION SESSIONS

SE7: Sensors on the Move

Organizer: **Kofi A.A. Makinwa**, *Delft University of Technology, Delft, The Netherlands*

Chair: **Herman Casier**, *AMI Semiconductor, Oudenaarde, Belgium*

The aim of this Special-Topic Evening Session is to highlight new developments in the field of sensors for automotive applications. Today, a typical light vehicle will employ more than 20 sensors, ranging in complexity from simple position sensors to MEMS accelerometers. Broadly speaking, these sensors are used to enhance engine and power-train performance and reliability, ensure compliance with various environmental standards, and increase occupant comfort and safety. Due to the constant demand for vehicles with increased performance, lower environmental impact, and greater levels of comfort and safety, it is certain that more sensors will be used in the vehicles of tomorrow.

The development of new automotive sensors is extremely challenging. Not only because such sensors must operate reliably in the relatively harsh (for electronic systems at least) automotive environment, but because they must also be suitable for mass production at low cost. Today, one of the main drivers of new sensor development is increased occupant comfort and safety. This trend is reflected in presentations describing new developments in tire-pressure monitoring systems, thermoelectric infrared image sensors, and MEMS inertial sensors. Another important driver of new developments is increased engine reliability, which is reflected in a presentation discussing a new class of oil-condition sensors.

<u>Time</u>	<u>Topics</u>
8:00	<i>Tire-Pressure Monitoring Systems,</i> Jakob Jongsma , <i>Infineon, Graz, Austria</i>
8:30	<i>Thermoelectric Infrared Image Sensors,</i> Masaki Hirota , <i>Nissan, Kanagawa, Japan</i>
9:00	<i>Oil-Condition Sensors,</i> Bernhard Jakoby , <i>Johannes Kepler University, Linz, Austria</i>
9:30	<i>Inertial Sensors for Automotive Applications,</i> John Geen , <i>Analog Devices, Cambridge, MA</i>

SESSION 22

LOW POWER MULTIMEDIA

Chair: Yiwan Wong, Hong Kong Applied Science and Technology Research Institute, Hong Kong, China

Associate Chair: Won Namgoong, University of Southern California, Los Angeles, CA

22.1 A 125 μ W Fully Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications

8:30 AM

T-M. Liu¹, T-A. Lir², S-Z. Wang², W-P. Lee¹, C-Y. Lee¹

¹National Chiao Tung University, Hsinchu, Taiwan

²MediaTek, Hsinchu, Taiwan

An MPEG-2 and H.264/AVC decoder occupies 3.9 \times 3.9mm² in 0.18 μ m 1P6M CMOS. To improve integration efficiency and transmission bandwidth, a scalable pipeline and prediction circuit is employed. The decoder performs real-time MPEG-2 and H.264/AVC QCIF at 15frames/s video decoding, dissipating 108 μ W and 125 μ W, respectively, at 1V with a clock frequency of 1.15MHz.

22.2 124MS/s Pixel-Pipelined Motion-JPEG 2000 Codec without Tile Memory

9:00 AM

Y-W. Chang, H-C. Fang, C-C. Cheng, C-C. Chen, C-J. Lian, L-G. Chen

National Taiwan University, Taipei, Taiwan

A JPEG2000 codec capable of processing 1920 \times 1080 HD video at 30frames/s is implemented on a 20.1mm² die with 0.18 μ m CMOS technology dissipating 345mW at 1.8V and 42MHz. The level-switched schedule eliminates the 192kB tile memory. Hardware sharing between encoder and decoder reduces silicon area by 40%.

22.3 A 160kGate 4.5kB SRAM H.264 Video Decoder for HDTV Applications

9:30 AM

C-C. Lin, J-I. Guo, H-C. Chang, Y-C. Yang, J-W. Chen, M-C. Tsai, J-S. Wang

National Chung Cheng University, Chia-Yi, Taiwan

Through both algorithmic and architectural optimization, the H.264 video decoder dissipates 320mW at 1.8V when operating at 120MHz for HD1080 (1920 \times 1088 at 30frames/s). The die contains 160kgates 4.5kB memory and occupies 2.9 \times 2.9mm² in 0.18 μ m CMOS.

Break 10:00 AM

22.4 A 120Mvertices/s Multi-Threaded VLIW Vertex Processor for Mobile Multimedia Applications

10:15 AM

C-H. Yu, K. Chung, D. Kim, L-S. Kim

KAIST, Daejeon, Korea

A 3D vertex processor with a floating-point 4-threaded and 4-issue VLIW architecture and a TnL vertex cache is implemented for mobile multimedia applications in a 0.18 μ m 4M CMOS process. The proposed architecture efficiently reduces the total energy consumption and achieves 120Mvertices/s with a 2.5GFLOPS datapath using 157mW when operating at 100MHz.

22.5 A 40GOPS 250mW Massively Parallel Processor Based on Matrix Architecture**10:45 AM**

M. Nakajima¹, H. Kondo¹, K. Mizumoto¹, M. Higashida¹, K. Nakata¹, O. Yamamoto¹, M. Kainaga², N. Okumura¹, H. Noda¹, T. Tanizaki¹, T. Gyohten¹, K. Dosaka¹, K. Yashida¹, Y. Okuno¹, Y. Kawamura¹, Y. Shimazu¹, K. Arimoto¹, K. Saito¹, K. Muramatsu¹, T. Shimizu²

¹Renesas Technology, Itami, Japan²Renesas Technology, Kodaira, Japan

The Matrix Processing Engine (MTX) is a massively parallel processor based on the Matrix architecture. 40GOPS (16b additions) is achieved at 200MHz clock frequency and 250mW power dissipation. 2048 ALUs and 1Mb SRAM connected by a flexible switching network are integrated in 3.1mm² using a 90nm CMOS process.

22.6 A 5mW MPEG4 SP Encoder with 2D Bandwidth-Sharing Motion Estimation for Mobile Applications**11:15 AM**

C-P. Lin¹, P-C. Tseng², Y-T. Chiu¹, S-S. Lin¹, C-C. Cheng¹, H-C. Fang⁴, W-M. Chao³, L-G. Chen¹

¹National Taiwan University, Taipei, Taiwan²Novatek, Taipei, Taiwan³Quanta Computer, Taipei, Taiwan⁴MediaTek, Taipei, Taiwan

A 5mW MPEG4 SP encoder is implemented on a 7.7mm² die in 0.18μm CMOS technology. It encodes CIF 30frames/s in real-time at 9.5MHz using 5mW at 1.3V and VGA 30frames/s at 28.5MHz uses 18mW at 1.4V. This chip employs a 2D bandwidth-sharing ME design, content-aware DCT/IDCT, and clock gating techniques to minimize power consumption.

22.7 6.33mW MPEG Audio Decoding on a Multimedia Processor**11:45 AM**

Y. Ueda¹, H. Yamauchi¹, M. Mukuno¹, S. Furuichi¹, M. Fujisawa¹, F. Qiao², H. Yang²

¹SANYO Electric, Gifu, Japan²Tsinghua University, Beijing, China

Low-power implementation techniques are used in the multimedia processor to achieve MPEG audio decoding in 6.33mW with a 1.1V supply. Three techniques are employed: a parallel processing DSP; dynamic voltage control using a multi-power domain; and a conditional pre-charge flip-flop. The processor occupies 6.5×6.5mm² in 0.15μm 6M CMOS.

Conclusion**12:15 PM**

SESSION 23

TECHNOLOGY AND ARCHITECTURE DIRECTIONS

Chair: Werner Weber, Infineon, Munich, Germany

Associate Chair: C-K Wang, National Taiwan University, Taipei, Taiwan

23.1 Active Circuits for Ultra-High-Efficiency Micropower Generators Using Nickel-63 Radioisotope 8:30 AM

R. Duggirala, H. Li, A. Lal

Cornell University, Ithaca, NY

Integration of betavoltaics with radioisotope-powered piezoelectric micropower generators (RPG) operating in new *resonant* modes, attains nuclear-electrical conversion efficiencies of up to 30%, generating 1 to 10 μ W peak power with 1 to 10 milliCurie of Nickel-63. A 20mV-voltage-drop ac-to-dc rectifier employing radioactively biased MOSFETs is developed for efficient conversion of RPG-generated low-amplitude power signals.

23.2 Circuit Design Issues in Multi-Gate FET CMOS Technologies 9:00 AM

C. Pacha¹, K. von Arnim¹, T. Schulz^{1,2}, W. Xiong^{2,3}, M. Gostkowski⁴, G. Knoblinger², A. Marshall⁴, T. Nirschl⁴, J. Berthold⁴, C. Russ⁴, H. Gossner⁴, C. Duvvury⁵, P. Patruno⁵, R. Cleavlin³, K. Schrueter¹

¹Infineon, Munich, Germany

²ATDF, Austin, TX

³Texas Instruments, Dallas, TX

⁴Infineon, Villach, Austria

⁵Soitec, Bernin, France

Multi-gate FETs are promising for sub-45nm CMOS technologies. To address the link between design and technology, basic digital and analog circuits are fabricated using FinFET and triple-gate FETs. Digital circuit performance, leakage currents, and power dissipation are characterized. The triple-gate FET achieves the lowest gate delay (27ps at 1.2V) and is >30% faster than FinFET with $L_g=80$ nm, $t_{ox}=2$ nm. A FinFET-based Miller opamp achieves 45dB dc gain at 1.5V.

23.3 A Low-Power True Random Number Generator Using the Random Telegraph Noise of Single Oxide-Traps 9:30 AM

R. Brederlow¹, R. Prakash², C. Paulus³, R. Thewes¹

¹Infineon, Munich, Germany

²now with Agere Systems, San Jose, CA

³now with Siemens, Munich, Germany

A true random number generator is realized by utilizing the noise produced by single oxide traps in small-area MOSFETs in combination with built-in redundancy. The circuit has an area of 0.009mm² in 0.12 μ m CMOS and consumes 50 μ W at 200kb/s random output data. The concept is robust against environmental noise and supply-voltage variations and is thus suitable for operation within security controllers.

Break 10:00 AM

23.4 A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link 10:15 AM

N. Miura¹, D. Mizoguchi¹, M. Inoue¹, K. Niitsu¹, Y. Nakagawa², M. Tago², M. Fukaishi², T. Sakurai³, T. Kuroda¹

¹Keio University, Yokohama, Japan

²NEC, Sagamihara, Japan

³University of Tokyo, Tokyo, Japan

A 1Tb/s 3W inter-chip transceiver transmits clock and data by inductive coupling at a clock rate of 1GHz and data rate of 1Gb/s per channel. 1024 data transceivers are arranged with a pitch of 30 μ m. The total layout area is 2mm² in 0.18 μ m CMOS and the chip thickness is 10 μ m. 4-phase TDMA reduces crosstalk and the BER is <10⁻¹². Bi-phase modulation is used to improve noise immunity, reducing power in the transceiver.

23.5 Optical Interconnect Technologies for High-Speed VLSI Chips Using Silicon Nano-Photonics

10:45 AM

K. Ohashi¹, J. Fujikata¹, M. Nakada¹, T. Ishi¹, K. Nishi¹, H. Yamada¹, M. Fukaishi², M. Mizuno², K. Nose², I. Ogura³, Y. Urino³, T. Baba¹

¹NEC, Tsukuba, Japan

²NEC, Sagamihara, Japan

³NEC, Kawasaki, Japan

Optoelectronic and electrooptic elements are integrated on VLSI chips. The junction capacitance of a nano-photodiode is extremely low (<10aF), which permits a high load resistance to be used, resulting in higher output voltage at high frequencies. A ceramic Pb(₂ZrTi)O₃ film with average crystallite diameter below 20nm has a high electro-optical coefficient (>150pm/V) suitable for on-chip modulators.

23.6 An Asynchronous Array of Simple Processors for DSP Applications

11:15 AM

Z. Yu, M. Meeuwsen, R. Apperson, O. Sattari, M. Lai, J. Webb, E. Work, T. Mohsenin, M. Singh, B. Baas

University of California, Davis, CA

An array of simple programmable processors designed for DSP applications is implemented in 0.18μm CMOS and contains 36 asynchronously clocked independent processors. The processors operate at 475MHz, and each processor has a maximum power of 144mW at 1.8V and occupies 0.66 mm².

23.7 System-in-Silicon Architecture and its Application to an H.264/AVC Motion Estimate for 1080HDTV

11:45 AM

K. Kumagai¹, C. Yang², H. Izumino¹, N. Narita¹, K. Shinjo¹, S-I. Iwashita¹, Y. Nakaoka¹, T. Kawamura¹, H. Komabashiri¹, T. Minato¹, A. Ambo¹, T. Suzuki¹, Z. Liu², Y. Song², S. Goto², T. Ikenaga², Y. Mabuchi¹, K. Yoshida¹

¹System Fabrication Technologies, Yokohama, Japan

²Waseda University, Kita-Kyushu, Japan

System-in-silicon (SiS) is a multi-chip architecture to realize wide bandwidth communication between logic and memory with low power. The application of SiS to H.264/AVC motion estimation is presented. DRAM is integrated with 23.1Gb/s bandwidth and 1.6pJ/b data transfer efficiency, realizing real-time 1080HDTV processing with 263.1GB/s.

23.8 A Chip-scale Electrical Soliton Modelocked Oscillator

12:00 PM

D. Ricketts, D. Ham

Harvard University, Cambridge, MA

This paper introduces a chip-scale electrical soliton modelocked oscillator, which self-generates a periodic train of electrical soliton pulses. This circuit is made possible by combining a nonlinear transmission line (NLTL) with a unique amplifier that tames the instability-prone soliton dynamics in a closed-loop NLTL. This chip-scale prototype produces a pulse width of 293ps and demonstrates the feasibility for future widths close to 1ps, adding a new direction in pulse-based electronics.

Conclusion

12:15 PM

SESSION 24

HIGH-PERFORMANCE DIGITAL CIRCUITS

Chair: David Blaauw, University of Michigan, Ann Arbor, MI

Associate Chair: Masayuki Mizuno, NEC, Kanagawa, Japan

24.1 4GHz+ Low-Latency Fixed-Point and Binary Floating-Point Execution Units for the POWER6 Processor

8:30 AM

B. Curran¹, B. McCredie², L. Sigal¹, E. Schwarz², B. Fleischer³, Y-H. Chan¹, D. Webber¹, M. Vader², A. Goyal¹

¹IBM, Poughkeepsie, NY

²IBM, Austin, TX

³IBM, Yorktown Heights, NY

A 1-pipe stage, low-latency, 13 FO4, 64b fixed-point execution unit, implemented in a 65nm SOI CMOS process, allows back-to-back execution of data dependent adds, subtracts, compares, shifts, rotates, and logical operations. A 7-pipe stage, 91 FO4, double-precision floating-point unit allows forwarding of dependent results after 6 cycles in most cases.

24.2 A 250ps 64b Carry-Lookahead Adder in 90nm CMOS

9:00 AM

S. Kao^{1,2}, R. Zlatanovic¹, B. Nikolic¹

¹University of California, Berkeley, CA

²Xilinx, San Jose, CA

A 64b adder with a single-execution cycle time of 250ps is fabricated in a 90nm CMOS technology. The adder is designed using an energy-delay optimization framework that can rapidly optimize different microarchitectures in the energy-delay space. The microarchitecture with the lowest delay, a sparse radix-4 Ling parallel prefix tree, is chosen. The carry tree uses footless domino logic to minimize delay while the non-critical paths use minimum-size static logic to reduce energy. The adder consumes 311mW from a 1V supply.

24.3 A 64b Adder Using Self-Calibrating Differential Output-Prediction Logic

9:30 AM

K. H. Chong¹, L. McMurchie¹, C. Secher²

¹University of Washington, Seattle, WA

²University of Texas, Dallas, TX

A 64b adder based on self-calibrating differential output-prediction logic is fabricated in a 0.13 μ m 1.2V process. It has a normalized worst-case delay of 238ps (3.9 FO4 inverter delays) and consumes 30pJ per operation, which is 1.8X faster and 2X lower in energy than previously published 64b adder results, which were based on domino logic.

Break 10:00 AM

- 24.4 A Leakage Current Replica Keeper for Dynamic Circuits** **10:15 AM**
Y. Lih, N. Tzartzanis, W. Walker
Fujitsu, Sunnyvale, CA
- A 1T-overhead keeper circuit for dynamic gates replicates the evaluation stack leakage current and thus provides PVT tracking. Implemented in a 90nm CMOS process, the keeper enables design of AND-OR circuits with 30% more legs; 16 to 24 leg dynamic AND-OR circuits are 25 to 40% faster than those with a conventional keeper at the same noise margin. The circuit operation is verified on a 72×1024 3W/4R SRAM.
- 24.5 An On-Chip Delay- and Skew-Insensitive Multi-Cycle Communication Scheme** **10:45 AM**
P. Caputa, C. Svensson
Linköping University, Linköping, Sweden
- A synchronous latency-insensitive design (SLID) method that mitigates unknown on-chip global wire delays and removes the need for controlling global clock skew is presented. An SLID-based 5.4mm-long on-chip global bus, fabricated in a standard 0.18μm CMOS process, supports 3Gb/s/wire and accepts ±2 clock cycles of data-clock skew.
- 24.6 A 14:1 Dynamic MUX FF with Select Activity Detection** **11:15 AM**
M. Sumita, T. Wada
Matsushita, Nagaokakyo, Japan
- A 14:1 dynamic MUX FF is discussed. The design uses 2 cascaded dynamic stages to investigate the 14:1 MUX with a dynamic FF. In addition, replication is used to maintain latch state when all selects are inactive. The timing of the MUX FF is evaluated with a proposed slew detector. Fabricated in a 90nm CMOS process, the chip has a 2× speed increase and 70% area reduction compared to conventional methods.
- 24.7 An 8.8GHz 198mW 16x64b 1R/1W Variation-Tolerant Register File in 65nm CMOS** **11:45 AM**
S. Hsu, A. Agarwal, M. Anders, S. Mathew, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR
- A 16×64b 1R/1W register file is fabricated in 65nm CMOS technology. The 0.017mm² chip performs 8.8GHz fused decode and read/write operations in a single cycle while dissipating 198mW at 1.2V, 50°C, with frequency scalable to 10.1GHz at 1.4V, 50°C. Variation-tolerant keeper compensation, leakage-tolerant BL/WL architecture and optimal non-minimum channel-length usage enable wide PVT operating range with an active leakage of 25mW and a BL noise droop •8mV.
- Conclusion** **12:15 PM**

SESSION 25

RF/IF CIRCUITS

Chair: Tom Schiltz, Linear Technology, Colorado Springs, CO

Associate Chair: Satoshi Tanaka, Hitachi, Tokyo, Japan

25.1 A Multipath Technique for Canceling Harmonics and Sidebands in a Wideband Power Upconverter

8:30 AM

R. Shrestha, E. Mensink, E. Klumperink, G. Wienk, B. Nauta

University of Twente, Enschede, The Netherlands

Switching mixers are power-efficient but produce unwanted harmonics and sidebands. A multipath technique to clean up the spectrum using digital circuits and mixers, but no filters, is applied to a 0.13 μ m CMOS power upconverter. The circuit delivers 8mW from dc to 2.4GHz with 11% drain efficiency, with spurs <-40dBc over more than 4 octaves in frequency, and consumes 228mW from a 1.2V supply.

25.2 A Complex Image-Rejection Circuit with Sign Detection Only

9:00 AM

S. Lerstaveesin, B-S. Song

University of California, San Diego, La Jolla, CA

The orthogonal property of I/Q channels is applied to adaptively correct path gain and phase errors using four sign detectors. A complex baseband S/H chip achieves an image rejection of 65dB while sampling at 40MS/s. The chip occupies 0.8 \times 0.45mm² in a 0.18 μ m CMOS process and consumes 23mW at 1.8V.

25.3 On-Chip Image Rejection in a Low-IF CMOS Receiver

9:30 AM

M. Hajirostam, K. Martin

University of Toronto, Toronto, Canada

An adaptive image-reject mixer is realized in a 0.18 μ m CMOS technology. The circuit achieves high image-rejection ratios without off-chip filters in applications such as TV tuners. Test results show a 54dB image-rejection ratio in a low-IF receiver. The circuit consumes 75mW from a 1.8V supply and occupies 2.25mm² including pads.

Break 10:00 AM

25.4 Active 2nd-Order Intermodulation Calibration for Direct-Conversion Receivers

10:15 AM

M. Cher¹, Y. Wu²

¹University of California, Los Angeles, CA

²Qualcomm, San Diego, CA

A temperature-compensated active IM2 calibration circuit for direct-conversion receivers is fabricated with a mixer in 0.25 μ m CMOS. A squaring circuit senses the RF signal and generates a calibration current to cancel mixer IM2 distortion. The loading effect and noise contribution are minimized by gain boosting. IIP2 is boosted >20dB to >80dBm in the IMT band. The calibration circuit draws 1.5mA.

25.5 A 2.2GHz Sub-Harmonic Mixer for Direct Conversion Receivers in 0.13 μ m CMOS

10:45 AM

H. Jer¹, S. Rose², R. Meyer¹

¹University of California, Berkeley, CA

²Analog Devices, Wilmington, MA

A 0.13 μ m CMOS sub-harmonic mixer uses a passive switching network to achieve a dc offset of 0.7mV and 2 \times LO leakage of -91dBm at the RF port. LO leakage is -95dBm, and the flicker-noise corner is 100kHz. The mixer requires an LO input power of -18dBm and consumes 13mW from a 1.2V supply.

25.6 A Blocker-Vigilant Channel-Select Filter with Adaptive IIP3 and Power Dissipation

11:15 AM

A. Yoshizawa, Y. Tsvividis

Columbia University, New York, NY

A dynamic biasing scheme that reduces the average dc power of channel-select filters is presented. An adaptive IIP3, 5th-order Butterworth low-pass filter is implemented in a 0.18 μ m CMOS process with a 1.8V supply voltage. The filter quiescent current is 1.2mA, with a -5dBV out-of-channel IIP3. With a blocker level of -13dBV, the supply current increases to 2.7mA and the IIP3 increases to +20dBV.

25.7 An IP2 Improvement Technique for Zero-IF Down-Converters

11:45 AM

H. Darabi, H. Kim, J. Chiu, B. Ibrahim, L. Serrano

Broadcom, Irvine, CA

An IP2 calibration circuit to improve the 2nd-order nonlinearity of mixers in zero or low-IF receivers is presented. The circuit allows the mixers to be optimized independently, and has negligible impact on receiver noise figure, area, and power consumption. A prototype transceiver including the calibration circuitry in 0.13 μ m CMOS is fabricated. An average IIP2 improvement of 18dB is measured.

25.8 Low Flicker Noise Quadrature Mixer Topology

12:00 PM

R. Pallela, T. Sowlati, D. Rozenblit

Skyworks Solutions, Irvine, CA

A mixer topology that improves NF at low offset frequencies by reducing 1/f noise contributions is fabricated in 0.13 μ m CMOS. The NF at 10kHz is 9dB, which is 9dB less than a conventional mixer. The mixer also has 2dB higher gain, improved quadrature matching, higher IP2, straightforward implementation, and is robust over PVT.

Conclusion

12:15 PM

SESSION 26

CELLULAR BUILDING BLOCKS AND SOCS

Chair: Charles Chien, SST Communications, Marina Del Rey, CA

Associate Chair: Jacques Rudell, Intel, Santa Clara, CA

26.1 A 750mV 15kHz 1/f Noise Corner 51dBm IIP2 Direct-Conversion Front-End for GSM in 90nm CMOS

8:30 AM

M. Brandolini, M. Sosio, F. Svelto

Università degli Studi di Pavia, Pavia, Italy

A direct-conversion front-end using a highly linear mixer is implemented in 90nm CMOS. The mixer has a 15kHz 1/f noise corner, 51dBm IIP2, 31.5dB gain, 3.5dB NF, and draws 15mA from 0.75 V.

26.2 A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO

8:45 AM

A. Liscidini¹, A. Mazzanti², R. Tonietto³, L. Vandl⁴, P. Andreani⁴, R. Castello¹

¹Università degli Studi di Pavia, Pavia, Italy; ²University of Modena and Reggio Emilia, Modena, Italy; ³ST Microelectronics, Pavia, Italy

⁴Technical University of Denmark, Lyngby, Denmark

A GPS RF front-end combines the LNA, mixer, and VCO in a single stage and can operate from a 1.2V supply. The chip is implemented in a 0.13 μ m CMOS process and occupies 1.5mm² active area. It consumes 5.4mW with a 4.8dB NF, 36dB gain, and a P_{1dB} of -31dBm.

26.3 A 20mW 3.24mm² Fully Integrated GPS Radio for Cell-Phones

9:00 AM

V. Della Torre¹, M. Conta¹, R. Chokkalingam¹, G. Cusma², P. Rossi³, F. Svelto²

¹RFDomus, Newport Beach, CA; ²Università degli Studi di Pavia, Pavia, Italy; ³Maxim Integrated Products, Rozzano, Italy

A GPS receiver that can coexist with cellular transceivers is implemented in a 0.18 μ m SiGe BiCMOS technology and occupies 3.24mm². The device integrates polyphase filters, VGA, ADCs, fractional-N synthesizer, LNA, and mixers, minimizing desensitization and reciprocal mixing. The receiver consumes 20mW from a 1.8V supply and has 1dB gain desensitization with a -8dBm 1.9GHz blocker

26.4 Wideband Image-Rejection Circuit for Low-IF Receivers

9:30 AM

K. Maeda¹, W. Hioe¹, Y. Kimura², S. Tanaka¹

¹Hitachi, Tokyo, Japan; ²Renesas Technology, Gunma, Japan

A wideband image-rejection circuit for GSM/EDGE low-IF receivers includes a reference signal source and digital correction circuit that compensate I/Q gain, phase, and frequency response mismatch. The chip integrates an LNA, mixers, PGAs, LPFs, and fractional-N synthesizer in a 0.25 μ m BiCMOS process and achieves 50dB IRR over the entire signal bandwidth at 200kHz IF.

26.5 A 1.8GHz Spur-Cancelled Fractional-N Frequency Synthesizer with LMS-Based DAC Gain Calibration

9:45 AM

M. Gupta, B-S. Song

University of California, San Diego, CA

A 1.8GHz wideband fractional-N synthesizer achieves the phase noise of an integer-N PLL using a noise-cancellation DAC calibrated with an adaptive LMS spur correlation technique. It exhibits in-band and integrated phase noises of -98dBc/Hz and 0.8^o, respectively. The chip in 0.18 μ m CMOS occupies 2mm², and consumes 29mW at 1.8V.

Break 10:00 AM

26.6 An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS **10:15 AM**

R. Bagheri^{1,2}, A. Mirzaei¹, S. Chehrazai¹, M. Heidari¹, M. Lee¹, M. Mokhema¹, W. Tang¹, A. Abidi¹

¹University of California, Los Angeles, CA; ²WiLinX, Los Angeles, CA

A 90nm CMOS RX operates over the 800MHz to 5GHz band uses a passive FET mixer driven by a capacitively coupled RF transconductor, and a combination of CT and DT analog FIR and IIR filters to achieve >100dB of programmable anti-aliasing. The RX chain has 5 to 5.5dB NF, -3.5dBm IIP3, 39dBm IIP2, 10 to 66dB of gain, and draws 11.4mA from 2.5V and 8 to 28mA (depending on RX mode) from 1V.

26.7 A Fully Integrated SoC for GSM/GPRS in 0.13μm CMOS **10:45 AM**

P-H. Bonnaud¹, M. Hammes², A. Hanke³, J. Kissing², R. Koch³, E. Labarre¹, C. Schwoerer³

¹Infineon, Sophia Antipolis, France; ²Infineon, Duisburg, Germany

³Infineon, Munich, Germany

A single-chip radio for quad-band GSM/GPRS applications integrates the RF, analog/mixed-signal blocks, DSP, application processor, RAM/ROM, and audio. It is implemented in a 0.13μm CMOS process. The RX achieves -112.5dBm/-110.5dBm sensitivity and the TX meets all the spectral mask requirements while using a 1.5V supply.

26.8 A 1.9GHz Single-chip CMOS PHS Cellphone **11:15 AM**

S. Mehta¹, W. Si¹, H. Samavat¹, M. Terrovitis¹, M. Mack¹, K. Onodera¹, S. Jen¹, S. Luschas¹, J. Hwang¹, S. Mendis¹, D. Su¹, B. Wooley²

¹Atheros, Santa Clara, CA; ²Stanford University, Stanford, CA

A single-chip CMOS PHS cellphone, fabricated in a 0.18μm CMOS process, implements all handset functions including radio, voice, audio, CPU, and digital interfaces. The IC has +4dBm EVM-compliant transmit power, -106dBm receiver sensitivity, and 15μs synthesizer settling time. It draws 81mA from a 1.8V supply while occupying 35mm² of chip area.

26.9 A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications **11:45 AM**

N. Wongkomet, L. Tee, P. Gray

University of California, Berkeley, CA

A fully differential Doherty PA is implemented in 0.13μm CMOS with MIM capacitors and a die size of 2.8x3.2mm². The prototype achieves a maximum output power of 1.5W at 1.7GHz with a drain efficiency of 39%. The peak PAE is 36% (33% with off-chip balun) including the driving stages and is >18% for a 10dB range of output power.

26.10 A 1.2V Dual-Mode GSM/WCDMA ΔΣ ADC in 65nm CMOS **12:00 PM**

J. Järvinen, K. Halonen

Helsinki University of Technology, Espoo, Finland

A dual-mode ΔΣ ADC for a GSM/WCDMA direct-conversion receiver is implemented in a standard 65nm digital CMOS process and has a core area of 0.1mm². With sampling frequencies of 48MHz and 96MHz, the ADC achieves peak SNDRs of 90dB and 62dB over the 100kHz GSM band and 1.92MHz WCDMA band, respectively. It draws 2.75mA in GSM mode and 3mA in WCDMA mode from a 1.2V supply.

Conclusion **12:15 PM**

SESSION 27

IMAGE SENSORS

Chair: Boyd Fowler, Fairchild Imaging, Milpatas, CA

Associate Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

27.1 A 1/1.8-inch 6.4MPixel 60frames/s CMOS Image Sensor with Seamless Mode Change

8:30 AM

S. Yoshihara¹, M. Kikuchi¹, Y. Ito¹, Y. Inada¹, S. Kuramochi¹, H. Wakabayashi¹, M.Okano¹, K. Koseki¹, H. Kuriyama¹, J. Inutsuka², A. Tajima², T. Nakajima¹, Y.Kudoh¹, F. Koga¹, Y. Kasagi², S. Watanabe², T. Nomoto¹

¹Sony, Atsugi, Japan;

²Sony, Nagasaki, Japan

A 1/1.8-inch 6.4MPixel 60frames/s CMOS image sensor fabricated in a 0.18 μ m 1P3M process is described. A Zigzag-shaped 1.75T/pixel architecture and a 10b counter-type column parallel ADC enables 2.5 \times 2.5 μ m² pixels. The resulting pixel has 38% fill factor, 12ke-/lux \bullet s, and random noise of 7e^{-rms}. A 12b parallel LVDS interface enables data rates of up to 5.18Gb/s with 218MHz DDR. Full frame and 2 \times 2 binning modes are interchangeable without an extra invalid frame.

27.2 1/2-inch 7.2MPixel CMOS Image Sensor with 2.25 μ m Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation

9:00 AM

Y. Kim, Y. Kim, S. Choi, H. Kong, S. Hwang, J. Ko, B. Kim, T. Asaba, S. Lim, J. Im, T. Oh, D. Yi, J. Lee, W. Yang, J. Ahn, E. Jung, Y. Lee, J. Hahn

Samsung, Yongin, Korea

A 1/2-inch 7.2MPixel CMOS image sensor with 2.25 μ m pixels employs a 4-shared pixel structure with pixel-level charge summation. It achieves a 57% fill factor, full well capacity of 14ke- with 41dB maximum SNR at full resolution, 8e- random noise, 15ke-/lux \bullet s sensitivity, and a 3dB increment in SNR for pixel-level charge summation and sub-sampling operation. A 0.13 μ m Cu process is used.

27.3 A 3MPixel Low-Noise Flexible-Architecture CMOS Image Sensor

9:30 AM

J. Yang, K. Fife, L. Brooks, C. Sodini, A. Betts, P. Mudunuru, H-S. Lee

Cypress Semiconductor, Cambridge, MA

An image sensor with a 2.54 μ m pixel fabricated in a 0.18 μ m CMOS technology is presented. The 3T pixel with drain-side row-select reduces reset noise by cascoded feedback reset and increases responsivity with common-source readout. The reset noise is 13e- and the responsivity at 550nm is 1.12V/lux \bullet s in source-follower readout mode and 5.6V/lux \bullet s in common-source readout mode.

27.4 A CMOS Imager with Column-Level ADC Using Dynamic Column FPN Reduction

9:45 AM

M. Snoeij, A. Theuwissen, K. Makinwa, J. Huijsing

Delft University of Technology, Delft, The Netherlands

A CMOS imager with a column-level ADC uses a dynamic column FPN reduction technique. This technique requires 5 extra switches per column and minimal digital overhead at the chip level while reducing the perceptual effect of column FPN. Measurements show that the prototype makes a column FPN of \pm 0.67% nearly invisible.

Break 10:00 AM

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor

10:15 AM

Y. Nitta, Y. Muramatsu, K. Amano, T. Toyama, J. Yamamoto, K. Mishina, A. Suzuki, T. Taura, A. Kato, M. Kikuchi, Y. Yasui, H. Nomura, N. Fukushima
Sony, Kanagawa, Japan

A progressive 1/1.8-inch 1920×1440 CMOS image sensor with a column-inline dual CDS architecture uses a 0.18 μ m CMOS process. This sensor implements digital double sampling with analog CDS on a column parallel ADC. Random noise is 5.2e⁻_{rms} and the DR is 68dB at 180frames/s(6.0Gb/s). FPN is <0.5e⁻_{rms} without the correction circuit.

27.6 A 14b 74MS/s CMOS AFE for True High-Definition Camcorders

10:45 PM

R. Kapusta, S. Hatanaka, S. Decker, P. Chen, D. Foley, A. Wellinger, M. Ozbas, D. Kelly, M. Sayuk, B. Schofield, K. Nakamura
Analog Devices, Wilmington, MA

A 14b 74MS/s CMOS AFE is designed for true high-definition camcorder applications. This is the first published AFE capable of high-definition sample rates. The AFE operates from a 1.8V supply, achieves 78dB peak SNR, 1.4V input range, and dissipates 70mW.

27.7 CMOS Image Sensor with Integrated 4Gb/s Camera Link Transmitter

11:00 AM

A. Krymski¹, K. Tajima²
¹Alexima, La Crescenta, CA;
²Photron, Tokyo, Japan

A 516×514 1000+ frames/s CMOS sensor with integrated camera link transmitter is designed in 0.35 μ m 2P3M CMOS and dissipates 1.2W at 3.3V. The sensor can drive a 3m cable delivering 4Gb/s of data.

27.8 A 128×128 33mW 30frames/s Single-Chip Stereo Imager

11:15 AM

R. Philipp, R. Etienne-Cummings
Johns Hopkins University, Baltimore, MD

A single-chip stereo imager incorporates two 128×128 linear current-mode active pixel sensors with 10 μ m pixel pitch and 1.2% uncorrected FPN. The chip, fabricated in a 0.35 μ m 3.3V 4M2P CMOS process, uses parallel computation of the sum-of-absolute-difference matching metric and confidence measures to produce 114×125 depth maps at 30frames/s using 33mW from 3.3V.

27.9 A 128×128 120dB 30mW Asynchronous Vision Sensor that Responds to Relative Intensity Change

11:45 AM

P. Lichtsteiner¹, C. Posch², T. Delbruck¹
¹ETH, Zurich, Switzerland
²ARC Seibersdorf Research, Vienna, Austria

A vision sensor responds to temporal contrast with asynchronous output. Each pixel independently and continuously quantizes changes in log intensity. The 128×128-pixel chip has 120dB illumination operating range and consumes 30mW. Pixels respond in <100 μ s at 1klux scene illumination with <10% contrast-threshold FPN.

Conclusion

12:15PM

SESSION 28

WIRELINE BUILDING BLOCKS

Chair: Kevin Kornegay, Georgia Institute of Technology, Atlanta, GA

Associate Chair: Herman Casier, AMI Semiconductors, Oudenaarde, Belgium

28.1 A 5V AC-Powered CMOS Filter-Selectivity Booster for POTS/ADSL Splitter Size Reduction

8:30 AM

E. Sackinger¹, A. Tennen¹, D. Shulman¹, B. Wani¹, M. Rambaud¹, D. Lim¹, F. Larsen¹, G. Moschytz²

¹Conexant Systems, Red Bank, NJ

²Bar-Ilan University, Ramat-Gan, Israel

A 0.5 μ m CMOS chip contains a 5th-order continuous-time filter, a low output-impedance driver, and an active rectifier. The chip boosts the selectivity of an external passive LC LPF and achieves an ADSL isolation of 70dB at 30kHz, while maintaining a passband flatness of 0.23dB. It consumes 35mW from a 5V supply and reduces the number of transformers and the size of POTS/ADSL splitters.

28.2 A DC-to-44GHz 19dB Gain Amplifier in 90nm CMOS Using Capacitive Bandwidth Enhancement

9:00 AM

J. Weiss, M. Kossel, C. Menolfi, T. Morf, T. Toifl, M. Schmatz

IBM, Rueschlikon, Switzerland

A dc-to-44GHz amplifier with 19dB differential gain in a standard 90nm CMOS technology is presented. Capacitive bandwidth and group-delay enhancements are combined with series peaking in a shunt-peaking amplifier. The circuit occupies 0.02mm² and dissipates 57mW at 1V.

28.3 A 10Gb/s CMOS AGC Amplifier with 35dB Dynamic Range for 10Gb Ethernet

9:30 AM

C-F. Liao, S-I. Liu

National Taiwan University, Taipei, Taiwan

A 10Gb/s AGC amplifier is implemented in 0.18 μ m CMOS technology. The circuit uses a linear-in-dB controlled VGA with 58dB tuning range. For input swings from 18mV_{pp} to 1V_{pp}, the output swing is 430mV_{pp} within +0.4 to -0.8dB variations. The measured dynamic range is 35dB with BER <10⁻¹². The AGC consumes 54mW from a 1.8V supply.

28.4 A 20Gb/s Bidirectional Transceiver Using a Resistor-Transconductor Hybrid

9:45 AM

Y. Tomita¹, H. Tamura², M. Kibune², J. Ogawa², K. Gotolf², T. Kuroda¹

¹Keio University, Yokohama, Japan, ²Fujitsu, Kawasaki, Japan

A 20Gb/s simultaneous bidirectional transceiver uses a resistor-transconductor hybrid in a standard 0.11 μ m CMOS process. The 7mW hybrid works in a continuous-time domain without any replica driver and eliminates the need for the precise matching between the replica- and main-driver characteristics.

Break 10:00 AM

28.5 A 1ps-Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling

10:15 AM

K. Nose¹, M. Kajita², M. Mizuno¹

¹NEC, Kanagawa, Japan

²NEC, Tokyo, Japan

An in-field real-time successive jitter-measurement macro is developed. It features interpolated jitter oversampling and feedforward calibration that help attain 1ps resolution and a hierarchical vernier jitter-measurement technique that exploits the trade-off between rms and deterministic jitter measurement characteristics.

28.6 1.83ps-Resolution CMOS Dynamic Arbitrary Timing Generator for >4GHz ATE Applications

10:45 AM

T. Okayasu, M. Suda, K. Yamamoto, S. Kantake, S. Sudou, D. Watanabe
Advantest, Gunma, Japan

A high-speed high-precision dynamic arbitrary timing generator, fabricated in a 0.18 μ m CMOS process, for >4GHz ATE applications is demonstrated. It exhibits a maximum operating frequency of 1.066 and 4.266GHz (multiplexed mode), a timing resolution of 1.83ps, an INL of $\leq \pm 4$ ps excluding the calibration RAM, and a random jitter of < 0.7 ps_{rms}.

28.7 A Clock Duty-Cycle Correction and Adjustment Circuit

11:15 AM

J. S. Humble, P. Zabinski, B. Gilbert, E. Daniel
Mayo Clinic, Rochester, MN

A clock duty-cycle correction circuit that accepts input duty cycles ranging from 30% to 70% and maintains a user-selectable output duty cycle over a frequency range of 500MHz to 6GHz is demonstrated. The output duty cycle is selectable from 41.25% to 58.75% in 1.25% increments. The circuitry is integrated into a clock-distribution chip which provides 10 identical outputs.

28.8 Performance Variations of a 66GHz Static CML Divider in 90nm CMOS

11:30 AM

J-O. Plouchart¹, J. Kim¹, V. Karam², R. Trzcinski¹, J. Gross¹

¹IBM, Hopewell Junction, NY

²Carleton University, Ottawa, Canada

A 66GHz maximum operating clock frequency is measured for a 90nm CMOS static CML divide-by-2 with a 25.5mW latch power dissipation. Statistical self-oscillation frequency measurements exhibit a mean of 42.6 and 39.2GHz at 25°C and 85°C, and a 2.8GHz standard deviation. The mean dissipated power is 44.3mW at 1.4V, with a 2.2mW standard deviation.

28.9 A 20Gb/s 1:4 DEMUX Without Inductors in 0.13 μ m CMOS

11:45 PM

B-G. Kim¹, L-S. Kim¹, S. Byun², H-K. Yu²

¹KAIST, Daejeon, Korea

²Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea

A 20Gb/s 1:4 DEMUX is implemented in a 0.13 μ m CMOS technology. The chip has no inductors and features a coupled latch with shared-current-source and buffer-insertion scheme, a divide-by-2 circuit with a static frequency divider, and a DLL. The measured eye-opening width and height are 71.3% and 52%, respectively. The 1.05 \times 0.92mm² chip consumes 210mW from a 1.2V supply.

28.10 104Gb/s 2¹¹-1 and 110Gb/s 2⁹-1 PRBS Generator in InP HBT Technology

12:00 AM

T. Kjellberg, J. Hallin, T. Swahn

Chalmers University of Technology, Göteborg, Sweden

A 2¹¹-1 PRBS generator with one output at a maximum data rate of 104Gb/s and 4 parallel outputs at 52Gb/s is presented together with a 2⁹-1 PRBS generator with a single output at 110Gb/s. The ICs are implemented in a 300GHz f_T InP HBT technology. The generator core is clocked at half the data rate of the high-speed output for both circuits. They dissipate 2.8W and 2.2W from a -3.5V supply, respectively.

Conclusion

12:15 PM

SESSION 29

POWER MANAGEMENT AND DISTRIBUTION

Chair: Atila Alvandpour, Linköping University, Sweden

Associate Chair: Hannu Tenhunen, Royal Institute of Technology, Sweden

29.1 Power Distribution Measurements of the Dual Core PowerPC™ 970MP Microprocessor

1:30 PM

H. Hamann¹, A. Weger¹, J. Lacey¹, E. Cohen², C. Atherton²

¹IBM, Yorktown Heights, NY

²IBM, Essex Junction, VT

Spatially-resolved imaging of microprocessor power (SIMP) is shown to be a critical tool for measuring temperature and power distributions of a microprocessor under full operating conditions. In this paper, the SIMP technique is applied to the dual-core PowerPC 970MP microprocessor.

29.2 A Linear Regulator with Fast Digital Control for Biasing Integrated DC-to-DC Converters

2:00 PM

P. Hazucha¹, S. Moon¹, G. Schrom¹, F. Paillet¹, D. Gardner¹, S. Rajapandiar², T. Karnik²

¹Intel, Hillsboro, OR

²Silicon Laboratories, Austin, TX

A high-voltage-tolerant 2.4 to 1.2V push-pull linear regulator with 1A output, 288ps response time, and 97.5% current efficiency for biasing integrated dc-to-dc converters is introduced. The regulator occupies 0.03mm² in 90nm CMOS and achieves 33A/mm² current density. Digital control with a flash ADC and a digital-to-current converter improve speed-power performance by 3X.

29.3 Increasing Microprocessor Speed by Massive Application of On-Die High-K MIM Decoupling Capacitors

2:30 PM

H. Sánchez, B. Johnstone, D. Roberts, O. Mandhana, B. Melnick, M. Celik, M. Baker, J. Hayden, B. Min, J. Edgerton, B. White

Freescale Semiconductor, Austin, TX

A 90nm SOI microprocessor with massive application of high-K MIM decoupling capacitor modules is proven to increase the maximum frequency of the processor by close to 10%. Simulations predict reduced power supply noise leading to improvements in Fmax by close to the equivalent of a transistor node increase. Simulations of applying MIM decoupling capacitors to high-speed I/O and PLL circuits show that they can further enhance performance and area requirements for these critical circuits in advanced technologies.

Break 3:00 PM

29.4 Hierarchical Power Distribution with 20 Power Domains in 90nm Low-Power Multi-CPU Processor

3:15 PM

Y. Kannō¹, H. Mizuno¹, Y. Yasu¹, K. Hirose², Y. Shimazaki², T. Hoshi², Y. Miyairi², T. Ishii², T. Yamada³, T. Irita³, T. Hattori³, K. Yanagisawa³, N. Irie³

¹Hitachi, Tokyo, Japan; ²Renesas Technology, Tokyo, Japan

³Hitachi, Fukuoka, Japan

Hierarchical power distribution using a power tree is developed. It supports fine-grained power gating with dozens of power domains like fine-grained clock gating and effectively reduces leakage currents for 1-million-gate power domains to 1/4000 in multi-CPU processors with minimal area overhead. This paper demonstrates the integration of 20 power domains in a 90nm single-chip 3G cellular phone processor.

29.5 A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor

3:30 PM

T. Hattori¹, T. Irita¹, M. Ito¹, E. Yamamoto¹, H. Kato¹, G. Sado¹, T. Yamada¹, K. Nishiyama¹, H. Yagi¹, T. Koike¹, Y. Tsuchihashi¹, M. Higashida¹, H. Asano¹, I. Hayashibara¹, K. Tatezawa¹, Y. Shimazaki¹, N. Morino¹, K. Hirose¹, S. Tamaki¹, S. Yoshioka¹, R. Tsuchihashi², N. Arai², T. Akiyama², K. Ohno²

¹Renesas Technology, Tokyo, Japan

²NTT DoCoMo, Tokyo, Japan

A power-management scheme for a single-chip multi-CPU processor uses 20 power domains. The scheme enables the minimization of leakage currents in each operating mode: 299 μ A in paging operation and 7 μ A in stand-by. The techniques for controlling and implementing power domains are also described.

29.6 A Signal-Integrity Self-Test Concept for Debugging Nanometer CMOS ICs

3:45 PM

V. Petrescu¹, M. Pelgrom¹, H. Veendrick¹, P. Pavithran², J. Wieling²

¹Philips, Eindhoven, The Netherlands

²Philips, Nijmegen, The Netherlands

A fully integrated signal-integrity self-test concept is implemented in a 90nm CMOS process. The outputs of different analog monitors are locally converted to digital form and then transported through a test-compatible scan chain. The temperature monitor has 4b resolution. The supply-noise monitor detects 10ps-wide pulses of 20mV. The total area overhead is <0.1%.

29.7 ESD Protection for Mixed-Voltage I/O in Low-Voltage Thin-Oxide CMOS

4:15 PM

M-D. Ker, W-J. Chang, C-T. Wang, W-Y. Chen

National Chiao-Tung University, Hsin-Chu, Taiwan

An ESD protection design for 1.2V/2.5V mixed-voltage I/O interfaces is discussed. A high-voltage-tolerant power-rail ESD clamp circuit is used; it is realized with low-voltage devices in a 0.13 μ m CMOS process. The four-mode ESD stresses on the mixed-voltage I/O pad and the whole-chip pin-to-pin ESD protection can be discharged by the proposed ESD protection scheme.

29.8 A Circuit for Reducing Large Transient Current Effects on a Processor Power Grid

4:45 PM

E. Hailu¹, D. W. Boerstler¹, K. Mik², J. Qi¹, M. Wang¹, M. Riley¹

¹IBM, Austin, TX

²Toshiba, Kawasaki, Japan

A circuit that reduces power supply transients by controlling the frequency ramp between the initial and final operating frequencies of a microprocessor is presented. This is accomplished by periodically 'masking' clock pulses to incrementally increase or decrease the average clock frequency until the final clock frequency is reached. This circuit is implemented in a 90nm partially-depleted SOI technology.

Conclusion

5:15 PM

SESSION 30

SILICON FOR BIOLOGY

Chair: Glenn Gulak, University of Toronto, Toronto, Canada
Associate Chair: Hoi-Jun Yoo, KAIST, Daejeon, Korea

30.1 Neurons to Silicon: Implantable Prosthesis Processor

1:30 PM

S. O'Driscoll, T. Meng, K. Shenoy, C. Kemere
Stanford University, Stanford, CA

A processor architecture for neural prosthesis control is described. It implements real-time neural decoding from a permanently implanted electrode array to reduce the data rate from 80Mb/s to 20b/s, minimizing the wireless communication requirements. The neural signals are digitized by a 100-channel 100kS/s adaptive-resolution ADC array consuming 1 μ W per channel.

30.2 A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System

2:00 PM

R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, R. Normann, F. Solzbacher
University of Utah, Salt Lake City, UT

An implantable IC receives power and commands wirelessly through an ASK inductive link, and transmits amplified neural data using a 433MHz FSK transmitter. A 10 \times 10 array of platinum-tipped silicon electrodes interfaces with a flip-chip bonded 4.7 \times 5.9mm² 0.5 μ m 3M2P CMOS 13.5mW IC containing 88 neural amplifiers, 9b ADC and spike detectors used for data reduction.

30.3 A 360-Channel Speech Preprocessor that Emulates the Cochlear Amplifier

2:30 PM

B. Wen, K. Boahen
University of Pennsylvania, Philadelphia, PA

A cochlea-based preprocessor for speech recognition emulates the fluid ducts with two 4680-element diffusive grids, the basilar membrane with 360 2nd-order sections, and the auditory nerve with 2160 pulse-frequency modulators. Integrated in 10.9mm² in 0.25 μ m CMOS and consuming 52mW, this silicon cochlea employs active bidirectional coupling, a selective amplification mechanism that sharpens tuning (Q_{10} is 2.7) and controls gain (24dB compression).

Break 3:00 PM

30.4 A 2Mb/s Wideband Pulse Transceiver with Direct-Coupled Interface for Human-Body Communications

3:15 PM

S-J. Song, N. Cho, S. Kim, J. Yoo, H-J. Yoo
KAIST, Daejeon, Korea

A battery-powered wideband pulse transceiver with a direct-coupled interface is presented for human-body communications. The optimum channel bandwidth of 10kHz to 100MHz is identified as the Bodywire Channel. The transceiver based on all-digital CDR circuit with quadratic sampling technique has 2Mb/s data rate at a BER of 10^{-7} . The 0.25 μ m CMOS transceiver occupies 0.85mm² and consumes less than 0.2mW from a 1V supply.

30.5 A CMOS Integrated DNA chip for Quantitative DNA Analysis

3:45 PM

M. Gemma¹, S-I. O'uchi^{1,2}, H. Funaki¹, J. Okada¹, S. Hongo¹

¹Toshiba, Kawasaki, Japan

²National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan

Quantitative gene expression analysis, based on an electrochemical DNA-detection method uses immobilized DNA probes on Au electrodes with diameters from 200 μ m to 2 μ m. Cyclic voltammetry is used to measure anodic current from the intercalators. The 25 \times 3mm² IC, fabricated in 1 μ m 2M CMOS, contains 40 electrodes, 1600 transistors and dissipates 150mW at \pm 3.3V.

30.6 A Wireless Bio-MEMS Sensor for C-Reactive Protein Detection Based on Nanomechanics

4:15 PM

C-H. Chen¹, R-Z. Hwang¹, L-S. Huang¹, S. Lin¹, H-C. Chen¹, Y-C. Yang¹, Y-T. Lin¹, S-A. Yu¹, Y-H. Wang², N-K. Chou², S-S. Lu¹

¹National Taiwan University, Taipei, Taiwan

²National Taiwan University Hospital, Taipei, Taiwan

A quick (<30min.), label-free detection of disease-related C-reactive proteins (CRP) is achieved using a 200 μ m MEMS microcantilever housed in a 7 \times 7mm² reaction chamber. The deflection of the cantilever due to specific CRP/anti-CRP binding is detected using a position-sensitive photodiode and the converted bio-signal is transmitted by a wireless ASK transceiver IC fabricated in a 0.18 μ m CMOS process. CRP concentrations from 1 μ g/mL to 500 μ g/mL can be detected. A 0.2Hz 1V ac signal is applied to the bio-MEMS sensor to unbind CRP from the cantilever for reuse.

Conclusion

4:45 PM

SESSION 31

VERY HIGH-SPEED ADCs AND DACs

Chair: Dieter Draxelmayr, Infineon, Villach, Austria

Associate Chair: Gabriele Manganaro, National Semiconductor, Salem, NH

31.1 A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process

1:30 PM

G. Van der Plas, S. Decoutere, S. Donnay
IMEC, Leuven, Belgium

A high-speed 4b flash ADC in 90nm digital CMOS is presented that uses a dynamic offset-compensation scheme in its comparators. It achieves a sampling rate of 1.25GS/s with 3.7 ENOB (23.8dB SNDR) from dc to Nyquist while consuming 2.5mW. It has an energy per conversion step of 0.16pJ.

31.2 A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC

2:00 PM

P. Figueiredo¹, P. Cardoso¹, A. Lopes¹, C. Fachada¹, N. Hamanishi², K. Tanabe², J. Vital¹

¹Chipidea Microelectrónica, Porto Salvo, Portugal

²Toshiba, Kawasaki, Japan

A 1.2V 6b 1GS/s ADC is fabricated in a 90nm CMOS process, occupies 0.13mm², and consumes 55mW. This ADC uses background offset-calibration to enable the use of minimum-size devices in pre-amplifiers and comparators. A solution that guarantees fast selection of the important reference voltages, and halves the number of switches in the resistor ladder, further improves high-frequency performance.

31.3 A 4GS/s 4b Flash ADC in 0.18μm CMOS

2:30 PM

S. Park¹, Y. Palaskas², M. Flynn¹

¹University of Michigan at Ann Arbor, Ann Arbor, MI

²Intel, Hillsboro, OR

A 0.18μm CMOS 4GS/s non-interleaved 4b flash ADC is presented. A comparator with a 32×32μm² on-chip inductor extends sampling rate without extra power consumption. DAC trimming and comparator redundancy reduce DNL and INL to less than 0.15LSB and 0.24LSB, respectively. The measured ENOB is 3.84b and 3.48b at 3GS/s and 4GS/s, respectively. The ADC achieves a BER of less than 10⁻⁸.

31.4 A 22GS/s 5b ADC in 130nm SiGe BiCMOS

2:45 PM

P. Schvan, D. Pollex, S-C. Wang, C. Falt, N. Ben-Hamida
Nortel, Ottawa, Canada

A 22GS/s 5b ADC implemented in 130nm SiGe BiCMOS technology is presented. The ADC has 0.64V input range and achieves 4.4b and 3.5b ENOB with 34dB and 29dB SFDR at 5GHz and 7GHz input frequencies, respectively. Measured DNL and INL are <0.5LSB and BER is 10⁻⁴ at 22GS/s. The ADC consumes 3W from a 3.3V supply.

Break 3:00 PM

31.5 A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13 μ m CMOS **3:15 PM**
S-W. Chen, R. Brodersen
University of California, Berkeley, CA

A 1.2V 6b ADC using asynchronous processing with dual time interleaving and non-binary successive approximation achieves 600MS/s while dissipating 5.3mW in a 0.13 μ m CMOS process. A capacitive ladder network is used to reduce the input capacitance without compromising matching accuracy. The ADC occupies an active area of 0.12mm² and has an input 3dB BW of over 4GHz.

31.6 A 1GS/s 11b Time-Interleaved ADC in 0.13 μ m CMOS **3:45 PM**
S. Gupta, M. Choi, M. Inerfield, J. Wang
Teranetics, Santa Clara, CA

A time-interleaved ADC architecture that eliminates the need to correct timing offsets and is scalable to high sampling rates is presented. This 1GS/s 11b ADC has 55dB peak SNDR, consumes 250mW power, and occupies 3.5mm² area.

31.7 A Bandpass $\Delta\Sigma$ RF-DAC with Embedded FIR Reconstruction Filter **4:15 PM**
S. Taleie, T. Copani, B. Bakkaloglu, S. Kiaei
Arizona State University, Tempe, AZ

A 1b bandpass $\Delta\Sigma$ DAC followed by a current steering FIR reconstruction filter and an embedded up-conversion mixer is presented. The RF DAC is implemented in 0.25 μ m digital CMOS, can be used in low-power digital-IF transmitters and eliminates the need for a transimpedance stage and a separate mixer. The RF DAC draws 49mA from a 2.5V supply, achieving -64.7dBc IM3 at 1.03GHz with an SFDR of 72dB in a 15MHz bandwidth.

31.8 A 0.36W 6b up to 20GS/s DAC for UWB Wave Formation **4:45 PM**
D. Baranauskas, D. Zelenin
Pulse~Link, Carlsbad, CA

A 6b up to 20GS/s DAC is presented. The DAC is used for direct synthesis of modulated waveforms for UWB communication. The DAC has a current-steering architecture for achieving 20GS/s, a 1.8V power supply, a 4:1 MUX for reducing the line data rate, and BIST. Fabricated in a SiGe process, it consumes 0.36W and has a FOM of 0.28pJ.

31.9 A 14b 100MS/s DAC with Fully Segmented Dynamic Element Matching **5:00 PM**
K. Chan, I. Galton
University of California, San Diego, CA

A 14b 100MS/s Nyquist-rate DAC using a segmented dynamic-element-matching technique involving all the DAC elements is demonstrated. The DAC is implemented in a 0.18 μ m CMOS process and worst-case SFDRs across Nyquist bands are 74.4dB and 78.9dB for sample-rates of 100MS/s and 70Ms/s, respectively.

Conclusion 5:15 PM

SESSION 32

PLLS, VCOS, AND DIVIDERS

Chair: Ian Galton, University of California, San Diego, La Jolla, California

Associate Chair: Takehiko Nakao, Toshiba, Kawasaki, Japan

32.1 A PVT-Tolerant Low-1/f-Noise Dual-Loop Hybrid PLL in 0.18 μ m CMOS

1:30 PM

H-R. Lee¹, O. Kim², K. Jung², J. Shir², D-K. Jeong¹

¹Seoul National University, Seoul, Korea;

²Silicon Image, Sunnyvale, CA

A dual-loop analog-digital hybrid PLL with a small-bandwidth digital loop and large-bandwidth analog loop achieves low jitter by suppressing 1/f noise and does not require off-chip R or C. The operating range using a narrow-range VCO is from 10 to 200MHz. The output jitter over this range is $<0.028U_{pp}$. The chip is implemented in a 0.18 μ m CMOS process and consumes 50mW from a 1.8V supply.

32.2 A 0.5 to 2.5GHz PLL with Fully Differential Supply-Regulated Tuning

2:00 PM

M. Brownlee, P. Hanumolu, K. Mayaram, U. Moon

Oregon State University, Corvallis, OR

A PLL uses a fully differential supply-regulated tuning scheme to combat power-supply noise. The charge pump uses a resistor to set the current and reduce the flicker noise corner. Fabricated in a 0.18 μ m CMOS process, the PLL area is 0.15mm². Operating at 2.4GHz, it has 3.29ps_{rms} jitter, a frequency range of 0.5 to 2.5GHz, and draws 14mA from a 1.8V supply.

32.3 A PLL for a DVDx16 Write System with 63 Output Phases and 32ps Resolution

2:30 PM

S. Dosho, S. Sakiyama, N. Takeda, Y. Tokunaga, T. Morie

Matsushita Electric, Moriguchi, Japan

A current-controlled oscillator (CCO) with 32ps phase resolution is realized by coupling ring oscillators in a 65nm CMOS process. A compact layout method achieves 36 \times 46 μ m² area and multiphase outputs whose timing errors are small. A CCO with 63 output phases is used in the PLL for a DVDx16 write system. The measured DNL of the output phases is within 1.0LSB at 490MHz.

Break 3:00 PM

32.4 A Spur Suppression Technique for Phase-Locked Frequency Synthesizers

3:15 PM

T-C. Lee, W-L. Lee

National Taiwan University, Taipei, Taiwan

A 4.8GHz integer- N frequency synthesizer with distributed phase-frequency detectors and charge pumps moves spurious tones to higher frequencies and reduces the spur levels. PPM is used to relax the analog circuit accuracy requirement. The circuit is fabricated in a 0.18 μ m CMOS technology, dissipates 18mW from a 1.8V supply and suppresses sidebands by 10dB.

-
- 32.5 A 6.25GHz 1V LC-PLL in 0.13 μ m CMOS** **3:45 PM**
R. Gu, A-H. Yee, Y Xie, W. Lee
Texas Instruments, Dallas, TX
- A 6.25GHz PLL with integrated LC-tank VCO, on-chip loop filter and quadrature outputs is fabricated in 0.13 μ m CMOS technology. Operated at 1V supply with 62.5MHz input reference clock frequency, an output clock jitter of 0.5ps_{rms} is achieved by using a charge pump with rail-to-rail operation and leakage-current cancellation.
- 32.6 A Reversible Poly-Phase Distributed VCO** **4:15 PM**
N. Tzartzanis, W. Walker
Fujitsu, Sunnyvale, CA
- A reversible 24-phase closed-loop distributed VCO is implemented in 90nm 10M triple-well 1.2V CMOS using co-planar transmission lines as delay elements. The measured tuning range is 10.4 to 11.4GHz, the phase noise is -96.65dBc/Hz at 1MHz offset, and the circuit uses 70mW from a 1.2V supply.
- 32.7 A Combined Dynamic and Static Frequency Divider for a 40GHz PLL in 80nm CMOS** **4:30 PM**
G. von Büren¹, C. Kromer¹, F. Ellinger¹, A. Huber², M. Schmatz³, H. Jäckel¹
¹ETH Zürich, Zürich, Switzerland; ²ZMA, Windisch, Switzerland
³IBM, Rüschlikon, Switzerland
- A divide-by-4 circuit operates for input frequencies from 31 to 41GHz at signal amplitudes $\leq 0.5V_{pp}$. The circuit consists of a dynamic followed by a static frequency divider. The dynamic and static frequency dividers consume 2mA and 1mA, respectively, from a 1.1V supply.
- 32.8 70GHz CMOS Harmonic Injection-Locked Divider** **4:45 PM**
K. Yamamoto, M. Fujishima
University of Tokyo, Kashiwa-shi, Japan
- A 70GHz CMOS harmonic injection-locked divider (HILD) is presented, where a third-harmonic mixer is realized by a differential-voltage-driven MOSFET. The chip is fabricated in a 6M 90nm CMOS process. A maximum operating frequency of 71.6GHz with a locking range of 12% at a supply voltage of 0.5V is measured. The chip consumes 2.75mW.
- 32.9 A 16-to-18GHz 0.18 μ m Epi-CMOS Divide-By-3 Injection-Locked Frequency Divider** **5:00 PM**
H. Wu, L. Zhang
University of Rochester, Rochester, NY
- A 16-to-18GHz injection-locked divide-by-3 frequency divider is implemented in a 0.18 μ m epi-CMOS process. It achieves 1GHz locking range with 3.7dBm injection power. The phase noise is close to the theoretical value of 9.5dB below the input signal. Spiral inductors are fabricated using the 2 μ m-thick top metal layer and the divider core draws 2.55mA from a 1.8V supply.
- Conclusion** **5:15 PM**
-

SESSION 33

MOBILE TV

Chair: Bud Taddiken, Microtune, Plano, TX
Associate Chair: Sang-Gug Lee, ICU, Daejeon, Korea

33.1 A 0.18 μ m CMOS Dual-Band Direct-Conversion DVB-H Receiver **1:30 PM**

I. Vassiliou, K. Vavelidis, S. Bouras, S. Kavadias, Y. Kokolakis, G. Kamoulakos, A. Kyranas, C. Kapnistis, N. Haralabidis
Athena Semiconductors, Athens-Alimos, Greece

A 0.18 μ m CMOS direct-conversion dual-band DVB-H receiver occupies 9.7mm² and achieves a 4dB/5dB NF at UHF/L-band, eliminating the need for an external LNA. By using a fractional-N synthesizer, the 470 to 890MHz and 1.4 to 1.8GHz bands are supported while achieving an integrated phase noise of <-41dBc. 6th-order LPF support channel bandwidths from 4 to 10 MHz. The overall power consumption is 295mW/280mW for continuous operation in the UHF/L-Band, respectively.

33.2 A Multi-Band Multi-Mode CMOS Direct-Conversion DVB-H Tuner **2:00 PM**

Y-J. Kim, J-W. Kim, V. Pakhomenko, D. Baek, J-H. Lee, E-Y. Sung, I. Nam, B-H. Park
Samsung, Yongin-City, Korea

A direct-conversion tuner is fabricated in a 0.18 μ m CMOS process. The vertical BJT is adopted to minimize the effects of 1/f noise. The tuner has a NF of 4.5dB (5dB), IIP3 of -5dBm (-6dBm), IIP2 of >40dBm, sensitivity of -89dBm (-88.5dBm) for 16-QAM CR 1/2, and draws 66mA (74mA) from a 2.8V for UHF (USA L-Band).

33.3 Dual-Band Single-Ended-Input Direct-Conversion DVB-H Receiver **2:30 PM**

M. Womac, A. Deiss, T. Davis, R. Spencer, B. Abesingha, P. Hisayasu
Microtune, Plano, TX

A 340mW single-chip direct-conversion tuner with single-ended input for UHF and L-band DVB-H is fabricated in a 0.35 μ m BiCMOS process. Included are 3 parallel LNAs, 2 I/Q mixers, 7th-order baseband filters, a fractional-N synthesizer, and dc-offset circuits. The NF is <3.6dB at maximum gain of >80dB, sensitivity is <-88dBm for 16-QAM CR 2/3, gain range is >60dB, IIP3 is >4dBm, IIP2 is >27dBm, die area is 12.25mm², and supply voltage is 2.7V.

Break 3:00 PM

33.4 A Dual-Channel Direct-Conversion CMOS Receiver for Mobile Multimedia Broadcasting **3:15 PM**

V. Peluso, Y. Xu, P. Gazzero, Y. Tang, L. Liu, Z. Li, W. Xiong, C. Persico
Qualcomm, San Diego, CA

A 0.25 μ m CMOS receiver circuit that operates from 698MHz to 746MHz, a spectrum allocated by the FCC for advanced mobile services for multimedia applications, is presented. The receiver supports an OFDM physical layer with modulation ranging from BPSK for pilot carriers to 16-QAM for high-rate data carriers. The RX has a NF of 2.6dB and an out-of-band IIP3 of -5.5dBm. It occupies 7mm² and draws 61mA from a 2.6V supply.

33.5 A 100mW Dual-Band CMOS Mobile-TV Tuner IC for T-DMB/DAB and ISDB-T**3:45 PM***B-K. Kim, T. Kim, Y. Cho, M-S. Jeong, S. Kim, H. Yoo, S-M. Moon, T-J. Lee, J-K. Lim, B-E. Kim*

Integrant Technologies, Seongnam, Korea

A 0.18 μ m CMOS dual-band low-IF mobile-TV tuner IC for T-DMB/DAB that supports Band-III and L-Band is presented. By modifying a few metal and via masks, the IC can support VHF and UHF bands for ISDB-T partial reception. The chip meets all the specifications of both applications with a sensitivity of <-98dBm while consuming 100mW from a 1.8V supply and occupying 3.4 \times 3.3mm².

33.6 A 1.8dB NF 112mW Single-Chip Diversity Tuner for 2.6GHz S-DMB Applications**4:15 PM***M-W. Hwang^{1,2}, S. Beck¹, S. Min¹, S. Lee¹, S. Yoo¹, K. Lim¹, H. Jung, J-C. Lee¹, J-C. Lee¹, S. Hong¹, G-H. Cho², S. Han¹*¹FCI, Seongnam, Korea; ²KAIST, Daejeon, Korea

The fully-monolithic diversity 2.6GHz S-DMB tuner IC features a NF of <1.8dB, a path isolation of over 25dB, a DR of over 100dB with <4dB path gain mismatch and a power consumption of 112mW. This IC is implemented in a 0.25 μ m SiGe BiCMOS process. The chip is verified in S-DMB systems using several commercially available S-DMB demodulator chips.

33.7 A sub-1.5^o_{rms} Phase-Noise Ring-Oscillator-Based Frequency Synthesizer for Low-IF Single-chip DBS Satellite Tuner-Demodulator SoC**4:45 PM***A. Maxim, R. Poorfard, J. Kao*
Silicon Laboratories, Austin, TX

A fully integrated 0.13 μ m CMOS ring-oscillator-based PLL for low-IF single-chip DBS satellite tuner-demodulator IC is presented. A noise-attenuating loop filter reduces the oscillator gain, helping both front-end noise and spur rejection and allowing the on-chip integration of the filter capacitance. The PLL shows <1.5^o_{rms} double-sided integrated phase noise, <-60dBc reference spurs, <-50dBc coupled spurs. It occupies 0.3mm² die area and consumes 40mA at 3.3V.

Conclusion**5:00 PM**

Chair: Bruce Bateman, T-RAM, San Jose, CA

Associate Chair: Jinyong Chung, Postech, Pohang, Korea

34.1 A 5.6GHz 64KB Dual-Read Data Cache for the POWER6™ Processor
1:30 PM

*J. Davis¹, D. Plass¹, P. Bunce¹, Y. Chan¹, A. Pelella¹, R. Joshf², A. Chen¹, W. Huott²,
T. Knips¹, P. Patel¹, K. Lo¹, E. Fluhr³*

¹IBM, Poughkeepsie, NY

²IBM, Yorktown Heights, NY

³IBM, Austin, TX

A dual-read 8-way set-associative data cache comprising four 16kB SRAMs and 2 set-prediction macros per POWER6 core is presented. The array utilizes a $0.75\mu\text{m}^2$ butted-junction split-wordline 6T cell in 65nm SOI. The design features dual power supplies, unidirectional polysilicon, and hierarchical unclamped bitlines for enhanced cell stability and performance.

34.2 A 4.2GHz 1.375mm² 256kb Dual-V_{cc} SRAM Building Block in 65nm CMOS
2:00 PM

*M. Khellah, N. Kim, J. Howard, G. Ruhl, Y. Ye, D. Somasekhar, N. Borkar,
F. Hamzaoglu, G. Pandya, A. Farhang, K. Zhang, V. De, J. Tschanz, M. Sunna*
Intel, Hillsboro, OR

An SRAM macro, implemented in a 65nm CMOS process, uses a dual supply to maximize density while enabling the use of low voltage for the processor core. Measurements of a 256kb block show 4.2GHz operation using 29mW from 1.2V at 85°C, with core logic operating down to 0.7V and a sleep biasing scheme that autonomously compensates for PVT and aging.

34.3 A 72Mb Separate-I/O Synchronous SRAM Chip with 504Gb/s Data Bandwidth
2:30 PM

*C. Tseng¹, J-H. Kim¹, S. Chen¹, M-H. Huang¹, C. Lu¹, I. Hashiguchi², Y. Miyazima²,
M. Ichihashi², K. Maki², P. Chuang¹*

¹Sony, San Jose, CA

²Sony, Nagasaki, Japan

A 72Mb 6T SRAM is designed with 2×144 separate-I/O and random R/W in parallel per cycle running at 875MHz DDR to achieve 504Gb/s bandwidth. It is fabricated in a 90nm CMOS process. Dual R/W self-timed clocks with core emulators are multiplexed to operate the SRAM core at 875MHz. On-chip DLL, programmable I/O skews, and programmable input termination and output driver impedance with precise linearity are essential for this 504Gb/s interface.

Break 3:00 PM

34.4 A 256kb Sub-threshold SRAM in 65nm CMOS

3:15 PM

B. Calhoun, A. Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA

A 256kb sub-threshold SRAM operates below 400mV from 0 to 85°C and is implemented in 65nm CMOS technology. For the same 6σ static-noise margin, the sub-threshold SRAM at 0.4V achieves 2.25-times lower leakage power and 2.25-times lower active energy than its 6T counterpart at 0.6V. The SRAM uses a 10T bitcell to enable sub-threshold functionality.

34.5 Redefinition of Write Margin for Next-Generation SRAM and Write-Margin Monitoring Circuit

3:45 PM

K. Takeda¹, H. Ikeda¹, Y. Hagihara¹, M. Nomura¹, H. Kobatake²

¹NEC, Sagamihara, Japan

²NEC, Kawasaki, Japan

We redefine write margin in order to be able to quantify the effect of both PVT variation and write-margin improvement. A write-margin monitoring circuit based on this definition is implemented in a 90nm CMOS process. This circuit can be applied to an SRAM power supply circuit to improve the write margin.

34.6 Thyristor-Based Volatile Memory in Nano-Scale CMOS

4:15 PM

R. Roy, F. Nematy, K. Young, B. Bateman, R. Chopra, S-O. Jung, C. Show, H-J. Cho
T-RAM Semiconductor, San Jose, CA

A thyristor-based memory cell technology provides SRAM-like performance at 2x to 3x the density of conventional 6T SRAM. The technology is readily embedded into conventional nano-scale CMOS and scales into future SOI and FinFET technologies. A 19mm² 0.13μm 9Mb SOI test chip has a 0.562μm² cell with a cell-R/W time <2ns.

Conclusion

4:45 PM

SHORT COURSE

Analog-to-Digital Converters

This **Short Course** is intended to provide both entry-level and experienced engineers with practical approaches to the design of analog-to-digital converters. The course provides an overall perspective on the technology considerations, circuit-design issues, and detailed design strategies, for circuit building blocks in analog-to-digital converters. Topics covered address the challenges faced by analog designers in current and future technologies, with an emphasis on detailed circuit-design approaches, and methodologies for deep-submicron integration.

To Register, please use the ISSCC2006 Registration Form on the Advance-Program Centerfold. **Sign-in** is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00 AM on Thursday, February 9, 2006.

The Short Course will be offered twice on Thursday, February 9:

The first offering is scheduled for **8:00AM to 4:30PM**.

The second offering is scheduled for **10:00AM to 6:30PM**.

A DVD of the Short Course & Selected Referenced Papers: Short-Course registrants will receive a DVD a month or so after the Conference. They can register to receive the DVD at registration time. This DVD includes: (1) The visuals of the four Short-Course presentations in PDF format, for printing hard copies; (2) Audio recording of the presentation along with a written transcription; (3) Bibliographies of background papers for all four presentations; and (4) PDF copies of selected relevant background material and important papers in the field (10 to 20 papers per presentation).

OUTLINE

Fundamental Limits and Practical Design Issues in A/D Converters

In this presentation, fundamental limitations of ADCs associated with noise, clock jitter, power consumption, and conversion rate, are discussed. Figures-of-merit (FoM) based on these fundamental limits will be compared in various ADC topologies including flash, pipeline, successive-approximation, and $\Delta\Sigma$ converters. Design strategies for improving FoMs in practical ADCs will also be discussed. Finally, practical design issues, such as component mismatch, finite-gain effects, charge injection, and substrate noise with techniques for reducing its effects, will be described.

Instructor: Hae-Seung Lee received his Ph.D. from the University of California, Berkeley, in 1984, where he pioneered self-calibration techniques for A/D converters. In 1984, he joined the faculty at the Massachusetts Institute of Technology, Cambridge, MA, where he is now Professor and Director of the Center for Integrated Circuits and Systems. Since 1985, he has acted as a consultant to Analog Devices, Lincoln Laboratories, and Cypress Semiconductor. He has authored or co-authored more than 100 journal and conference papers. He is a Fellow of the IEEE.

Pipelined A/D Converters

As CMOS processes scale down, ADC designers benefit greatly from both device speed and lithographic accuracy: Device speed contributes directly to the prevailing trend toward oversampling techniques in high-resolution ADC designs. On the other hand, finer-line feature size offers better component matching for a fixed device size, and Nyquist-rate pipelined techniques still provide power- and area-efficient solutions for high-speed medium-resolution applications. Correspondingly, advanced pipelined ADC techniques have been further developed to enhance resolution. This presentation begins by identifying the fundamental limits in achieving accuracy and speed with basic pipelining techniques. It will then focus on design issues related to high speed and high resolution.

Instructor: Bang-Sup Song received his Ph.D. from the University of California, Berkeley, in 1983. He was with AT&T Bell Laboratories, Murray Hill, and the ECE Department, University of Illinois, Urbana-Champaign, before he joined the ECE Department, University of California, San Diego, in 1999, where he is endowed as the Charles Lee Powell Chair Professor in Wireless Communication. His current interest is in CMOS analog circuits including data converters, wireless transceivers, TV tuners, frequency synthesizers, image-rejection techniques, active filters, and timing recovery. His research has been focused on improving analog-circuit performance using digital aids. He is an IEEE Fellow.

$\Delta\Sigma$ ADCs

Delta-sigma ADCs are the preferred architecture when dynamic-range requirements exceed 13 bits or so. This presentation will explore the most important properties of delta-sigma ADCs, including inherent linearity, and (for continuous-time systems) inherent anti-aliasing. These properties are illustrated in the context of the simplest delta-sigma ADC, the first-order modulator, and then generalized to second- and higher-order modulators. Then, bandpass modulation, quadrature modulation, cascade modulation, and mismatch-shaping, are introduced, and shown to fit into the same basic framework, namely that of high-gain linear feedback around a nonlinear element. Each of these delta-sigma variants is illustrated with examples constructed using the Delta-Sigma Toolbox.

Instructor: Richard Schreier received his Ph.D. from the University of Toronto, in 1991. From 1985 to 1987, he worked at Bell-Northern Research in Ottawa, Canada, and, from 1991 to 1997, he was an Assistant/Associate Professor at Oregon State University in Corvallis. Since 1997, he has been working for Analog Devices, Inc. in Wilmington, Massachusetts. In 2002, he received the ISSCC outstanding-paper award for a paper describing a 50mW bandpass delta-sigma ADC with 90dB of dynamic range, and 300kHz of bandwidth. He co-edited an IEEE Press book (with S.R. Norsworthy and G.C. Temes), published in 1997. His second book (with G.C. Temes) on delta-sigma modulation was published in 2004. He is also the author of the freeware Delta-Sigma Toolbox for MATLAB.

Sub-1V Analog-to-Digital Converters

The analog-to-digital converter is an important analog-interface circuit-block. However, it is becoming a critical bottleneck in mixed-signal IC systems, as CMOS-transistor dimensions shrink in state-of-the-art technology. This is due to the fact that transistors of smaller dimensions can tolerate only a proportionally smaller voltage stress. This presentation will review the low-voltage problem, summarize some of the well-known solutions currently in use (and their associated problems), and introduce recently-developed circuit techniques. A few IC-implementation results for both oversampling and Nyquist analog-to-digital converters which operate below 1V will be presented as possible design solutions for future low-voltage submicron CMOS processes.

Instructor: Un-Ku Moon received his B.S. from the University of Washington, his M.Eng. from Cornell University, and his Ph.D. from the University of Illinois, Urbana-Champaign, all in electrical engineering. He has been with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, since 1998, where he is currently an Associate Professor. Before joining Oregon State University, he was with Bell Laboratories from 1994 to 1998, as well as from 1988 to 1989. His research interests include highly-linear and tunable continuous-time filters, telecommunication circuits including timing-recovery and data-converters, and ultra-low-voltage analog circuits.

CIRCUIT DESIGN FORUM

F4: COLOR IMAGING

Organizer: Albert Theuwissen, *DALSA, Eindhoven, The Netherlands*

Committee: Dan McGrath, *Eastman Kodak, Rochester, NY*
Jed Hurwitz, *Gigle Semiconductor, Edinburgh, United Kingdom*,
Hirofumi Sumi, *Sony, Tokyo, Japan*
Boyd Fowler, *Agilent, Palo Alto, CA*
Ralph Etienne-Cummings, *John Hopkins University, Baltimore, MD*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Takao Kuroda, *Matsushita, Kyoto, Japan*
Johannes Solhusvik, *Micron Technology, Pasadena, CA*

Color Imaging is a very interesting topic, because the signals that are delivered by the image sensor or the imaging system are not colored at all! Color imaging relies very much on all kinds of signal-processing tricks and optimizations. On the other hand, silicon chips react in a completely different way to color signals than the human visual system reacts. That makes color imaging quite complex and difficult! To contribute to a better understanding of the color imaging, and to stimulate creativity in this field, the ISSCC Subcommittee on Imagers has organized a forum around this theme.

The speakers at the forum are world experts in their fields. They are invited to present up-to-date material on various topics. The presentations are intended to address the material in all of its technical detail.

In the first presentations, the human visual system will be discussed. Certain aspects of color perception are quantitatively summarized in standard color spaces (e.g., CIE-XYZ and CIELAB), and the experimental and biological basis for these color spaces will be explained. The second presentation will provide an overview of color-imaging systems and will discuss which is the best sensor to produce the most-beautiful images.

The third presentation will concentrate on color-filter technology. Important characteristics in filter technology are high integration, overlay, making of the thin film, high sensitivity, and external issues (transport, storage, etc.).

Presentations four and five concentrate on the digital processing of color signals: color matrixing and demosaicing. The quality of the image obtained with a color camera is heavily dependant on the quality of the algorithms used during the matrixing operation and during the demosaicing operation. Both presentations will give an overview of state-of-the-art work in these fields.

It is a property of the human visual system to reduce the effect of illumination when looking at a scene. This property, known as Colour Constancy, is such that a white object is perceived as white independently of the color of the light source. Automatic White-Balance (AWB) algorithms aim to provide an image-capture device with the Same Color Constancy functionality. This is the subject of the sixth presentation.

The last presentation will concentrate on color coding. Digital-camera systems obviously deliver digital-image data, however, there is a wide variety of digital-image standards to which that data can be encoded. In this presentation, the technical parameters of digital-image-exchange standards will be reviewed.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of color imaging.

<u>Time</u>	<u>Topic</u>
8:00	Breakfast
8:30	Welcome and Overview <i>Albert Theuwissen, DALSA, Eindhoven, The Netherlands</i>
8:45	Human Vision System <i>Brian Wandell, Stanford University, Stanford, CA</i>
9:35	Capturing Color Images <i>Tetsuya Kuno, Mitsubishi, Kyoto, Japan</i>
10:25	Break
10:40	Color-Filter Technology <i>Katsumi Yamamoto, Toppan SMIC Electronics, Shanghai, China</i>
11:30	Color Matrixing <i>Gennady Agranov, Micron, Boise, ID</i>
12:20	Lunch
1:20	Color Interpolation <i>Takashi Saito, Kanagawa University, Yokohama, Japan</i>
2:10	White Balancing <i>Massimo Mancuso, ST Microelectronics, Milan, Italy</i>
3:00	Break
3:15	Color Coding <i>Charles Poynton, ATI Technologies, Toronto, Canada</i>
4:05	Panel Discussion
4:50	Conclusion

CIRCUIT DESIGN FORUM

F5: ATAC: High-Speed Interconnect

Organizer/Chair: **Wolfgang Pribyl**, *austriamicrosystems & CONPRI, Graz, Austria*

Committee: **Atila Alvandpour**, *Linköping University, Linköping, Sweden*
Franz Dielacher, *Infineon, Villach, Austria*
Yuriy M. Greshishchev, *PMC-Sierra, Kanata, Canada*
John Long, *Delft University of Technology, Delft, The Netherlands*
Sam Naffziger, *Intel, Fort Collins, CO*
Mehmet Soyuer, *IBM, Yorktown Heights, NY*

This forum will begin with a comprehensive overview of high-speed interconnect techniques, standards, and application areas, given by **Yuriy Greshishchev**.

The next two presentations will discuss requirements and implementation choices for high-speed interfaces in chip-to-chip applications. **Christian Sauer** and **Anthony Sanders** will focus on specific challenges in the high-performance processor arena, and in memory systems for consumer applications, respectively.

A variety of techniques for channel equalization, based partly on traditional communications techniques, are available for this field. **Evelina Yeung** and **Bryan Casper** will analyze and compare techniques such as linear and non-linear equalization, decision-feedback equalizers, transmit pre-emphasis, continuous-time linear equalizers, etc., with respect to their performance, power, and cost.

The next sequence will deal with 802.3ap 10Gb/s over backplanes (presented by **Troy Beukema**) and over UTP cables (by **Scott Powell**). Both presentations will provide an in-depth analysis of architectures, coding schemes, and simulation of those channels, and will compare the results with measured performance data.

As electrical interfaces approach their limits, even with the use of special signal-processing techniques, new techniques, such as optical signaling with integration of photonic and electronic functions on a single silicon (CMOS) chip, are gaining more and more interest. **Mario Paniccia** will review this field, show recent results, and give a perspective on future developments and opportunities for all-silicon photonics.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of high-speed interconnect.

Forum Agenda:

<u>Time</u>	<u>Topic</u>
8:00	Breakfast
8:30	Welcome and Introduction <i>Wolfgang Pribyl, austriamicrosystems & CONPRI, Graz, Austria</i>
8:40	High-Speed Interconnect Techniques, Standards and Application Areas <i>Yuriy Greshishchev, PMC-Sierra, Kanata, Canada</i>
9:20	Implementing Chip- and Board-level Protocols on Programmable Platforms <i>Christian Sauer, Infineon, Munich, Germany</i>
10:00	The Evolution of High-Speed Interfaces into Memory Applications <i>Antony Sanders, Infineon, Munich, Germany</i>
10:40	Break
11:00	Receiver Decision-Feedback Equalization for Multi-Gigabit Server Links <i>Evelina Yeung, Intel, Santa Clara, CA</i>
11:40	Tradeoffs of Receive and Transmit Equalization Architectures in 10 to 20 Gb/s I/O Systems <i>Bryan Casper, Intel, Hillsboro, OR</i>
12:20	Lunch
1:40	A Study of FFE/DFE Performance for Application to 10Gb/s 802.3ap Ethernet over Backplane Channels <i>Troy Beukema, IBM, Yorktown Heights, NY</i>
2:20	Multi-Gigabit Signaling Over UTP Cables <i>Scott Powell, Broadcom, Irvine, CA</i>
3:00	Break
3:20	Silicon Photonics in High-Speed Interconnects – Overview, Results, and Future Perspectives <i>Mario Paniccia, Intel, Santa Clara, CA</i>
4:00	Panel Discussion
4:45	Conclusion

CIRCUIT DESIGN FORUM

F6: Multi-Core Architectures, Designs, and Implementation Challenges

Organizer/Chair: Peter Kogge, *University of Notre Dame, Notre Dame, IN*

Committee: Atila Alvandpour, *Linköping University, Linköping, Sweden*
Georgios Konstadinidis, *Sun Microsystems, Sunnyvale, CA*
Chin-Yi Lee, *National Chiao Tung University, Hsinchu, Taiwan*
Masayuki Mizuno, *NEC, Sagami-hara-shi, Japan*
Shannon Morton, *Icera, Bristol, United Kingdom*
Norman Rohrer, *IBM, Essex Junction, VT*
Hector Sanchez, *Freescale, Austin, TX*
Alice Wang, *Texas Instruments, Dallas, TX*
James Warnock, *IBM, Yorktown Heights, NY*

This forum will begin with a presentation by **Peter Kogge** of the rationale and taxonomy of multicore processing chips (often called Chip-Level Multiprocessors or CMPs) and, what attributes make them attractive, and what are key metrics and design issues.

The next three presentations will describe specific issues in the design of multicore chips, with emphasis on architectural, interconnect, and floor-planning issues, as well as on coping with physical and electrical design constraints. **James Laudon** will discuss critical issues in designing highly-multi-threaded multicore chips such as Niagara, that are specifically designed for commercial server-level systems. **James Kahle** will address heterogeneous CMPs that have a particular emphasis on high-end multimedia performance, such as those found in the Cell design. **Satoshi Matsushita** will address those unique issues associated with mobile embedded multicore technologies, where the given power budget is less than one watt, and real-time response and robustness are important.

The second set of presentations addresses topics related to multicore designs in general, and their effects on overall CAD and design flows. **Dan Bouvier** will use a high-performance dual-core design to highlight the challenges of interconnecting and integrating a wide range of on- and off-chip interfaces, custom and soft IP. **Stefan Rusu** will cover circuit-technology aspects of multicore microprocessor design such as clock and power distribution, cache and external bus interfaces, and packaging, thermal and test challenges, with specific examples from Intel CMPs. Finally, **Juan Rosal** will touch on the many challenges, and current methodologies, related to yield enhancement and test of multicore SoCs for a variety of product arenas, including performance-closure efforts, redundancy schemes, characterization, and modeling that allows for block-level yield enhancement.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of Multicore Architectures.

Forum Agenda:

<u>Time</u>	<u>Topic</u>
8:00	Breakfast
8:30	Welcome Peter Kogge , <i>University of Notre Dame, Notre Dame, IN</i>
8:40	An Introduction to Multicore Chip Design Peter Kogge , <i>University of Notre Dame, Notre Dame, IN</i>
9:30	Niagara: Architecture and Physical Design of a 32-Threaded General-Purpose CPU James Laudon , <i>Sun Microsystems, Madison, WI</i>
10:20	Break
10:40	The Cell Processor's Multicore Architecture: Impact and Influence of Physical Design James Kahle , <i>IBM, Austin, TX</i>
11:30	Low-Power Multicore Chips for Mobile Embedded Applications Satoshi Matsushita , <i>NEC, Sagamihara, Japan</i>
12:20	Lunch
1:50	Challenges of Multicore Processors for Embedded Infrastructure Requiring High-Bandwidth I/O, Memory Interfaces, and On-Chip Accelerators Dan Bouvier , <i>Freescale Semiconductor, Austin, TX</i>
2:40	Circuit Technologies for Multicore Processor Design Stefan Rusu , <i>Intel, Santa Clara, CA</i>
3:30	Break
3:50	Multicore-SoC Test and Yield Enhancement—Challenges and Advancements in a Complex Environment Juan Rosal , <i>Texas Instruments, Dallas, TX</i>
4:30	Panel Discussion: How Does Future Technology Scaling Affect a Multicore World?
5:00	Conclusion

INFORMATION

CONFERENCE REGISTRATION

ISSCC offers online registration. This is the fastest, most convenient way to register and will give you immediate confirmation of whether or not you have a place in the Tutorial and Short Course sessions of your choice, as well as in any of the Forums offered. If you register online, which requires a credit card, your registration is processed while you are online, and your written confirmation can be downloaded and printed for your recordkeeping. If you register by fax or mail, you will not receive confirmation for several days. **Registration forms received without full payment will not be processed until payment is received at Event Solutions.**

To register online, go to the ISSCC website at www.isscc.org or go directly to the registration website at www.yesevents.com/isscc/index.asp. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2006". Payments by credit card will appear on your monthly statement as a charge from ISSCC.

For those who wish to register by fax or mail, the Advance Registration Form can be found at the center of this booklet. Please read the explanations and instructions on the back of the form carefully.

The deadline for receipt of Early Registration fees is **December 30, 2005**. After December 30th, and on or before January 13, 2006, registrations will be processed only at the Late Registration rates. **After January 13th, you must pay the onsite/highest registration fees.** Because of limited seating capacity in the meeting rooms and hotel fire regulations, onsite registrations may be limited. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2006.

Full conference registration includes one copy each of the Digest of Technical Papers in both hard copy and on CD, the Visuals Supplement (mailed in March) and the ISSCC 2006 DVD that includes the Digest and Visuals (mailed in June). **Student registration does not include the Visuals Supplement or the ISSCC 2006 DVD.** All students must present their Student ID at the Conference Registration Desk to receive the student rate. Those registering at the IEEE Member rate must also provide their IEEE Membership number. Those individuals who are members of both IEEE and SSCS will also receive a complimentary copy of the SSCS Digital Archive DVD set for years through 2005.

The Onsite and Advance Registration Desks at ISSCC 2006 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except as noted below, must pick up their registration materials at these desks as soon as they arrive at the hotel. **Pre-registered Presenting Authors for each paper, and all pre-registered members of the ISSCC Program Committee, must go directly to Golden Gate A3 to collect their conference materials.**

The Digest of Technical Papers will be available for pick-up onsite beginning on Sunday evening, and during registration hours on Monday through Wednesday.

INFORMATION

REGISTRATION HOURS:

Saturday, February 4	4:00 PM to 7:00 PM (Tutorial and Forum Attendees Only)
Sunday, February 5	6:30 AM to 11:30 AM (Tutorial and Forum Attendees Only) 11:30 AM to 8:00 PM
Monday, February 6	6:30 AM to 3:00 PM
Tuesday, February 7	8:00 AM to 3:00 PM
Wednesday, February 8	8:00 AM to 3:00 PM
Thursday, February 9	7:00 AM to 1:00 PM

NEXT ISSCC DATES AND LOCATION

ISSCC 2007 will be held on February 11-15, 2007 at the San Francisco Marriott Hotel.

FURTHER INFORMATION

Please visit the ISSCC website at www.isscc.org
To be placed on the Conference Mailing List, please contact the Conference Office,
c/o Courtesy Associates,

2025 M Street, N.W., Suite 800,
Washington, DC 20036
Email: ISSCC@courtesyassoc.com
Fax: 202-973-8722

HOTEL RESERVATIONS

ISSCC participants are urged to make their hotel reservations online. To do this, go to the conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott. In order to receive the special group rates you will need to enter the following Group Codes: SCCSCCA for a single or double; SCCSCCB for a triple; or SCCSCCC for a quad. The special ISSCC group rates are \$204/single; \$244/double; \$264/triple; and \$284/quad (per night plus tax). The dates of your reservation must fall within the period of February 3-9, 2006. All online reservations require the use of a credit card. Online reservations are confirmed immediately, while you are online. We suggest that you print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. Once made and confirmed, your online reservation can be changed by calling the Marriott at 1-800-228-9290 (toll free) or 415-896-1600, or by faxing your change to the Marriott at 415-442-0141.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet. Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax.

Reservations must be received at the San Francisco Marriott no later than January 13, 2006 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. Once this limit is reached and/or after January 13th, the group rate will no longer be available and reservation requests will be filled at the best available rate.

INFORMATION

IMPORTANT NOTICE FOR ALL 2006 ISSCC PARTICIPANTS: It is vitally important that all 2006 ISSCC participants who do not live within driving distance of San Francisco make their hotel room reservations at the San Francisco Marriott, which is the conference hotel and location of all technical sessions and all other conference activities. The room rates have been negotiated based upon our need to use all available meeting space in the hotel. If we do not fill our negotiated room block, the ISSCC must pay huge fees for using all of the space. This will then result in unnecessary and unpopular increases in registration fees for ISSCC in future years. Please support the Executive Committee in their attempt to keep your ISSCC registration fees reasonable. Book your room at the San Francisco Marriott hotel for ISSCC 2006.

CONFERENCE PUBLICATIONS

Additional ISSCC 2006 publications can be purchased at the Conference Registration Desks. Prices are lower for purchases collected onsite than for those publications ordered after the Conference that must be shipped to the purchaser for an additional fee. **Following ISSCC 2006, please order publications directly from the publisher, issccorders@s3digitalpub.com.**

TECHNICAL BOOK DISPLAY AND STUDENT POSTERS

A number of technical publishers will have a collection of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The Book Display is in the Golden Gate Hall C, located one level above the ballroom. The Book Display will be open on Monday from 12:00Noon - 8:00PM; on Tuesday from 10:00AM to 8:00PM; and on Wednesday from 10:00AM to 3:00PM.

The ISSCC/DAC and Student Poster Contest winners for 2006 will also display their winning papers in this area during the book display hours. The three winners of the IEEE Asian Solid-State Circuits Conference (A-SSCC) 2005, held on November 1-3, 2005 in Hsinchu, Taiwan, will also present their posters in Golden Gate Hall C. **All student poster authors will be available to present their posters during the Social Hours on Monday and Tuesday in Golden Gate Hall C.**

AUTHOR INTERVIEWS

This year Author Interviews will be held in the Club Room (one level above the hotel lobby) on Monday and Tuesday. Social Hour refreshments will also be available in the Club Room and surrounding Atrium during the Author Interviews. Please note that the Author Interviews will move to the South Grand Assembly on Wednesday.

INFORMATION

SSCS DIGITAL-ARCHIVE DVD SET

All ISSCC registrants who are members of the IEEE Solid State-Circuits Society (SSCS) will receive a complementary SSCS Digital-Archive DVD Set. The two DVD set contains the IEEE Journal of Solid-State Circuits (1966-2005) and the conference records of the ISSCC (1955-2005), the Symposium on VLSI Circuits (1988-2005), the Custom-Integrated-Circuits Conference (1988-2005), and the European Solid State Circuits Conference (1997-2005).

- To add SSCS membership while renewing IEEE membership, go to www.ieee.org/renew
- To add SSCS membership after renewing IEEE membership, go to www.ieee.org/addservices
- To join IEEE and SSCS, go to www.ieee.org/join

Check-off boxes are provided on the registration form for ordering additional copies of the Digital-Archive DVD.

CD OF THE ISSCC DIGEST AND DVD OF THE ISSCC DIGEST AND SLIDE SUPPLEMENT

Conference attendees will receive a complementary CD of the ISSCC 2006 Digest of Technical Papers, in addition to the printed Digest, at the Conference. This CD will allow easy access to an electronic version of the technical papers. In addition, all conference attendees (except student registrants) will receive (by mail) a complementary DVD containing the ISSCC 2006 Digest of Technical Papers and the ISSCC 2006 Visuals Supplement. This DVD will be mailed in June, 2006.

ISSCC 2004, 2005, and 2006 SHORT-COURSE DVDs

DVDs of the ISSCC 2004 Short Course, "Deep-Submicron Analog and RF Circuit Design", the ISSCC 2005 Short Course, "RF CMOS Circuits", and the ISSCC 2006 Short Course "Analog-to-Digital Converters" will be available for purchase at the Conference. These DVDs contain the audio and written textual transcripts synchronized with the presentation visuals. In addition, the DVDs will contain a pdf of the presentations suitable for printing, along with pdfs of key reference material. Check-off boxes are provided on the registration form for purchasing the DVDs; they will not be available for purchase after the Conference. As well quantities of the earlier DVDs are limited.

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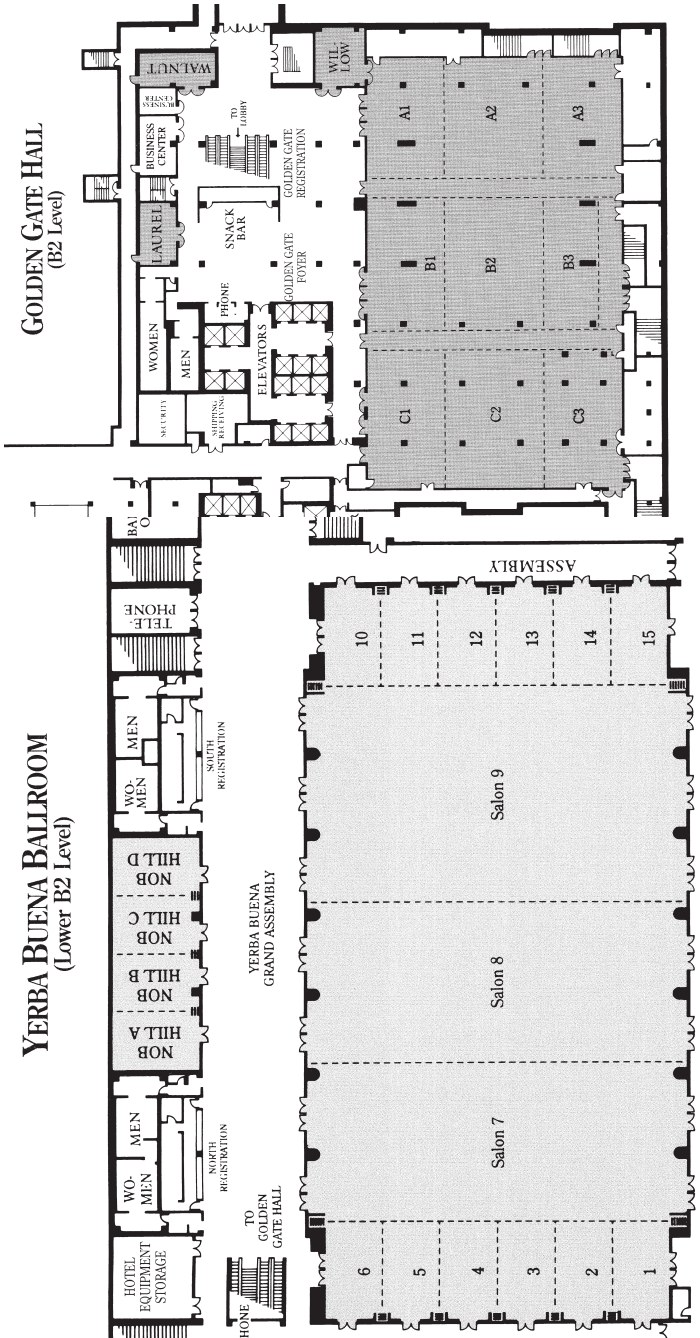
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