IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2012 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 19, 20, 21, 21, 23

CONFERENCE THEME:

SILICON SYSTEMS FOR SUSTAINABILITY

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
DEMOS EXTENDED TO AN ACADEMIC DEMONSTRATION SESSION (ADS)

5-DAY PROGRAM

SUNDAY ALL-DAY
2 FORUMS ON RF beamforming, and green circuit design
9 TUTORIALS ON RF mixers, Flash-memory, mobile GHz processors, wideband delta-sigma, jitter, integrated voltage regulators, digital calibration for RF, offset and flicker noise, and MEMS
2 EVENING EVENTS ON graduate student research in progress, and smarter robotics

THURSDAY ALL-DAY
4 FORUMS ON data communications, computational imaging, biolectronics, and many-core SoC optmization
A SHORT-COURSE ON low-power analog signal processing

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 19th**, the day before the official opening of the Conference, ISSCC 2012 offers:

- A choice of up to 4 of a total of 9 Tutorials
- A choice of 1 of 2 Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, **"What's Next in Robots?….."** will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. A distinguished circuit designer, Professor Willy Sansen will provide introductory remarks at the Preview.

On **Monday, February 20th**, ISSCC 2012 offers four plenary papers on the theme: "Silicon Systems for Sustainability". On Monday at 12:15 pm, there will be a Women's Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour held in conjunction with the Book Display will also include the Academic Demonstration Session (ADS), featuring posters and live demonstrations for selected papers from universities. Monday evening features a panel discussion on "**Is RF Doomed to Digitization?…..**", as well as two Special-Topic Sessions on "**Technologies that Could Change the World…..",** and **"Optical PCB Interconnects…..".**

On **Tuesday, February 21st**, there are five parallel morning and afternoon technical sessions. A Social Hour open to all ISSCC attendees will follow. The Social Hour held in conjunction with the Book Display will include the Industrial Demonstration Session (IDS), featuring posters and live demonstrations for selected papers from industry. Tuesday evening sessions include two evening panels on "**Little-Known Features of Well-Known Creatures**", and **"What is the Next RF Frontier?"**, as well as one Special-Topic Session on "**Vision for Future Television**".

On Wednesday, February 22nd, there will be five parallel sessions morning and afternoon.

On **Thursday, February 23rd**, ISSCC offers a choice of five events:

- A Short Course on **"Low-Power Analog Signal Processing"**
- Four Advanced-Circuit-Design Forums on high-speed data communications, computational imaging, bioelectronics, and many-core SoC optimization

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

Need Additional Information?
Go to: www.isscc.org

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T1: RF Mixers: Analysis and Design Trade-offs

Mixers are essential building blocks of every RF transceiver, often compromising the noise and linearity performance of the entire receive or transmit chain. Specifically, the switching action involved in mixing typically dictates the choice of the radio architecture and proper frequency planning to avoid the receiver desensitization. In this tutorial various mixer architectures such as passive and active, current-mode and voltage-mode, and their properties are analyzed and discussed. Of special importance is the noise response of mixers, which is not very well understood due to the nonlinear and time varying nature of the block, and the fact that conventional linear noise analysis applicable to amplifiers often does not hold. We will focus on intuitive and qualitative ways of analyzing the noise of both passive and active mixers as well.

Instructor: Hooman Darabi

Hooman Darabi received the BS and MS degrees both in Electrical Engineering from Sharif University of Technology, Tehran, Iran, in 1994, and 1996, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a Sr. Technical Director and a Fellow with Broadcom Corporation, Irvine, CA, as a part of the mobile and wireless group. His interests include analog and RF IC design for wireless communications. Dr. Darabi holds over 170 issued or pending patents with Broadcom, and has published over 50 peer-reviewed journal and conference papers.

T2: Flash-Memory Based Circuit, System, and Platform Design

Applications using flash memory are rapidly increasing in number. Different applications of flash memory demand various Circuit, System, Software and Platform Co-Design to optimize usage. Even for a given application these tradeoffs should be considered. Unlike tutorials on flash memory in the past that mostly focus on circuit design, this tutorial will consider System, Software, and Platform Design from the application perspective. The tutorial will also be of interest to the broader audience with interests beyond memory field.

Instructor: Mark Bauer

Mark Bauer is a Fellow at Micron working in the NAND Solutions Group where he is responsible for the vertical integration of Non Volatile Memory and memory systems. He joined Micron in 2010 as part of the Numonyx aqusition. Prior to Micron he spent three years at Numonyx on advanced Phase Change Memory designs in technology. From 1985 to 2008 he worked at Intel developing EPROM, NOR Flash, NAND Flash and Phase Change Memory designs. He holds more than 30 US Patents, has published numerous technical papers in the field of Non Volitile Memory, has been an invited speaker at technical conferences, served on the ISSCC Memory Technical Program Committee for 11 years and is currently on the VLSI Symposium Technical Program Committee. He recieved the BSEE from the University of California in 1985.

T3: Mobile GHz Processor Design Techniques

Mobile computing devices such as smart-phones and smart-pads open up new challenges in mobile processor designs in terms of their speed and power targets. Mobile processors are getting more powerful in order to run increasingly complex software. Therefore, the design of high-speed low-power mobile processors is becoming the major challenge. In this tutorial, design techniques for high-speed mobile CPU and GPU are discussed at several design levels. The talk will go through the architecture, circuit, device level optimization and also consider chip-wise power management techniques. Special considerations for cost-effective micro-architectures, high-speed logic, low-power arithmetic, and DVFS will be highlighted.

Instructor: Byeong-Gyu Nam

Byeong-Gyu Nam received his Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007. His Ph.D. work focused on low-power GPU design for mobile devices. From 2007 to 2010, he was with Samsung Electronics, Giheung, Korea, where he worked on the world's first low-power 1-GHz ARM microprocessor design. Dr. Nam is currently with Chungnam National University, Daejeon, Korea, as an assistant professor. His current interests include mobile GPU, embedded CPU, low-power SoC, and their associated SW platforms. He is serving as a program committee member of the IEEE ISSCC, A-SSCC, COOL Chips, and VLSI-DAT.

T4: Wideband Delta-Sigma Modulators

The application space of delta-sigma analog-to-digital converters has been greatly extended during the last few decades with applications ranging from traditional applications such as audio and hearing aids that require only a few (tens of) kHz bandwidth to a multitude of cellular standards that need up to 40MHz bandwidth. To enable this bandwidth range of four orders of magnitude, new innovative wideband delta-sigma architectures and circuits have been developed that operate at GHz rate sampling frequencies. This tutorial gives an introduction to the system design and implementation of wideband delta-sigma modulators. A review of wideband delta-sigma architectures, loop stability, filter implementations and circuit designs is presented. Some case studies illustrate wideband delta-sigma modulators that have bandwidths in the range from several tens of MHz to beyond 100MHz.

Instructor: Lucien Breems

Lucien Breems received the M.Sc. degree and the Ph.D. degree in Electrical Engineering from the Delft University of Technology, The Netherlands, in 1996 and 2001, respectively. From 2000 to 2007 he was with Philips Research, Eindhoven the Netherlands and in 2007 he joined NXP Semiconductors where he currently leads a team working on delta-sigma A/D converters. Since 2008, he has been a lecturer at the Delft University of Technology on the topic of delta-sigma modulation and since 2011 he is a part-time Professor at the Eindhoven University of Technology. His research interests are in the field of mixed-signal circuit design. In 2001, he received the ISSCC "Van Vessem Outstanding Paper Award".

T5: Jitter: Basic and Advanced Concepts, Statistics, and Applications

Jitter and phase noise are key factors that deeply impact the performance of circuits in modern communication applications. Within the industry, many types of jitter must be and are considered, including cycle-to-cycle, accumulated, deterministic, random, total, absolute, integrated, TIE, and more. Understanding the implications of each of these jitter types demands clear jitter term definitions as well as a common understanding of their practical meaning. In response to this need, this tutorial will presents basic and advanced concepts of jitter. The first part of the tutorial will focus on jitter definitions, statistics, and the relationship of jitter to phase noise. The second part of the tutorial will explore the impact of jitter on a variety of applications, drawing on examples from wireline as well as other technical areas. The overall goal of the tutorial is to provide a solid understanding of what jitter is, how to correctly specify it, and to enhance understanding of jitter specifications for different applications.

Instructor: Nicola Da Dalt

Nicola Da Dalt received the Master degree from University of Padova, Italy, in 1994 and the PhD degree from RWTH Aachen, Germany, in 2007, both in Electronic Engineering. From 1996 to 1998 he was with Telecom Italia, Italy, as concept engineer for architectures and synchronization of data transmission networks and satellite communications. Since 1998 he has been with Infineon Technologies, Austria, as an IC design and concept engineer for clock systems in applications ranging from wireline, to memory and wireless. Since March 2005 he leads the Clocking and Interface Systems group. He received the 2010 IEEE Guillemin-Cauer Best Paper Award. He holds four granted patents and is the author of several publications in conferences and journals.

T6: Power Management Using Integrated Voltage Regulators

Aggressive technology scaling has enabled very high levels of transistor integration. Managing total power consumption has emerged as the most challenging task in today's highly complex microprocessor systems. In this tutorial, we will review power management techniques implemented in recent designs. Independent per-core dynamic voltage scaling is proven to be an effective way to minimize power consumption. Due to the size and routing planes, the number of independent platform rails is limited to a very small number. Near-load voltage regulators provide a practical solution. This tutorial includes a survey of recent innovations in near-load voltage regulators.

Instructor: Tanay Karnik

Tanay Karnik is Principal Engineer and Program Director in Intel Lab's Academic Research Office. He received his Ph.D. in Computer Engineering from University of Illinois at Urbana-Champaign in 1995. His research interests are in the areas of variation tolerance, power delivery, soft errors and physical design. He has published 50 technical papers, has 44 issued and 33 pending patents. He received an Intel Achievement Award for the pioneering work on integrated power delivery. Tanay was the General Chair of ASQED'10, ISQED'09, ISQED'08 and ICICDT'08. Tanay is IEEE Senior Member, Associate Editor for TVLSI and Guest Editor for JSSC.

T7: Digital Calibration for RF Transceivers

Designing high-precision RF transceivers in deep submicron technologies is increasingly challenging due to reduced supply headroom, non-linearities of transistors, and large process parameter spread. By taking advantage of the cheaper and faster digital computing power, digital calibration is becoming an increasingly common practice to overcome such challenges and enhance transceiver performance. Calibration techniques covered include I/Q mismatch calibration, DC offset and LO leakage removal, closed-loop power control and envelope tracking, analog filter response calibration, digital pre-distortion for PAs, and antenna tuning. The tutorial will also cover DSP methods and algorithms and provide specific examples of digitally calibrated transceivers.

Instructor: Albert Jerng

Albert Jerng received his BSEE, MSEE from Stanford University, and his PhD EE from MIT in 1994, 1996, and 2006, respectively. While at MIT, he conducted research on CMOS VCO design and digital TX architectures for Gb/s OFDM systems. Since 2007, he has been with Ralink Technologies as Sr. Director for Advanced Circuits and Systems working on Bluetooth and WiFi products, and is now employed as Deputy Director at Mediatek, responsible for the WiFi RF transceiver division, after their merger with Ralink. He is also serving as General Chair for the IEEE RFIC Symposium in 2012.

T8: Managing Offset and Flicker Noise

A large number of circuits require DC accuracy and low noise at low frequencies. Sensor interfaces are a good example, but comparators, ADC's, and many other blocks need it too. This tutorial will provide a review of techniques to achieve low offset and flicker noise.
Techniques such as chopper stabilization, correlated double sampling, auto-zero, digital startup calibration, and digital background calibration will be reviewed. Implementation examples will be shown and noise and aliasing and other artifacts will be analyzed. Techniques to master these artifacts will be discussed. The ideas will then be taken into the mixed signal domain.

Instructor: Axel Thomsen

Axel Thomsen received his PhD from the Georgia Institute of Technology in 1992. He has held positions at the University of Alabama in Huntsville, University of Texas, and Cirrus Logic. Currently he is a Distinguished Engineer at Silicon Laboratories in Austin, TX. He has worked on chips for industrial measurement, timing, isolation and power applications. He has a strong interest in precision measurement. Currently he is working in the Embedded Mixed Signal Division on data converters and amplifiers. He holds more than 40 patents.

T9: Getting In Touch With MEMS: The Electromechanical Interface

MEMS systems include mechanical structures and electronic sense and drive circuits. Between these is an electromechanical interface, which can be capacitive, piezoresistive, piezoelectric, ferroelectric, electromagnetic, thermal, optical or can take some other form. The selection of this interface is the single most critical decision in the system definition, and it determines the eventual capabilities and limits of the device. The interface fundamentally sets the device's sensitivity, accuracy, drift, ageing, temperature behavior, and environmental capabilities. The interface determines the MEMS production technology and hence the fab selection, the cost structure, and the time to market. This tutorial examines and compares the available options and application drivers. Which interface technologies can be used? Why is one more suitable for a particular application than another? How do they scale? What is on the horizon? The goal is to expand the attendee's potential role from circuit designer to system designer. From "Here is the MEMS device, design the interface circuit." into "Here is the problem, define an optimal solution."

Instructor: Aaron Partridge

Aaron Partridge received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University, Stanford, CA, in 1996, 1999, and 2003, respectively. In 2004 he cofounded SiTime Corp. where he is Chief Science Officer. SiTime is the leading supplier of MEMS oscillators, resonators, and timing devices. From 2001 through 2004 he was Project Manager at Robert Bosch Research and Technology Center, Palo Alto, CA, where he coordinated the MEMS resonator research. He serves on the IEEE International Solid-State Circuits Conference IMMD subcommittee and is the Editorial Chair of the IEEE International Frequency Control Symposium.

F1: Beamforming Techniques and RF Transceiver Design

Organizers: **Eric Klumperink,** *University of Twente, Enschede, The Netherlands*
Domine Leenaerts, *NXP Semiconductors, Eindhoven, The Netherlands*

Committee: **Albert Jerng,** *Ralink, Jhubei, Taiwan*
Yorgos Palaskas, *Intel, Hillsboro, OR*
Didier Belot, *ST Microelectronics, Crolles, France*

Phased arrays exploit electronic beamforming to create an electronically steerable beam pattern. This reinforces antenna gain in certain directions and reduces gain in others, i.e. spatial filtering. Until recently, phased-array systems exploited dedicated RF technologies leading to relatively costly systems, e.g. for nautical systems, airplane radar systems, and satellite communication. More recently, low-cost highly integrated beamforming concepts received considerable interest in academia but also industry, enabling consumer applications e.g. in base stations for macro- and femto-cells, car radar and 60GHz wideband radio links. (Bi-)CMOS beamforming techniques are at the heart of such systems. This forum reviews beamforming techniques suitable for IC integration, and discusses related (Bi-)CMOS transceiver designs. Several techniques will be discussed, e.g. RF phase shifting, LO phase shifting, I/Q vector modulation and digital processing. Also the relation between key radar and communication system requirements and transceiver IC requirements will be considered. Finally, trends and challenges will be discussed in a panel.

Forum Agenda

Time	Topic
08:00	Breakfast
08:30	**Introductory Overview of Beamforming** **Gabriel Rebeiz,** *UC San Diego, LaJolla, CA*
09:00	**S-Band Phased-Array Radar with 2-D Digital Beamforming** **Wim de Heij,** *THALES Nederland BV, Hengelo, The Netherlands*
09:30	**SiGe BiCMOS Single-Chip Receiver for S-Band Phased-Array Radars** **Frank van Vliet,** *TNO, The Hague, The Netherlands*
10:00	Break
10:30	**Silicon RF Phased-Arrays at X-, Q-, W-Band and Beyond** **Kwang-Jin Koh,** *Virginia Tech, Blacksburg, VA*
11:15	**Butler Matrix Beamforming Phased Arrays and CMOS Implementation** **Sheng-Fuh Chang,** *Chung Cheng University, Chiaya, Taiwan*
11:45	Lunch
1:00	**Silicon-Based Integrated Beamforming and On-Chip Radiators** **Ali Hajimiri,** *California Institute of Technology, Pasadena, CA*
1:45	**Vector Modulation Techniques and Interference Nulling** **Jeyanandh Paramesh,** *Carnegie Mellon University, Pittsburgh, PA*
2:15	Break
2:45	**RF Beamforming and 60GHz BiCMOS Chipsets** **Scott Reynolds,** *IBM T.J. Watson Research Center, Yorktown Heights, NY*
3:30	Panel Discussion: **Challenges for the future?**
4:00	Closing Remarks (Chair)

F2: Robust VLSI Circuit Design and Systems for Sustainable Society

Organizer/Chair: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
Co-Chair: **Jan Crols,** *AnSem, Heverlee, Belgium*

Committee: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
Jan Crols, *AnSem, Heverlee, Belgium*
Kevin Zhang, *Intel, Hillsboro, OR*
Mike Clinton, *Texas Instruments, Dallas, TX*
Tadaaki Yamauchi, *Renesas Electronics, Itami, Japan*

Technology scaling brings new challenges to the design of reliable and robust VLSI circuits and systems – challenges that arise at the system, circuit and device levels.

This Forum provides an overview of such challenges, as well as overviews recent advances in the domain of reliable and robust VLSI systems. Topics covered include the fault-tolerance requirements for microcontrollers in automotive applications, recent trends in CMOS variability, design techniques for robust non-volatile and volatile memories, as well as directions for improving the robustness of analog, communications, and voltage regulator circuits and systems.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
8:30	**Future Development of Robustness and Fault Tolerance Requirements for Microcontrollers in Safety Relevant Automotive Applications** **Bernd Müller,** *Robert Bosch GmbH, Stuttgart, Germany*
9:20	**Understanding CMOS Variability and Soft errors for Robust Circuit Design** **Hidetoshi Onodera,** *Kyoto University, Kyoto, Japan*
10:10	Break
10:25	**Robust SRAM Design in Nano-Scale CMOS: Circuit and Technology** **Yih Wang,** *Intel, Portland, OR*
11:15	**Embedded Non-Volatile Memory Design for Highly Reliable Applications** **Takashi Kono,** *Renesas Electronics, Itami, Japan*
12:05	Lunch
1:00	**Dependable SSD Design** **Hiroshi Sukegawa,** *Toshiba, Yokohama, Japan*
1:50	**Robust System Design: Overcoming Complexity and Reliability Challenges** **Subhasish Mitra,** *Stanford University, Stanford, CA*
2:40	Break
2:55	**Reliability Considerations in Deep Submicron Analog Circuit Design** **Terry Mayhugh,** *Texas Instruments, Richardson, TX*
3:45	**Channel Coding in Wireless** **Martin Bossert,** *Ulm University, Ulm, Germany*
4:35	**Voltage Regulator Circuits and System Energy Management** **Dave Freeman,** *Texas Instruments, Dallas, TX*
5:25	Conclusion

ES1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 23 one-minute presentations followed by a Poster Session, by graduate students (Masters and PhDs) from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three sessions: Analog, Mixed-Signal and RF Circuits; High-Performance Systems and Imagers; Techniques for Ultra-Low-Power Sensors.

The Student Research Preview will begin with a brief talk by the distinguished circuit designer, Professor Willy Sansen, K.U. Leuven. His talk on careers in solid-state circuits is scheduled for Sunday,February 19th, starting at 7:30pm, and is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel**	*University of Pennsylvania*
Co-Chair:	**Makoto Ikeda**	*University of Tokyo, Japan*
Co-Chair:	**Eugenio Cantatore**	*Technical University Eindhoven, The Netherlands*
Secretary:	**SeongHwan Cho**	*KAIST, Korea*
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Boris Murmann	Stanford University, USA
Bing Sheu	TSMC, Taiwan
Sameer Sonkusale	Tufts University, USA
Jan Van der Spiegel	University of Pennsylvania, USA
Marian Verhelst	Kath. University of Leuven, Belgium
Zhihua Wang	Tsinghua University, P.R. China

ES2: What's Next in Robots?
~ Sensing, Processing, Networking Toward Human Brain and Body

Organizer: **Kazutami Arimoto,** *Renesas Electronics, Itami, Hyogo, Japan*

Organizer: **Sam Kavusi,** *Bosch Research, Palo Alto, CA*

Chair: **Kenneth Salisbury,** *Stanford University, Stanford, CA*

Most of us dreamt about robots in our childhood interacting and assisting us in our daily life. They are way beyond fiction and have emerged to become unavoidable in minimally-invasive surgery and industrial automation. There is also an explosion in research areas around autonomous cars, humanoid/android, and personal assistance robots. Such advances are largely due to the advances in semiconductor technologies driven by consumer and automotive electronics. Increasingly robotic platforms are also benefiting from the wirelessly connected infrastructure and the cloud. This session provides an overview of the major areas and their challenges that may be addressed by semiconductor technologies.

Time	Topic
8:00	**Robot Society with Teleoperated Robots and Androids** **Hiroshi Ishiguro,** *Osaka University and ATR, Osaka and Kyoto, Japan*
8:25	**Robotics for Minimally-Invasive Surgery and Therapy** **Simon DiMaio,** *Intuitive Surgical, Sunnyvale, CA*
8:50	**Advancing Personal Robotics** **Günter Niemeyer,** *Willow Garage, Menlo Park, CA*
9:15	**Humanoid Robotics for Services** **Bruno Maisonnier,** *ALDEBARAN Robotics, Paris, France*

PLENARY SESSION — INVITED PAPERS

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair:
Hideto Hidaka, *Renesas Electronics, Itami, Japan*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:30AM**

1.1 **Flash Memory — The Great Disruptor!** **8:45AM**
Eli Harari, *Co-Founder, Former CEO, and Chairman (retired), SanDisk , Milpitas, CA*

Since its commercial introduction in 1988 Flash-memory chip density has advanced through 19 technology nodes, doubling the number of bits per chip with each successive node, with sub 20nm 128Gb Flash chips entering volume production in 2012. This incredible pace has been made possible by the use of the industry-workhorse floating-gate Fowler-Nordheim tunneling cell, first employed in EEPROM, then in NOR and NAND Flash EEPROM. The convergence of NAND Flash with System-Flash and Multi Level Cells (MLC) in the past decade transformed Flash from primarily a code-store memory to a highly-reliable low-cost data-store medium, bringing enormous price reductions and capacity growth to consumers. Flash became an enabling technology to, as well as a prime beneficiary from, the digital consumer electronics revolution, the rise of the Internet, and the proliferation of wireless mobile devices (most recently, smartphones and tablets), fueling the rapid growth of Flash storage into a $25 billion industry today.

Over the past decade, Flash storage profoundly disrupted analog film, floppy disks, magnetic tapes, micro-drives, and optical CDs. Price elasticity drove rapid growth in consumer demand for Flash units and megabytes. Fierce competition among Flash suppliers ensured an ample supply, and created Flash-card format standards developed by Industry Associations, thereby open to all. Billions of units of SD, micro-SD, USB Flash-drive, and embedded Flash are sold by the industry each year, working seamlessly in literally tens of thousands of different host devices that are used in a broad spectrum of industries and applications.

I have been fortunate to have been involved with the semiconductor Non-Volatile-Memory industry over its 40-year history, first as a device physicist, then as an entrepreneur and businessman. In this presentation, I will provide my personal recollections of some of the past milestones of this industry, and commentary on the profound impact that Flash has had on Consumer Electronics and Mobile Computing. Looking forward, I will briefly discuss the substantial opportunities, as well as the considerable challenges for NAND Flash and post-NAND 3D Flash in the sub-20nm era ahead. I foresee that technology and manufacturing challenges will be overcome through device and architectural innovations, and that in the coming decade NAND and post-NAND 3D Flash will grow to eclipse all other storage media, whether semiconductor, magnetic, or optical, thereby completing a breathtaking odyssey spanning 50 years!

1.2 The Role of Semiconductors in the Energy Landscape **9:20AM**

Carmelo Papa, *Senior Executive VP/GM, STMicroelectronics, Geneva, Switzerland*

The exponential increase of world energy demand, with a forecasted rise in electricity consumption of 45% between 2010 and 2030, makes energy management one of the most urgent topics of this century, and a key driver of the evolution semiconductors and electronics components.

Furthermore, the Kyoto Protocol on Climate Change targets a limitation of global temperature increase to 2°C maximum, within 2030, through two primary interventions: by increasing electricity production from renewable and bio-fuel sources, and by increasing energy efficiency, using a wider adoption of microelectronics. Energy efficiency can contribute up to 54% of the required CO2 reduction.

From the application point of view, electricity consumption comes from 3 major areas of use: Power Supply (24%), Lighting (21%), and Motor Control (55%). Semiconductors will play an essential role in this scenario, thanks to a continuous improvement in silicon technologies, innovative IC topologies, and system design methodologies.

For example, for the past 10 years, appliances have seen a progressive replacement of universal motors with brushless motors using powerful and cost-efficient microcontrollers with embedded advanced software algorithms, such as the ultimate Field-Oriented Controls.

Thanks to this development, the market welcomes new Class-A+ Home Appliances with average energy efficiency increase by 30% or more, that provide a saving of up to 50TWh by 2020, today's equivalent electricity consumption of Portugal and Latvia.

Cost-effective IC solutions make today's CFL (Compact Fluorescent Lamp) and LED lighting technology adoption more affordable, with corresponding power-consumption reduction. For instance, the replacement of incandescent lamps with CFL in Europe will allow a saving of 11.5TWh by 2025, that is, one third of Denmark's current electricity consumption.

"More Moore" and "More than Moore" technologies will play an important role in the energy revolution involving aspects of the Smart Grid, particularly in Power-Conversion and Connectivity Systems. The first, with the adoption of finer lithography geometries, will allow miniaturization and integration at the component level, while the latter with heterogeneous system integration will allow the introduction of more functions like micro-batteries, smart sensors, plastic electronics, energy harvesting, and so on.

What we see is a kind of revolution, with an enormous impact on sustainability, quality of life, and societal change!

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55AM**

BREAK **10:20AM**

1.3 Take the Expressway to Go Greener **10:35AM**

Yoichi Yano, *Executive VP, Renesas Electronics, Tokyo, Japan*

Society is going green! Increasingly, people commit to choosing equipment with lower energy demands. Historically, the growth of green has been repeatedly motivated by various economic shocks, such as the 1973 oil crisis. More recently, the Lehman Brothers crisis in 2008 inspired green initiatives in various industry sectors: surges in solar-power generation, eco-friendly white-goods products, consumer electronics, and green hybrid cars. Most recently, the 3.11 earthquake and tsunami in Japan triggered another wave in energy-saving life style motivated by the shortage of electric power. Now, the world is demanding greener products for a greener society on a scale never seen before. How can we reduce power consumption?

Over time, microelectronics has evolved to save power. Semiconductor technology has been in the lead in the reduction of power consumption, by enabling monitoring, controlling, and managing of energy consumption. The key product in this advance has been a less-commonly-known semiconductor device called the microcontrollers.

Microcomputers were introduced to the market in the early 1970s, firstly for electronic calculators, then in electro-mechanical controllers such as in cash registers, white goods, and consumer electronics. Then, microcomputers evolved along two different paths – one, called Microprocessors (MPU), for Personal Computers and Servers, and another called Microcontrollers (MCUs) for embedded controls. Beginning in 1987, market research firms began to track world-wide shipment data for these two categories. Thus, we know that in 2010, 500 million MPUs and 13 billion MCUs were shipped — the latter being 20x expansion since 1987. Currently, about 400 MCUs are shipped EVERY SECOND!

Now, that MCUs are “everywhere you imagine”, we see more than one hundred such devices in every modern home – in white goods, consumer electronics, remote controllers, metering, and so on. We find approximately one hundred MCUs in a modern car – in engine control, transmission control, body electronics, HVAC, window control, mirror control, Hybrid and all Electric Vehicle, and so on. Wide acceptance of MCUs in various embedded applications results from their ease of use, the availability of a wide range of products, and their self containment – everything needed is integrated on a tiny piece of silicon. In short, MCUs are low-power, small in foot print, adequate in performance, and low-cost.

Technology-wise, the strength of an MCU comes from its programmability via on-board Flash-memory technology. While the introduction of Flash-based MCUs goes back to the early 1990s, its widespread use in low-end microcontrollers was delayed to the early 2000s. Flash-based MCUs changed the world because of their programmability within a very small foot print and at low power. Thus, the huge current market! Most recently an MCU has been developed that can operate from one lemon as a battery source. Such MCUs can save tremendous amounts of power through their vast use in a myriad of applications. They are truly the core technology for everything going greener! Yet, MCUs will evolve further to save power, in wide spread applications including the “energy harvesting” environment. On the other hand, the automotive industry requires higher real-time performance with a much higher level of functional safety in addition to lower power. Such requirements will drive the development of next generation Flash MCUs on the expressway to going green!

1.4 Sustainability in Silicon and Systems Development **11:10AM**
David Perlmutter, *Executive VP, Intel, Santa Clara, CA*

It has been predicted that Moore's Law will continue to double transistor-integration capacity every two years, providing the abundance of transistors needed to realize novel architectures for future platforms. These platforms will enable more more-intelligent electronic gadgets and devices to enrich our lives. Harnessing Moore's Law and sustaining this growth over the last four decades has not been easy. The task has been challenging; overcoming design-productivity limitations in the 80s; power dissipation in the 90s; and leakage power in the last decade. However, we have persevered! But now, the major challenge we will face in the coming decade is not just power, but energy efficiency. Imagine a 100 giga-operations-per-second mobile device, a product that we would expect by the end of the decade, consuming hundreds of watts of power! Likewise, with present techniques, a high-end exascale supercomputer would be expected to consume in excess of 1 gigawatts of power; not a practical solution. While Moore's Law continues to provide more transistors, power budgets limit our ability to use them.

However, there are several technologies on the horizon which provide relief, and that we must exploit. Advances in transistor structures such as 3D tri-gate transistors in 22nm, 3D die stacking, and future heterogeneous technologies, will provide higher performance at lower energy and leakage. Circuit technologies such as near-threshold-voltage logic can boost energy efficiency by an order of magnitude. Novel architectures can implement fine-grain power and energy management. System software can be smarter and self-aware to manage the entire platform with an order-of-magnitude improvement in energy efficiency. Clearly, in the expansion of the compute continuum, the energy-efficiency challenge is best served with the co-design spirit; from top to bottom and from applications to process technology, all in harmony.

Energy efficiency of the compute sector will become increasingly important, with exponential growth, and we must make smart choices about resource consumption that can help save the environment. Intel recognizes the importance of caring for the planet by developing technological solutions to reducing the environmental impact of computing. This talk will addresses energy efficiency, and outlines challenges, solutions, and opportunities in the next decade for the compute continuum.

PRESENTATION TO PLENARY SPEAKERS **11:45AM**

CONCLUSION **11:55AM**

HIGH-BANDWIDTH DRAM & PRAM

Session Chair: **Joo Sun Choi,** *Samsung Electronics, Hwasung, Korea*
Associate Chair: **Daisaburo Takashima,** *Toshiba, Yokohama, Japan*

2.1 A 1.2V 30nm 3.2Gb/s/pin 4Gb DDR4 SDRAM With Dual-Error Detection and PVT-Tolerant Data-Fetch Scheme **1:30 PM**

K. Sohn, T. Na, I. Song, Y. Shim, W. Bae, S. Kang, D. Lee, H. Jung, H. Jeoung, K-W. Lee, J. Park, J. Lee, B. Lee, I. Jun, J. Park, J. Park, H. Choi, S. Kim, H. Chung, Y. Choi, D-H. Jung, J. Choi, B. Moon, J-H. Choi, B. Kim, S-J. Jang, J. Choi, K. Oh
Samsung Electronics, Hwasung, Korea

2.2 A 1.2V 38nm 2.4Gb/s/pin 2Gb DDR4 SDRAM With Bank Group and ×4 Half-Page Architecture **2:00 PM**

K. Koo, S. Ok, Y. Kang, S. Kim, C. Song, H. Lee, H. Kim, Y. Kim, J. Lee, S. Oak, Y. Lee, J. Lee, J. Lee, H. Lee, J. Jang, J. Jung, B. Choi, Y. Kim, Y. Hur, Y. Kim, B. Chung, Y. Kim
Hynix Semiconductor, Icheon, Korea

2.3 A 1.2V 23nm 6F² 4Gb DDR3 SDRAM With Local-Bitline Sense Amplifier, Hybrid LIO Sense Amplifier and Dummy-Less Array Architecture **2:30 PM**

K-N. Lim, W-J. Jang, H-S. Won, K-Y. Lee, H. Kim, D-W. Kim, M-H. Cho, S-L. Kim, J-H. Kang, K-W. Park, B-T. Jeong
Hynix Semiconductor, Icheon, Korea

Break 3:00 PM

2.4 A 1.2V 30nm 1.6Gb/s/pin 4Gb LPDDR3 SDRAM With Input Skew Calibration and Enhanced Control Scheme **3:15 PM**

Y-C. Bae, J-Y. Park, S. Rhee, S. Ko, Y. Jeong, K-S. Noh, Y. Son, J. Youn, Y. Chu, H. Cho, M. Kim, D. Yim, H-C. Kim, S-H. Jung, H-I. Choi, S. Yim, J-B. Lee, J. Choi, K. Oh
Samsung Electronics, Hwasung, Korea

2.5 A 20nm 1.8V 8Gb PRAM With 40MB/s Program Bandwidth **3:45 PM**

Y. Choi, I. Song, M-H. Park, H. Chung, S. Chang, B. Cho, J. Kim, Y. Oh, D. Kwon, J. Sunwoo, J. Shin, Y. Rho, C. Lee, M. Kang, J. Lee, Y. Kwon, S. Kim, J. Kim, Y-J. Lee, Q. Wang, S. Cha, S. Ahn, H. Horii, J. Lee, K. Kim, H. Joo, K. Lee, Y-T. Lee, J. Yoo, G. Jeong
Samsung Electronics, Hwasung, Korea

2.6 A 283.2μW 800Mb/s/pin DLL-Based Data Self-Aligner for Through-Silicon Via (TSV) Interface **4:15 PM**

H-W. Lee[1,2], S-B. Lim[1], J. Song[1], J-B. Koo[1], D-H. Kwon[2], J-H. Kang[2], Y. Kim[2], Y-J. Choi[2], K. Park[2], B-T. Chung[2], C. Kim[1]
[1]Korea University, Seoul, Korea [2]Hynix Semiconductor, Icheon, Korea

2.7 An 8Gb/s/pin 4pJ/b/pin Single-T-Line Dual (Base+RF) Band Simultaneous Bidirectional Mobile Memory I/O Interface With Inter-Channel Interference Suppression **4:30 PM**

Y. Kim[1], G-S. Byun[2], A. Tang[1], C-P. Jou[3], H-H. Hsieh[3], G. Reinman[1], J. Cong[1], M-C. Chang[1]
[1]University of California, Los Angeles, Los Angeles, CA
[2]West Virginia University, Morgantown, WV
[3]TSMC, Hsinchu, Taiwan

2.8 A 7Gb/s/Link Non-Contact Memory Module for Multi-Drop Bus System Using Energy-Equipartitioned Coupled Transmission Line **4:45 PM**

W-J. Yun, S. Nakano, W. Mizuhara, A. Kosuge, N. Miura, H. Ishikuro, T. Kuroda
Keio University, Yokohama, Japan

Conclusion 5:00 PM

PROCESSORS

Session Chair: **Joshua Friedrich,** *IBM, Austin, TX*
Associate Chair: **Luke Shin,** *Oracle, Santa Clara, CA*

3.1 A 22nm IA Multi-CPU and GPU System-on-Chip IDS **1:30 PM**

S. Damaraju[1], V. George[1], S. Jahagirdar[1], T. Khondker[1], R. Milstrey[1], S. Sarkar[1], S. Siers[1], I. Stolero[2], A. Subbiah[1]
[1]Intel, Folsom, CA
[2]Intel, Haifa, Israel

3.2 A 32-Core RISC Microprocessor With Network Accelerators, Power Management and Testability Features **2:00 PM**

B. Miller, D. Brasili, T. Kiszely, R. Kuhn, R. Mehrotra, M. Salvi, M. Kulkarni, A. Varadharajan, S-H. Yin, W. Lin, A. Hughes, B. Stysiack, V. Kandadi, I. Pragaspathi, D. Hartman, D. Carlson, V. Yalala, T. Xanthopoulos, S. Meninger, E. Crain, M. Spaeth, A. Aina, S. Balasubramanian, J. Vulih, P. Tiwary, D. Lin, R. Kessler, B. Fishbein, A. Jain
Cavium, Marlboro, MA

3.3 The Next-Generation 64b SPARC Core in a T4 SoC Processor **2:30 PM**

J. Shin, H. Park, H. Li, A. Smith, Y. Choi, H. Sathianathan, S. Dash, S. Turullols, S. Kim, R. Masleid, G. Konstadinidis, R. Golla, M. Doherty, G. Grohoski, C. McAllister
Oracle, Santa Clara, CA

Break 3:00 PM

3.4 32nm x86 OS-Compliant PC On-Chip With Dual-Core Atom® Processor and RF WiFi Transceiver **3:15 PM**

H. Lakdawala[1], M. Schaecher[2], C-T. Fu[1], R. Limaye[3], J. Duster[1], Y. Tan[1], A. Balankutty[1], E. Alpman[1], C. Lee[1], S. Suzuki[1], B. Carlton[1], H. Kim[1], M. Verhelst[1], S. Pellerano[1], T. Kim[2], D. Srivastava[1], S. Venkatesan[3], H-J. Lee[1], P. Vandervoorn[1], J. Rizk[1], C-H. Jan[1], K. Soumyanath[1], S. Ramamurthy[1]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ; [3]Intel, Santa Clara, CA

3.5 An 800MHz 320mW 16-Core Processor With Message-Passing and Shared-Memory Inter-Core Communication Mechanisms **3:45 PM**

Z. Yu, K. You, R. Xiao, H. Quan, P. Ou, Y. Ying, H. Yang, M. Jing, X. Zeng
Fudan University, Shanghai, China

3.6 A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS IDS **4:15 PM**

S. Jain[1], S. Khare[1], S. Yada[1], A. V[1], P. Salihundam[1], S. Ramani[1], S. Muthukumar[1], S. M[1], A. Kumar[1], S. Gb[1], R. Ramanarayanan[1], V. Erraguntla[1], J. Howard[2], S. Vangal[2], S. Dighe[2], G. Ruhl[2], P. Aseron[2], H. Wilson[2], N. Borkar[2], V. De[2], S. Borkar[2]
[1]Intel, Bangalore, India; [2]Intel, Hillsboro, OR

3.7 Resonant Clock Design for a Power-Efficient High-Volume x86-64 Microprocessor **4:45 PM**

V. Sathe[1], S. Arekapudi[2], A. Ishii[3], C. Ouyang[2], M. Papaefthymiou[3,4], S. Naffziger[1]
[1]AMD, Fort Collins, CO [2]AMD, Sunnyvale, CA
[3]Cyclos Semiconductor, Berkeley, CA; [4]University of Michigan, Ann Arbor, MI

3.8 A Reconfigurable Distributed All-Digital Clock Generator Core With SSC and Skew Correction in 22nm High-k Tri-Gate LP CMOS **5:00 PM**

Y. Li[1], C. Ornelas[2], H. Kim[1], H. Lakdawala[1], A. Ravi[1], K. Soumyanath[1]
[1]Intel, Hillsboro, OR; [2]Intel, Guadalajara, Mexico

Conclusion 5:15 PM

RF TECHNIQUES

Session Chair: **Masoud Zargari,** *Qualcomm, Irvine, CA*
Associate Chair: **Songcheol Hong,** *KAIST, Daejeon, Korea*

4.1 A Blocker-Tolerant Wideband Noise-Cancelling Receiver With a 2dB Noise Figure **1:30 PM**

D. Murphy[1,2], A. Hafez[1,2], A. Mirzaei[2], M. Mikhemar[2], H. Darabi[2], M-C. Chang[1], A. Abidi[1]
[1]University of California, Los Angeles, Los Angeles, CA
[2]Broadcom, Irvine, CA

4.2 8-Path Tunable RF Notch Filters for Blocker Suppression **2:00 PM**

A. Ghaffari, E. Klumperink, B. Nauta
University of Twente, Enschede, The Netherlands

4.3 A Wideband IM3 Cancellation Technique for CMOS Attenuators **2:30 PM**

W. Cheng, M. Oude Alink, A. Annema, G. Wienk, B. Nauta
University of Twente, Enschede, The Netherlands

4.4 A 1-to-2.5GHz Phased-Array IC Based on g_m-RC All-Pass Time-Delay Cells **2:45 PM**

S. Garakoui, E. Klumperink, B. Nauta, F. Van Vliet
University of Twente, Enschede, The Netherlands

Break **3:00 PM**

4.5 A Fully Integrated Dual-Mode CMOS Power Amplifier for WCDMA Applications **3:15 PM**

B. Koo[1], T. Joo[1], Y. Na[2], S. Hong[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electro-Mechanics, Suwon, Korea

4.6 A 28.3mW PA-Closed Loop for Linearity and Efficiency Improvement Integrated in a +27.1dBm WCDMA CMOS Power Amplifier **3:45 PM**

S. Kousai, K. Onizuka, T. Yamaguchi, Y. Kuriyama, M. Nagaoka
Toshiba, Kawasaki, Japan

4.7 A Fully Integrated Triple-Band CMOS Power Amplifier for WCDMA Mobile Handsets **4:15 PM**

K. Kanda[1], Y. Kawano[2], T. Sasaki[2], N. Shirai[2], T. Tamura[2], S. Kawai[2], M. Kudo[2], T. Murakami[2], H. Nakamoto[1], N. Hasegawa[2], H. Kano[2], N. Shimazui[2], A. Mineyama[3], K. Oishi[1], M. Shima[4], N. Tamura[4], T. Suzuki[3], T. Mori[1], K. Niratsuka[2], S. Yamaura[2]
[1]Fujitsu Laboratories, Kawasaki, Japan
[2]Fujitsu Semiconductor, Yokohama, Japan
[3]Fujitsu Laboratories, Atsugi, Japan
[4]Fujitsu Semiconductor, Mie, Japan

4.8 A 45nm SOI CMOS Class-D mm-Wave PA With >10V_{pp} Differential Swing **4:45 PM**

I. Sarkas, A. Balteanu, E. Dacquay, A. Tomkins, S. Voinigescu
University of Toronto, Toronto, ON, Canada

Conclusion **5:15 PM**

AUDIO AND POWER CONVERTERS

Session Chair: **Wing-Hung Ki,** *HKUST, Hong Kong, China*
Associate Chair: **Jed Hurwitz,** *Consultant, Edinburgh, United Kingdom*

5.1 An 8Ω 2.5W 1%-THD 104dB(A)-Dynamic-Range Class-D Audio Amplifier With an Ultra-Low EMI System and Current Sensing for Speaker Protection IDS **1:30 PM**

A. Nagari, E. Allier, F. Amiard, V. Binet, C. Fraisse
ST-Ericsson, Grenoble, France

5.2 A 1.5W 10V-Output Class-D Amplifier Using a Boosted Supply From a Single 3.3V Input in Standard 1.8V/3.3V 0.18μm CMOS **2:00 PM**

B. Serneels, E. Geukens, B. De Muer, T. Piessens
ICsense, Leuven, Belgium

5.3 A 0.028% THD+N, 91% Power-Efficiency, 3-Level PWM Class-D Amplifier With a True Differential Front-End **2:30 PM**

S. Kwon[1], I. Kim[2], S. Yi[1], S. Kang[1], S. Lee[1], T. Hwang[1], B. Moon[1], Y. Choi[1], H. Sung[1], J. Koh[1]
[1]Dongbu Hitek, Seoul, Korea
[2]Samsung Electronics, Kyunggi-Do, Korea

5.4 A 41-Phase Switched-Capacitor Power Converter With 3.8mV Output Ripple and 81% Efficiency in Baseline 90nm CMOS **2:45 PM**

G. Villar Piqué
NXP Semiconductors, Eindhoven, The Netherlands

Break 3:00 PM

5.5 A High-Voltage CMOS IC and Embedded System for Distributed Photovoltaic Energy Optimization With Over 99% Effective Conversion Efficiency and Insertion Loss Below 0.1% **3:15 PM**

J. Stauth[1,2], M. Seeman[2], K. Kesarwani[2]
[1]Dartmouth College, Hanover, NH
[2]Solar Semiconductor, Sunnyvale, CA

5.6 A Maximum Power-Point Tracker Without Digital Signal Processing in 0.35μm CMOS for Automotive Applications **3:45 PM**

R. Enne, M. Nikolic, H. Zimmermann
Vienna University of Technology, Vienna, Austria

5.7 A 40mV Transformer-Reuse Self-Startup Boost Converter With MPPT Control for Thermoelectric Energy Harvesting **4:15 PM**

J-P. Im[1], S-W. Wang[1], K-H. Lee[1], Y-J. Woo[2], Y-S. Yuk[1], T-H. Kong[1], S-W. Hong[1], S-T. Ryu[1], G-H. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Siliconworks, Daejeon, Korea

5.8 A 330nA Energy-Harvesting Charger With Battery Management for Solar and Thermoelectric Energy Harvesting IDS **4:45 PM**

K. Kadirvel[1], Y. Ramadass[2], U. Lyles[1], J. Carpenter[1], A. Chandrakasan[3], B. Lum-Shue-Chan[1]
[1]Texas Instruments, Melbourne, FL
[2]Texas Instruments, Dallas, TX
[3]Massachusetts Institute of Technology, Cambridge, MA

Conclusion 5:15 PM

MEDICAL, DISPLAYS AND IMAGERS

Session Chair: **Yusuke Oike,** *Sony, Atsugi, Japan*
Associate Chair: **Maysam Ghovanloo,** *Georgia Institute of Technology, Atlanta, GA*

6.1 A Sampling-Based 128×128 Direct Photon-Counting X-Ray Image Sensor With 3 Energy Bins and Spatial Resolution of 60μm/pixel **1:30 PM**

H-S. Kim[1], S-W. Han[2], J-H. Yang[1], S. Kim[2], Y. Kim[2], S. Kim[2], D-K. Yoon[2], J-S. Lee[2], J-C. Park[2], Y. Sung[2], S-D. Lee[2], S-T. Ryu[1], G-H. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Advanced Institute of Technology, Yongin, Korea

6.2 A 1.36μW Adaptive CMOS Image Sensor With Reconfigurable Modes of Operation From Available Energy/Illumination for Distributed Wireless Sensor Network **2:00 PM**

J. Choi, S. Park, J. Cho, E. Yoon; University of Michigan, Ann Arbor, MI

6.3 A 0.5V 4.95μW 11.8fps PWM CMOS Imager With 82dB Dynamic Range and 0.055% Fixed-Pattern-Noise **2:30 PM**

M-T. Chung, C-C. Hsieh; National Tsing Hua University, Hsinchu, Taiwan

6.4 A Capacitive Touch Controller Robust to Display Noise for Ultrathin Touch Screen Displays **2:45 PM**

K-D. Kim, S-H. Byun, Y-K. Choi, J-H. Baek, H-H. Cho, J-K. Park, H-Y. Ahn, C-J. Lee, M-S. Cho, J-H. Lee, S-W. Kim, H-D. Kwon, Y-Y. Choi, H. Na, J. Park, Y-J. Shin, K. Jang, G. Hwang, M. Lee
Samsung Electronics, Yongin, Korea

Break 3:00 PM

6.5 A 160μA Biopotential Acquisition ASIC With Fully Integrated IA and Motion-Artifact Suppression IDS **3:15 PM**

N. Van Helleputte[1], S. Kim[1], H. Kim[1], J. Kim[2], C. Van Hoof[1,3], R. Yazicioglu[1]
[1]imec, Heverlee, Belgium; [2]Samsung Advanced Institute of Technology, Yongin, Korea
[3]KU Leuven, Leuven, Belgium

6.6 CMOS Capacitive Biosensor With Enhanced Sensitivity for Label-Free DNA Detection **3:45 PM**

K-H. Lee, S. Choi, J. Lee, J-B. Yoon, G-H. Cho; KAIST, Daejeon, Korea

6.7 A 100Mphoton/s Time-Resolved Mini-Silicon Photomultiplier With On-Chip Fluorescence Lifetime Estimation in 0.13μm CMOS Imaging Technology **4:00 PM**

D. Tyndall[1], B. Rae[2], D. Li[3], J. Richardson[4], J. Arlt[1], R. Henderson[1]
[1]University of Edinburgh, Edinburgh, United Kingdom
[2]STMicroelectronics, Edinburgh, United Kingdom
[3]University of Sussex, Brighton, United Kingdom
[4]Dialog Semiconductor, Edinburgh, United Kingdom

6.8 A Wireless Magnetoresistive Sensing System for an Intra-Oral Tongue-Computer Interface ADS **4:15 PM**

H. Park[1], B. Gosselin[2], M. Kiani[1], H-M. Lee[1], J. Kim[1], X. Huo[1], M. Ghovanloo[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Laval University, Quebec, QC, Canada

6.9 A CMOS 10kpixel Baseline-Free Magnetic Bead Detector With Column-Parallel Readout for Miniaturized Immunoassays **4:45 PM**

S. Gambini, K. Skucha, P. Liu, J. Kim, R. Krigel, R. Mathies, B. Boser
University of California at Berkeley, Berkeley, CA

Conclusion 5:15 PM

ACADEMIC DEMONSTRATION SESSION (ADS)*

ISSCC 2012 is expanding the industrial demonstration event introduced last year to include the Academic Demonstration Session (ADS), to be held on Monday February 20th, from 4 to 7 pm, Golden Gate Hall. ADS will feature live demonstrations of selected ICs presented by academics in regular paper sessions. ADS is intended to demonstrate real-life applications made possible by new ICs presented this year. In the Advance Program, papers for which demonstrations are available will be notated by the symbol ADS, ADS

Monday, February 20th

6.8	**A Wireless Magnetoresistive Sensing System for an Intra-Oral Tongue-Computer Interface**	**4:15 PM**

Tuesday, February 21st

10.6	**3D-MAPS: 3D Massively Parallel Processor With Stacked Memory**	**10:45 AM**
10.7	**Centip3De: A 3930DMIPS/W Configurable Near-Threshold 3D Stacked System With 64 ARM Cortex-M3 Cores**	**11:15 AM**
11.5	**A ±0.4°C (3σ) -70 to 200°C Time-Domain Temperature Sensor Based on Heat Diffusion in Si and SiO_2**	**10:15 AM**
12.4	**A 320mW 342GOPS Real-Time Moving Object Recognition Processor for HD 720p Video Streams**	**3:15 PM**
15.1	**A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications**	**1:30 PM**
16.8	**Voltage-Boosting Wireless Power Delivery System With Fast Load Tracker by ΔΣ-Modulated Sub-Harmonic Resonant Switching**	**5:00 PM**
17.2	**A 259.6μW Nonlinear HRV-EEG Chaos Processor With Body Channel Communication Interface for Mental Health Monitoring**	**2:00 PM**
17.3	**A Sub-10nA DC-Balanced Adaptive Stimulator IC With Multimodal Sensor for Compact Electro-Acupuncture System**	**2:30 PM**

Wednesday, February 22nd

22.2	**A Global-Shutter CMOS Image Sensor With Readout Speed of 1Tpixel/s Burst and 780Mpixel/s Continuous**	**9:00 AM**
25.2	**Over-10×-Extended-Lifetime 76%-Reduced-Error Solid-State Drives (SSDs) With Error-Prediction LDPC Architecture and Error-Recovery Scheme**	**2:00 PM**
26.4	**An Interference-Aware 5.8GHz Wake-Up Radio for ETCS**	**3:15 PM**
28.4	**A 200mV 32b Subthreshold Processor With Adaptive Supply Voltage Control**	**2:45 PM**

**ADS may include additional demonstrations of work reported at the Student Research Preview.*

ES3: Technologies that Could Change the World – You Decide!

Organizer: Jed Hurwitz, *Broadcom, Edinburgh, United Kingdom*

Chair: Jafar Savoj, *Xilinx, San Jose, CA*

Often a new technology comes along that is just plain different than incumbent solutions or approaches. This session looks at a number of recent ideas that are asking us to re-assess the way things are done today. It should be an entertaining evening, providing an overview of the new technologies, their key benefits (and weaknesses) and an update on where they now sit, and which barriers and markets they may conquer.

There will be an opportunity for the audience to question the speakers, as there will undoubtedly be interesting alternative viewpoints!

Time	Topic
8:00	**MEMS-Based Resonators and Oscillators are Now Replacing Quartz** **Aaron Partridge,** *SiTime, Sunnyvale, CA*
8:25	**Thermal Diffusivity Sensors: Temperature Sensors that Scale!** **Kofi Makinwa,** *Delft University of Technology, Delft, The Netherlands*
8:50	**VCO-Based Quantizers: Has Their Time Arrived?** **Michael H. Perrot,** *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*
9:15	**Continuous Time DSPs** **Yannis Tsividis,** *Columbia University, New York, NY*
9:40	**Analog Syntheses: Computer-Aided Design to Secure Analog Design Quality and Productivity** **Georges Gielen,** *Katholik University of Leuven, Leuven, Belgium*

ES4: Optical PCB Interconnects, Niche or Mainstream?

Organizer: **Ichiro Fujimori,** *Broadcom, Irvine, CA*
Organizer: **SeongHwan Cho,** *KAIST, Daejon, Korea*
Organizer: **Joshua Friedrich,** *IBM, Austin, TX*

Chair: **John Stonick,** *Synopsis, Hillsboro, OR*

Efforts in the area of optical backplane technology have been underway for several years, generating significant interest. Recently, these efforts have led to discussions regarding the role of embedded optics for chip-to-chip communication on printed circuit boards. A consensus appears to be emerging that PCB interconnects for mainframes and high-end servers will leverage optical technologies, but will these approaches ever go mainstream? In this evening session, we will review the latest in optical interconnect-related circuit design, the prospects for optics use in mainstream I/O applications, and to provide comparison to copper-based solutions and associated roadmaps.

Time	Topic
8:00	**Optical Interconnects – Why We Will Have To Use Them** **David Miller** *Stanford University, Stanford, CA*
8:30	**Optical PCB Interconnects For Computing Applications: From Niche to Mainstream** **Bert Offrein** *IBM Research, Zurich, Switzerland*
9:00	**Integrated Silicon Photonics and Applications In and Around PC/Servers** **Mario Paniccia,** *Intel, Santa Clara, CA*
9:30	**The Final Push to Mainstream; Can Integrated Optics Learn From Integrated Magnetics?** **Keishi Ohashi,** *NEC, Tsukuba, Japan*

EP1: "Is RF Doomed to Digitization? What Shall RF Circuit Designers Do?"

Organizer: **R. Bogdan Staszewski,** *Delft University of Technology, Delft, The Netherlands*

Moderator: **Jacques Rudell**, *University of Washington, Seattle, WA*

The most recent trend in RF design is toward more and more digital content. This is very intriguing but, at the same time, it could be quite challenging to traditionally-minded designers as well as new entrants who have been educated using contemporary textbooks that are yet to be updated. What is the ultimate destiny of RF architectural and circuit design? Will RF share the same digitization fate as, for example, the audio on cellular phones? Are there any alternatives or safe havens far from the digital encroachment? Seven leading experts from industry and academia will debate this controversial topic.

Panelists:

Borivoje Nikolic, *UC Berkeley, Berkeley, CA*
Oren Eliezer, *Xtendwave, Plano, TX*
Ken Hansen, *Freescale, Austin, TX*
Rik Jos, *NXP, Nijmegen, The Netherlands*
Andreas Kaiser, *IEMN-ISEN, Lille, France*
Lawrence Loh, *Mediatek, Hsinchu, Taiwan*
Akira Matsuzawa, *Tokyo Institute of Technology, Tokyo, Japan*

MULTI GB/s RECEIVER AND PARALLEL I/O TECHNIQUES

Session Chair: **Bob Payne,** *Texas Instruments, Dallas, TX*
Associate Chair: **Tatsuya Saito,** *Hitachi, Kawasaki, Kanagawa, Japan*

7.1 An 18.6Gb/s Double-Sampling Receiver in 65nm CMOS for Ultra-Low-Power Optical Communication **8:30 AM**

M. Honarvar Nazari, A. Emami-Neyestanak
California Institute of Technology, Pasadena, CA

7.2 A 0.4mW/Gb/s 16Gb/s Near-Ground Receiver Front-End With Replica Transconductance Termination Calibration **9:00 AM**

K. Kaviani, A. Amirkhany, C. Huang, P. Le, C. Madden, K. Saito, K. Sano, V. Murugan, W. Beyene, K. Chang, C. Yuan
Rambus, Sunnyvale, CA

7.3 A 19Gb/s Serial Link Receiver With Both 4-Tap FFE and 5-Tap DFE Functions in 45nm SOI CMOS **9:30 AM**

A. Agrawal, J. Bulzacchelli, T. Dickson, Y. Liu, J. Tierno, D. Friedman
IBM T. J. Watson, Yorktown Heights, NY

Break 10:00 AM

7.4 An 8GB/s Quad-Skew-Cancelling Parallel Transceiver in 90nm CMOS for High-Speed DRAM Interface **10:15 AM**

Y-S. Kim[1], S-K. Lee[1], S-J. Bae[2], Y-S. Sohn[2], J-B. Lee[2], J. Choi[2], H-J. Park[1], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwasung, Korea

7.5 A 4.1pJ/b 16Gb/s Coded Differential Bidirectional Parallel Electrical Link IDS **10:45 AM**

A. Amirkhany[1], K. Kaviani[1], A. Abbasfar[1], F. Shuaeb[2], W. Beyene[1], C. Hoshino[3], C. Madden[1], K. Chang[1], C. Yuan[1]
[1]Rambus, Sunnyvale, CA
[2]Rambus, Bangalore, India
[3]Rambus, Tokyo, Japan

7.6 A 5Gb/s Single-Ended Parallel Receiver With Adaptive FEXT Cancellation **11:15 AM**

S-K. Lee, H. Ha, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

7.7 A Compact Low-Power 3D I/O in 45nm CMOS **11:45 AM**

Y. Liu, W. Luk, D. Friedman
IBM T. J. Watson, Yorktown Heights, NY

Conclusion 12:15 PM

DELTA-SIGMA CONVERTERS

Session Chair: **Brian Brandt,** *Maxim Integrated Products, North Chelmsford, MA*
Associate Chair: **Gerhard Mitteregger,** *Intel Mobile, Villach, Austria*

8.1 An LC Bandpass ΔΣ ADC With 70dB SNDR Over 20MHz Bandwidth Using CMOS DACs **8:30 AM**

J. Harrison[1], M. Nesselroth[1], R. Mamuad[1], A. Behzad[2], A. Adams[1], S. Avery[1]
[1]Broadcom, Sydney, Australia
[2]Broadcom, San Diego, CA

8.2 A 12mW Low-Power Continuous-Time Bandpass ΔΣ Modulator With 58dB SNDR and 24MHz Bandwidth at 200MHz IF **9:00 AM**

H. Chae[1,2], J. Jeong[1], G. Manganaro[2], M. Flynn[1]
[1]University of Michigan, Ann Arbor, MI
[2]Analog Devices, Wilmington, MA

8.3 A DC-to-1GHz Tunable RF ΔΣ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW **9:30 AM**

H. Shibata[1], R. Schreier[1], W. Yang[2], A. Shaikh[2,3], D. Paterson[2], T. Caldwell[1], D. Alldred[1], P. Lai[2]
[1]Analog Devices, Toronto, ON, Canada
[2]Analog Devices, Wilmington, MA
[3]now independent consultant, Lahore, Pakistan

Break 10:00 AM

8.4 A 16mW 78dB-SNDR 10MHz-BW CT-ΔΣ ADC Using Residue-Cancelling VCO-Based Quantizer **10:15 AM**

K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, P. Hanumolu
Oregon State University, Corvallis, OR

8.5 A 72dB-DR ΔΣ CT Modulator Using Digitally Estimated Auxiliary DAC Linearization Achieving 88fJ/conv in a 25MHz BW **10:45 AM**

P. Witte[1], J. Kauffman[1], J. Becker[1], Y. Manoli[2], M. Ortmanns[1]
[1]Ulm University, Ulm, Germany
[2]University of Freiburg - IMTEK, Freiburg, Germany

8.6 A 15mW 3.6GS/s CT-ΔΣ ADC With 36MHz Bandwidth and 83dB DR in 90nm CMOS **11:15 AM**

P. Shettigar, S. Pavan
IIT Madras, Chennai, India

8.7 A 20mW 61dB SNDR (60MHz BW) 1b 3rd-Order Continuous-Time Delta-Sigma Modulator Clocked at 6GHz in 45nm CMOS **11:45 AM**

V. Srinivasan, V. Wang, P. Satarzadeh, B. Haroun, M. Corsi
Texas Instruments, Dallas, TX

Conclusion 12:15 PM

WIRELESS TRANSCEIVER TECHNIQUES

Session Chair: **Sven Mattisson,** *Ericsson, Lund, Sweden*
Associate Chair: **Shouhei Kousai,** *Toshiba, Kawasaki, Japan*

9.1 A 40MHz-to-1GHz Fully Integrated Multistandard Silicon Tuner in 80nm CMOS — 8:30 AM

J. Greenberg[1], F. De Bernardinis[2], C. Tinella[2], A. Milani[2], J. Pan[1], P. Uggetti[2], M. Sosio[3], S. Dai[1], S. Tang[1], G. Cesura[2], G. Gandolfi[2], V. Colonna[2], R. Castello[2,3]
[1]Marvell, Santa Clara, CA
[2]Marvell, Pavia, Italy
[3]University of Pavia, Pavia, Italy

9.2 A Multiband Multimode Transmitter Without Driver Amplifier — 9:00 AM

O. Oliaei, M. Kirschenmann, D. Newman, K. Hausmann, H. Xie, P. Rakers, M. Rahman, M. Gomez, C. Yu, B. Gilsdorf, K. Sakamoto
Fujitsu Semiconductor Wireless, Tempe, AZ

9.3 Active Feedback Receiver With Integrated Tunable RF Channel Selectivity, Distortion Cancelling, 48dB Stopband Rejection and >+12dBm Wideband IIP3, Occupying <0.06mm² in 65nm CMOS — 9:30 AM

S. Youssef, R. Van der Zee, B. Nauta
University of Twente, Enschede, The Netherlands

Break 10:00 AM

9.4 A 20dBm 2.4GHz Digital Outphasing Transmitter for WLAN Application in 32nm CMOS — 10:15 AM

P. Madoglio[1], A. Ravi[1], H. Xu[1], K. Chandrashekar[1], M. Verhelst[1], S. Pellerano[1], L. Cuellar[2], M. Aguirre[2], M. Sajadieh[3], O. Degani[4], H. Lakdawala[1], Y. Palaskas[1]
[1]Intel, Hillsboro, OR
[2]Intel, Guadalajara, Mexico
[3]Intel, Santa Clara, CA
[4]Intel, Haifa, Israel

9.5 A 60GHz Outphasing Transmitter in 40nm CMOS With 15.6dBm Output Power — 10:30 AM

D. Zhao, S. Kulkarni, P. Reynaert
KU Leuven, Leuven, Belgium

9.6 A 4-in-1 (WiFi/BT/FM/GPS) Connectivity SoC With Enhanced Co-Existence Performance in 65nm CMOS — 10:45 AM

Y-H. Chung[1], M. Chen[1], W-K. Hong[1], J-W. Lai[1], S-J. Wong[2], C-W. Kuan[1], H-L. Chu[1], C. Lee[1], C-F. Liao[1], H-Y. Liu[1], H-K. Hsu[1], L-C. Ko[1], K-H. Chen[1], C-H. Lu[1], T-M. Chen[1], Y. Hsueh[1], C. Chang[1], Y-H. Cho[1], C-H. Shen[1], Y. Sun[2], E-C. Low[2], X. Jiang[2], D. Hu[2], W. Shu[2], J-R. Chen[1], J-L. Hsu[1], C-J. Hsu[1], J-H. Zhan[1], O. Shana¡¦A[2], G-K. Dehng[1], G. Chien[3]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Singapore
[3]MediaTek, San Jose, CA

9.7 A 1.5-to-5.0GHz Input-Matched +2dBm P_{1dB} All-Passive Switched-Capacitor Beamforming Receiver Front-End in 65nm CMOS — 11:15 AM

M. Soer[1], E. Klumperink[1], B. Nauta[1], F. Van Vliet[1,2]
[1]University of Twente, Enschede, The Netherlands
[2]TNO Science and Industry, The Hague, The Netherlands

Conclusion 11:30 AM

HIGH-PERFORMANCE DIGITAL

Session Chair: **Lew Chua-Eoan,** *Qualcomm, San Diego, CA*
Associate Chair: **Se-Hyun Yang,** *Samsung Electronics, Yongin, Korea*

10.1 A 280mV-to-1.1V 256b Reconfigurable SIMD Vector Permutation Engine With 2-Dimensional Shuffle in 22nm CMOS **8:30 AM**

S. Hsu, A. Agarwal, M. Anders, S. Mathew, H. Kaul, F. Sheikh, R. Krishnamurthy
Intel, Hillsboro, OR

10.2 A Source-Synchronous 90Gb/s Capacitively Driven Serial On-Chip Link Over 6mm in 65nm CMOS **9:00 AM**

D. Walter, S. Höppner, H. Eisenreich, G. Ellguth, S. Henker, S. Hänzsche, R. Schüffny, M. Winter, G. Fettweis
Technical University Dresden, Dresden, Germany

10.3 A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit With Certainty Tracking in 32nm CMOS IDS **9:30 AM**

H. Kaul, M. Anders, S. Mathew, S. Hsu, A. Agarwal, F. Sheikh, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

10.4 A 2.05GVertices/s 151mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32nm CMOS **9:45 AM**

F. Sheikh, S. Mathew, M. Anders, H. Kaul, S. Hsu, A. Agarwal, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

Break 10:00 AM

10.5 A 3D System Prototype of an eDRAM Cache Stacked Over Processor-Like Logic Using Through-Silicon Vias **10:15 AM**

M. Wordeman[1], J. Silberman[1], G. Maier[2], M. Scheuermann[1]
[1]IBM T. J. Watson, Yorktown Heights, NY
[2]IBM Systems and Technology Group, Fishkill, NY

10.6 3D-MAPS: 3D Massively Parallel Processor With Stacked Memory ADS **10:45 AM**

D. Kim[1], K. Athikulwongse[1], M. Healy[1], M. Hossain[1], M. Jung[1], I. Khorosh[1], G. Kumar[1], Y-J. Lee[1], D. Lewis[1], T-W. Lin[1], C. Liu[1], S. Panth[1], M. Pathak[1], M. Ren[1], G. Shen[1], T. Song[1], D. Woo[1], X. Zhao[1], J. Kim[2], H. Choi[3], G. Loh[1], H-H. Lee[1], S. Lim[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]KAIST, Daejeon, Korea
[3]Amkor Technology, Seoul, Korea

10.7 Centip3De: A 3930DMIPS/W Configurable Near-Threshold 3D Stacked System With 64 ARM Cortex-M3 Cores ADS **11:15 AM**

D. Fick, R. Dreslinski, B. Giridhar, G. Kim, S. Seo, M. Fojtik, S. Satpathy, Y. Lee, D. Kim, N. Liu, M. Wieckowski, G. Chen, T. Mudge, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

10.8 K Computer: 8.162 PetaFLOPS Massively Parallel Scalar Supercomputer Built With Over 548k Cores **11:45 AM**

H. Miyazaki[1], Y. Kusano[1], H. Okano[1], T. Nakada[1], K. Seki[1], T. Shimizu[1], N. Shinjo[1], F. Shoji[2], A. Uno[2], M. Kurokawa[2]
[1]Fujitsu, Kanagawa, Japan
[2]RIKEN, Hyogo, Japan

Conclusion 12:15 PM

SENSORS & MEMs

Session Chair: **Christoph Hagleitner,** *IBM Research, Ruschlikon, Switzerland*
Associate Chair: **Maurits Ortmanns,** *University of Ulm, Ulm, Germany*

11.1 A ΔΣ Interface for MEMS Accelerometers Using Electrostatic Spring-Constant Modulation for Cancellation of Bondwire Capacitance Drift **8:30 AM**

P. Lajevardi[1], V. Petkov[2], B. Murmann[1]
[1]Stanford University, Stanford, CA
[2]Robert Bosch, Palo Alto, CA

11.2 A Capacitance-to-Digital Converter for Displacement Sensing with 17b Resolution and 20μs Conversion Time **9:00 AM**

S. Xia, K. Makinwa, S. Nihtianov
Delft University of Technology, Delft, The Netherlands

11.3 A 50μW Biasing Feedback Loop With 6ms Settling Time for a MEMS Microphone With Digital Output **9:15 AM**

J. Van den Boom
NXP Semiconductors, Nijmegen, The Netherlands

11.4 ASIC for a Resonant Wireless Pressure-Sensing System for Harsh Environments Achieving ±2% Error Between -40 and 150°C Using Q-Based Temperature Compensation **9:30 AM**

M. Rocznik[1], F. Henrici[2], R. Has[2]
[1]Robert Bosch, Palo Alto, CA
[2]Robert Bosch, Stuttgart, Germany

Break **10:00 AM**

11.5 A ±0.4°C (3σ) -70 to 200°C Time-Domain Temperature Sensor Based on Heat Diffusion in Si and SiO_2 ADS **10:15 AM**

C. Van Vroonhoven[1], D. D'Aquino[2], K. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]National Semiconductor, Santa Clara, CA

11.6 A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator With Better Than ±0.5ppm Frequency Stability IDS **10:45 AM**

M. Perrott[1], J. Salvia[2], F. Lee[3], A. Partridge[2], S. Mukherjee[2], C. Arft[2], J-T. Kim[2], N. Arumugam[2], P. Gupta[2], S. Tabatabaei[2], S. Pamarti[4], H. Lee[2], F. Assaderaghi[2]
[1]Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
[2]SiTime, Sunnyvale, CA
[3]Fairchild Semiconductor, San Jose, CA
[4]University of California, Los Angeles, Los Angeles, CA

11.7 A CMOS Temperature Sensor With a Voltage-Calibrated Inaccuracy of ±0.15°C (3σ) From -55 to 125°C **11:15 AM**

K. Souri, Y. Chae, K. Makinwa
Delft University of Technology, Delft, The Netherlands

11.8 Ratiometric BJT-Based Thermal Sensor in 32nm and 22nm Technologies **11:45 AM**

J. Shor, K. Luria, D. Zilberman
Intel, Yakum, Israel

Conclusion **12:15 PM**

MULTIMEDIA & COMMUNICATIONS SOCs

Session Chair: **Byeong-Gyu Nam,** *Chungnam National University, Daejeon, Korea*
Associate Chair: **Shannon Morton,** *Nvidia, Bristol, United Kingdom*

12.1 A 32nm High-k Metal Gate Application Processor with GHz Multi-Core CPU IDS **1:30 PM**

S-H. Yang, S. Lee, J. Lee, J. Cho, H-J. Lee, D. Cho, J. Heo, S. Cho, Y. Shin, S. Yun, E. Kim, U. Cho, J. Son, C. Kim, J. Youn, Y. Chung, S. Park, S. Hwang
Samsung Electronics, Yongin, Korea

12.2 A 335Mb/s 3.9mm² 65nm CMOS Flexible MIMO Detection-Decoding Engine Achieving 4G Wireless Data Rates **2:00 PM**

M. Winter[1], S. Kunze[1], E. Perez Adeva[1], B. Mennenga[1], E. Matûs[1], G. Fettweis[1], H. Eisenreich[1], G. Ellguth[1], S. Höppner[1], S. Scholze[1], R. Schüffny[1], T. Kobori[2]
[1]Technical University Dresden, Dresden, Germany
[2]NEC, Tokyo, Japan

12.3 A Full 4-Channel 6.3Gb/s 60GHz Direct-Conversion Transceiver With Low-Power Analog and Digital Baseband Circuitry **2:30 PM**

K. Okada[1], K. Kondou[2], M. Miyahara[1], M. Shinagawa[2], H. Asada[1], R. Minami[1], T. Yamaguchi[1], A. Musa[1], Y. Tsukui[1], Y. Asakura[2], S. Tamonoki[2], H. Yamagishi[2], Y. Hino[2], T. Sato[1], H. Sakaguchi[1], N. Shimasaki[1], T. Ito[1], Y. Takeuchi[1], N. Li[1], Q. Bu[1], R. Murakami[1], K. Bunsen[1], K. Matsushita[1], M. Noda[2], A. Matsuzawa[1]
[1]Tokyo Institute of Technology, Tokyo, Japan
[2]Sony, Tokyo, Japan

Break 3:00 PM

12.4 A 320mW 342GOPS Real-Time Moving Object Recognition Processor for HD 720p Video Streams ADS **3:15 PM**

J. Oh, G. Kim, J. Park, I. Hong, S. Lee, H-J. Yoo
KAIST, Daejeon, Korea

12.5 A 464GOPS 620GOPS/W Heterogeneous Multi-Core SoC for Image-Recognition Applications IDS **3:45 PM**

Y. Tanabe, M. Sumiyoshi, M. Nishiyama, I. Yamazaki, S. Fujii, K. Kimura, T. Aoyama, M. Banno, H. Hayashi, T. Miyamori
Toshiba, Kawasaki, Japan

12.6 A 2Gpixel/s H.264/AVC HP/MVC Video Decoder Chip for Super Hi-Vision and 3DTV/FTV Applications **4:15 PM**

D. Zhou[1], J. Zhou[1], J. Zhu[2], P. Liu[2], S. Goto[1]
[1]Waseda University, Kitakyushu, Japan
[2]Shanghai Jiao Tong University, Shanghai, China

12.7 A True Multistandard, Programmable, Low-Power, Full HD Video-Codec Engine for Smartphone SoC IDS **4:45 PM**

M. Mehendale[1], S. Das[1], M. Sharma[1], M. Mody[1], R. Reddy[1], J. Meehan[2], H. Tamama[3], B. Carlson[3], M. Polley[3]
[1]Texas Instruments, Bangalore, India
[2]Texas Instruments, Nice, France
[3]Texas Instruments, Dallas, TX

Conclusion 5:15 PM

HIGH-PERFORMANCE EMBEDDED SRAM

Session Chair: **Leland Chang,** *IBM T.J. Watson, Yorktown Heights, NY*
Associate Chair: **Michael Clinton,** *Texas Instruments, Dallas, TX*

13.1 A 4.6GHz 162Mb SRAM Design in 22nm Tri-Gate CMOS Technology With Integrated Active V_{MIN}-Enhancing Assist Circuitry **1:30 PM**

E. Karl, Y. Wang, Y-G. Ng, Z. Guo, F. Hamzaoglu, U. Bhattacharya, K. Zhang, K. Mistry, M. Bohr
Intel, Hillsboro, OR

13.2 A 6T SRAM With a Carrier-Injection Scheme to Pinpoint and Repair Fails That Achieves 57% Faster Read and 31% Lower Read Energy **2:00 PM**

K. Miyaji[1], T. Suzuki[2], S. Miyano[2], K. Takeuchi[1]
[1]University of Tokyo, Tokyo, Japan
[2]Semiconductor Technology Academic Research Center, Yokohama, Japan

13.3 Capacitive-Coupling Wordline Boosting with Self-Induced V_{CC} Collapse for Write V_{MIN} Reduction in 22-nm 8T SRAM **2:30 PM**

J. Kulkarni, B. Geuskens, T. Karnik, M. Khellah, J. Tschanz, V. De
Intel, Hillsboro, OR

13.4 A 28nm 360ps-Access-Time Two-Port SRAM With a Time-Sharing Scheme to Circumvent Read Disturbs **2:45 PM**

Y. Ishii[1], Y. Tsukamoto[1], K. Nii[1], H. Fujiwara[1], M. Yabuuchi[1], K. Tanaka[2], S. Tanaka[1], Y. Shimazaki[1]
[1]Renesas Electronics, Kodaira, Tokyo, Japan
[2]Renesas Electronics, Itami, Hyogo, Japan

Break 3:00 PM

DIGITAL CLOCKING & PLLs

Session Chair: **Anthony Hill,** *Texas Instruments, Dallas, TX*
Associate Chair: **Hiroo Hayashi,** *Toshiba Semiconductor, Kawasaki, Japan*

14.1 A 0.004mm² 250μW ΔΣ TDC With Time-Difference Accumulator and a 0.012mm² 2.5mW Bang-Bang Digital PLL Using PRNG for Low-Power SoC Applications **3:15 PM**

J-P. Hong, S-J. Kim, J. Liu, N. Xing, T-K. Jang, J. Park, J. Kim, T. Kim, H. Park
Samsung Electronics, Yongin, Korea

14.2 A 1.5GHz 890μW Digital MDLL With 400fs$_{rms}$ Integrated Jitter, -55.6dBc Reference Spur and 20fs/mV Supply-Noise Sensitivity Using 1b TDC **3:45 PM**

A. Elshazly, R. Inti, B. Young, P. Hanumolu
Oregon State University, Corvallis, OR

14.3 A 6.7MHz-to-1.24GHz 0.0318mm² Fast-Locking All-Digital DLL in 90nm CMOS **4:15 PM**

M-H. Hsieh, L-H. Chen, S-I. Liu, C-P. Chen
National Taiwan University, Taipei, Taiwan

14.4 A TDC-Less ADPLL With 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS **4:30 PM**

N. August, H-J. Lee, M. Vandepas, R. Parker
Intel, Portland, OR

14.5 A Digitally Stabilized Type-III PLL Using Ring VCO With 1.01ps$_{rms}$ Integrated Jitter in 65nm CMOS **4:45 PM**

A. Sai, Y. Kobayashi, S. Saigusa, O. Watanabe, T. Itakura
Toshiba, Kawasaki, Japan

Conclusion **5:15 PM**

mm-WAVE & THz TECHNIQUES

Session Chair: **Ehsan Afshari,** *Cornell University, Ithaca, NY*
Associate Chair: **Yorgos Palaskas,** *Intel, Hillsboro, OR*

15.1 A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications ADS **1:30 PM**

H. Sherry[1,2,3], J. Grzyb[2], Y. Zhao[2], R. Al Hadi[2], A. Cathelin[1], A. Kaiser[3], U. Pfeiffer[2]
[1]STMicroelectronics, Crolles, France; [2]University of Wuppertal, Wuppertal, Germany
[3]IEMN / ISEN, Lille, France

15.2 280GHz and 860GHz Image Sensors Using Schottky-Barrier Diodes in 0.13μm Digital CMOS **2:00 PM**

R. Han[1,2], Y. Zhang[3], Y. Kim[3], D. Kim[3], H. Shichijo[3], E. Afshari[2], K. O[3]
[1]University of Florida, Gainesville, FL; [2]Cornell University, Ithaca, NY
[3]University of Texas at Dallas, Richardson, TX

15.3 A 0.28THz 4×4 Power-Generation and Beam-Steering Array **2:30 PM**
K. Sengupta, A. Hajimiri; California Institute of Technology, Pasadena, CA

15.4 A 283-to-296GHz VCO With 0.76mW Peak Output Power in 65nm CMOS **2:45 PM**

Y. M. Tousi, O. Momeni, E. Afshari; Cornell University, Ithaca, NY

Break 3:00 PM

15.5 A 1V 19.3dBm 79GHz Power Amplifier in 65nm CMOS **3:15 PM**

K-Y. Wang, T-Y. Chang, C-K. Wang
National Taiwan University, Taipei, Taiwan

15.6 A 9% Power Efficiency 121-to-137GHz Phase-Controlled Push-Push Frequency Quadrupler in 0.13μm SiGe BiCMOS **3:30 PM**

Y. Wang[1,2], W. Goh[1], Y-Z. Xiong[2,3]
[1]Nanyang Technological University, Singapore; [2]Institute of Microelectronics, Singapore
[3]MicroArray Technologies, Chengdu, China

15.7 A 144GHz 0.76cm-Resolution Sub-Carrier SAR Phase Radar for 3D Imaging in 65nm CMOS **3:45 PM**

A. Tang[1], G. Virbila[1], D. Murphy[1], F. Hsiao[1], Y. Wang[1], Q. Gu[2], Z. Xu[3], Y. Wu[4], M. Zhu[1], M-C. Chang[1]
[1]University of California, Los Angeles, Los Angeles, CA; [2]University of Florida, Gainsville, FL
[3]HRL, Malibu, CA; [4]Northrop Grumman Aerospace Systems, Los Angeles, CA

15.8 A 2Gb/s-Throughput CMOS Transceiver Chipset With In-Package Antenna for 60GHz Short-Range Wireless Communication **4:15 PM**

T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, T. Tomizawa
Toshiba, Kawasaki, Japan

15.9 A Low-Power 57-to-66GHz Transceiver in 40nm LP CMOS With -17dB EVM at 7Gb/s **4:45 PM**

V. Vidojkovic[1], G. Mangraviti[1,2], K. Khalaf[1,2], V. Szortyka[1,2], K. Vaesen[1], W. Van Thillo[1], B. Parvais[1], M. Libois[1], S. Thijs[1], J. Long[3], C. Soens[1], P. Wambacq[1,2]
[1]imec, Heverlee, Belgium; [2]Vrije Universiteit Brussel, Brussel, Belgium
[3]Delft University of Technology, Delft, The Netherlands

15.10 A 4-Path 42.8-to-49.5GHz LO Generation With Automatic Phase Tuning for 60GHz Phased-Array Receivers **5:00 PM**

L. Wu, A. Li, H. Luong
Hong Kong University of Science and Technology, Hong Kong, China

Conclusion 5:15 PM

Sunday, February 19th			ISSCC
8:00AM	**T1:** RF Mixers: Analysis & Design Trade-offs		**T2:** Flash-Memory
10:00AM	**T3:** Mobile GHz Processor Design Techniques		**T4:** W
12:30PM	**T6:** Power Management Using Integrated Voltage Regulators		**T7:** Dig
2:30PM	**T8:** Managing Offset & Flicker Noise		**T9:** Getting In Touch
			ISSCC
8:00AM	**F1:** Beamforming Techniques & RF Transceiver Design		
			ISSCC 2012
	7:30 PM ES1: Student Research Review: Poster Session with Short Presentations		What's Ne
Monday, February 20th			ISSCC 201
8:15AM			**Session**
1:30PM	**Session 2:** High Bandwidth DRAM & PRAM	**Session 3:** Processors	**Session 4:** RF Technique
5:15PM	Academic Demo Session (4-7), Author Interviews, Book Display, Social Hour		
			ISSCC
8:00PM	**ES3:** Technologies that Could Change the World - You Decide!		**ES4:** Optical PCB Int
Tuesday, February 21st			ISSCC 201
8:30AM	**Session 7:** Multi-Gb/s Receiver & Parallel I/O Techniques	**Session 8:** Delta-Sigma Converters	**Session 9:** Wireless Transceiver T
1:30PM	**Session 12:** Multimedia & Communications SoCs	**Session 13:** High-Performance Embedded SRAM	
		Session 14: Digital Clocking and PLLs	
5:15PM	Industrial Demo Session (4-7), Author Interviews, Book Display, Social Hour		
			ISSCC 2012
8:00PM	**ES5:** Vision for Future Television		**EP2:** Little-Known F
Wednesday, February 22nd			ISSCC 201
8:30AM	**Session 18:** Innovated Circuits in Emerging Technologies		**Session 19:** 20+Gb/s Wireline Tran Injection-Locked Cl
1:30PM	**Session 23:** Advances in Heterogeneous Integration		**Session 25:** Non-Volatile Memory
	Session 24: 10G BaseT & Optical Frontends		
5:15 PM	Author Interviews		
Thursday, February 23rd			ISSCC 20
8:00 AM			**SC1:** Low-Powe
			ISSCC
8:00AM	**F3:** 10-40 Gb/s I/O Design for Data Communications		**F4:** Computational Imaging

CC 2012 SESSIONS

2012 TUTORIALS

Based Circuits, System, and Platform Design	
Videband Delta-Sigma Modulators	**T5:** Jitter: Basic & Advanced Concepts, Statistics, & Applications
ital Calibration for RF Transceivers	
n With MEMS: The Electromechanical Interface	

2012 FORUMS

	F2: Robust VLSI Circuit Design & System for a Sustainable Society

EVENING SESSIONS

8:00 PM ES2:
xt in Robots? - Sensing, Processing, Networking Toward Human Brain & Body

2 PAPER SESSIONS

1: Plenary Session

es	**Session 5:** Audio & Power Converters	**Session 6:** Medical, Displays & Imagers	

2012 SESSIONS

erconnects, Niche or Mainstream?	**EP1:** Is RF Doomed to Digitization? - What Shall RF Circuit Designers Do?

2 PAPER SESSIONS

Techniques	**Session 10:** High-Performance Digital	**Session 11:** Sensors and MEMs	
	Session 15: mm-Wave and THz Techniques	**Session 16:** Switching Power Control Techniques	**Session 17:** Diagnostic & Therapeutic Techologies for Health

EVENING SESSIONS

Features of Well-Known Creatures	**EP3:** What is the Next RF Frontier?

2 PAPER SESSIONS

sceivers & locking	**Session 20:** RF Frequency Generation	**Session 21:** Analog Techniques	**Session 22:** Image Sensors
Solutions	**Session 26:** Short-Range Wireless Transceivers	**Session 27:** Data Converter Techniques	Session 28: Adaptive & Low-Power Circuits

12 SHORT COURSE

r Analog Signal Processing

C 2012 FORUMS

g	**F5:** Bioelectronics for Sustainable Healthcare	**F6:** Power/Performance Optimization of Many-Core Processor SoCs

SWITCHING POWER CONTROL TECHNIQUES

Session Chair: **Baher Haroun,** *Texas Instruments, Dallas, TX*
Associate Chair: **Gyu-Hyeong Cho,** *KAIST, Daejeon, Korea*

16.1 Near Independently Regulated 5-Output Single-Inductor DC-DC Buck Converter Delivering 1.2W/mm² in 65 nm CMOS **1:30 PM**

C-W. Kuan, H-C. Lin
MediaTek, Hsinchu, Taiwan

16.2 A High-Stability Emulated Absolute Current Hysteretic Control Single-Inductor 5-Output Switching DC-DC Converter With Energy Sharing and Balancing **2:00 PM**

S-W. Wang[1], G-H. Cho[2], G-H. Cho[1]
[1]KAIST, Daejeon, Korea
[2]JDA, Daejeon, Korea

16.3 Off-the-Line Primary-Side Regulation LED Lamp Driver With Single-Stage PFC and TRIAC Dimming Using LED Forward Voltage and Duty Variation Tracking Control **2:30 PM**

J. Hwang, M. Jung, D. Kim, J. Lee, M. Jung, J. Shin
Anaperior Technology, Seoul, Korea

Break **3:00 PM**

16.4 A 0.18µm CMOS 91%-Efficiency 0.1-to-2A Scalable Buck-Boost DC-DC Converter for LED Drivers **3:15 PM**

P. Malcovati[1], M. Belloni[1], F. Gozzini[2], C. Bazzani[2], A. Baschirotto[3]
[1]University of Pavia, Pavia, Italy
[2]Mindspeed, Newport Beach, CA
[3]University of Milano-Bicocca, Milano, Italy

16.5 A 92% Efficiency Wide-Input Voltage Range Switched-Capacitor DC-DC Converter **3:45 PM**

V. Ng, S. Sanders
University of California at Berkeley, Berkeley, CA

16.6 An Optimized Driver for SiC JFET-Based Switches Delivering More Than 99% Efficiency **4:15 PM**

K. Norling, C. Lindholm, D. Draxelmayr
Infineon Technologies, Villach, Austria

16.7 An Adaptive Reconfigurable Active Voltage Doubler/Rectifier for Extended-Range Inductive Power Transmission **4:45 PM**

H-M. Lee, M. Ghovanloo
Georgia Institute of Technology, Atlanta, GA

16.8 Voltage-Boosting Wireless Power Delivery System With Fast Load Tracker by ΔΣ-Modulated Sub-Harmonic Resonant Switching ADS **5:00 PM**

R. Shinoda, K. Tomita, Y. Hasegawa, H. Ishikuro
Keio University, Yokohama, Japan

Conclusion **5:15 PM**

DIAGNOSTIC & THERAPEUTIC TECHNOLOGIES FOR HEALTH

Session Chair: **Alison Burdett,** *Toumaz Technology, Abingdon, United Kingdom*
Associate Chair: **Fu-Lung Hsueh,** *TSMC, Hsinchu, Taiwan*

17.1 An 8-Channel Scalable EEG Acquisition SoC With Fully Integrated Patient-Specific Seizure Classification and Recording Processor **1:30 PM**

J. Yoo[1], L. Yan[2], D. El-Damak[3], M. Bin Altaf[1], A. Shoeb[4], H-J. Yoo[5], A. Chandrakasan[3]
[1]Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
[2]imec, Leuven, Belgium
[3]Massachusetts Institute of Technology, Cambridge, MA
[4]Massachusetts General Hospital, Harvard Medical School, Cambridge, MA
[5]KAIST, Daejeon, Korea

17.2 A 259.6μW Nonlinear HRV-EEG Chaos Processor With Body Channel Communication Interface for Mental Health Monitoring ADS **2:00 PM**

T. Roh, S. Hong, H. Cho, H-J. Yoo
KAIST, Daejeon, Korea

17.3 A Sub-10nA DC-Balanced Adaptive Stimulator IC With Multimodal Sensor for Compact Electro-Acupuncture System ADS **2:30 PM**

K. Song, H. Lee, S. Hong, H. Cho, H-J. Yoo
KAIST, Daejeon, Korea

Break 3:00 PM

17.4 A Batteryless 19μW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC **3:15 PM**

F. Zhang[1], Y. Zhang[2], J. Silver[1], Y. Shakhsheer[2], M. Nagaraju[1], A. Klinefelter[2], J. Pandey[1], J. Boley[2], E. Carlson[1], A. Shrivastava[2], B. Otis[1], B. Calhoun[2]
[1]University of Washington, Seattle, WA
[2]University of Virginia, Charlottesville, VA

17.5 A 1V 5mA Multimode IEEE 802.15.6/Bluetooth Low-Energy WBAN Transceiver for Biotelemetry Applications **3:45 PM**

A. Wong, M. Dawkins, G. Devita, N. Kasparidis, A. Katsiamis, O. King, F. Lauria, J. Schiff, A. Burdett
Toumaz, Abingdon, United Kingdom

17.6 A mm-Sized Wirelessly Powered and Remotely Controlled Locomotive Implantable Device **4:15 PM**

A. Yakovlev, D. Pivonka, T. Meng, A. Poon
Stanford University, Stanford, CA

17.7 A CMOS Impedance Cytometer for 3D Flowing Single-Cell Real-Time Analysis With ΔΣ Error Correction **4:45 PM**

K-H. Lee[1], J. Nam[2], S. Choi[1], H. Lim[2], S. Shin[2], G-H. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Korea University, Seoul, Korea

Conclusion 5:15 PM

INDUSTRY DEMONSTRATION SESSION (IDS)

ISSCC 2012 continues this year with the Industry Demonstration Session (IDS), to be held on Tuesday February 21st, from 4 to 7 pm, Golden Gate Hall. IDS will feature live demonstrations of selected ICs presented by industry in regular paper sessions. IDS is intended to demonstrate real-life applications made possible by new ICs presented this year. In the Advance Program, papers for which demonstrations are available will be notated by the symbol IDS. 

Monday, February 20th

3.1	**A 22nm IA Multi-CPU and GPU System-on-Chip**	**1:30 PM**
3.6	**A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS**	**4:15 PM**
5.1	**An 8Ω 2.5W 1%-THD 104dB(A)-Dynamic-Range Class-D Audio Amplifier With an Ultra-Low EMI System and Current Sensing for Speaker Protection**	**1:30 PM**
5.8	**A 330nA Energy-Harvesting Charger With Battery Management for Solar and Thermoelectric Energy Harvesting**	**4:45 PM**
6.5	**A 160μA Biopotential Acquisition ASIC With Fully Integrated IA and Motion-Artifact Suppression**	**3:15 PM**

Tuesday, February 21st

7.5	**A 4.1pJ/b 16Gb/s Coded Differential Bidirectional Parallel Electrical Link**	**10:45 AM**
10.3	**A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit With Certainty Tracking in 32nm CMOS**	**9:30 AM**
11.6	**A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator With Better Than ±0.5ppm Frequency Stability**	**10:45 AM**
12.1	**A 32nm High-k Metal Gate Application Processor with GHz Multi-Core CPU**	**1:30 PM**
12.5	**A 464GOPS 620GOPS/W Heterogeneous Multi-Core SoC for Image-Recognition Applications**	**3:45 PM**
12.7	**A True Multistandard, Programmable, Low-Power, Full HD Video-Codec Engine for Smartphone SoC**	**4:45 PM**

Wednesday, February 22nd

19.3	**A 40nm CMOS Single-Chip 50Gb/s DP-QPSK/BPSK Transceiver With Electronic Dispersion Compensation for Coherent Optical Channels**	**9:30 AM**
22.9	**A 1920×1080 3.65μm-Pixel 2D/3D Image Sensor With Split and Binning Pixel Structure in 0.11μm Standard CMOS**	**12:00 PM**
26.6	**A Meter-Range UWB Transceiver Chipset for Around-the-Head Audio Streaming**	**4:15 PM**
26.8	**A 915MHz 120μW-RX/900μW-TX Envelope-Detection Transceiver With 20dB In-Band Interference Tolerance**	**5:00 PM**

ES5: Vision for Future Television

Organizer: **Atsuki Inoue,** *Fujitsu Laboratories, Kawasaki, Japan*
Masaitsu Nakajima, *Panasonic, Moriguchi, Japan*

Chair: **Masaitsu Nakajima,** *Panasonic, Moriguchi, Japan*

Until recently, TV technology (e.g. analog color TV and broadcast by air) was seen to have matured. However, the introduction of digital TV technology, including high-speed IP-based networking, has given consumers additional "freedom" to view content, and is presenting new technological challenges. Users experience this freedom through multiple types of devices and sources of content.

The introduction of 3D imaging displays represents a great advance for TV receiver equipment. However, the gap between current TV capabilities and customer demand remains large and additional technology is necessary.

The aim of this Evening Session is to discuss future technologies that could close the customer demand gap, from the viewpoints of service, platform and device.

Time	Topic
8:00	**Television Futures** **Brendan Traw,** *Intel, Portland, OR*
8:30	**3D and Smart TV in the Future** **David K. Min,** *LG Electronics, Seoul, Korea*
9:00	**Glasses-Free 3D Technologies for Future Digital TV Systems** **Yuzo Hirayama,** *Toshiba, Kawasaki, Japan*
9:30	**FTV (Free-Viewpoint Television) as the Ultimate 3D TV** **Masayuki Tanimoto,** *Nagoya University, Nagoya, Japan*

EP2: Little-Known Features of Well-Known Creatures

Organizer: **Un-Ku Moon,** *Oregon State University, Corvallis, OR*
Co-Organizer: **Shanthi Pavan**, *Indian Institute of Technology, Madras, India*

Moderator: **Shanthi Pavan**, *Indian Institute of Technology, Madras, India*

This panel discussion will feature experts from academia and industry, spanning the broad landscape of solid state circuits - analog, digital, microwave, mixed signal and RF. They will unleash their bag of tricks - things you thought you knew, but probably did not quite appreciate, an interesting way of looking at a well known circuit or a system, a less known facet of a commonly used idea, little known facts now finding increasing application

Panelists:

Asad A. Abidi, *University of California, Los Angeles, CA*
A. Paul Brokaw, *Integrated Device Technology, Tucson, AZ*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Mark Horowitz, *Stanford University, Stanford, CA*
Thomas H. Lee, *DARPA, Arlington, VA*
David Robertson, *Analog Devices, Wilmington, MA*

EP3: What is the Next RF Frontier?

Organizer: **Gangadhar Burra,** *Texas Instruments, Dallas, TX*
Co-Organizer: **Hossein Hashimi**, *University of Southern California, Los Angeles, CA*

Moderator: **Gangadhar Burra**, *Texas Instruments, Dallas, TX*

What are the next BIG ideas in wireless communications? What will you see at ISSCC, five years from now? Will these new ideas be adopted by consumers? A panel of experts will make their predictions, focusing on applications ranging from low power to high speed, including:

Medical RF/nano-power – after tele-health, what is next? Energy-scavenged ultra-low-power wireless techniques and integrated bio-sensors may become the frontier for the next generation of wireless technologies.

mm-Wave & TerraHertz – ultra-high-frequency RF circuits beyond mm-Wave frequencies show promise in medical (diagnostic), security and consumer applications.

Connected home – is “Internet of Things” going to be viable – what are the challenges?

Panelists:

Jan Rabaey, *University of California at Berkeley, Berkeley, CA*
Jerald Yoo, *Masdar Institute of Science & Technology, Abu Dhabi, UAE*
Chris Toumazou, *Imperial College, London, United Kingdom*
Ullrich Pfeiffer, *University of Wuppertal, Wuppertal, Germany*
Ajith Amerasekera, *Texas Instruments, Dallas, TX*
Inyup Kang, *Samsung Electronics, Gyeonggi-do, South Korea*

INNOVATIVE CIRCUITS IN EMERGING TECHNOLOGIES

Session Chair: **Masaitsu Nakajima,** *Panasonic, Moriguchi, Japan*
Associate Chair: **Shekhar Borkar,** *Intel, Hillsboro, OR*

18.1 Insole Pedometer With Piezoelectric Energy Harvester and 2V Organic Digital and Analog Circuits **8:30 AM**

K. Ishida[1], T-C. Huang[1], K. Honda[1], Y. Shinozuka[1], H. Fuketa[1], T. Yokota[1], U. Zschieschang[2], H. Klauk[2], G. Tortissier[1], T. Sekitani[1,3], M. Takamiya[1], H. Toshiyoshi[1], T. Someya[1,3], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan
[2]Max Planck Institute for Solid State Research, Stuttgart, Germany
[3]JST/ERATO, Tokyo, Japan

18.2 1D and 2D Analog 1.5kHz Air-Stable Organic Capacitive Touch Sensors on Plastic Foil **9:00 AM**

H. Marien[1], M. Steyaert[1], E. Van Veenendaal[2], P. Heremans[1,3]
[1]KU Leuven, Heverlee, Belgium
[2]Polymer Vision, Eindhoven, The Netherlands
[3]imec, Heverlee, Belgium

18.3 Bidirectional Communication in an HF Hybrid Organic/Solution-Processed Metal-Oxide RFID Tag **9:30 AM**

K. Myny[1,2], M. Rockelé[1,2], A. Chasin[1,2], D-V. Pham[3], J. Steiger[3], S. Botnaras[3], D. Weber[3], B. Herold[4], J. Ficker[4], B. Van der Putten[5], G. Gelinck[5], J. Genoe[1,6], W. Dehaene[1,2], P. Heremans[1,2]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium
[3]Evonik Degussa, Marl, Germany; [4]PolyIC, Fürth, Germany
[5]Holst Centre/TNO, Eindhoven, The Netherlands; [6]KHLim, Diepenbeek, Belgium

Break **10:00 AM**

18.4 A 6b 10MS/s Current-Steering DAC Manufactured With Amorphous Gallium-Indium-Zinc-Oxide TFTs Achieving SFDR > 30dB up to 300kHz **10:15 AM**

D. Raiteri[1], F. Torricelli[1], K. Myny[2], M. Nag[2], B. Van der Putten[3], E. Smits[3], S. Steudel[2], K. Tempelaars[3], A. Tripathi[3], G. Gelinck[3], A. Van Roermund[1], E. Cantatore[1]
[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]imec, Leuven, Belgium
[3]TNO Science and Industry, Eindhoven, The Netherlands

18.5 A Low-Overhead Self-Healing Embedded System for Ensuring High Yield and Long-Term Sustainability of 60GHz 4Gb/s Radio-on-a-Chip **10:45 AM**

A. Tang[1], F. Hsiao[1], D. Murphy[1], I-N. Ku[1], J. Liu[1], S. D'Souza[1], N-Y. Wang[1], H. Wu[1], Y-H. Wang[1], M. Tang[1], G. Virbila[1], M. Pham[1], D. Yang[1], Q. Gu[2], Y-C. Wu[1], Y-C. Kuan[1], C. Chien[3], M-C. Chang[1]
[1]University of California, Los Angeles, Los Angeles, CA
[2]University of Florida, Gainsville, FL
[3]CreoNex Systems, Westlake Village, CA

18.6 Power-Efficient Readout Circuit for Miniaturized Electronic Nose **11:15 AM**

V. Petrescu, J. Pettine, D. Karabacak, M. Vandecasteele, M. Crego Calama, C. Van Hoof
imec - Holst Centre, Eindhoven, The Netherlands

18.7 Towards Ultra-Dense Arrays of VHF NEMS With FDSOI-CMOS Active Pixels for Sensing Applications **11:45 AM**

G. Arndt, C. Dupré, J. Arcamone, G. Cibrario, O. Rozeau, L. Duraffourg, E. Ollier, E. Colinet
CEA-LETI-MINATEC, Grenoble, France

Conclusion **12:00 PM**

20+GB/S WIRELINE TRANSCEIVERS & INJECTION-LOCKED CLOCKING

Session Chair: **Ken Chang,** *Xilinx, San Jose, CA*
Associate Chair: **SeongHwan Cho,** *KAIST, Daejeon, Korea*

19.1 A 28Gb/s 4-Tap FFE/15-Tap DFE Serial Link Transceiver in 32nm SOI CMOS Technology **8:30 AM**

J. Bulzacchelli[1], T. Beukema[1], D. Storaska[2], P-H. Hsieh[1,3], S. Rylov[1], D. Furrer[4], D. Gardellini[4], A. Prati[4], C. Menolfi[5], D. Hanson[2], J. Hertle[4], T. Morf[6], V. Sharma[4], R. Kelkar[6], H. Ainspan[1], W. Kelly[2], G. Ritter[2], J. Garlett[2], R. Callan[2], T. Toifl[5], D. Friedman[1]
[1]IBM Research, Yorktown Heights, NY
[2]IBM Systems and Technology Group, Hopewell Junction, NY
[3]National Tsing Hua University, Hsinchu, Taiwan; [4]Miromico, Zurich, Switzerland
[5]IBM Research, Zurich, Switzerland
[6]IBM Systems and Technology Group, Essex Junction, VT

19.2 A 225mW 28Gb/s SerDes in 40nm CMOS With 13dB of Analog Equalization for 100GBASE-LR4 and Optical Transport Lane 4.4 Applications **9:00 AM**

M. Harwood[1], S. Nielsen[2], A. Szczepanek[1], R. Allred[2], S. Batty[1], M. Case[2], S. Forey[1], K. Gopalakrishnan[3], L. Kan[3], B. Killips[1], P. Mishra[2], R. Pande[3], H. Rategh[3], A. Ren[3], J. Sanders[2], A. Schoy[3], R. Ward[3], M. Wetterhorn[2], N. Yeung[2]
[1]Inphi, Northampton, United Kingdom; [2]Inphi, Westlake Village, CA
[3]Inphi, Santa Clara, CA

19.3 A 40nm CMOS Single-Chip 50Gb/s DP-QPSK/BPSK Transceiver With Electronic Dispersion Compensation for Coherent Optical Channels IDS **9:30 AM**

D. Crivelli[1,2], M. Hueda[1,2], H. Carrer[1,2], J. Zachan[3], V. Gutnik[3], M. Del Barco[1], R. Lopez[1], G. Hatcher[3], J. Finochietto[2], M. Yeo[3], A. Chartrand[3], N. Swenson[3], P. Voois[3], O. Agazzi[1,3]
[1]ClariPhy, Cordoba, Argentina; [2]National University of Cordoba, Cordoba, Argentina
[3]ClariPhy, Irvine, CA

Break 10:00 AM

19.4 A Dual 23Gb/s CMOS Transmitter/Receiver Chipset for 40Gb/s RZ-DQPSK and CS-RZ-DQPSK Optical Transmission **10:15 AM**

D. Cui, B. Raghavan, U. Singh, A. Vasani, Z. Huang, M. Khanpour, A. Nazemi, H. Maarefi, T. Ali, N. Huang, W. Zhang, B. Zhang, A. Momtaz, J. Cao
Broadcom, Irvine, CA

19.5 A Versatile Multi-Modality Serial Link **10:45 AM**

Y. Tanaka[1], Y. Hino[1], Y. Okada[1], T. Takeda[1], S. Ohashi[1], H. Yamagishi[1], K. Kawasaki[1], A. Hajimiri[2]
[1]Sony, Tokyo, Japan; [2]California Institute of Technology, Pasadena, CA

19.6 A 28Gb/s Source-Series Terminated TX in 32nm CMOS SOI **11:15 AM**

C. Menolfi[1], J. Hertle[2], T. Toifl[1], T. Morf[1], D. Gardellini[2], M. Braendli[1], P. Buchmann[1], M. Kossel[1]
[1]IBM, Rueschlikon, Switzerland; [2]Miromico, Zurich, Switzerland

19.7 An All-Digital Clock Generator Using a Fractionally Injection-Locked Oscillator in 65nm CMOS **11:30 AM**

P. Park[1], H. Park[2], J. Park[2], S. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Yongin, Korea

19.8 A 2.4GHz Sub-Harmonically Injection-Locked PLL With Self-Calibrated Injection Timing **11:45 AM**

Y-C. Huang, S-I. Liu; National Taiwan University, Taipei, Taiwan

Conclusion 12:15 PM

RF FREQUENCY GENERATION

Session Chair: **Bogdan Staszewski,** *TU Delft, Delft, The Netherlands*
Associate Chair: **Taizo Yamawaki,** *Renesas Mobile, Takasaki, Japan*

20.1 A 20Mb/s Phase Modulator Based on a 3.6GHz Digital PLL with -36dB EVM at 5mW Power **8:30 AM**

G. Marzin, S. Levantino, C. Samori, A. Lacaita
Politecnico di Milano, Milan, Italy

20.2 A 14.2mW 2.55-to-3GHz Cascaded PLL With Reference Injection, 800MHz Delta-Sigma Modulator and 255fs$_{rms}$ Integrated Jitter in 0.13μm CMOS **9:00 AM**

D. Park, S. Cho
KAIST, Daejeon, Korea

20.3 A 40nm CMOS All-Digital Fractional-N Synthesizer Without Requiring Calibration **9:30 AM**

F. Opteynde, F. Opteynde
Audax-Technologies, Leuven, Belgium

Break **10:00 AM**

20.4 A 36mW/9mW Power-Scalable DCO in 55nm CMOS for GSM/WCDMA Frequency Synthesizers **10:15 AM**

A. Liscidini[1], L. Fanori[1], P. Andreani[2], R. Castello[1]
[1]University of Pavia, Pavia, Italy
[2]Lund University, Lund, Sweden

20.5 A Clip-and-Restore Technique for Phase Desensitization in a 1.2V 65nm CMOS Oscillator for Cellular Mobile and Base Stations **10:45 AM**

A. Visweswaran, R. Staszewski, J. Long
Delft University of Technology, Delft, The Netherlands

20.6 A 32nm CMOS All-Digital Reconfigurable Fractional Frequency Divider for LO Generation in Multistandard SoC Radios With On-the-Fly Interference Management **11:15 AM**

K. Chandrashekar, S. Pellerano, P. Madoglio, A. Ravi, Y. Palaskas
Intel, Hillsboro, OR

20.7 A 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO **11:45 AM**

L. Fanori[1,2], A. Liscidini[1], P. Andreani[2]
[1]University of Pavia, Pavia, Italy
[2]Lund University, Lund, Sweden

Conclusion **12:15 PM**

ANALOG TECHNIQUES

Session Chair: **Jafar Savoj,** *Xilinx, San Jose, CA*
Associate Chair: **Chris Mangelsdorf,** *Analog Devices, Tokyo, Japan*

21.1 A 0.3-to-1.2GHz Tunable 4th-Order Switched g_m-C Bandpass Filter With >55dB Ultimate Rejection and Out-of-Band IIP3 of +29dBm **8:30 AM**

M. Darvishi, R. Van der Zee, E. Klumperink, B. Nauta
University of Twente, Enschede, The Netherlands

21.2 A 0.55V 61dB-SNR 67dB-SFDR 7MHz 4th-Order Butterworth Filter Using Ring-Oscillator-Based Integrators in 90nm CMOS **9:00 AM**

B. Drost[1], M. Talegaonkar[2], P. Hanumolu[2]
[1]Silicon Laboratories, Corvallis, OR; [2]Oregon State University, Corvallis, OR

21.3 A 65nm CMOS 1-to-10GHz Tunable Continuous-Time Lowpass Filter for High-Data-Rate Communications **9:30 AM**

F. Houfaf[1,2,3], M. Egot[1], A. Kaiser[2], A. Cathelin[1], B. Nauta[3]
[1]STMicroelectronics, Crolles, France; [2]IEMN / ISEN, Lille, France
[3]University of Twente, Enschede, The Netherlands

21.4 A 0.0025mm² Bandgap Voltage Reference for 1.1V Supply in Standard 0.16μm CMOS **9:45 AM**

A-J. Annema[1], G. Goksun[2]
[1]University of Twente, Enschede, The Netherlands
[2]Anagear B.V., Rosmalen, The Netherlands

Break 10:00 AM

21.5 A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications **10:15 AM**

D. Yoon, D. Sylvester, D. Blaauw; University of Michigan, Ann Arbor, MI

21.6 A 0.016mm² 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load With >0.95MHz GBW **10:45 AM**

Z. Yan[1], P-I. Mak[1], M-K. Law[1], R. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico, Lisbon, Portugal

21.7 A 90V_{pp} 720MHz GBW Linear Power Amplifier for Ultrasound Imaging Transmitters in BCD6-SOI **11:15 AM**

D. Bianchi[1], F. Quaglia[2], A. Mazzanti[1], F. Svelto[1]
[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Cornaredo, Italy

21.8 On-Chip Gain Reconfigurable 1.2V 24μW Chopping Instrumentation Amplifier With Automatic Resistor Matching in 0.13μm CMOS **11:30 AM**

F. Michel, M. Steyaert; KU Leuven, Leuven, Belgium

21.9 A Capacitively Coupled Chopper Instrumentation Amplifier With a ±30V Common-Mode Range, 160dB CMRR and 5μV Offset **11:45 AM**

Q. Fan, J. Huijsing, K. Makinwa; Delft University of Technology, Delft, The Netherlands

21.10 A 60V Capacitive-Gain 27nV/√Hz 137dB CMRR PGA With ±10V Inputs **12:00 PM**

C. Birk[1], G. Mora-Puchalt[2]
[1]Analog Devices, Cork, Ireland; [2]Analog Devices, Valencia, Spain

Conclusion 12:15 PM

IMAGE SENSORS

Session Chair: **David Stoppa,** *Fondazione Bruno Kessler, Trento, Italy*
Associate Chair: **Robert Johansson,** *Aptina Imaging, Oslo, Norway*

22.1 An 83dB-Dynamic-Range Single-Exposure Global-Shutter CMOS Image Sensor With In-Pixel Dual Storage **8:30 AM**

M. Sakakibara[1], Y. Oike[1], T. Takatsuka[1], A. Kato[1], K. Honda[1], T. Taura[1], T. Machida[1], J. Okuno[2], A. Ando[2], T. Fukuro[2], T. Asatsuma[1], S. Endo[2], J. Yamamoto[2], Y. Nakano[2], T. Kaneshige[2], I. Yamamura[1], T. Ezaki[1], T. Hirayama[1]
[1]Sony, Atsugi, Japan; [2]Sony Semiconductor, Kumamoto, Japan

22.2 A Global-Shutter CMOS Image Sensor With Readout Speed of 1Tpixel/s Burst and 780Mpixel/s Continuous ADS **9:00 AM**

Y. Tochigi[1], K. Hanzawa[1], Y. Kato[1], R. Kuroda[1], H. Mutoh[2], R. Hirose[3], H. Tominaga[3], K. Takubo[3], Y. Kondo[3], S. Sugawa[1]
[1]Tohoku University, Sendai, Japan; [2]Link Research, Odawara, Japan; [3]Shimadzu, Kyoto, Japan

22.3 A 0.7e^-_{rms}-Temporal-Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging **9:30 AM**

Y. Chen[1], Y. Xu[1], Y. Chae[1], A. Mierop[2], X. Wang[3], A. Theuwissen[1,4]
[1]Delft University of Technology, Delft, The Netherlands
[2]Teledyne DALSA Semiconductors, Eindhoven, The Netherlands
[3]CMOSIS NV, Antwerp, Belgium; [4]Harvest Imaging, Bree, Belgium

Break 10:00 AM

22.4 A 256×256 CMOS Image Sensor With ΔΣ-Based Single-Shot Compressed Sensing **10:15 AM**

Y. Oike[1,2], A. El Gamal[1]; [1]Stanford University, Stanford, CA; [2]Sony, Atsugi, Japan

22.5 A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs **10:45 AM**

T. Watabe[1], K. Kitamura[1], T. Sawamoto[2], T. Kosugi[3], T. Akahori[3], T. Iida[3], K. Isobe[3], T. Watanabe[3], H. Shimamoto[1], H. Ohtake[1], S. Aoyama[3], S. Kawahito[2,3], N. Egami[1]
[1]NHK Science & Technology Research Laboratories, Tokyo, Japan
[2]Shizuoka University, Hamamatsu, Japan; [3]Brookman Technology, Hamamatsu, Japan

22.6 A 14b Extended Counting ADC Implemented in a 24MPixel APS-C CMOS Image Sensor **11:00 AM**

J-H. Kim, W-K. Jung, S-H. Lim, Y-J. Park, W-H. Choi, Y-J. Kim, C-E. Kang, J-H. Shin, K-J. Choo, W-B. Lee, J-K. Heo, B-J. Kim, S-J. Kim, M-H. Kwon, K-S. Yoo, J-H. Seo, S-H. Ham, C-Y. Choi, G-S. Han
Samsung Electronics, Yongin, Korea

22.7 A 1.5Mpixel RGBZ CMOS Image Sensor for Simultaneous Color and Range Image Capture **11:15 AM**

W. Kim[1], W. Yibing[2], I. Ovsiannikov[2], S. Lee[1], Y. Park[1], C. Chung[1], E. Fossum[1,2]
[1]Samsung Electronics, Hwasung, Korea; [2]Samsung Semiconductor, Pasadena, CA

22.8 A QVGA-Range Image Sensor Based on Buried-Channel Demodulator Pixels in 0.18μm CMOS With Extended Dynamic Range **11:45 AM**

L. Pancheri, N. Massari, M. Perenzoni, M. Malfatti, D. Stoppa
Fondazione Bruno Kessler, Trento, Italy

22.9 A 1920×1080 3.65μm-Pixel 2D/3D Image Sensor With Split and Binning Pixel Structure in 0.11μm Standard CMOS IDS **12:00 PM**

S-J. Kim, B. Kang, J. Kim, K. Lee, C-Y. Kim, Kinam Kim
Samsung Advanced Institute of Technology, Yongin, Korea

Conclusion 12:15 PM

ADVANCES IN HETEROGENEOUS INTEGRATION

Session Chair: **Tadahiro Kuroda,** *Keio University, Yokohama, Japan*
Associate Chair: **David Ruffieux,** *CSEM, Neuchatel, Switzerland*

23.1 A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer Delivering 10.8A/mm² **1:30 PM**

N. Sturcken[1], E. O'Sullivan[2], N. Wang[2], P. Herget[3], B. Webb[2], L. Romankiw[2], M. Petracca[1], R. Davies[1], R. Fontana[3], G. Decad[3], I. Kymissis[1], A. Peterchev[4], L. Carloni[1], W. Gallagher[2], K. Shepard[1]
[1]Columbia University, New York, NY
[2]IBM T. J. Watson, Yorktown Heights, NY
[3]IBM Almaden Research Center, San Jose, CA
[4]Duke University, Durham, NC

23.2 A Modular 1mm³ Die-Stacked Sensing Platform With Optical Communication and Multi-Modal Energy Harvesting **2:00 PM**

Y. Lee, G. Kim, S. Bang, Y. Kim, I. Lee, P. Dutta, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

23.3 A DC-Isolated Gate Drive IC With Drive-by-Microwave Technology for Power Switching Devices **2:30 PM**

S. Nagai, N. Negoro, T. Fukuda, N. Otsuka, H. Sakai, T. Ueda, T. Tanaka, D. Ueda
Panasonic, Seika, Japan

23.4 Nonvolatile 3D-FPGA With Monolithically Stacked RRAM-Based Configuration Memory **2:45 PM**

Y. Yang Liauw, Z. Zhang, W. Kim, A. El Gamal, S. Wong
Stanford University, Stanford, CA

Break 3:00 PM

10GBASE-T & Optical Frontends

Session Chair: **Miki Moyal,** *Intel, Bet Hananya, Israel*
Associate Chair: **Chewnpu Jou,** *TSMC, Hsinchu, Taiwan*

24.1 A Sub-2W 10GBASE-T Analog Front-End in 40nm CMOS process **3:15 PM**

T. Gupta[1], F. Yang[1], D. Wang[1], A. Tabatabaei[1], R. Singh[1], H. Aslanzadeh[1], A. Khalili[1], S. Vats[1], S. Arno[1], S. Campeau[2]
[1]Applied Micro, Sunnyvale, CA
[2]Applied Micro, Kanata, ON, Canada

24.2 A 16-Port FCC-Compliant 10GBASE-T Transmitter and Hybrid With 76dBc SFDR up to 400MHz Scalable to 48 Ports **3:45 PM**

F. Gerfers, R. Farjad, M. Brown, A. Tavakoli, D. Nguyen, H-T. Ng, R. Shirani
Aquantia, Milpitas, CA

24.3 A 10Gb/s Burst-Mode Laser Diode Driver for Burst-by-Burst Power Saving **4:00 PM**

H. Koizumi, M. Togashi, M. Nogawa, Y. Ohtomo
NTT, Atsugi, Japan

24.4 A 10Gb/s Burst-Mode TIA With On-Chip Reset/Lock CM Signaling Detection and Limiting Amplifier With a 75ns Settling Time **4:15 PM**

X. Yin[1], J. Put[1], J. Verbrugghe[1], J. Gillis[1], X-Z. Qiu[1], J. Bauwelinck[1], J. Vandewege[1], H-G. Krimmel[2], M. Achouche[3]
[1]imec - Ghent University, Gent, Belgium
[2]Bell Laboratories, Stuttgart, Germany
[3]III-V Lab, Marcoussis, France

24.5 25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-Based Optical Links in 90nm CMOS **4:45 PM**

J. Proesel, C. Schow, A. Rylyakov
IBM T. J. Watson, Yorktown Heights, NY

Conclusion **5:15 PM**

NON-VOLATILE MEMORY SOLUTIONS

Session Chair: **Tadaaki Yamauchi,** *Renesas Electronics, Itami, Japan*
Associate Chair: **Satoru Hanzawa,** *Hitachi Central Research Laboratory, Tokyo, Japan*

25.1 A 19nm 112.8mm² 64Gb Multi-Level Flash Memory With 400Mb/s/pin 1.8V Toggle Mode Interface — 1:30 PM

N. Shibata[1], K. Kanda[1], T. Hisada[1], K. Isobe[1], M. Sato[1], Y. Shimizu[1], T. Shimizu[1], T. Sugimoto[1], T. Kobayashi[1], K. Inuzuka[1], N. Kanagawa[1], Y. Kajitani[1], T. Ogawa[1], J. Nakai[1], K. Iwasa[1], M. Kojima[1], T. Suzuki[1], Y. Suzuki[1], S. Sakai[1], T. Fujimura[1], Y. Utsunomiya[1], T. Hashimoto[1], M. Miakashi[1], N. Kobayashi[1], M. Inagaki[1], Y. Matsumoto[1], S. Inoue[1], Y. Suzuki[1], D. He[1], Y. Honda[1], J. Musha[1], M. Nakagawa[1], M. Honma[1], N. Abiko[1], M. Koyanagi[1], M. Yoshihara[1], K. Ino[1], M. Noguchi[1], T. Kamei[2], Y. Kato[2], S. Zaitsu[2], H. Nasu[2], T. Ariki[2], H. Chibvongodze[2], M. Watanabe[2], H. Ding[2], N. Ookuma[2], R. Yamashita[2], G. Liang[2], G. Hemink[2], F. Moogat[2], C. Trinh[2], M. Higashitani[2], T. Pham[2], K. Kanazawa[1]
[1]Toshiba, Yokohama, Japan; [2]Sandisk, Milpitas, CA

25.2 Over-10×-Extended-Lifetime 76%-Reduced-Error Solid-State Drives (SSDs) With Error-Prediction LDPC Architecture and Error-Recovery Scheme — ADS — 2:00 PM

S. Tanakamaru, Y. Yanagihara, K. Takeuchi; University of Tokyo, Tokyo, Japan

25.3 6.4Gb/s Multi-Threaded BCH Encoder and Decoder for Multi-Channel SSD Controllers — 2:30 PM

Y. Lee, H. Yoo, I. Yoo, I-C. Park; KAIST, Daejeon, Korea

25.4 Bitline-Capacitance-Cancelation Sensing Scheme with 11ns Read Latency and Maximum Read Throughput of 2.9GB/s in 65nm Embedded Flash for Automotive — 2:45 PM

M. Jefremow[1,2], T. Kern[1], U. Backhausen[1], C. Peters[1], C. Parzinger[1], C. Roll[1], S. Kassenetter[1], S. Thierold[1], D. Schmitt-Landsiedel[2]
[1]Infineon, Neubiberg, Germany; [2]Technical University Munich, Munich, Germany

Break 3:00 PM

25.5 A 64Gb 533Mb/s DDR Interface MLC NAND Flash in Sub-20nm Technology — 3:15 PM

D. Lee, I. Chang, S-Y. Yoon, J. Jang, D-S. Jang, W-G. Hahn, J-Y. Park, D-G. Kim, C. Yoon, B-S. Lim, B-J. Min, S-W. Yun, J-S. Lee, I-H. Park, K-R. Kim, J-Y. Yun, Y. Kim, Y-S. Cho, K-M. Kang, S-H. Joo, J-Y. Chun, J-N. Im, S. Kwon, S. Ham, A. Park, J-D. Yu, N-H. Lee, T-S. Lee, M. Kim, H. Kim, K-W. Song, B-G. Jeon, K. Choi, J-M. Han, K. Kyung, Y-H. Lim, Y-H. Jun
Samsung Electronics, Hwasung, Korea

25.6 An 8Mb Multi-Layered Cross-Point ReRAM Macro With 443MB/s Write Throughput — 3:45 PM

A. Kawahara[1], R. Azuma[1], Y. Ikeda[1], K. Kawai[1], Y. Katoh[1], K. Tanabe[2], T. Nakamura[2], Y. Sumimoto[2], N. Yamada[2], N. Nakai[2], S. Sakamoto[2], Y. Hayakawa[1], K. Tsuji[1], S. Yoneda[1], A. Himeno[1], K-I. Origasa[2], K. Shimakawa[1], T. Takagi[1], T. Mikawa[1], K. Aono[1]
[1]Panasonic, Moriguchi, Japan; [2]Panasonic, Nagaokakyo, Japan

25.7 A 0.5V 4Mb Logic-Process Compatible Embedded Resistive RAM (ReRAM) in 65nm CMOS Using Low-Voltage Current-Mode Sensing Scheme with 45ns Random Read Time — 4:15 PM

M-F. Chang[1], C-W. Wu[1], C-C. Kuo[1], S-J. Shen[1], K-F. Lin[2], S-M. Yang[1], Y-C. King[1], C-J. Lin[1], Y-D. Chih[2]
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan

25.8 128Gb 3b/Cell NAND Flash Memory in 19nm Technology With 18MB/s Write Rate and 400Mb/s Toggle Mode — 4:45 PM

Y. Li[1], S. Lee[1], K. Oowada[1], H. Nguyen[1], Q. Nguyen[1], N. Mokhlesi[1], C. Hsu[1], J. Li[1], V. Ramachandra[1], T. Kamei[1], M. Higashitani[1], T. Pham[1], M. Honma[2], Y. Watanabe[2], K. Ino[2], B. Le[1], B. Woo[1], K. Htoo[1], T-Y. Tseng[1], L. Pham[1], F. Tsai[1], K-H. Kim[1], Y-C. Chen[1], M. She[1], J. Yuh[1], A. Chu[1], C. Chen[1], R. Puri[1], H-S. Lin[1], Y-F. Chen[1], W. Mak[1], J. Huynh[1], J. Chan[1], M. Watanabe[1], D. Yang[1], G. Shah[1], P. Souriraj[1], D. Tadepalli[1], S. Tenugu[1], R. Gao[1], V. Popuri[1], B. Azarbayjani[1], R. Madpur[1], J. Lan[1], E. Yero[1], F. Pan[1], P. Hong[1], J. Kang[1], F. Moogat[1], Y. Fong[1], R. Cernea[1], S. Huynh[1], C. Trinh[1], M. Mofidi[1], R. Shrivastava[1], K. Quader[1]
[1]Sandisk, Milpitas, CA; [2]Toshiba Semiconductor, Yokohama, Japan

Conclusion 5:15 PM

SHORT-RANGE WIRELESS TRANSCEIVERS

Session Chair: **Ranjit Gharpurey,** *University of Texas at Austin, Austin, TX*
Associate Chair: **Woogeun Rhee,** *Tsinghua University, Beijing, China*

26.1 A 1V 357Mb/s-Throughput TransferJet™ SoC With Embedded Transceiver and Digital Baseband in 90nm CMOS **1:30 PM**

M. Tamura[1], F. Kondo[1], K. Watanabe[1], Y. Aoki[1], Y. Shinohe[1], K. Uchino[1], Y. Hashimoto[1], F. Nishiyama[1], H. Miyachi[1], I. Nagase[2], I. Uezono[2], R. Hisamura[2], I. Maekawa[1]
[1]Sony, Tokyo, Japan
[2]Sony Semiconductor, Kagoshima, Japan

26.2 A 2Gb/s 150mW UWB Direct-Conversion Coherent Transceiver With IQ-Switching Carrier-Recovery Scheme **2:00 PM**

T. Abe, Y. Yuan, H. Ishikuro, T. Kuroda
Keio University, Yokohama, Japan

26.3 3-to-5GHz 4-Channel UWB Beamforming Transmitter With 1° Phase Resolution Through Calibrated Vernier Delay Line in 0.13μm CMOS **2:30 PM**

L. Wang, Y. Guo, Y. Lian, C. Heng
National University of Singapore, Singapore

Break **3:00 PM**

26.4 An Interference-Aware 5.8GHz Wake-Up Radio for ETCS ADS **3:15 PM**

J. Choi[1], K. Lee[2], S-O. Yun[2], S-G. Lee[1], J. Ko[2]
[1]KAIST, Daejeon, Korea
[2]PHYCHIPS, Daejeon, Korea

26.5 A 2.7nJ/b Multi-Standard 2.3/2.4GHz Polar Transmitter for Wireless Sensor Networks **3:45 PM**

Y-H. Liu[1], X. Huang[1], M. Vidojkovic[1], K. Imamura[2], P. Harpe[1], G. Dolmans[1], H. De Groot[1]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Panasonic, Osaka, Japan

26.6 A Meter-Range UWB Transceiver Chipset for Around-the-Head Audio Streaming IDS **4:15 PM**

X. Wang[1], Y. Yu[2], B. Busze[1], H. Pflug[1], A. Young[1], X. Huang[1], C. Zhou[1], M. Konijnenburg[1], K. Philips[1], H. De Groot[1]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands

26.7 A 90nm CMOS 5Mb/s Crystal-Less RF Transceiver for RF-Powered WSN Nodes **4:45 PM**

G. Papotto[1], F. Carrara[2], A. Finocchiaro[2], G. Palmisano[1]
[1]University of Catania, Catania, Italy
[2]STMicroelectronics, Catania, Italy

26.8 A 915MHz 120μW-RX/900μW-TX Envelope-Detection Transceiver With 20dB In-Band Interference Tolerance IDS **5:00 PM**

X. Huang[1], A. Ba[1,2], P. Harpe[1,3], G. Dolmans[1], H. De Groot[1], J. Long[2]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands
[3]Eindhoven University of Technology, Eindhoven, The Netherlands

Conclusion **5:15 PM**

DATA CONVERTER TECHNIQUES

Session Chair: **Dieter Draxelmayr,** *Infineon Techologies, Villach, Austria*
Associate Chair: **Takahiro Miki,** *Renesas, Itami, Japan*

27.1 A 14b 3/6GHz Current-Steering RF DAC in 0.18μm CMOS With 66dB ACLR at 2.9GHz **1:30 PM**

G. Engel, S. Kuo, S. Rose
Analog Devices, Wilmington, MA

27.2 Ring Amplifiers for Switched-Capacitor Circuits **2:00 PM**

B. Hershberg[1], S. Weaver[1], K. Sobue[2], S. Takeuchi[2], K. Hamashita[2], U-K. Moon[1]
[1]Oregon State University, Corvallis, OR
[2]Asahi Kasei EMD, Atsugi, Japan

27.3 A 5.37mW 10b 200MS/s Dual-Path Pipelined ADC **2:30 PM**

Y. Chai, J-T. Wu
National Chiao Tung University, Hsinchu, Taiwan

Break 3:00 PM

27.4 A 13b 315fs$_{rms}$ 2mW 500MS/s 1MHz Bandwidth Highly Digital Time-to-Digital Converter Using Switched Ring Oscillators **3:15 PM**

A. Elshazly, S. Rao, B. Young, P. Hanumolu
Oregon State University, Corvallis, OR

27.5 A 1.7mW 11b 250MS/s 2× Interleaved Fully Dynamic Pipelined SAR ADC in 40nm Digital CMOS **3:45 PM**

B. Verbruggen[1], M. Iriguchi[2], J. Craninckx[1]
[1]imec, Leuven, Belgium
[2]Renesas Electronics, Kawasaki, Japan

27.6 A 90MS/s 11MHz Bandwidth 62dB SNDR Noise-Shaping SAR ADC **4:15 PM**

J. Fredenburg, M. Flynn
University of Michigan, Ann Arbor, MI

27.7 A 70dB DR 10b 0-to-80MS/s Current-Integrating SAR ADC With Adaptive Dynamic Range **4:45 PM**

B. Malki[1,2], T. Yamamoto[3], B. Verbruggen[1], P. Wambacq[1,2], J. Craninckx[1]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium
[3]Renesas Electronics, Takasaki, Japan

27.8 A 7-to-10b 0-to-4MS/s Flexible SAR ADC With 6.5-to-16fJ/conversion-step **5:00 PM**

P. Harpe[1,2], Y. Zhang[1], G. Dolmans[1], K. Philips[1], H. De Groot[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

27.9 A 31.3fJ/conversion-step 70.4dB SNDR 30MS/s 1.2V Two-Step Pipelined ADC in 0.13μm CMOS **5:15 PM**

H-Y. Lee[1], B. Lee[2], U-K. Moon[1]
[1]Oregon State University, Corvallis, OR
[2]National Semiconductor, Santa Clara, CA

Conclusion 5:30 PM

ADAPTIVE & LOW-POWER CIRCUITS

Session Chair: **Michael Phan,** *Qualcomm, Raleigh, NC*
Associate Chair: **Masaya Sumita,** *Panasonic, Moriguchi, Japan*

28.1 A 4.5Tb/s 3.4Tb/s/W 64×64 Switch Fabric With Self-Updating Least-Recently-Granted Priority and Quality-of-Service Arbitration in 45nm CMOS **1:30 PM**

S. Satpathy, K. Sewell, T. Manville, Y-P. Chen, R. Dreslinski, D. Sylvester, T. Mudge, D. Blaauw
University of Michigan, Ann Arbor, MI

28.2 A 1.0TOPS/W 36-Core Neocortical Computing Processor With 2.3Tb/s Kautz NoC for Universal Visual Recognition **2:00 PM**

C-Y. Tsai, Y-J. Lee, C-T. Chen, L-G. Chen
National Taiwan University, Taipei, Taiwan

28.3 Conditional Push-Pull Pulsed Latches With 726fJ·ps Energy-Delay Product in 65nm CMOS **2:30 PM**

E. Consoli[1], M. Alioto[2,3], G. Palumbo[1], J. Rabaey[4]
[1]University of Catania, Catania, Italy
[2]University of Siena, Siena, Italy
[3]University of Michigan, Ann Arbor, MI
[4]University of California at Berkeley, Berkeley, CA

28.4 A 200mV 32b Subthreshold Processor With Adaptive Supply Voltage Control ADS **2:45 PM**

S. Luetkemeier[1], T. Jungeblut[2], M. Porrmann[1], U. Rueckert[2]
[1]University of Paderborn, Paderborn, Germany
[2]Bielefeld University, Bielefeld, Germany

Break 3:00 PM

28.5 13% Power Reduction in 16b Integer Unit in 40nm CMOS by Adaptive Power Supply Voltage Control With Parity-Based Error Prediction and Detection (PEPD) and Fully Integrated Digital LDO **3:15 PM**

K. Hirairi[1], O. Yasuyuki[1], H. Fuketa[2], T. Yasufuku[2], M. Takamiya[2], M. Nomura[1], H. Shinohara[1], T. Sakurai[2]
[1]Semiconductor Technology Academic Research Center, Tokyo, Japan
[2]University of Tokyo, Tokyo, Japan

28.6 Bubble Razor: An Architecture-Independent Approach to Timing-Error Detection and Correction **3:45 PM**

M. Fojtik[1], D. Fick[1], Y. Kim[1], N. Pinckney[1], D. Harris[2], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI
[2]Harvey Mudd College, Claremont, CA

28.7 A 25MHz 7μW/MHz Ultra-Low-Voltage Microcontroller SoC in 65nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes **4:15 PM**

D. Bol[1], J. De Vos[1], C. Hocquet[1], F. Botman[1], F. Durvaux[1], S. Boyd[2], D. Flandre[1], J-D. Legat[1]
[1]Université catholique de Louvain, Louvain-la-Neuve, Belgium
[2]P.E. International, Berkeley, CA

28.8 A 530mV 10-Lane SIMD Processor With Variation Resiliency in 45nm SOI **4:45 PM**

R. Pawlowski[1], E. Krimer[2], J. Crop[1], J. Postman[1], N. Moezzi-Madani[3], M. Erez[2], P. Chiang[1]
[1]Oregon State University, Corvallis, OR
[2]University of Texas, Austin, TX
[3]Qualcomm, San Diego, CA

Conclusion 5:15 PM

Low-Power Analog Signal Processing

Organizer: **Willy Sansen,** *K.U. Leuven, Leuven, Belgium*

Instructors: **Christian Enz,** *CSEM, Neuchatel, Switzerland*
Willy Sansen, *K.U. Leuven, Leuven, Belgium*
Boris Murmann, *Stanford University, Stanford, CA*
Philip Mok, *Hong Kong University of Science and Technology, Hong Kong*

Overview

The reduction of the power consumption of all electronic functions is a continuous endeavor. This endeavor requires judicious comparison of analog and digital realizations from the point of view of performance per unit of power consumed. Analog signal processing offers the advantage that power consumption can be minimized at both very low and very high frequencies. This short course explores the limits in reduction of power consumption for important analog blocks.

The first presentation defines the physical limits of supply voltages and power consumption based on present-day technologies and transistor models. The second presentation addresses the limits of amplifiers and filters. For all circuit blocks, figures of merit are derived, followed by circuit techniques to improve them.

In the third presentation, new opportunities are identified to reduce the power consumption in all types of analog-to-digital converters, with emphasis on the improvement of the FOM with technology. Finally, in the fourth presentation, power minimization techniques are discussed for power management blocks such as dc-dc converters.

The Short Course

8 am-9.30 am: **Christian Enz:** Ultra-low Power/Ultra-low Voltage Analog Circuit Design

9.30 am-10 am: Break

10 am-11.30 am: **Willy Sansen:** Power Limits for Amplifiers and Filters

11.30 am-12.30 am: Lunch

12.30 am-2 pm: **Boris Murmann:** Energy Limits in Current A/D Converter Architectures

2 pm-2.30 pm: Break

2.30 pm-4 pm: **Philip Mok:** Low-Power and Low-Voltage DC-DC Converter Design

OUTLINE:

Ultra-Low-Power/Ultra-Low-Voltage Analog Circuit Design

The supply voltage of CMOS chips has been scaled down in recent years, today reaching the sub-1V region. Analog circuits unfortunately do not take advantage of this voltage scaling. In fact, almost all analog performance metrics are degraded at lower voltages. We first recall the fundamental limits of the design of low-power analog circuits. We then look at the main challenges when designing analog circuits for ultra-low-voltage (ULV) operation. We take a closer look at the MOS transistor operation with a particular focus on weak inversion. We then review several basic building blocks capable of operating at ULV.

Instructor: Christian Enz is VP heading the Integrated and Wireless Systems Division of the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, Switzerland. He is also Professor at the Swiss Federal Institute of Technology, Lausanne (EPFL), where he is lecturing and supervising students in the field of analog and RF IC design. He received the PhD from the EPFL in 1989. His technical interests and expertise are in the field of ultralow-power analog and RF IC design, wireless sensor networks and semiconductor device modeling. Together with E. Vittoz and F. Krummenacher, he is the developer of the EKV MOS transistor model.

Power Limits for Amplifiers and Filters

Increasing power consumption in amplifiers increases the speed and also reduces noise and distortion. The most common operational amplifiers, g_m blocks and wideband amplifiers are compared using a power-based FOM. Also discussed are continuous-time filters, switched-capacitor filters and G_mC filters. They are classified and compared based on a unified FOM. Again power is optimized in view of speed, noise and distortion.

Instructor: Willy Sansen received a PhD degree from U.C. Berkeley in 1972. Since 1980 he has been full professor at the Catholic University of Leuven, in Belgium, where he has headed the ESAT-MICAS laboratory on analog design up till 2008. He has been supervisor of sixty-four PhD theses and has authored and coauthored more than 650 publications and fifteen books among which the Powerpoint slide based book "Analog Design Essentials" (Springer 2006). He was Program chair of the ISSCC-2002 conference and President of the IEEE Solid-State Circuits Society in 2008-2009. He is the recipient of the D.O.Pederson award of the IEEE Solid-State Circuits in 2011. He is a Life Fellow of the IEEE.

Energy Limits in Current A/D Converter Architectures

Driven by ever-increasing application demands, the energy expended per A/D conversion has been reduced substantially over the last decade. This presentation surveys the most recent trends and investigates energy limits as they apply to A/D converter architectures commonly employed in fine-line CMOS technology (Flash, Pipeline, SAR and Oversampling Converters). Through this analysis, opportunities for further improvements are identified and discussed in detail, specifically emphasizing the impact of technology scaling.

Instructor: Boris Murmann is an Associate Professor in the Department of Electrical Engineering, Stanford, CA. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. He is a member of the International Solid-State-Circuits Conference (ISSCC) program committee, an associate editor of the IEEE Journal of Solid-State Circuits and a Distinguished Lecturer of the IEEE Solid-State Circuits Society.

Low-Power and Low-Voltage DC-DC Converter Design

With the recent advanced development of the VLSI system, power management circuits will be operated with lower output power requirement and with lower supply voltage. Several strategies to improve the power efficiency of low-power DC-DC converter are described and their pros and cons are discussed. Different design techniques for low-voltage dc-dc converter design are also included.

Instructor: Philip Mok is a Professor at the Department of Electronic and Computer Engineering, the Hong Kong University of Science and Technology in Hong Kong. He received his PhD in Electrical and Computer Engineering from the University of Toronto, Toronto, Canada, in 1995. His current research interests include power management integrated circuits and low-voltage analog integrated circuits design.

F3: 10-40 Gb/s I/O Design for Data Communications

Organizer: **Ken Chang,** *Xilinx, San Jose, CA*
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The importance of I/O data rates beyond 10Gb/s is growing rapidly. Supporting these data rates introduces new challenges beyond those faced at lower data rates. The objective of this Forum is to present both electrical and optical I/O approaches to meeting these challenges at the architecture and circuit levels. The Forum commences with two talks offering an overview of circuits and systems issues in CMOS technology. They are followed by two presentations focusing on the challenges of 20Gb/s+ over electrical backplanes and very lossy electrical channels. The next talk compares conventional analog equalization versus digital (data-converter-based) approaches from a system perspective. The final two talks focus on optical solutions, highlighting the relative strengths and weaknesses of electrical and optical approaches. The Forum concludes with a panel discussion providing an opportunity for participants to give feedback and ask questions. The Forum is aimed at circuit designers and engineers working on high-speed wireline transceivers.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction:** **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
08:30	**10-to-40Gb/s I/O Circuits and System Design: Techniques to Improve Power Efficiency** **James Jaussi,** *Intel, Hillsboro, OR*
09:20	**Design of 40Gb/s Broadband Transceivers in CMOS Technology** **Jri Lee,** *National Taiwan Univeristy, Taipei, Taiwan*
10:10	Break
10:35	**(What is so Hard About) SerDes Design Challenges for 20Gb/s+ Data Rates over Electrical Backplanes?** **Andy Joy,** *Texas Instruments, Northampton, United Kingdom*
11:25	**10-20Gb/s+ Equalizer Design for Electrical Channel with 40dB+ Loss** **Yasuo Hidaka,** *Fujitsu Laboratories of America, Sunnyvale, CA*
12:15	Lunch
1:20	**Equalization for High-Speed SerDes Systems – a System-Level Comparison of Analog and Digital Techniques** **Vivek Telang,** *Broadcom, Austin, TX*
2:10	**Optical vs. Electrical I/O: Reach, Bandwidth, Power Efficiency, Density and Cost** **Alexander Rylyakov,** *IBM T.J. Watson Research Center, Yorktown Heights, NY*
3:00	Break
3:20	**A System-Level Look at Silicon Photonics** **Ron Ho,** *Oracle, Redwood Shores, CA*
4:10	Panel Discussion
5:00	Closing Remarks (Chair)

F4: Computational Imaging

Organizers: **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
Albert Theuwissen, *Harvest Imaging, Bree, Belgium, Delft University of Technology, Delft, The Netherlands*
Johannes Solhusvik, *Aptina Imaging, Oslo, Norway*

Committee: **Jan Bosiers,** *Teledyne DALSA, Eindhoven, The Netherlands*

Computational imaging is becoming widely adopted in consumer products to reconstruct high-quality pictures from raw pixel data provided by special optics and image sensors. This forum provides details of such systems. We commence with an overview of computational photograpy and imaging. This is followed by object recognition and tracking techniques including interesting point techniques and face-detection algorithms optimized for cameras. Camera array techniques, multiple shot techniques and coded aperture techniques for improved resolution and extended depth-of-field are presented. The popular compressed sensing technique is also covered with the aim to reduce data rate without severely impacting image quality. Last, existing implementations on parallel-processing architectures are introduced.

Forum Agenda

Time	Topic
08:00	Breakfast
08:30	**Introduction** **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
08:35	**Overview of Computational Photography and Imaging** **Shinsaku Hiura,** *Hiroshima City University, Hiroshima, Japan*
09:20	**Interest Point and Local Descriptor Generation in Silicon** **Graham Kirsch,** *Aptina UK, Berkshire, United Kingdom*
10:05	Break
10:30	**Face Detection in Embedded Systems** **Petronel Bigioi,** *DigitalOptics, San Jose, CA*
11:15	**Light Field Imaging with Regular Arrays of Inexpensive Cameras (RayCam)** **Kartik Venkataraman,** *Pelican Imaging, Mountain View, CA*
12:00	Lunch
1:00	**Super-Resolution by Multiple Shots: From Myths to Methods** **Lucas van Vliet,** *Delft University of Technology, Delft, The Netherlands*
1:45	**Image and Depth from a Conventional Camera with a Coded Aperture** **Bill Freeman,** *Massachusetts Institute of Technology, Cambridge, MA*
2:30	Break
2:50	**Is Compressed Sensing Relevant to Image Sensors?** **Abbas El Gamal,** *Stanford University, Stanford, CA*
3:35	**Processing Device Prospectives for Computational Imaging Applications** **Yuki Kobayashi,** *Renesas Electronics, Kanagawa, Japan*
4:20	Closing Remarks (Chair)

F5: Bioelectronics for Sustainable Healthcare

Organizers: **Chris Van Hoof,** *imec, Leuven, Belgium*
Wim Dehaene, *Katholieke Universiteit Leuven, Leuven, Belgium*
Wentai Liu, *UC Santa Cruz, Santa Cruz, CA*

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Chris Van Hoof, *imec, Leuven, Belgium*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*

The forum gives a broad view on the role of Bioelectronics in the world of tomorrow. It starts from a holistic view on the importance of sustainable and affordable health care from a societal and economical perspective. Next the forum addresses key application challenges that need to be met to achieve those goals. The circuit and system requirements for these applications is derived. In the third part of the forum, the realization of the circuit building blocks (and their remaining challenges) is discussed. Circuit and component innovation is shown to be crucial for achieving advanced technological tools that will underpin sustainable health care.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Introduction** **Chris Van Hoof,** *imec, Leuven, Belgium*
8:40	**Societal and Economical Healthcare Challenges** **Bill Heetderks,** *NIH-BIBIB, Bethesda, MD*
9:40	**Electronic System Challenges for Healthcare** **Gene Frantz,** *Texas Instruments, Dallas, TX*
10:40	Break
10:55	**Retinal Prosthesis and Hybrid Neural Interfaces** **James D Weiland,** *USC, Los Angeles, CA*
11:40	**Chip-Level Electronic Noses for a Sustainable Society** **Sywert Brongersma,** *Holst Centre, Eindhoven, The Netherlands*
12:25	Lunch
1:15	**Low-Cost MR-compatible Neuroprosthetics** **Sung June Kim,** *Seoul National University, Seoul, Korea*
2:00	**THz Bio-Imaging Systems** **Frank Chang,** *UCLA, Los Angeles, CA*
2:45	**Low Noise Design and Integration Challenges for Neurophysiology Probes** **Zhi Yang,** *Singapore National University, Singapore, Singapore*
3:30	**Low-Power Wireless and Implantable Sensor Interfaces** **Georges Gielen,** *University of Leuven, Leuven, Belgium*
4:15	Break
4:30	Conclusion

F6: Power/Performance Optimization of Many-Core Processor SoCs

Organizers: **Stephen Kosonocky,** *Advanced Micro Devices, Fort Collins, CO*
Vladimir Stojanovic, *MIT, Cambridge, MA*

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Joshua Friedrich, *IBM, Austin, TX*

As performance scaling per-core continues to slow-down, designers are faced with a myriad of challenges in efficiently using the transistors offered by modern processes. This Forum will address next generation computing challenges in the context of highly parallel manycore processors. The key design challenge in the many-core era is management and efficient use of resources across the layers of design hierarchy. In this context, the Forum will focus on key challenges that lie ahead:

- Architecture balancing: homogeneous vs. heterogeneous processors
- Embedded multicore challenges in mobile platforms
- Power management and optimization
- On-chip network and memory system design for ease of programming and balancing of compute/communication power
- Design tool challenges for many-core SOCs

Forum Agenda

Time	Topic
08:00	Breakfast
08:30	**Introduction** **Stephen Kosonocky,** *AMD, Fort Collin, CO*
08:45	**Integration Choices for Heterogeneous SoCs** **Jim Kahle,** *IBM, Austin, TX*
09:30	**Embedded Multicore in Mobile Platforms** **Alain Artieri,** *ST-Ericsson, Grenoble, France*
10:15	*Break*
10:30	**Heterogeneous Many-Core Processors and the Fusion System Architecture** **Michael Schulte,** *AMD, Austin, TX*
11:15	**Power Optimization Through Many-Core Multiprocessing** **John Goodacre,** *ARM, Cambridge, United Kingdom*
12:00	Lunch
11:00	**High-Performance Energy-Efficient NoC Fabrics** **Mark A. Anders,** *Intel, Hillsboro, OR*
11:45	**System-Level Power Management Methodology for Real-Time Applications: From Application to Silicon** **Se-Joong Lee,** *Texas Instruments, Dallas, TX*
2:30	**Randomized Modeling of Performance and Power in Heterogeneous Multi-Core SOC** **Michael Frank,** *MediaTek, San Jose, CA*
3:15	**The Layout Evaluation and Hierarchical Layout Method of MPSoC** **Yuichi Nakamura,** *NEC, Kawasaki, Japan*
4:00	Break
4:15	Panel Discussion – Moderator: **Vladimir Stojanovic**, *MIT, Cambridge, MA*
5:00	**Conclusion**

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HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX or mail: Use the "2012 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2012". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

Onsite: The Onsite Registration and Advance Registration Pickup Desks at ISSCC 2012 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	February 18	4:00 pm to 7:00 pm
Sunday,	February 19	6:30 am to 8:30 pm
Monday,	February 20	6:30 am to 3:00 pm
Tuesday,	February 21	8:00 am to 3:00 pm
Wednesday,	February 22	8:00 am to 3:00 pm
Thursday,	February 23	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 13, 2012.** After January 13th, and on or before 11:59 pm Pacific Time Monday January 30, 2012, registrations will be processed **at the Late Registration rates. After January 30th, you must register onsite at the Onsite rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC 2012.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Monday January 30, 2012,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 30, 2012.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

MEMBERSHIP SAVES YOU ON ISSCC REGISTRATION

Take advantage of reduced ISSCC registration fees by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register onsite without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join at any time and you'll receive your member number by email. If you join at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

All IEEE members are invited to drop into the Member Lounge in the Willow Room behind the IEEE Exhibit this year. Meet and greet other IEEE members and IEEE staff, learn more about products/services, IEEE grade elevations, or just relax.

Upgrade your IEEE membership to Solid-State Circuits Society membership for $28. SSCS membership provides tutorials and short courses free online at sscs.ieee.org/tutorials-online. Students are eligible for conference travel grants with SSCS membership and an application. Add Society membership at sscs.ieee.org/membership or renew or join during ISSCC at the onsite IEEE Exhibit.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: A number of technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 8:00 pm; on Tuesday from 10:00 am to 8:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demo Sessions: Hardware demonstrations will support selected papers from industry and academia during the Social Hours.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm on Monday and Tuesday in both the Book Display and Author Interview areas.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC logo umbrella: A folding umbrella will be provided to all conference registrants.

Publications: Conference registration includes:
-The **Digest of Technical Papers** in both hard copy and on CD (available onsite beginning on Sunday at 4:00 pm, and during registration hours on Monday through Wednesday).
-The **ISSCC 2012 Conference DVD** that includes the Digest and Visuals Supplement (to be mailed in April). **Student registration does not include the ISSCC 2011 Conference DVD, however it is available for purchase at a reduced fee for students.**

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2012 for an additional fee. There are nine 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The all-day events also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be sponsoring a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. By registering and paying a nominal fee for this event, you will receive a ticket, a chance to build new friendships, and an opportunity to expand your professional network. Please indicate on your ISSCC registration form if you plan to attend this special event, open to women only.

OPTIONAL PUBLICATIONS

ISSCC 2012 Publications: The following ISSCC 2012 publications can be purchased in advance or onsite:
Additional copies of the **Digest of Technical Papers** in book or CD format.
Additional copies of the **ISSCC 2012 Conference DVD (mailed in April).**
ISSCC 2012 Conference DVD at the special student price **(mailed in April).**
2012 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**
2012 Short Course DVD: "Low Power Analog Signal Processing" **(mailed in May)**.
Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVDs contain a pdf file of the presentations suitable for printing, and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference or mailed to you when available.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can pick up (or order for future delivery) materials at this desk. Tutorial and Short Course DVDs from prior conferences are available. See the order form for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail or fax. For a small shipping fee, this material will be sent to you immediately (or when available) and you will not have to wait until you attend the conference to get it.

CONFERENCE INFORMATION

HOW TO MAKE HOTEL RESERVATIONS

TO ALL ATTENDEES WHO NEED A HOTEL ROOM: We are offering this year a $100 Marriott rebate coupon! If you register for ISSCC 2012 and spend at least three nights at the San Francisco Marriott Marquis, a credit of $100 will be applied to your hotel bill. Enjoy the convenience of staying at the Conference hotel AND save money too! See the hotel reservations site for details.

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $215 for a single/double, $235 for a triple and $255 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.
Telephone: Call 800-266-9432 (US) or 506-474-2009 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2012 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 30, 2012 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 30th, the group rates will no longer be available and reservations will be filled at the best available rate.**
Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the deadline, call the Marriott Marquis at 888-575-8934 (ask for "Reservations"). Have your hotel confirmation number ready.

REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis 55 Fourth Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@cs.com Phone: 416-418-3034 Fax: 416-971-2286
Registration:	YesEvents P.O. Box 32862 Baltimore, MD 21282 Email: issccinfo@yesevents.com Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2013 will be held on February 17-21, 2013 at the San Francisco Marriott Marquis Hotel.

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ISSCC 2012 ADVANCE PROGRAM