ADVANCE PROGRAM

2005 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference — September 13-15, 2005
Short Course — September 12, 2005
Place — International Conference Center Kobe (Hyogo, Japan)

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS
Technical-Cosponsored by
IEEE Electron Devices Society
in cooperation with
The Electrochemical Society of Japan
IEEE EDS Japan Chapter
IEEE Japan Council
The Institute of Electrical Engineers of Japan
The Institute of Electronics, Information and Communication Engineers
The Institute of Image Information and Television Engineers
Japan Institute of Electronics Packaging

ssdm 2005

Website : http://www.ssdm.jp

2005 International Conference on Solid State Devices and Materials (SSDM 2005)

SECRETARIAT
c/o Inter Group Corp.
Toranomon Takagi Bldg., 1-7-2, Nishishinbashi,
Minato-ku, Tokyo 105-0003 Japan
TEL:+81-3-3597-1108
FAX:+81-3-3597-1097
E-mail: ssdm@intergroup.co.jp
URL: www.ssdm.jp

ssdm

SSDM 2005 Time Table

* P# means the poster presentation of Area #

Tuesday, September 13

MAIN HALL

10:00-12:00 PL: Opening Session

Room 301	Room 501	Room 502	Room 503	Room 504	Room 505	Room 401	Room 402	Room 403
13:30-15:20 **Area1: Advanced Gate Stack/Si Processing Science** A-1: High-k Gate Dielectric Stacks I	**13:30-15:20** **Area3: CMOS Devices/Device Physics** B-1: Advanced CMOS Technology I	**13:30-15:40** **Area2: Characterization and Materials Engineering for Device Integration** C-1: Device Integration I	**13:30-15:30** **Area11: Micro/Nano Electromechanical and Bio-Systems** D-1: Micro/Nano Sensing Devices	**13:30-15:30** **Area7: Photonic Device Physics and Devices** E-1: Quantum Dot Nanostructure and Devices	**13:30-15:30** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-1: Growth and Synthesis of New Materials I	**13:30-15:30** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-1: Quantum Devices	**13:30-15:20** **Area4: Advanced Memory Technology** H-1: DRAM	**13:30-15:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-1: High-Voltage Devices
15:45-17:45 **Area1: Advanced Gate Stack/Si Processing Science** A-2: High-k Gate Dielectric Stacks II	**15:45-17:25** **Area3: CMOS Devices/Device Physics** B-2: Mobility Enhancement Technology	**15:45-17:35** **Area2: Characterization and Materials Engineering for Device Integration** C-2: New Technology	**15:45-17:15** **Area11: Micro/Nano Electromechanical and Bio-Systems** D-2: Design and Packaging	**15:45-17:45** **Area7: Photonic and Device Physics Devices** E-2: Lasers and LEDs	**15:45-17:15** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-2: Growth and Synthesis of New Materials II	**15:45-17:45** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-2: Silicon Nanodevices	**15:45-17:35** **Area4: Advanced Memory Technology** H-2: Flash Memory I	**15:45-17:15** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-2: Novel Devices and Applications

18:30-20:30 Banquet (PORTOPIA HOTEL Room KAIRAKU)

Wednesday, September 14

Room 301	Room 501	Room 502	Room 503		Room 505	Room 401	Room 402	Room 403
9:15-10:15 **Area1: Advanced Gate Stack/Si Processing Science** A-3: High-k Gate Dielectric Stacks III	**9:15-10:15** **Area3: CMOS Devices/Device Physics** B-3: Carrier Transport I			**9:15-10:30** **Area7: Photonic Device Physics Devices and** E-3: Photonic Crystals and Light Control	**9:15-10:30** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-3: Nanostructure Fabrications	**9:15-10:30** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-3: Quantum Information Devices	**9:15-10:15** **Area4: Advanced Memory Technology** H-3: SRAM	
10:45-12:15 **Area1: Advanced Gate Stack/Si Processing Science** A-4: Characterization of Gate Dielectrics	**10:45-12:05** **Area3: CMOS Devices/Device Physics** B-4: Carrier Transport Modeling	**10:30-12:15** **Short Presentation** **P1, P2 and P4**	**10:30-12:15** **Short Presentation** **P6, P7, P8 and P9**	**10:45-12:15** **Area7: Photonic Device Physics Devices and** E-4: Si Photonics and Optical Interconnects	**10:45-12:15** **Area8: Advanced Material Synthesis and Crystal Growth Technology** F-4: Si and Related Materials	**10:45-12:00** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-4: Novel Devices I	**10:45-11:45** **Area4: Advanced Memory Technology** H-4: Flash Memory II	**10:30-12:15** **Short Presentation** **P3, P5, P10 and P11**

13:00-15:00 Poster Session (Reception Hall)

15:15-16:35 **Area1: Advanced Gate Stack/Si Processing Science** A-5: Characterization & Reliability of Gate Dielectrics	**15:15-16:45** **Area3: CMOS Devices/Device Physics** B-5: Advanced CMOS Technology II	**15:15-16:45** **Area2: Characterization and Materials Engineering for Device Integration** C-5: Characterization	**15:15-16:35** **Area5: Advanced Circuits and Systems** D-5: Antennas and Sensor	**15:15-16:45** **Area7: Photonic Device Physics Devices and** E-5: Detectors and Sensors I	**15:15-16:45** **Area10: Organic Materials Science, Device Physics, and Applications** F-5: Molecular Electronics and Physics I	**15:15-16:45** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-5: Novel Devices II	**15:15-16:45** **Area11: Micro/Nano Electromechanical and Bio-Systems** H-5: Bio Sensors and Chips I	**15:15-16:45** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-5: Nitride Devices
17:00-18:00 **Area1: Advanced Gate Stack/Si Processing Science** A-6: Alternative High-k Gate Dielectrics	**17:00-18:00** **Area3: CMOS Devices/Device Physics** B-6: Device Modeling	**17:00-18:00** **Area2: Characterization and Materials Engineering for Device Integration** C-6: Device Integration II	**17:00-18:10** **Area5: Advanced Circuits and Systems** D-6: Advanced System LSIs	**17:00-17:45** **Area7: Photonic Device Physics Devices and** E-6: Detectors and Sensors II	**17:00-18:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-6: Molecular Electronics and Physics II	**17:00-18:00** **Area9: Physics and Applications of Novel Functional Materials and Devices** G-6: Spintronics	**17:00-18:15** **Area11: Micro/Nano Electromechanical and Bio-Systems** H-6: Bio Sensors and Chips II	**17:00-18:00** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-6: Nitride Devices

18:30-20:30 Rump Session
Room 501 "Beyond the Scaling Limit—Innovative Devices and Materials—"
Room 502 "Flexible Electronics—Is it Real?"

Thursday, September 15

Room 301	Room 501	Room 502	Room 503		Room 505	Room 401	Room 402	Room 403
9:15-10:25 **Area1: Advanced Gate Stack/Si Processing Science** A-7: Metal Gates I	**9:15-10:15** **Area3: CMOS Devices/Device Physics** B-7: Carrier Transport II	**9:15-10:15** **Joint Area 1, 2 and 3** C-7: Germanide and Defects	**9:15-10:25** **Area5: Advanced Circuits and Systems** D-7: Mixed-Signal Design		**9:15-10:30** **Area10: Organic Materials Science, Device Physics, and Applications** F-7: Organic Light Emitting Devices I	**9:15-10:45** **Joint Area 8 and 9** G-7: Joint Session Nanotubes and Nanowires I	**9:15-10:25** **Area4: Advanced Memory Technology** H-7: FeRAM I	**9:15-10:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-7: Modeling and Simulation
10:45-12:05 **Area1: Advanced Gate Stack/Si Processing Science** A-8: Metal Gates II	**10:45-12:15** **Area3: CMOS Devices/Device Physics** B-8: Device Reliability	**10:45-12:15** **Joint Area 1, 2 and 3** C-8: Advanced Source/Drain Technology	**10:45-12:05** **Area5: Advanced Circuits and Systems** D-8: High-Frequency Circuits		**10:45-12:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-8: Organic Light Emitting Devices II	**11:00-12:30** **Joint Area 8 and 9** G-8: Joint Session Nanotubes and Nanowires II	**10:45-12:05** **Area4: Advanced Memory Technology** H-8: FeRAM II	**10:45-11:30** **Area6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-8: Modeling and Simulation

12:30-13:30 SSDM 2005 Luncheon (PORTOPIA HOTEL Room KAIRAKU)

13:30-14:50 **Area1: Advanced Gate Stack/Si Processing Science** A-9: GeFETs & Simulation	**13:30-14:50** **Area3: CMOS Devices/Device Physics** B-9: Device Technology I	**13:30-14:50** **Joint Area 1, 2 and 3** C-9: Shallow Junction	**13:30-14:50** **Area5: Advanced Circuits and Systems** D-9: Device Characteristics and Circuits		**13:30-15:00** **Area10: Organic Materials Science, Device Physics, and Applications** F-9: Organic Transistors I	**13:30-15:00** **Joint Area 8 and 9** G-9: Joint Session Nanotubes and Nanowires III	**13:30-15:00** **Area4: Advanced Memory Technology** H-9: MRAM	
	15:15-16:15 **Area3: CMOS Devices/Device Physics** B-10: Device Technology II	**15:15-16:35** **Area1: Advanced Gate Stack/Si Processing Science** C-10: Metal Gates III	**15:15-16:25** **Area5: Advanced Circuits and Systems** D-10: Power Devices and Packaging Technologies		**15:15-16:15** **Area10: Organic Materials Science, Device Physics, and Applications** F-10: Organic Transistors II		**15:15-16:15** **Area4: Advanced Memory Technology** H-10: PRAM	

SSDM 2005 Advance Program
General Information

DATE
Conference: **September 13-15, 2005 (Official language is English)**
Short Course: **September 12, 2005 (in Japanese)**

LOCATION
International Conference Center Kobe
6-9-1 Minatojima-Nakamachi, Chuo-ku, Kobe 650-0046, Japan
Phone: +81-78-302-5200 Fax: +81-78-302-6485
International Conference Center Kobe opened in 1981. Conveniently situated on Port Island, it effectively functions as the core of Kobe's well developed convention facilities.
A Limousine bus takes you from Kansai International Airport (KIX) to Kobe in 80 minutes. International Conference Center Kobe is only 10 minutes from the center of downtown Kobe by Port Liner.
For further information, see
http://www.kcva.or.jp/kcc/icck/e-index.html

REGISTRATION
The registration desk will be open from September 12 to 15 in the entrance hall on the third floor (conference site). The registration hours are as follows:

September	12	9:00-17:00
	13	9:00-17:00
	14	9:00-17:00
	15	9:00-15:30

Advance registration will be accepted only through the conference website until August 31, 2005, 17:00 Japan time. (http://www.ssdm.jp)
After the deadline, registration can be made at the conference site as on-site registration. Early registration is recommended.

	Registration Fee		Short Courses (in Japanese)	Banquet
	On or Before August 12	On or After August 13		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanied person(s)				¥4,000/person

1) The registration fee includes one copy of the abstract book and a CD-ROM. However, it does not include the banquet, and an additional payment is required to attend the banquet (Regular: ¥7,000, Student/Accompanied person: ¥4,000).
2) Those who register as students are required to fax a copy of their current student ID to JTB Corp. (Fax: +81-45-316-5701) at the time of registration and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of the online registration of individual information.
3) Registration is complete only after payment is made in full.

Payment Procedure
Payment can be made by:
- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. American Express
- A bank transfer to JTB Corp. (Message: SSDM)
  Account at the Bank of Tokyo Mitsubishi, Yokohama Branch #480, 3-27-1 Honcho, Naka-ku, Yokohama-shi, Kanagawa 231-0005, Japan (Ordinary Account: 0043079)

* Personal checks are not acceptable.

Confirmation of Pre-Registration
Upon receipt of your online registration, a written confirmation will be faxed or e-mailed to you after your payment is confirmed.
Please bring this confirmation slip with you and present it to the registration desk.

Registration Cancellation
Conference:
Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to JTB Corp. No cancellation will be accepted after August 17, 2005. Extended Abstracts will be sent to absent registrants after the conference.

Short Course:
A cancellation fee of ¥2,000 will be deducted from the refund. Cancellations should be made in writing to JTB Corp. No cancellation will be accepted after August 17. Short-course textbooks will be sent to the absent registrants after the conference.

Inquiries for Registration
JTB Corp., Yokohama Group Tours Office
SSDM 2005 Desk
TEL: +81-45-316-4602
FAX: +81-45-316-5701
E-mail: jtb_convention@jtb.jp
Office hours: 9:30-17:30 (weekdays only)

On-site Registration
Registration fees should be paid in Japanese Yen or credit cards. VISA, MasterCard, Diners Club and American Express are acceptable. No personal checks are acceptable.

BANQUET
The conference banquet will be held in the Kairaku banquet room at the Portopia Hotel (B1 floor of the hotel main building) on September 13, 18:30-20:30. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the registration fee. Participants who wish to attend the banquet are requested to order the banquet tickets through the on-line registration. Banquet tickets may also be purchased at the registration desk.

LATE NEWS PAPERS
Submission of Late News Papers has been already closed on July 29, 2005. The accepted papers will be on "Advanced Program Part II" which will be distributed at the venue during the conference.

SPECIAL ISSUE OF JJAP
Authors of papers accepted for SSDM 2005 are encouraged to submit the original and significant part of the papers to the special issue of the *Japanese Journal of Applied Physics*. The special issue will be published in April 2006. Please refer to the conference website for details.

RUMP SESSION - September 14 (Wednesday) 18:30-20:30

Session A (Room 501, 5F)

"Beyond the Scaling Limit—Innovative Devices and Materials—"

Within 10 years, device sizes will surely reach less than 10 nm and we will then face a problem called the scaling limit. As we approach or go beyond the scaling limit, we need innovative concepts in signal transfer and processing. We will also have to take into account quantum effects in addition to classical effects even at room temperature. In this rump session, we would like to discuss what will happen in this situation from technological and physical viewpoints and what will be necessary to overcome this near-future problem. Innovative device designs, process technologies and integration methods will be played up in this rump session. The introduction of innovative materials will be a key issue for future devices. Our discussions will not be limited to conventional silicon devices; they will extend to compound semiconductors and non-silicon based materials, i.e. oxides, carbon based compounds and molecules, as well. It is our hope that this rump session will get everyone thinking about the scaling-limit and that the discussions in this session become a starting point for new scaling concepts.

Organizers/Moderators:	Y. Hirayama (NTT, Japan) K. Masu (Tokyo Tech, Japan) H. Tabata (Osaka Univ., Japan) S. Zaima (Nagoya Univ., Japan)
Panelists:	J. Barker (Univ. of Glasgow, UK) S. Biesemans (IMEC, Belgium) F. Boeuf (STMicroelectronics, France) F. Kreupl (Infineon, Germany) S. Sugahara (Univ. of Tokyo, Japan) A couple of additional panelists will be invited.

Session B (Room 502, 5F)

"Flexible Electronics—Is It Real?"

Special attention has been given to flexible electronics because of the remarkable progress of device technology, such as organic thin-film transistors and semiconductor nanowire. Recently, many interesting applications have been proposed, such as wearable computers, flexible image scanners, and flexible displays. Flexible electronics has the potential to offer advantages over existing technologies and open a new market. In this rump session, we would like to discuss the following issues:

(1) What are the merits of "flexibility"?
(2) Where are we now in terms of fabrication and technology level?
(3) When will it be real?
(4) What technical hurdles must be overcome? How can we overcome them? Where can we go?

We hope you will become acquainted with the present status of flexible electronics and join in on a discussion on the future prospect of this fascinating technology.

Moderators:	S. Tokito (NHK, Japan) T. Someya (Univ. of Tokyo, Japan)
Organizer:	H. Matsuoka (Hitachi, Japan)
Panelists:	J. Kanicki (Univ. of Michigan, USA) H. Kawai (Seiko Epson, Japan) M. Ando (Hitachi, Japan) T. Kamiya (Tokyo Tech, Japan) A couple of additional panelists will be invited.

SHORT COURSE

Short Course entitled “Organic Semiconductor Devices with Attractive and Possible Properties” will be held on Monday, September 12. All lectures are given in Japanese.

SSDM 2005 LUNCHEON

As the event of the World Year of Physics 2005, the SSDM luncheon, featuring an address by Prof. Hiroshi Ezawa, will be held on Thursday, September 15, at 12:30 p.m. in the Kairaku banquet room at the Portopia Hotel. Prof. Ezawa is one of the pioneers in quantum field theory method in statistical mechanics. The title of his presentation is “Einstein’s Miracle Year.” Luncheon tickets will be available on-site at a cost of ¥500. Seating is limited to 100 people.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

Submission of an abstract for review and subsequent acceptance is considered by the committee as an agreement that the work will not be published by the author prior to the presentation at the conference. This policy will be enforced by the automatic withdrawal of the paper by the conference committee.

AWARDS

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for outstanding contribution to the field of solid state devices and materials, among papers presented prior to 1999.

SSDM Paper Award

Given for the best paper presented at SSDM 2004.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at SSDM 2004.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted.
Late news papers are not eligible for travel grants.
An application form for the Marubun Grant will be sent to eligible authors. The grant is authorized by Marubun Research Promotion Foundation (MRPF).

VISA REQUIREMENT

All foreign participants must have a valid passport. Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or Consulate as soon as possible.
Concerning visa applications, generally, in applying for a visa each applicant is requested to submit the documents listed below:
(1) an invitation letter (an optional document written in English)
(2) a letter of guarantee (written in Japanese)
(3) documents certifying the purpose of the visit (written in Japanese)
(4) the applicant’s schedule in Japan (written in Japanese)

Please ask the nearest Japanese Embassy to make sure what documents are required to obtain a visa first, and then contact the SSDM Secretariat. The Secretariat will send the Reply Form for Visa Application in order to obtain the required documents. Please complete the Reply Form for Visa Application and submit it to the secretariat. We will send you all the requested documents as soon as we receive the Reply Form.

OFFICIAL TRAVEL AGENT

JTB Corp.
Yokohama Group Tours Office
6F, 3-29-1 Tsuruya-cho, Kanagawa-ku, Yokohama 221-0835, Japan
Phone:+81-45-316-4602 Fax: +81-45-316-5701 E-mail: jtb_convention@jtb.jp

Hotel accommodations

JTB has blocked rooms at following hotels in Kobe for the conference period. Reservations can be made through the conference website.

Hotel Name	**Kobe Portopia Hotel**
Room Rates	Single: ¥9,450 Twin: ¥16,800 (per room, per night) Single Use of Twin or Double Room: ¥12,600
Check-in/out	Check-in:13:00/Check-out:12:00
Address	6-10-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-302-1111
Access to Hotel	1 min. walk from Port Liner Shimin-Hiroba Sta.
To Conference site	next to the site

Hotel Name	**Hotel Pearl City Kobe**
Room Rates	Single: ¥9,975 Twin: ¥17,850 (per room, per night)
Check-in/out	Check-in:14:00/Check-out:11:00
Address	7-5-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-303-0100
Access to Hotel	2 min. walk from Port Liner Nakafutou Sta.
To Conference site	5 min. walk to the site

Hotel Name	**Quality Hotel Kobe**
Room Rates	Single: ¥7,500 Twin: ¥17,000 (per room, per night)
Check-in/out	Check-in:15:00/Check-out:10:00
Address	6-1, Minatojima Nakamachi, Chuo-ku, Kobe, 650-0046, Japan
Phone	+81-78-303-5555
Access to Hotel	5 min. walk from Port Liner Shimin Hiroba Sta.
To Conference site	5 min. walk to the site

Hotel Name	**Sannomiya Terminal Hotel**
Room Rates	Single: ¥8,820 Twin: ¥17,220 (per room, per night)
Check-in/out	Check-in:13:00/Check-out:11:00
Address	8-1-2, Kumoi-dori, Chuo-ku, Kobe, 651-0096, Japan
Phone	+81-78-291-0001
Access to Hotel	Connecting to JR Sannomiya Sta.
To Conference site	15 min. by Port Liner & walk to the site

Hotel Name	**Sanside Hotel**
Room Rates	Single: ¥6,090 Twin: not available
Check-in/out	Check-in:15:00/Check-out:10:00
Address	4-1-3, Kumoi-dori, Chuo-ku, Kobe, 651-0096, Japan
Phone	+81-78-232-3331
Access to Hotel	5 min. walk from JR Sannomiya Sta.
To Conference site	20 min. by Port Liner & walk to the site

Note: Room rates include tax and service charge. No meals are included.

Application and payment

Participants wishing to reserve hotel accommodations should access the Online Registration page of the conference website. Reservations should be made no later than August 19, 2005. (A confirmation sheet will be sent by JTB.)
Application should be accompanied by a remittance covering the total accommodation fee plus handling fee (¥525) due JTB.

No reservation will be confirmed in the absence of this payment. All payment must be in Japanese yen. If the remitter's name is different from the participant's name, or if the amount covers more than one person, please inform us of the details for the payment.

Payment should be in the form of:

- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. American Express
- A bank transfer to JTB Corp. (Message: SSDM)
  Account at the Bank of Tokyo Mitsubishi, Yokohama Branch #480, 3-27-1 Honcho, Naka-ku, Yokohama-shi, Kanagawa 231-0005, Japan (Ordinary Account: 0043079)

Cancellation policy for accommondations

In the event of cancellation, written notification should be sent to JTB. Do not contact hotels directly. The following cancellation fees will be deducted before refunding.

Hotels: Up to 21 days before the arrival date.....¥525
2 to 20 days before.....20% of daily room charge (minimum ¥525)
1 day before .....80% of daily room charge
On the day of arrival or no notice given.....100% of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Kobe is warm and sometimes humid in September. The temperature range is 18-30˚C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tokyo, and 60 Hz in western Japan including Kobe (conference site), Kyoto and Osaka.

SSDM 2005 INSTRUCTION for SPEAKERS

Oral Presentation

Presentation Time

	Session Time	Presentation Time	Discussion
Plenary	50 min.	45 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of the presentation time, Third: End of the discussion time.

Audio-Visual Equipment

The meeting rooms will contain the following audiovisual equipment:

- LCD data projector (PC not provided)
- Overhead projector
- Microphone
- Projection laser pointer

Speakers wishing to present their papers using the LCD projector are requested to verify their PC's compatibility with the sample LCD projector that will be located in the Preview Rooms (306 and 307) on the third floor prior to their presentations.
They are also recommended to bring transparencies for the overhead projector in case there is a problem with the LCD data projector. If presentations are interrupted due to problems caused by inadequate preparations, the time allotted to speakers will not be extended.

Poster Presentation

Poster sessions are scheduled for Wednesday, September 14, from 13:00 to 15:00. Poster boards will be available with identifying labels at the Reception Hall on the third floor. Authors are requested to prepare their posters between 9:00 and 12:00 on September 14 and remove their posters by 17:00 on September 14. Any posters remaining after 17:00 will be disposed of by the secretariat. Usable space on each poster board will be approximately 900mm wide and 1,500mm high. Pushpins will be available. Each presentation will be assigned a board, labeled with the paper number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are asked to give a short oral presentation in the morning of September 14. The presentation time should be kept strictly to two minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations be held in a quick, successive sequence. While one speaker is giving his/her presentation, the next several speakers should wait nearby in line for their turn in order to move on to the next presentation. Note that any absent speakers will be skipped and each presentation will be automatically stopped after two minutes have elapsed. Only a PC projector will be made available. You should send your presentation file to the secretariat (ssdm@intergroup.co.jp) by e-mail by August 24. The file must be an exact "2-page" landscape PDF. Because the presentation time is limited, please describe your research objective and results clearly and do NOT show the author list or the title on your file, those of which will be prepared by the SSDM Secretariat.

Due to the limited space, poster presentations will be divided into three sessions, as follows. Please check your poster number. (P# means the poster presentation of Area #.)

Room 502 P1, P2, P4
Room 503 P6, P7, P8, P9
Room 403 P3, P5, P10, P11

Tuesday, September 13

MAIN HALL, 1F

PL: Opening Session (10:00–12:00)
Chairpersons: M. Morita, Osaka Univ. and A. Toriumi (Univ. of Tokyo)

10:00 Pl-0
Welcome Address and Award Presentation
K. Taniguchi, Osaka Univ.

10:20 PL-1 (Plenary)
Development of Clinical Chips for Home Medical Diagnostics
Y. Horiike, NIMS, Japan

11:10 PL-2 (Plenary)
Electronics and Optoelectronics with Single Carbon Nanotubes
P. Avouris, IBM, USA

12:00-13:30 Lunch

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-1: High-k Gate Dielectric Stacks I
(13:30-15:20)
Chairs: Y. Nara (Selete)
H. Satake (ASET)

13:30 A-1-1 (Invited)
Current Status and Addressing the Challenges of Hf-based Gate Stack toward 45nm-LSTP Application
M. Niwa[1,2], R. Mitsuhashi[1,2], K. Yamamoto[1,2], S. Hayashi[2], Y. Harada[2], A. Rothchild[3], T. Hoffmann[3], S. Kubicek[3], S. De Gendt[3], M. Heyns[3], S. Biesemans[3] and M. Kubota[2], *[1]Matsushita assignee at IMEC, [2]Matsushita Electric and [3]IMEC, Belgium*

14:00 A-1-2
The Impact of Thickness Control in HfSiON Gate Dielectric on Electron Mobility with sub-nm EOT
M. Mizutani[1], T. Hayashi[1], M. Inoue[1], K. Nomura[2], J. Yugami[1], J. Tsuchimoto[1], Y. Ohno[1] and M. Yoneda[1], *[1]Renesas Technology Corp. and [2]Renesas Semiconductor Engineering, Japan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-1: Advanced CMOS Technology I
(13:30-15:20)
Chairs: K. Shibahara (Hiroshima Univ.)
J. C. S. Woo (UCLA)

13:30 B-1-1 (Invited)
45nm Conventional Bulk and "Bulk+" Architectures for Low-Cost GP/LP Applications
F. Boeuf[1], S. Monfray[1], A. Pouydebasque[2], M. Müller[2], F. Payet[1], C. Ortolland[2] and T. Skotnicki[1], *[1]STMicroelectronics and [2]Philips Semiconductor, France*

14:00 B-1-2
A 90nm Hybrid SOI CMOS Technology Integrating PDSOI and Bulk Devices for Bulk-designed MPU Performance Booster
S. Miyake, T. Suzuki, T. Watanabe, O. Fujita, N. Harada, K. Doumeki, T. Fukai, T. Syo, T. Moriya, S. Haruta, Y. Takeshita, M. Ikeda and K. Imai, *NEC Corp., Japan*

Room 502 (C)

Area 2: Characterization and Materials Engineering for Device Integration

C-1: Device Integration I
(13:30-15:40)
Chairs: S. Ogawa (Matsushita Electric)
K. Ueno (NEC)

13:30 C-1-1 (Invited)
Cu/low-k Process Integration for 65nm and 45nm SoC Devices
N. Matsunaga, *Toshiba Corp., Japan*

14:00 C-1-2
Mechanical Strength of Multilayered Dielectric Structures Measured by Laser-Pulse Generated Surface-Acoustic-Wave Technique
T. Takimura[1], N. Hata[1,2], T. Nakayama[3], Y. Shishida[3], R. Yagi[3], J. Kawahara[3], S. Chikaki[3], N. Fujii[3] and T. Kikkawa[2,4], *[1]AIST, [2]MIRAI-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*

Room 503 (D)

Area 11: Micro / Nano Electromechanical and Bio-Systems

D-1: Micro/Nano Sensing Devices
(13:30-15:30)
Chairs: Y. Yoshino (Murata Mfg.)
K. Sawada (Toyohashi Univ. of Tech.)

13:30 D-1-1 (Invited)
Computational MEMS Process Design and Development
O. Tabata, *Kyoto Univ., Japan*

14:00 D-1-2
Piezoresistive Rotation Angle Sensor Integrated in Micromirror
M. Sasaki, M. Tabata, T. Haga and K. Hane, *Tohoku Univ., Japan*

Room 504 (E)

Area 7: Photonic Devices and Device Physics

E-1: Quantum Dot and Nanostructure Devices
(13:30-15:30)
Chairs: M. Sugawara (Fujitsu Labs.)
K. Komori (AIST)

13:30 E-1-1 (Invited)
Exciton - Photon Interactions in a Quantum Dot Microcavity
A. Forchel, *Univ. of Wüerzburg, Germany*

14:00 E-1-2
1.55-μm-waveband lasing operation of Sb-based quantum-dot vertical-cavity surface-emitting lasers (Sb-based QD-VCSELs) fabricated on GaAs substrate
N. Yamamoto[1], K. Akahane[1], S. Gozu[1], A. Ueta[1] and N. Ohtani[2], *[1]National Inst. of Information and Communications Technology and [2]Doshisha Univ., Japan*

Room 505 (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-1: Growth and Synthesis of New Materials I
(13:30-15:30)
Chairs: H. Yamaguchi (NTT)
M. Tanaka (Univ. of Tokyo)

13:30 F-1-1 (Invited)
Spintronics Based on ZnO Thin Films
H. Tabata, *H. Saeki and H. Matsui, Osaka Univ., Japan*

14:00 F-1-2
A Novel Buffer Layer using Titanium-Oxide for ZnO epitaxial growth on Sapphire
T. Miyamura and S. Yamauchi, *Ibaraki Univ., Japan*

Room 401 (G)

Area 9: Physics and Applications of Novel Functional Materials and Devices

G-1: Quantum Devices
(13:30-15:30)
Chairs: J. Motohisa (Hokkaido Univ.)
T. Fujisawa (NTT)

13:30 G-1-1 (Invited)
Fabrication and Demonstration of Quantum-Dot Cellular Automata Systems
G. H. Bernstein, A. Imre, K. Sarveswaran, M. Lieberman and W. Porod, *Univ. of Notre Dame, USA*

14:00 G-1-2
Embedded Nanowire Network Growth and Node Device Fabrication for GaAs-Based High-Density Hexagonal BDD Quantum Circuits
T. Tamura, I. Tamai, S. Kasai, T. Sato, H. Hasegawa and T. Hashizume, *Hokkaido Univ., Japan*

Room 402 (H)

Area 4: Advanced Memory Technology

H-1: DRAM
(13:30-15:20)
Chairs: I . Asano (Elpida)
H. S. Jeong (Samsung Electronics)

13:30 H-1-1 (Invited)
Physical and Microscopic Understanding of Data Retention Properties of DRAM
K. Okonogi and K. Ohyu, *Elpida Memory Inc., Japan*

14:00 H-1-2
Optimization of Layout and Doping Profile Design for BT(Body Tied)-FinFET DRAM
C. H. Lee, C. Lee, J. M. Yoon, K. Kim, S. B. Park, H. S. Kang and Y. J. Ahn, *Samsung Electronics Co. Ltd., Korea*

Room 403 (I)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

I-1: High-Voltage Devices
(13:30-15:30)
Chairs: R. Hattori (Mitsubishi Electric)
A. Nakagawa (New Japan Radio)

13:30 I-1-1 (Invited)
Physics of AlGaN/GaN Electronic and Photonic Devices
M. S. Shur[1] and R. Gaska[2], *[1]Rensselaer Polytechnic Inst. and [2]Sensor Electronic Technology Inc., USA*

14:00 I-1-2
High-Voltage 4H-SiC RESURF MOSFETs Processed by Oxide Deposition and N_2O Annealing
T. Kimoto, H. Kawano, M. Noborio and J. Suda, *Kyoto Univ., Japan*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
14:20 A-1-3 Extendibility of High Mobility HfSiON Gate Dielectrics S. Inumiya, T. Miura, K. Shirai, T. Matsuki, K. Torii and Y. Nara, *Semiconductor Leading Edge Technologies, Inc., Japan*	**14:20 B-1-3** Combining Embedded and Overlayer Compressive Stressors in Advanced SOI CMOS Technologies A. Wei[1], T. Kammler[1], J. Höntschel[1], H. Bierstedt[1], J. P. Biethan[1], A. Hellmich[1], K. Hempel[1], J. Klais[1], G. Koerner[1], M. Lenski[1], T. Mantei[1], A. Neu[1], R. Otterbach[1], C. Reichel[1], B. Trui[1], G. Burbach,[1] T. Feudel[1], P. Javorka[1], C. Schwan[1], N. Kepler[1], H. J. Engelmann[1], C. Ziemer-Popp[1], O. Herzog[1], D. Greenlaw[1], M. Raab[1], R. Stephan[1], M. Horstmann[1], P. O. Hansson[2], A. Samoilov[2], E. Sanchez[2], O. Luckner[2] and S. Weiher-Telford[2], *[1]AMD, [2]Applied Materials, Inc., Germany*	**14:20 C-1-3** Properties of Low-*k* (*k*~2.05)Plasma Polymer Films Deposited by PECVD Using Decamethyl-cyclopentasiloxane and Cyclohexane as the Precursors J. Yang, S. Lee, K. Kim, H. Chae and D. Jung, *Sungkyunkwan Univ., Korea*	**14:15 D-1-3** A CMOS Image Sensor for *in vitro* and *in vivo* Imaging of the Mouse Hippocampus D. C. Ng, M. Matsuo, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, *Nara Inst. of Science and Technology, Japan*
			14:30 D-1-4 Photo-sensing Resolution of Unwired-communication Chip in Inhomogeneous RF-magnetic Field T. Hasebe, Y. Yazawa, T. Tase, M. Kamahori, K. Watanabe and T. Oonishi, *Hitachi, Ltd., Japan*
14:40 A-1-4 Influence of pre-existing electron traps on drive current in MISFETs with HfSiON gate dielectrics R. Iijima, M. Takayanagi, T. Yamaguchi, M.Koyama and A. Nishiyama, *Toshiba Corp., Japan*	**14:40 B-1-4** Effect of Process Induced Strain in 35 nm FDSOI Devices with Ultra-Thin Silicon Channels C. Gallon[1,5], C. Fenouillet-Beranger[2], S. Denorme[1], F. Boeuf[3], V. Fiori[1], N. Loubet[1], T. Kormann[3], M. Broekaart[3], P. Gouraud[1], F. Leverd[1], G. Imbert[1], C. Chaton[2], C. Laviron[2], L. Gabette[3], F. Vigilant[3], P. Garnier[4], H. Bernard[1], A. Tarnowka[3], A. Vandooren[4], R. Pantel[1], F. Pionnier[1], S. Jullian[3], S. Cristoloveanu[5] and T. Skotnicki[1], *[1]STMicroelectronics, [2]CEA-LETI, [3]Philips, [4]Freescale Semiconductors and [5]IMEP, France*	**14:40 C-1-4** A Novel Short-time Characterization Method of SIV Properties by Using the Empirical Equation M. Takahashi[1], T. Harada[2], N. Mitsu[1], K. Tsukamoto[2], S. Ogawa[2] and T. Ueda[2], *[1]Matsushita Semi-Conductor Engineering Co. Ltd. and [2]Matsushita Electric, Japan*	**14:45 D-1-5** Micro-Heater Array for Tunable Fiber-Bragg Grating V. K. Singh[1], M. Sasaki[1], K. Hane[1], S. Okude[2] and H. Hosoya[2], *[1]Tohoku Univ. and [2]Fujikura Ltd., Japan*

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
14:15 E-1-3 Broad-band Superluminescent Light Emitting Diodes Incorporating Quantum Dots in Compositionally Modulated Quantum Wells S. Ray, K. Groom, H. Y. Liu, M. Hopkinson and R. Hogg, *Univ. of Sheffield, UK*	**14:15 F-1-3** Electrical, Optical and Structure Properties of ITO Films Cosputtered with ZnO D. S. Liu[1], C. C. Wu[1], C. H. Lin[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*	**14:15 G-1-3** GaAs DH-HEMT channel coupled InAs quantum dot memory device by selective area metal organic vapor phase epitaxy D. Nataraj, N. Ooike, J. Motohisa, T. Fukui, *Hokkaido Univ., Japan*	**14:20 H-1-3** Application of HfSiON to Deep Trench Capacitors of Sub-45nm Node Embedded DRAM T. Ando[1], N. Sato[1], S. Hiyama[1], T. Hirano[1], K. Nagaoka[1], H. Abe[1], A. Okuyama[1], H. Ugajin[1], K. Tai[1], R. Katsumata[2], J. Idebuchi[2], T. Suzuki[2], T. Hasegawa[1], H. Iwamoto[1] and S. Kadomura[1], *[1]Sony Corp. and [2]Toshiba Corp., Japan*	**14:15 I-1-3** Normally-off AlGaN/GaN HEMT with Recessed Gate for High Power Applications T. Kawasaki, K. Nakata and S. Yaegassi, *Eudyna Devices Inc., Japan*
14:30 E-1-4 Self-formation of High-Density and High-Uniformity InAs Quantum-Dots on GaSb/GaAs Layers by Molecular Beam Epitaxy M. Ohta, T. Kanto and K. Yamaguchi, *Univ. of Electro-Communications, Japan*	**14:30 F-1-4** A Piezoelectric ZnO Film Prepared by RF Magnetron Sputtering D. S. Liu[1], C. H. Li[1], C. Y. Wu[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*	**14:30 G-1-4** Independent Tuning of the Confinement and Density in a Quantum Point Contact using a Center Gate and a Back Gate H. M. Lee[1,2], K. Muraki[1], E. Y. Chang[2] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs., [2]National Chiao Tung Univ. and [3]SORST-JST, Japan*		**14:30 I-1-4** Enhanced Breakdown Characteristic of AlGaN/GaN HEMTs Using a Gate/Drain Double Field-Plate Structure S. Kim and K. Yang, *KAIST, Korea*
14:45 E-1-5 Long-Wavelength Emission from Strain Controlled InAs/GaAs Self-Assembled Quantum Dots T. Inoue[1], K. Matsushita[1], M. Kikuno[1], T. Kita[1], O. Wada[1], H. Mori[2], T. Sakata[2] and H. Yasuda[1], *[1]Kobe Univ. and [2]Osaka Univ., Japan*	**14:45 F-1-5** Studies on the Nature of Deep Level Defects in GaCrN Diluted Magnetic Semiconductor S. Shanthi, S. Kimura, S. Kobayashi, M. S. Kim, Y. K. Zhou, H. Hasegawa and H. Asahi, *Osaka Univ., Japan*	**14:45 G-1-5** Relaxation Behavior of Sputter Epitaxy $Si_{1-x}Ge_x$ Film on P-Type Si(001) and NDR Observation from Hole-Tunneling RTD at RT J. Kubota, A. Hashimoto and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan*	**14:40 H-1-4** Performance and Reliability of MIM (Metal-Insulator-Metal) Capacitors with ZrO_2 for 50nm DRAM Application K. R. Yoon, K. V. Im, J. H. Yeo, E. A. Chung, Y. S. Kim, C. Y. Yoo, S. T. Kim, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*	**14:45 I-1-5** A New ICP-CVD SiO_2 Passivation for High Voltage Switching AlGaN/GaN HFETs M. W. Ha, S. C. Lee, J. C. Her, K. S. Seo and M. K. Han, *Seoul National Univ., Korea*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
15:00 A-1-5 Effects of Aluminum and Nitrogen Profile Control on Electrical Properties of HfAlON Gate Dielectric MOSFETs H. Ota[1], A. Ogawa[2], M. Kadoshima[2], W. Mizubayashi[1], K. Okada[2], T. Nabatame[2], H. Satake[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*	**15:00 B-1-5** Performance Enhancement under High-Temperature Operation and Physical Origin of Mobility Characteristics in Ge-rich strained SiGe-on-Insulator pMOSFETs T. Tezuka[1], S. Nakaharai[1], Y. Moriyama[1], N. Hirashita[1], N. Sugiyama[1], A. Tanabe[1], K. Usuda[1] and S. Takagi[2,3], *[1]MIRAI-ASET, [2]MIRAI-AIST and [3]Univ. of Tokyo, Japan*	**15:00 C-1-5** Electrical Characteristics of Porous Zeolite Interlayer Dielectrics T. Yoshino[1], G. Guan[2], N. Hata[1], N. Fujii[3] and T. Kikkawa[1,4], *[1]MIRAI-ASRC-AIST, [2]ASRC-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*	**15:00 D-1-6** Thickness Effects on pH Response of HfO_2 Sensing Dielectric Improved by Rapid Thermal Annealing C. S. Lai, C. M. Yang and T. F. Lu, *Chang Gung Univ., Taiwan*
			15:15 D-1-7 Resonant Silicon Mass Sensor with Capacitive Readout S. J. Kim, T. Ono and M. Esashi, *Tohoku Univ., Japan*

Break

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
15:00 E-1-6 Highly enhanced efficiency and stability of Photo- and Electro-Luminescence of Nano-Crystalline Porous Silicon by High-Pressure Water Vapor Annealing B. Gelloz[1] and N. Koshida[1,2], *[1]Tokyo Univ. of Agriculture and Technology and [2]Quantum 14 Co., Japan*	**15:00 F-1-6** Growth and Characterization of GaCrN/AlGaN/GaCrN Trilayer Structures M. S. Kim, Y. K. Zhou, S. Emura, S. Hasegawa and H. Asahi, *Osaka Univ., Japan*	**15:00 G-1-6** Fabrication of Fluoride Resonant Tunneling Diodes on V-grooved Si(100) Substrates S. Watanabe, T. Sugisaki, Y. Toriumi, M. Maeda and K. Tsutsui, *Tokyo Tech, Japan*	**15:00 H-1-5** Improvement of Retention time by Hydrogen Penentration Slit in DRAM Integration with Triple Metallization. J. H. Lee, J. S. Park, I. G. Kim, T. S. Kim, S. H. Cheon, A. R. Hong, J. M. Chang, D. J. Kim, J. Y. Noh, Y. S. Kim, J. S. Yoon, K. H. Yang and K. Oh, *Samsung Electronics Co. Ltd., Korea*	**15:00 I-1-6** High Speed AlGaN/GaN MIS-HEMT with High Drain and Gate Breakdown Voltages S. Yagi[1], M. Inada[1], Y. Yamamoto[1], G. Piao[1], Y. Yano[2], K. Hikosaka[1], M. Shimizu[1] and H. Okumura[1], *[1]AIST and [2]Taiyo Nippon Sanso Corp., Japan*
15:15 E-1-7 Higher luminance LEDs with nano-structured surface fabricated by self-assembled block-copolymer A. Fujimoto and K. Asakwa, *Corporate Research & Development Center, Toshiba, Japan*	**15:15 F-1-7** Controlled Growth of High Quality and Surface-Clean Multicomponent Thin Films for Nanoelectronics Applications by Using Substrates with Artificial Steps K. Endo[1], P. Badica[2,3], H. Sato[4] and H. Akoh[4], *[1]NeRI, AIST, [2]Tohoku Univ., [3]INCDFM and [4]CERC, AIST, Japan*	**15:15 G-1-7** High Peak-to-Valley Current Ratio of CdF_2/CaF_2 Resonant Tunneling Diode grown on Si(100) substrates by Nanoarea Local Epitaxy T. Kanazawa[1], A. Morosawa[1], M. Watanabe[1,2] and M. Asada[1,3], *[1]Tokyo Tech, [2]SORST-JST and [3]CREST-JST, Japan*		**15:15 I-1-7** Suppression of the leakage current of a Ni/Au Schottky Barrier Diode fabricated on AlGaN/GaN hetero-structure by oxidation S. C. Lee, M. W. Ha, J. C. Her, J. Y. Lim, K. S. Seo and M. K. Han, *Seoul National Univ., Korea*

Break

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
Area 1: Advanced Gate Stack / Si Processing Science A-2: High-k Gate Dielectric Stacks II (15:45-17:45) Chairs: S. Miyazaki (Hiroshima Univ.) M. Niwa (Matsushita)	**Area 3: CMOS Devices / Device Physics** B-2: Mobility Enhancement Technology (15:45-17:25) Chairs: K. Ohuchi (Toshiba) D. Hisamoto (Hitachi)	**15:45 C-1-6** Study on Reliability of Metal Fuse for Sub-100nm Technology D. Park, C. S. Hyun, H. C. Kim, H. J. Kang, T. H. Cho, S. G. Kim, H. J. Moon, J. W. Jung, K. Y. Lee and K. S. Oh, *Samsung Electronics Co. Ltd., Korea*	**Area 11: Micro / Nano Electromechanical and Bio-Systems** D-2: Design and Packaging (15:45-17:15) Chairs: T. Ono (Tohoku Univ.) Y. Takamura (JAIST)
15:45 A-2-1 Physical Origin of Fast Transient Charging in Hafnium Based Gate Dielectrics B. H. Lee[1,2], R. Choi[1], S. C. Song[1], J. Sim[1], C. D. Young[1], G. Bersuker[1], H. K. Park[1,3] and H. Hwang[3], *[1]International Sematech, [2]IBM and [3]GIST, USA*	**15:45 B-2-1** Examination of the Universality of Hole Mobility in Strained-Si p-MOSFETs S. Takagi[1], K. Takeda[1], S. Sugahara[1] and T. Numata[2], *[1]Univ. of Tokyo and [2]MIRAI-ASET, Japan*	**Area 2: Characterization and Materials Engineering for Device Integration** C-2: New Technology (15:45-17:55) Chairs: T. Yoda (Toshiba) M. Nihei (Fujitsu Labs.)	**15:45 D-2-1 (Invited)** Programmable Self-Assembly Across the Micro and Nano Scales K. F. Böhringer, *Univ. of Washington, USA*
16:05 A-2-2 Exact Trap Level Estimation of HfSiON Films with Various Atomic Compositions M. Koike, T. Ino, Y. Kamimuta, Y. Mitani and A. Nishiyama, *Toshiba Corp., Japan*	**16:05 B-2-2** Direct Measurement of Circuit Performance Enhancement under Mechanically Applied Uniaxial Strain T. Miyashita and T. Tanaka, *Fujitsu Labs. Ltd., Japan*	**16:05 C-2-1** Innovative Al Damascene Process for Nanoscale Interconnects K. I. Choi, S. H. Han, D. Y. Kim, S. Yun, J. W. Hong, S. W. Lee, B. H. Kim, S. T. Kim, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*	**16:15 D-2-2** Integrated RF-MEMS Technology with Wafer-Level Encapsulation K. Kuwabara[1], M. Urano[1], J. Kodate[1], N. Sato[1], T. Sakata[1], H. Ishii[1], T. Kamei[2], K. Kudou[2], M. Yano[2] and K. Machida[1], *[1]NTT Microsystem Integration Labs. and [2]NTT Advanced Technology, Japan*
16:25 A-2-3 Influences of Initial Bulk Traps on Negative Bias Temperature Instability of HfSiON I. Hirano, T. Yamaguchi, Y. Mitani, R. Iijima, K. Sekine, M. Takayanagi, K. Eguchi and N. Fukushima, *Toshiba Corp., Japan*	**16:25 B-2-3** Unified Roughness Scattering Model Incorporating Scattering Component induced by Thickness Fluctuation in SOI MOSFETs T. Ishihara[1], K. Uchida[1], J. Koga[1] and S. Takagi[2], *[1]Toshiba Corp. and [2]Univ. of Tokyo, Japan*	**16:25 C-2-2** Microstructural evolution of MIM capacitor prepared by ALD system at elevated temperature C. H. Lin, C. C. Wang, P. J. Tzeng, C. S. Liang, W. M. Lo, H. Y. Li, L. S. Lee, S. C. Lo, Y. W. Chou and M. J. Tsai, *Industrial Technology Research Inst., Taiwan*	**16:30 D-2-3** Thinning technology for lithium niobate wafer by surface activated bonding and chemical mechanical polishing C. C. Wu[1], R. H. Horng[1], D. S. Wuu[1], C. J. Ting[2, 3], H. Y. Tsai[2] and C. P. Chou[3], *[1]National Univ. of Chung-Hsing, [2]Industrial Technology Research Inst. and [3]National Chiao Tung Univ., China*

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
Area 7: Photonic Devices and Device Physics E-2: Lasers and LEDs (15:45-17:45) Chairs: O. Wada (Kobe Univ.) M. Ezaki (Toshiba)	**Area 8: Advanced Material Synthesis and Crystal Growth Technology** F-2: Growth and Synthesis of New Materials II (15:45-17:15) Chairs: H. Asahi (Osaka Univ.) Y. Nanishi (Ritsumeikan Univ.)	**Area 9: Physics and Applications of Novel Functional Materials and Devices** G-2: Silicon Nanodevices (15:45-17:45) Chairs: Y. Takahashi (Hokkaido Univ.) M. Tabe (Shizuoka Univ.)	**Area 4: Advanced Memory Technology** H-2: Flash Memory I (15:45-17:35) Chairs: T. Kobayashi (Hitachi) C. Hsu (eMemory Tech.)	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** I-2: Novel Devices and Applications (15:45-17:15) Chairs: S. Tanaka (NEC) S. Kuroda (Eudina Devices)
15:45 E-2-1 (Invited) Recent Trend in High-Speed/Low-Power-Consumption Light Sources for MAN/Ethernet Applications M. Aoki, S. Makino, J. Shimizu, H. Arimoto and K. Nakahara, *Hitachi, Ltd., Japan*	**15:45 F-2-1** Growth of Boron Nitride on 6H-SiC Substrate by Flow-rate Modulation Epitaxy Y. Kobayashi and T. Makimoto, *NTT Basic Research Labs., Japan*	**15:45 G-2-1** Large Temperature Dependence of Coulomb Blockade Oscillations in Room-Temperature Operating Silicon Single-Hole Transistor M. Kobayashi, M. Saitoh and T. Hiramoto, *Univ. of Tokyo, Japan*	**15:45 H-2-1 (Invited)** Nitride-based Nonvolatile Memory and Role of SiON Dielectric Film for Performance Improvement T. Ishimaru[1], N. Matsuzaki[1], T. Hashimoto[2] and H. Kume[1], *[1]Hitachi, Ltd., [2]Renesas Technology Corp., Japan*	**15:45 I-2-1** N-type Diamond Schottky Diodes M. Suzuki[1], S. Koizumi[2], M. Katagiri[2,3], T. Ono[1], N. Sakuma[1], H. Yoshida[1] and T. Sakai[1], *[1]Toshiba Corp., [2]NIMS and [3]Univ. of Tsukuba, Japan*
16:15 E-2-2 Optical 3R Wavelength Conversion by a combination of Self-pulsating DFB Laser and SOA-based Mach-Zehnder Interferometer S. Nishikawa[1,2], M. Gotoda[1,2], T. Nishimura[1,2], T. Miyahara[1,2], T. Hatta[1,2], K. Matsumoto[1,2], K. Takagi[1,2], T. Aoyagi[1,2] and Y. Tokuda[1,2], *[1]Mitsubishi Electric Corp. and [2]OITDA, Japan*	**16:00 F-2-2** Flow-rate modulation epitaxy of wurtzite AlBN T. Akasaka and T. Makimoto, *NTT Basic Research Labs., Japan*	**16:00 G-2-2** Very Sharp Room-Temperature Negative Differential Conductance in Silicon Single-Hole Transistor with High Voltage Gain K. Miyaji, M. Saitoh and T. Hiramoto, *Univ. of Tokyo, Japan*	**16:15 H-2-2** Study of Temperature Effect on Low V_T State Behavior of NBit Cells E. Chen, K. F. Chen, N. K. Zous, I. Huang, L. Liu, Y. J. Chen, S. Chen, M. S. Chen, L. T. Ho, W. P. Lu, W. Ting, J. Ku, A. Weng, H. C. Liou and C. Y. Lu, *Macronix International Ltd., Corp., Taiwan*	**16:00 I-2-2** Sensing Mechanism of InP Hydrogen Sensors Using Pt Schottky Diodes Formed by Electrochemical Process T. Kimura, H. Hasegawa, T. Sato and T. Hashizume, *Hokkaido Univ., Japan*
16:30 E-2-3 Continuous-Wave Operation of 1.23μm Highly Strained InGaAs Quantum-Well Ridge Waveguide Lasers on GaAs Substrates M. Ezaki[1,2], M. Kushibe[1,2], R. Hashimoto[1,2], G. I. Hatakoshi[1,2], M. Nishioka[1] and Y. Arakawa[1], *[1]Univ. of Tokyo and [2]Toshiba Corp., Japan*	**16:15 F-2-3** First-Principles Calculation of Bandgap Bowing Parameter for Wurzite InAlGaN Quaternary Alloy using Large Supercell T. Takizawa[1], S. Nakazawa[1], T. Ueda[1], T. Tanaka[1] and T. Egawa[2], *[1]Matsushita Electric and [2]Research Center for Nano-Device and System, Nagoya Inst. of Technology, Japan*	**16:15 G-2-3** Multifunctional device by using a quantum dot array T. Kaizawa, T. Oya, M. Arita and Y. Takahashi, *Hokkaido Univ., Japan* **16:30 G-2-4** Multi-Charge Turnstile Operation in Random-Multidot Channel FET H. Ikeda and M. Tabe, *Shizuoka Univ., Japan*	**16:35 H-2-3** NeoFlash® - True Logic Based 0.18μm Single Poly Embedded SONOS Flash H. M. Lee[1], L. Lim[2], S. M. Jung[2], S. T. Woo[2], H. M. Chen[1], C. Y. Lin[1], R. Shen[1], C. D. Wang[2], C. C. H. Hsu[1] and S. C. Sun[2], *[1]eMemory Technology Inc. and [2]Chartered Semiconductor Manufacturing, Taiwan*	**16:15 I-2-3** Experimental Demonstration of Ideal Noise Shaping in Resonant Tunneling Delta-Sigma Modulator for High resolution, Wide Band A/D Converters K. Maezawa[1], M. Sakou[1], W. Matsubara[1], T. Mizutani[1] and H. Matsuzaki[2], *[1]Nagoya Univ. and [2]NTT, Japan*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
16:45 A-2-4 NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ ALD-TiN Gate Stacks S. A. Krishnan[1], M. Quevedo[2], R. Harris[3], P. D. Kirsch[4], R. Choi[1], B. H. Lee[4], G. Bersuker[1], J. Peterson[1], H. J. Li[5], C. Young[1] and J. C. Lee[6], *[1]International Sematech, [2]Texas Instruments, [3]AMD, [4]IBM, [5]Infineon and [6]Univ. of Texas at Austin, USA*	**16:45 B-2-4** Physical Origins of Surface Carrier Density Dependences of Interface- and Remote-Coulomb Scattering Mobility in Si MOS Inversion Layer Y. Nakabayashi[1], J. Koga[1], T. Ishihara[1] and S. Takagi[2], *[1]Toshiba Corp. and [2]Univ. of Tokyo, Japan*	**16:45 C-2-3** New Three-Dimensional Integration Technology Using Chip-to-Wafer Bonding to Achieve Ultimate Super Chip Integration T. Fukushima, Y. Yamada, H. Kikuchi and M. Koyanagi, *Tohoku Univ., Japan*	**16:45 D-2-4** Magnetic capture of a single magnetic nanoparticle using nano-electromagnets H. K. Kim[1], S. H. Hong[1], S. W. Hwang[1,2], J. S. Hwang[2], D. Ahn[2], S. Seong[3] and T. H. Park[3], *[1]Korea Univ., [2]Inst. of Quantum Information Processing and Systems and [3]Seoul National Univ., Korea*
17:05 A-2-5 Improvement in the asymmetric Vfb shift of poly-Si/HfSiON/Si by inserting oxygen diffusion barrier layers into the interfaces Y. Kamimuta, M. Koyama, T. Ino, K. Sekine, M. Sato, K. Eguchi, M. Takayanagi, M. Tomita and A. Nishiyama, *Toshiba Corp., Japan*	**17:05 B-2-5** Improvement of Mobility on Ultra-thin Body SOI MOSFETs by Use of High Pressure Hydrogen Annealing Y. Son, M. S. Rahman, K. Im, M. Chang, H. Park and H. Hwang, *Gwangju Inst. of Science and Technology, Korea*	**17:05 C-2-4** Characteristics of Silicon-on-Low-K Insulator (SOLK) MOSFET with Metal Back-Gate Y. Yamada, H. Oh, T. Sakaguchi, T. Fukushima and M. Koyanagi, *Tohoku Univ., Japan*	**17:00 D-2-5** Beam forming in solids with a microstructured surface J. Kapelewski and B. Lila, *Military Univ. of Technology, Poland*
17:25 A-2-6 Effects of Nitrogen Concentration and Post-treatment on Reliability of HfSiON Gate Dielectrics in Inversion States M. Sato, T. Aoyama, K. Sekine, T. Yamaguchi, I. Hirano, K. Eguchi and Y. Tsunashima, *Toshiba Corp., Japan*		**17:25 C-2-5 (Invited)** Integration Challenges for Carbon Nanotubes F. Kreupl, M. Liebau, R. Seidel, A. P. Graham, G. S. Duesberg and E. Unger, *Infineon, Germany*	

18:30-20:30 Banquet (PORTOPIA HOTEL Room KAIRAKU)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
16:45 E-2-4 MBE Growth and Characterization of InGaAsSbN Quantum Well Laser Diodes at 2 μm Wavelength Region grown on InP Substrates Y. Kawamura[1,2], T. Nakagawa[1] and N. Inoue[1], *[1]Osaka Prefecture Univ. and [2]CREST-JST, Japan*	**16:30 F-2-4** InGaN quantum wells with small potential fluctuation T. Akasaka, H. Gotoh, H. Nakano and T. Makimoto, *NTT Basic Research Labs., Japan*	**16:45 G-2-5** Artificial Dislocation Network in Silicon-on-Insulator Layer for Single-Electron Devices Y. Ishikawa, C. Yamamoto and M. Tabe, *Shizuoka Univ., Japan*	**16:55 H-2-4** Program Boosting with Local Short-Channel-Effect (LSCE) Unique to Charge Trapping Memory Using Hot-Carrier-Injection T. Kobayashi[1], H. Tomiye[1], O. Oka[1], H. Futai[2], S. Hara[1], K. Koyama[1] and T. Oda[1], *[1]Sony Corp. and [2]Sony Semiconductor Kyushu Corp., Japan*	**16:30 I-2-4** Novel Differential-Mode RTD/HBT MOBILE-based D-Flip Flop IC Y. Jeong, T. Kim and K. Yang, *KAIST, Korea*
17:00 E-2-5 High Power operation of GaN-based laser diode with high slope efficiency K. Kuramoto[1], A. Ohno[1], T. Yamada[2], H. Okagawa[2], Z. Kawazu[1], K. Kawasaki[1], N. Tomita[1], K. Shiozawa[1], K. Kanamoto[1], H. Watanabe[1], M. Takemi[1], T. Yagi[1], H. Murata[2] and A. Shima[1], *[1]Mitsubishi Electric Corp. and [2]Mitsubishi Cable Industries, Ltd., Japan*	**16:45 F-2-5** Triple Luminescence Peaks Observed in the InGaAsN/GaAs Single Quantum Well Grown by MOVPE W. C. Chen, Y. K. Su, R. W. Chuang and S. H. Hsu, *National Cheng Kung Univ., Taiwan*	**17:00 G-2-6** Characterization of MultiStep Electron Charging to Silicon-Quantum-Dot Floating Gate by Applying Pulsed Gate Biases T. Nagai, M. Ikeda, Y. Shimizu, S. Higashi and S. Miyazaki, *Hiroshima Univ., Japan*	**17:15 H-2-5** Data Retention Characteristics of MONOS Devices with High-*k* Dielectrics and High-work Function Metal-gates for Multi-gigabit Flash Memory J. S. Lee, C. S. Kang, Y. C. Shin, C. H. Lee, K. T. Park, J. S. Sel, V. Kim, B. I. Choe, J. S. Sim, J. Choi and K. Kim, *Samsung Electronics Co. Ltd., Korea*	**16:45 I-2-5** High-Speed Digital Circuits Using RTD as Load-Element H. Kim, S. Yeon, S. Song, S. Park and K. Seo, *Seoul National Univ., Korea*
17:15 E-2-6 High Power Operation of 660-nm Laser Diodes with a Long Cavity K. Shibata, H. Nishiguchi, Y. Yoshida, M. Sasaki, K. I. Ono, T. Yagi and A. Shima, *Mitsubishi Electric Corp., Japan*	**17:00 F-2-6** Growth and characteristics of GaNAs/GaAs MQW by molecular beam epitaxy K. Takao[1], K. Fujii[1], H. Miyagawa[1], N. Tsurumachi[1], H. Itoh[1], N. Sumida[1], S. Nakanishi[1], H. Akiyama[2] and S. Koshiba[1], *[1]Univ. of Kagawa and [2]Univ. of Tokyo, Japan*	**17:15 G-2-7** Studies on MOSFET Low-Frequency Noise for Electrometer Applications N. Clement, H. Inokawa and Y. Ono, *NTT Basic Research Labs., Japan*		**17:00 I-2-6** Low leakage gate current of InP transistors with hot electron extracted by attractive potential around i-InP/metal gate Y. Miyamoto[1,2], R. Nakagawa[1], I. Kashima[1], M. Ishida[1] and K. Furuya[1,2], *[1]Tokyo Tech and [2]CREST-JST, Japan*
17:30 E-2-7 Improvements in for N-Side-Up GaN/Mirror/Si LEDs Using High Reflective Ohmic Contacts S. H. Huang[1], D. S. Wuu[1,2], K. F. Pan[3] and R. H. Horng[3], *[1]National Chung Hsing Univ., [2]National Formosa Univ. and [3]National Chung Hsing Univ., Taiwan*		**17:30 G-2-8** Fowler-Nordheim current oscillations in Si(111)/SiO_2/twisted-Si(111) tunneling structures D. Moraru[1], H. Kato[1], S. Horiguchi[2], Y. Ishikawa[1], H. Ikeda[1] and M. Tabe[1], *[1]Shizuoka Univ. and [2]Akita Univ., Japan*		

18:30-20:30 Banquet (PORTOPIA HOTEL Room KAIRAKU)

Wednesday, September 14

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-3: High-k Gate Dielectric Stacks III
(9:15-10:15)
Chairs: J. Yugami (Renesas)
Y. Nara (Selete)

9:15 A-3-1
Dielectric Constant Behavior of Hf-O-N System
T. Ino, Y. Kamimuta, M. Suzuki, M. Koyama and A. Nishiyama, *Toshiba Corp., Japan*

9:35 A-3-2
Permittivity Enhancement of $Hf_{(1-x)}Si_xO_2$ Film with High Temperature Annealing
K. Tomida, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*

9:55 A-3-3
Thermal Stability Improvements for HfO_2 by Fluorine Implantation
C. S. Lai[1], W. C. Wu[2], J. C. Wang[3] and T. S. Chao[2], *[1]Chang Gung Univ. and [2]National Chiao Tung Univ., [3]Nanya Technology Corp., Taiwan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-3: Carrier Transport I
(9:15-10:15)
Chairs: H. C. Lin (National Chiao Tung Univ.)
M. Ogawa (Kobe Univ.)

9:15 B-3-1
Impact of The Improved High Performance Si(110) Oriented MOSFETs by Using Accumulation-Mode Fully Depleted SOI Devices
W. Cheng, A. Teramoto, M. Hirayama, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

9:35 B-3-2
Si Substrate Orientation Induced Worse Hot Carrier Degradation in Novel (110)/<111'> Oriented Devices
S. Chiang, M. F. Lu, Y. C. Liu, S. Huang-Lu, W. T. Shiau and S. C. Chien, *United Microelectronics Corp., Taiwan*

9:55 B-3-3
Device Design of High-Speed Source-Heterojunction-MOS-Transistors (SHOT) under 10-nm Regime
T. Mizuno[1,2] and S. Takagi[1,3], *[1]MIRAI-AIST, [2]Kanagawa Univ. and [3]Univ. of Tokyo, Japan*

Room 502 (C)

Room 503 (D)

Room 504 (E)

Area 7: Photonic Devices and Device Physics

E-3: Photonic Crystals and Light Control
(9:15-10:30)
Chairs: S. Noda (Kyoto Univ.)
M. Tokushima (NEC)

9:15 E-3-1
Design and Simulation of Ring Resonator Switches using Electro-Optic Materials
Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*

9:30 E-3-2
Optical Properties of Line-Defect Waveguides in Square-Lattice-of-Pillars Photonic Crystals for Optical Buffer Application
M. Tokushima, J. Ushida, A. Gomyo and K. Shinoda, *NEC Corp., Japan*

9:45 E-3-3
Highly Enhanced Speed and Efficiency of Si Nano-Photodiode with a Surface-Plasmon Antenna
J. Fujikata, T. Ishi, K. Makita, T. Baba and K. Ohashi, *NEC Corp., Japan*

Room 505 (F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-3: Nanostructure Fabrications
(9:15-10:30)
Chairs: S. Shimomura (Osaka Univ.)
H. Yamaguchi (NTT)

9:15 F-3-1 (Invited)
Quantum Dots, Quantum Dot Molecules and Quantum Dot Crystals
O. G. Schmidt[1], A Rastelli[1], S. Kiravittaya[1], L. Wang[1], M. Stoffel[1], G. J. Beirne[2], C. Hermannstaedter[2] and P. Micher[2], *[1]Max-Planck-Inst. fuer Festkoerperforschung and [2]Universitaet Stuttgart, Germany*

9:45 F-3-2
Formation of Germanium-Rich Nanodots by Selective Oxidation of An As-Deposited Thin Hydrogenated Amorphous Silicon-Germanium Layer
S. Y. Lo, P. J. Wu, R. H. Yeh and J. W. Hong, *National Central Univ., Taiwan*

10:00 F-3-3
Study of InGaN red emission multiple Quantum Dots
T. C. Wang[1], H. C. Kuo[2], C. E. Tsai[1], M. Y. Tsai[2], J. T. Hsu[1] and T. D. Lee[1], *[1]Industrial Technology Research Inst. and [2]National Chiao Tung Univ., Taiwan*

Room 401 (G)

Area 9: Physics and Applications of Novel Functional Materials and Devices

G-3: Quantum Information Devices
(9:15-10:30)
Chairs: T. Usuki (Fujitsu)
T. Fujisawa (NTT)

9:15 G-3-1 (Invited)
Probing Charge and Spin Excitations in Quantum Dots and Molecules
J. J. Finley, H. J. Krenner, E. Clark, M. Kroutvar, D. Heiss, S. Schäck, M. Bichler and G. Abstreiter, *Walter Schottky Inst., Germany*

9:45 G-3-2
Pulse Area Control of the Exciton Rabi Oscillation in InAs/GaAs Single Quantum Dot
K. Goshima[1,2], K. Komori[1,2], S. Yamauchi[1,2], I. Morohashi[1,2], A. Shikanai[1,2] and T. Sugaya[1,2], *[1]AIST and [2]CREST-JST, Japan*

10:00 G-3-3
Development of Electrically Driven Single-Photon Emitter at Optical Fiber Bands
T. Miyazawa[1], J. Tatebayashi[1], T. Nakaoka[1], M. Takatsu[1], S. Ishida[1], S. Iwamoto[1], K. Takemoto[2], S. Hirose[2], T. Usuki[2], N. Yokoyama[2] and Y. Arakawa[1], *[1]Univ. of Tokyo and [2]Fujitsu Labs. Ltd., Japan*

Room 402 (H)

Area 4: Advanced Memory Technology

H-3: SRAM
(9:15-10:15)
Chairs: C. Hsu (eMemory Tech.)
Y. Yamauchi (Sharp)

9:15 H-3-1
High Density and Ultra-Low Power Mobile SRAM Using the Novel Double S^3 (Stacked Single-crystal Silicon) Technology and KrF lithography
K. Kwak, W. Cho, J. Kim, J. Shim, H. Lim, J. Jeong, C. Hong, J. Kim, H. Cho, B. Choi, J. Kim, S. Kwon, S. M. Jung and K. Kim, *Samsung Electronics Co. Ltd., Korea*

9:35 H-3-2
Highly Reliable and Manufacturable Low-Temperature Plasma Assisted Oxidation for High Density SRAM with Double Stacked Cell Structure
C. S. Kim, Y. J. Noh, J. H. Kim, B. Y. Koo, J. H. Heo, D. C. Kim, Y. G. Shin, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*

9:55 H-3-3
Technology Trend of Soft Errors based on Accurate Estimation Method
Y. Tosaka[1], R. Takasu[1], H. Ehara[2], T. Uemura[1], H. Oka[1], S. Satoh[1], N. Matsuoka[3] and K. Hatanaka[3], *[1]Fujitsu Labs. Ltd., [2]Fujitsu Ltd. and [3]Osaka Univ., Japan*

Room 403 (I)

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)

Break

Area 1: Advanced Gate Stack / Si Processing Science

A-4: Characterization of Gate Dielectrics
(10:45-12:15)
Chairs: H. Satake (ASET)
K. Shiraishi (Univ. of Tsukuba)

10:45 A-4-1 (Invited)
Nanoscale Observations for Degradation Phenomena in SiO_2 and High-k Gate Insulators using Conductive-Atomic Force Microscopy
S. Zaima, A. Seko, M. Sakashita, H. Kondo, A. Sakai and M. Ogawa, *Nagoya Univ., Japan*

11:15 A-4-2
A novel inversion pulse measurement technique to investigate transient charging characteristics in high-k NMOS transistors
R. Choi[1], B. H. Lee[2], H. K. Park[3], C. D. Young[1], J. H. Sim[1], S. C. Song[1] and G. Bersuker[1], *[1]International Sematech, [2]IBM and [3]GIST, USA*

Area 3: CMOS Devices / Device Physics

B-4: Carrier Transport Modeling
(10:45-12:05)
Chairs: M. Ogawa (Kobe Univ.)
K. Kurimoto (Matsushita Electric)

10:45 B-4-1
Effects of Electron-Phonon Interaction on Transport Characteristics of Sub-10-nm Bulk-MOSFETs
H. Takeda and N. Mori, *Osaka Univ., Japan*

11:05 B-4-2
Suppression of the rebound of hot-electrons from the drain region in ballistic transport due to device geometry: A Monte Carlo study
T. Kurusu and K. Natori, *Univ. of Tsukuba, Japan*

Short Presentation P1, P2 and P4
(10:30-12:15)
Chair: H. Matsuoka (Hitachi)

Short Presentation P6, P7, P8 and P9
(10:30-12:15)
Chair: Y. Hirayama (NTT)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)

10:00 E-3-4 (Invited)
Slow Light Using Semiconductor Quantum Wells and Quantum Dots for Future Optical Networks
S. L. Chuang, S. W. Chang and H. Su, *Univ. of Illinois at Urbana Champaign, USA*

10:15 F-3-4
Selective Formation of Self-Organized InAs QDs on Patterned GaAs Substrates by Molecular Beam Epitaxy
A. Ueta[1], K. Akahana[1], S. Gozu[1], N. Yamamoto[1] and N. Ohtani[2], *[1]National Inst. of Information and Communications Technology and [2]Doushisya Univ., Japan*

10:15 G-3-4
Real-time observation of charge state transitions in a double quantum dot
T. Hayashi[1], T. Fujisawa[1,2], R. Tomita[2] and Y. Hirayama[1,3], *[1]NTT Basic Research Labs., [2]Tokyo Tech and [3]SORST-JST, Japan*

Break

Area 7: Photonic Devices and Device Physics

E-4: Si Photonics and Optical Interconnects
(10:45-12:15)
Chairs: M. Tokushima (NEC)
M. Ezaki (Toshiba)

10:45 E-4-1
Novel Laser Diode Structure consisting of a Si Waveguide and Compound-Semiconductor MQW layers for Si Platform Integration
S. Kodama[1,2], H. Park[1], A. Fang[1] and J. E. Bowers[1], *[1]Univ. of California Santa Barbara and [2]NTT, Japan*

11:00 E-4-2
Electroluminescence from MOS Capacitors with Si Implanted Oxide on p-type and n-type Si Substrate
T. Matsuda[1], T. Ibe[1], K. Nishihara[1], H. Iwata[1], S. Iwatsubo[2] and T. Ohzone[3], *[1]Toyama Prefectural Univ., [2]Toyama Industrial Technology Center and [3]Okayama Prefectural Univ., Japan*

Area 8: Advanced Material Synthesis and Crystal Growth Technology

F-4: Si and Related Materials
(10:45-12:15)
Chairs: O. G. Schmidt (Max-Planck-Inst.)
S. Miyazaki (Hiroshima Univ.)

10:45 F-4-1
Creation of Strained and Relaxed SiGe films simultaneously through Ge condensation on SOI
M. Mukherjee-Roy, A. Agarwal, C. H. Tung, R. Kumar, L. K. Bera, N. Balasubramanian and D. L. Kwong, *Inst. of Microelectronics, Singapore*

11:00 F-4-2
A Novel Approach to fabricate High Ge content SiGe on Insulator from Amorphous SiGe deposited on SOI wafers
S. Balakumar[1]. F. Gao[1,2], S. J. Lee[2], C. H. Tung[1], R. Kumar[1], T. Sudhiranjan[3], Y. L. Foo[3], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics, [2]National Univ. of Singapore and [3]Inst. of Materials Research and Engineering, Singapore*

Area 9: Physics and Applications of Novel Functional Materials and Devices

G-4: Novel Devices I
(10:45-12:00)
Chairs: K. Ishibashi (RIKEN)
H. Mizuta (Tokyo Tech)

10:45 G-4-1
Acoustic Emission Characteristics of Nanocrystalline Porous Silicon Device Driven as an Ultrasonic Speaker
K. Tsubaki[1], T. Komoda[1] and N. Koshida[2], *[1]Matsushita Electric and [2]Tokyo Univ. of Agriculture and Technology, Japan*

11:00 G-4-2
Superconducting Proximity Effect on Piezoresistance in a Superconductor-Semiconductor Junction
H. Okamoto[1], T. Akazaki[1], M. Ueki[2] and H. Yamaguchi[1], *[1]NTT Basic Research Labs. and [2]NTT Electronics Techno Corp., Japan*

Area 4: Advanced Memory Technology

H-4: Flash Memory II
(10:45-11:45)
Chairs: Y. Yamauchi (Sharp)
T. Kobayashi (Hitachi)

10:45 H-4-1
Feasibility analysis of direct tunneling through medium-κ dielectrics for embedded RAM applications
B. Govoreanu[1], R. Degraeve[1], T. Kauerauf[1,2], W. Magnus[1], D. Wellekens[1], G. Groeseneken[1,2] and J. V. Houdt[1], *[1]IMEC and [2]Katholieke Univ. Leuven, Belgium*

11:05 H-4-2
Impact of Vth interference suppression using a novel Poly Si shield on FLASH memories.
T. Fukumura, S. Shimizu, Y. Ikeda, M. Shimizu, M. Fujinaga, K. Ishikawa, F. Ohta, A. Fukasawa, T. Yoshitake, K. Hirao, O. Tsuchiya and Y. Ohji, *Renesas Technology Corp., Japan*

Short Presentation P3, P5, P10 and P11
(10:30-12:15)
Chair: T. Ichiki (Univ. of Tokyo)

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
11:35 A-4-3 Evidence of Electrical and Structural Evolution of Gate Dielectric Breakdown Observed by Conductive Atomic Force Microscopy L. Zhang and Y. Mitani, *Toshiba Corp., Japan*	**11:25 B-4-3** A First Principles Study on Electronic Band Structures of Nano-Scaled SOI Films Y. Teratani, T. Ando, H. Tsuchiya and T. Miyoshi, *Kobe Univ., Japan*		
11:55 A-4-4 Characterization of Novel HfTiO Gate Dielectrics Post-treated by NH_3 Plasma and Ultra-violet Rays J. C. Wang[1], W. C. Wu[2], C. S. Lai[3], J. W. Lee[4], K. C. Chiang[2], D. C. Shie[2], T. F. Lei[2] and C. L. Lee[2], *[1]Nanya Technology Corp., [2]National Chiao Tung Univ., [3]Chang Gung Univ. and [4]National Nano Device Labs., Taiwan*	**11:45 B-4-4** Development of Electric Conductivity Simulator Based on Tight-Binding Quantum Chemical Molecular Dynamics H. Tsuboi[1], H. Setogawa[1], M. Koyama[1], A. Endou[1], M. Kubo[1,2], E. Broclawik[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO-JST, Japan*		

Lunch

13:00–15:00 Poster Session (Reception Hall, 3F)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
11:15 E-4-3 Investigation of β-$FeSi_2$/Si Heterostructures by Photoluminescence with Different Optical Configurations Y. Terai[1], Y. Maeda[2], K. Akiyama[3] and Y. Fujiwara[1], *[1]Osaka Univ., [2]Kyoto Univ. and [3]Kanagawa Industrial Technology Research Inst., Japan*	**11:15 F-4-3** Influence of H_2/SiH_4 Ratio on the Deposition Rate and Morphology of Polycrystalline Silicon Films Deposited by Atmospheric Pressure Plasma CVD H. Ohmi[1], H. Kakiuchi[1], K. Yasutake[1], Y. Nakahama[2], Y. Ebata[2], Y. Kumayasu[1] and Y. Mori[1], *[1]Osaka Univ. and [2]Sharp, Japan*	**11:15 G-4-3** Room Temperature Electroluminescence of CdF_2/CaF_2 Inter-sub-band Transition Laser Structures grown on Si Substrate K. Jinen[1], T. Kikuchi[1], M. Watanabe[1,2] and M. Asada[1,3], *[1]Tokyo Tech, [2]SORST-JST and [3]CREST-JST, Japan*	**11:25 H-4-3** Highly Reliable 256Mb NOR Flash MLC with Self-Aligned Process and Controlled Edge Profile W. H. Kwon[1], J. I. Han[1], B. Kim[2], C. K. Baek[2], S. P. Sim[1], W. H. Lee[1], J. H. Han[1], C. Jung[1], H. K. Lee[1], Y. K. Jang[1], J. H. Park[1], D. M. Kim[2], C. K. Park[1] and K. Kim[1], *[1]Samsung Electronics Co. Ltd. and [2]Korea Inst. for Advanced Study, Korea*	
11:30 E-4-4 Fabrication of spin-coat optical waveguides for optically interconnected LSI and influence of fabrication process on lower layer MOS capacitors T. Tabei[1], K. Maeda[2], S. Yokoyama[1] and H. Sunami[1], *[1]Hiroshima Univ. and [2]Central Glass Co.,LTD, Japan*	**11:30 F-4-4** Epitaxial Growth of Ferromagnetic Silicide Fe_3Si on Si (111) Substrate T. Sadoh, H. Takeuchi, K. Ueda, A. Kenjo and M. Miyao, *Kyushu Univ., Japan*	**11:30 G-4-4** Electroluminescence of Oxygen Deficient $YAlO_3$ Crystals M. Ando[1], T. Sakaguchi[1], A. Yamanaka[2], Y. Kawabe[2] and E. Hanamura[2], *[1]CREST-JST and [2]Chitose Inst. of Science & Technology & CREST-JST, Japan*		
11:45 E-4-5 Multi-Chip Shared-Memory Module with Optical Interconnection for Parallel Processor System H. Kuribara, H. Hashimoto, T. Fukushima and M. Koyanagi, *Tohoku Univ., Japan*	**11:45 F-4-5** Nanoporous Ultra Low-k Dielectrics Prepared with Covalently Bonded Adamantylphenol Pore Generators B. J. Cha, S. Kim and K. Char, *Seoul National Univ., Korea*	**11:45 G-4-5** Resonant terahertz photomixing in integrated HEMT-QWIP device V. Ryzhii[1], M. Ryzhii[1], I. Khmyrova[1], T. Otsuji[2] and M. S. Shur[3], *[1]Univ. of Aizu, [2]Tohoku Univ. and [3]Rensselaer Polytechnic Inst, Japan*		
12:00 E-4-6 A 51,272-gate-count Dynamic Optically Reconfigurable Gate Array in a standard 0.35μm CMOS Technology M. Watanabe and F. Kobayashi, *Kyushu Inst. Of Technology, Japan*	**12:00 F-4-6** Surface Hall Potentiometry to Characterize Functional Semiconductor Films K. Arima, K. Hiwa, R. Nakaoka and M. Morita, *Osaka Univ., Japan*			

Lunch

13:00–15:00 Poster Session (Reception Hall, 3F)

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-5: Characterization & Reliability of Gate Dielectrics
(15:15-16:35)
Chairs: S. Miyazaki (Hiroshima Univ.)
B. Mizuno (UJT Lab.)

15:15 A-5-1
Thermal Degradation of HfSiON Dielectrics Caused by TiN Gate Electrodes and Its Impact on Electrical Properties
H. Watanabe[1], S. Yoshida[1], Y. Watanabe[1], T. Shimura[1], K. Yasutake[1], Y. Akasaka[2], Y. Nara[2], K. Nakamura[2] and K. Yamada[3], *[1]Osaka Univ., [2]SELETE and [3]Waseda Univ., Japan*

15:35 A-5-2
Local Current Leakage Characterization in La_2O_3-Al_2O_3 Composite Films by Conductive Atomic Force Microscopy
A. Seko, T. Sago, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*

15:55 A-5-3
Importance of Leakage Current *Noise* Analysis for Accurate Lifetime Prediction of High-k Gate Dielectrics
K. Okada[1], H. Ota[2], T. Horikawa[2], Y. Tamura[3], T. Sasaki[3], T. Aoyama[3], F. Ootsuka[3] and A. Toriumi[2,4], *[1]MIRAI-ASET, [2]MIRAI-ASRC-AIST, [3]SELETE and [4]Univ. of Tokyo, Japan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-5: Advanced CMOS Technology II
(15:15-16:45)
Chairs: K. Ohuchi (Toshiba)
D. Hisamoto (Hitachi)

15:15 B-5-1 (Invited)
Perspective on Emerging Devices and their Impact on Scaling Technologies
S. Biesemans, *IMEC, Belgium*

15:45 B-5-2
Investigation of N-Channel Triple-Gate MOSFETs on (100) SOI Substrate
K. Endo, M. Masahara, Y. Liu, T. Matsukawa, K. Ishii, E. Sugimata, H. Takashima, H. Yamauchi and E. Suzuki, *AIST, Japan*

16:05 B-5-3
A Surrounding-Gate Transistor with Multi-Pillar Silicon Channels
J. Park and J. C. S. Woo, *Univ. of California Los Angeles, USA*

Room 502 (C)

Area 2: Characterization and Materials Engineering for Device Integration

C-5: Characterization
(15:15-16:45)
Chairs: N. Hata (AIST)
F. Mizuno (Meisei Univ.)

15:15 C-5-1 (Invited)
Nano-meter order Structures of Porous Low-k Films and their Impacts on Cu/Low-k Processes
M. Shimada[1], J. Shimanuki[2], Y. Otsuka[3], T. Harada[3], Y. Inoue[2] and S. Ogawa[1], *[1]SELETE, [2]NISSAN ARC, Ltd. and [3]Toray Research Center, Japan*

15:45 C-5-2
Comparison of Pore Shape Models for Small Angle X-ray Scattering of a Disordered Porous Silica Low-*k* Film
N. Kunishige[1], N. Hata[1,2], N. Fujii[3] and T. Kikkawa[2,4], *[1]AIST, [2]MIRAI-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*

16:05 C-5-3
Adsorption in-situ Spectroscopic Ellipsometry Analysis of Disordered Porous Silica Low-*k* Films
X. Li[1], N. Fujii[2], N. Hata[1,3] and T. Kikkawa[3,4], *[1]AIST, [2]MIRAI-ASET, [3]MIRAI-AIST and [4]Hiroshima Univ., Japan*

Room 503 (D)

Area 5: Advanced Circuits and Systems

D-5: Antennas and Sensor
(15:15-16:35)
Chairs: K. Masu (Tokyo Tech)
R. Fujimoto (Toshiba)

15:15 D-5-1
An SOI-CMOS Active Magnetic Probe for High-Frequency Electromagnetic Emissions
S. Aoyama[1], S. Kawahito[1], T. Yasui[2] and M. Yamaguchi[2], *[1]Shizuoka Univ. and [2]Tohoku Univ., Japan*

15:35 D-5-2
Integration of 0.45-mm^2 On-Chip-Antenna (OCA) with High Output Power for 2.45GHz RFID Tag
L. H. Guo, H. Y. Li, A. P. Popov, Y. B. Choi, Y. H. Wang, V. Bliznetsov, W. G. Yeoh, G. Q. Lo, N. Balasubramanian and D. L. Kwong, *Inst. of Microelectronics, Singapore*

15:55 D-5-3
Analysis of Transmission Characteristics of Gaussian Monocycle Pulse for Silicon Integrated Antennas
K. Kimoto, N. Sasaki, P. K. Saha, M. Nitta, T. Kikkawa and M. Sasaki, *Hiroshima Univ., Japan*

Room 504 (E)

Area 7: Photonic Devices and Device Physics

E-5: Detectors and Sensors I
(15:15-16:45)
Chairs: T. Hatta (Mitsubishi Electric)
K. Komori (AIST)

15:15 E-5-1
Active Pixel Sensor Using a PMOSFET-Type Photodetector with a Transfer Gate for Variable Photosensitivity
S. H. Seo, S. H. Lee, M. Y. Do, J. K. Shin and P. Choi, *Kyungpook National Univ., Korea*

15:30 E-5-2
Reduction of Random Noise for CMOS Image Sensors with 22μmx2.2μm Pixel
J. Jung, J. Lyu, H. Y. Kim, H. Lee, J. Song, Y. You, H. Noh, D. Lee and K. Kim, *Samsung Electronics Co. Ltd., Korea*

15:45 E-5-3
Improved Efficiency-Bandwidth Product of Modified Uni-Traveling Carrier Photodiode Structures Utilizing an Undoped Photo-Absorption Layer
D. H. Jun[1], J. H. Jang[1], I. Adesida[2] and J. I. Song[1], *[1]Gwangju Inst. of Science and Technology and [2]Univ. of Illinois at Urbana Champaign, Korea*

Room 505 (F)

Area 10: Organic Materials Science, Device Physics, and Applications

F-5: Molecular Electronics and Physics I
(15:15-16:45)
Chairs: K. Kudo (Chiba Univ.)
Y. Ohmori (Osaka Univ.)

15:15 F-5-1 (Invited)
Recent Progress of Organic Transistor Integrated Circuits for Large-Area Sensor Applications
T. Someya, T. Sakurai, T. Sekitani, H. Kawaguchi, S. Iba, Y. Kato and Y. Noguchi, *Univ. of Tokyo, Japan*

15:45 F-5-2
Effects of CsF/Metal Cathode Interface on Electron Injection in Organic Light-Emitting Diodes Fabricated by Wet-Process
Z. Kin[1], K. Yoshihara[2], H. Kajii[1], K. Hayashi[2] and Y. Ohmori[1], *[1]Osaka Univ. and [2]Kinki Univ., Japan*

16:00 F-5-3
Electrical bistability of organic thin-film devices using Ag electrode
M. Terai, K. Fujita and T. Tsutsui, *Kyushu Univ., Japan*

Room 401 (G)

Area 9: Physics and Applications of Novel Functional Materials and Devices

G-5: Novel Devices II
(15:15-16:45)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Takahashi (Hokkaido Univ.)

15:15 G-5-1
Fabrication of Defect-Free Sub-10 nm Si Nanocolumn for Quantum Effect Devices Using Cl Neutral Beam Process
T. Kubota[1], J. K. Chen[1], Y. Uraoka[2], T. Fuyuki[2], I. Yamashita[2,3], S. Yamasaki[4] and S. Samukawa[1], *[1]Tohoku Univ., [2]Nara Inst. of Science and Technology, [3]Matsushita Electric and [4]AIST, Japan*

15:30 G-5-2
Effect of ion diffusion on switching voltage of solid-electrolyte nanometer switch
N. Banno[1,2], T. Sakamoto[1,2], T. Hasegawa[2,3], K. Terabe[2,3] and M. Aono[2,3], *[1]NEC Corp., [2]JST and [3]NIMS, Japan*

15:45 G-5-3
Temperature dependence of Space Charge Limited Current (SCLC) in thin films of silicon nanocrystals
M. A. Rafiq[1], Y. Tsuchiya[2], H. Mizuta[2], S. Uno[3], Z. A. K. Durrani[1] and W. I. Milne[1], *[1]Univ. of Cambridge, [2]Tokyo Tech and [3]Hitachi Cambridge Lab., UK*

Room 402 (H)

Area 11: Micro / Nano Electromechanical and Bio-Systems

H-5: Bio Sensors and Chips I
(15:15-16:45)
Chairs: H. Tabata (Osaka Univ.)
H. Sugihara (Matsushita Electric)

15:15 H-5-1 (Invited)
Bionanotechnology with Membrane Proteins: Mechanics and Electronics
S. A. Contera[1], K. Voïtchovsky[1], H. Hamnett[1], C. S. Ramanujan[1], N. Toledo[1], V. Lemaître[1], M. de. Planque[1], A. Watts[1], K. Sumitomo[2], K. Torimitsu[2] and J. F. Ryan[1], *[1]Univ. of Oxford and [2]NTT Corp., UK*

15:45 H-5-2
High-throughput Screening of Mutant Biomolecules Using mRNA Display and Microreactor Array Chips
Y. Hosoi[1], K. Takahashi[1], M. Biyani[2], N. Nemoto[3], T. Akagi[1] and T. Ichiki[1,4], *[1]Univ. of Tokyo, [2]Saitama Small Enterprise Promotion Corp., [3]AIST and [4]PRESTO-JST, Japan*

16:00 H-5-3
Immobilization of DNA Probes onto Gold Surface and its Application for a Fully Electric Detection of DNA Hybridization by Field Effect Transistor Sensor
Y. Ishige[1], M. Shimoda[2] and M. Kamahori[1], *[1]Central Research Lab., Hitachi, Ltd. and [2]Hitachi ULSI Systems Co., Ltd., Japan*

Room 403 (I)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

I-5: Nitride Devices
(15:15-16:45)
Chairs: T. Hashizume (Hokkaido Univ.)
T. Enoki (NTT)

15:15 I-5-1 (Invited)
Characterization of AlGaN/GaN HFETs on a Si Substrate Grown
T. Egawa, *Nagoya Inst. of Technology, Japan*

15:45 I-5-2
Normally-off Operation of Non-polar AlGaN/GaN Heterojunction FETs Grown on R-plane Sapphire
M. Kuroda, H. Ishida, T. Ueda and T. Tanaka, *Matsushita Electric, Japan*

16:00 I-5-3
AlGaN/GaN HEMTs with inclined-gate-recess structure
Y. Aoi, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, *Nagoya Univ., Japan*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
16:15 A-5-4 Reliable Extractions of EOT and V_{fb} in Poly-Si Gate High-k MISFETs through Advanced Modeling of Gate and Substrate Capacitances N. Yasuda[1], H. Ota[2], T. Horikawa[2], T. Nabatame[1], H. Satake[1], A. Toriumi[2,3], Y. Tamura[4], T. Sasaki[4] and F. Ootsuka[4], *[1]MIRAI-ASET, [2]MIRAI-ASRC-AIST, [3]Univ. of Tokyo and [4]SELETE, Japan*	**16:25 B-5-4** Analytical model for subband engineering in undoped double gate MOSFETs M. Ferrier[1,2], R. Clerc[1], G. Panakakis[1], G. Ghibaudo[1], F. Boeuf[2] and T. Skotnicki[2], *[1]Lab. IMEP and [2]STMicroelectronics, France*	**16:25 C-5-4** Width Scaling and Layout Variation Effects on Dual Damascene Copper Interconnects Electromigration M. H. Lin[1,2], K. P. Chang[2], K. C. Su[2] and T. Wang[1], *[1]National Chiao Tung Univ. and [2]United Microelectronics Corp., Taiwan*	**16:15 D-5-4** A 2.4 GHz Differential Wavelet Generator in 0.18 µm CMOS for 1.4 Gbps UWB Impulse Radio in Wireless Inter/Intra-Chip Data Communication P. K. Saha, N. Sasaki and T. Kikkawa, *Hiroshima Univ., Japan*

Break

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
16:00 E-5-4 A Bias-Dependent Equivalent-Circuit Model of High Performance Evanescently Coupled Photodiode with Partially P-Doped Absorption Layer Y. S. Wu, D. M. Lin, F. H. Huang, W. Y. Chiu, J. W. Shi and Y. J. Chan, *National Central Univ., Taiwan*	**16:15 F-5-4** Memory Effect of Device Based on a Conjugated Donor-Acceptor Copolymer Y. Song[1], Q. Ling[1], C. Zhu[1], E. T. Kang[1], S. H. Chan[1], Y. Wang[2] and D. L. Kwong[2], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*	**16:00 G-5-4** Temperature dependent characteristics of diamond MESFET H. Ye, M. Kasu, Y. Yamauchi, N. Maeda, S. Sasaki and T. Makimoto, *NTT, Japan*	**16:15 H-5-4** Silicon-Nitride-Coated Silicon Biochip for Real-time Optical Sensing of Biomolecular Interaction T. Fujimura, S. Taniguchi, K. Takenaka and Y. Goto, *Hitachi, Ltd., Japan*	**16:15 I-5-4** Novel quaternary AlInGaN/GaN HFET grown by MOCVD on sapphire substrate Y. Liu, T. Egawa, H. Jiang and H. Ishikawa, *Nagoya Inst. of Technology, Japan*
16:15 E-5-5 Heterojunction Bipolar Phototransistor with Monolithic Integrated Microlens S. J. Cho, J. Kim, S. H. Shin, H. Y. Yang and Y. S. Kwon, *KAIST, Korea*	**16:30 F-5-5** Spectroscopy of Photocurrent Transients to Study Polaron states in the HOMO-LUMO Gap of MEH-PPV G. S. Samal, S. Nandi, S. P. Singh and Y. N. Mohapatra, *Indian Inst. of Technology Kanpur, India*	**16:15 G-5-5** High frequency gate bias response of carbon nanotube field effect transistor S. H. Hong[1], H. T. Kim[1], H. K. Kim[1,2], M. G. Kang[1], J. S. Hwang[2], G. T. Kim[1], S. W. Hwang[1,2] and D. Ahn[2], *[1]Korea Univ. and [2]Univ. of Seoul, Korea*	**16:30 H-5-5** DNA Immobilization on Au/Sapphire Substrate Patterned by Nanolithography S. Horiike, Y. Oikawa and T. Nishimoto, *Shimadzu Corp., Japan*	**16:30 I-5-5** Barrier Height Enhancement of AlGaN/GaN Schottky Diodes by $P_2S_5/(NH_4)_2S_x$ Surface Treatments L. B. Chang[1], M. J. Jeng[2], C. H. Chang[3], L. Z. Hsieh[3] and P. Y. Kuei[3], *[1]Chang Gung Univ., [2]St Johns and St Marys Inst. of Technology and [3]Chung-Cheng Inst. of Technology, Taiwan*
16:30 E-5-6 Nitride-based p-i-n photodetectors with ITO p-contacts T. K. Ko[1], S. J. Chang[1], Y. K. Su[1], Y. Z. Chiou[2], C. S. Chang[1], S. C. Shei[3], W. S. Chen[1] and C. F. Shen[1], *[1]National Cheng Kung Univ., [2]Southern Taiwan Univ. of Technology and [3]South Epitaxy Corp., Taiwan*		**16:30 G-5-6** Phonon Limited Electron Transport In SOI and Double-Gate MOSFETs Incorporating Realistic Acoustic Phonon Waves S. Uno[1] and N. Mori[2], *[1]Claremont Graduate Univ. and [2]Osaka Univ., USA*		

Break

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
Area 1: Advanced Gate Stack / Si Processing Science	**Area 3: CMOS Devices / Device Physics**	**Area 2: Characterization and Materials Engineering for Device Integration**	**Area 5: Advanced Circuits and Systems**
A-6: Alternative high-k gate dielectrics (17:00-18:00) Chairs: H. Hwang (Gwangju Inst. of Sci. & Tech.) Y. Tsunashima (Toshiba)	B-6: Device Modeling (17:00-18:00) Chairs: J. C. S. Woo (UCLA) Y. Momiyama (Fujitsu)	C-6: Device Integration II (17:00-18:00) Chairs: T. Tatsumi (Sony) M. Matsuura (Renesas)	D-6: Advanced System LSIs (17:00-18:10) Chairs: M. Mizuno (NEC) H. Yamauchi (Sanyo Electric)
17:00 A-6-1 A New Hf-based Dielectric Member, HfLaOx, for Amorphous High-k Gate Insulators in Advanced CMOS Y. Yamamoto, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*	**17:00 B-6-1** MOSFET Harmonic Distortion up to the Cutoff Frequency: Measurement and Theoretical Analysis Y. Takeda[1], D. Navarro[1], S. Chiba[1], T. Ezaki[1], M. Miura-Mattausch[1], H. J. Mattausch[1], T. Ohguro[2], T. Iizuka[2], M. Taguchi[2], S. Kumashiro[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]Semiconductor Technology Academic Research Center, Japan*	**17:00 C-6-1** Comparison between UV and EB cure method for porous PAr / porous MSX hybrid structure K. Fujita, H. Miyajima, S. Nakao, T. Sakanaka, R. Nakata, H. Yano and T. Yoda, *Toshiba Corp., Japan*	**17:00 D-6-1 (Invited)** Design and Architecture Exploration for Image and Video Coding Systems C. T. Huang and L. G. Chen, *National Taiwan Univ., Taiwan*
17:20 A-6-2 Design Methodology for La_2O_3-Based Ternally Higher-κ Dielectrics K. Kita, Y. Zhao, Y. Yamamoto, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*	**17:20 B-6-2** Modeling of Body Factor and Subthreshold Swing in Short Channel Bulk MOSFETs A. Tamsir, M. Saitoh, G. Tsutsui and T. Hiramoto, *Univ. of Tokyo, Japan*	**17:20 C-6-2** Via-Profile Controlled, Porous Low-k/ Cu DDIs with High Thermal Stability H. Ohtake, S. Saito, M. Tagami, M. Tada, M. Abe, N. Furutake and Y. Hayashi, *NEC Corp., Japan*	
17:40 A-6-3 Film structures and electrical properties of Pr silicate formed by pulsed laser deposition K. Ariyoshi, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*	**17:40 B-6-3** Capacitance Due to the Charge Layer Thickness in Nanoscale Capacitors K. Natori, M. Oniki, T. Kurusu and T. Shimizu, *Univ. of Tsukuba, Japan*	**17:40 C-6-3** Comparative Studies of Pore Seal Films for Porous-Silica / Cu Interconnect Y. Shishida[1], S. Chikaki[1], M. Shimoyama[1], R. Yagi[1], T. Yoshino[2], T. Ono[1], A. Ishikawa[1], N. Fujii[1], T. Nakayama[1], K. Kohmura[1], H. Tanaka[1], J. Kawahara[1], Y. Sonoda[1], H. Matsuo[1], S. Hishiya[1], T. Yamanishi[1], K. Kinoshita[1] and T. Kikkawa[2,3], *[1]MIRAI-ASET, [2]MIRAI-AIST and [3]Hiroshima Univ., Japan*	**17:30 D-6-2** A Memory-Based Programmable Logic Device Using a Look-Up Table Cascade with Synchronous SRAMs K. Nakamura[1], T. Sasao[1], M. Matsuura[1], K. Tanaka[1], K. Yoshizumi[1], H. Nakahara[1] and Y. Iguchi[2], *[1]Kyushu Inst. of Technology and [2]Meiji Univ., Japan*

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
Area 7: Photonic Devices and Device Physics	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 9: Physics and Applications of Novel Functional Materials and Devices**	**Area 11: Micro / Nano Electromechanical and Bio-Systems**	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**
E-6: Detectors and Sensors II (17:00-17:45) Chairs: Y. Lee (Hitachi) T. Hatta (Mitsubishi Electric)	F-6: Molecular Electronics and Physics II (17:00-18:15) Chairs: K. Kato (Niigata Univ.) M. Iwamoto (Tokyo Tech)	G-6: Spintronics (17:00-18:00) Chairs: Y. Ohno (Tohoku Univ.) J. Motohisa (Hokkaido Univ.)	H-6: Bio Sensors and Chips II (17:00-18:15) Chairs: H. Oana (Univ. of Tokyo) T. Nishimoto (Shimadzu)	I-6: Nitride Devices (17:00-18:00) Chairs: T. Hashizume (Hokkaido Univ.) T. Enoki (NTT)
17:00 E-6-1 Schottky-barrier diamond photodiode using thermally stable WC-based contacts M. Liao, J. Alvarez and Y. Koide, *NIMS, Japan*	**17:00 F-6-1** Photocarrier Generation in Organic Thin Film Solar Cells T. Osasa, S. Yamamoto and M. Matsumura, *Osaka Univ., Japan*	**17:00 G-6-1 (Invited)** Spin Hall Effect in a Two Dimensional Spin-Orbit Coupled Semiconductor System J. Wunderlich[1], B. Kaestner[2], K. Nomura[3], J. Sinova[4], A. H. MacDonald[3] and T. Jungwirth[5,6], *[1]Hitachi Cambridge Lab., [2]National Physical Lab., [3]Univ. of Texas at Austin, [4]Texas A&M Univ., [5]Inst. of Physics ASCR and [6]Univ. of Nottingham, UK*	**17:00 H-6-1 (Invited)** Integrated Microfluidic Systems for Cell and Tissue Engineering T. Fujii, *Univ. of Tokyo, Japan*	**17:00 I-6-1** Gamma Radiation Effects on the Ohmic Contact of AlGaN/GaN HEMTs J. P. Ao[1], R. Kan[1], T. Hirao[2], H. Okada[1], M. Okada[1], D. Kikuta[1], S. Onoda[2], H. Itoh[2] and Y. Ohno[1], *[1]Univ. of Tokushima and [2]Japan Atomic Energy Research Inst., Japan*
17:15 E-6-2 Fabrication of GaAs/GaInNAs Heterojunction Solar Cells Applicable To High-Efficiency Multi-junction Tandem Structures N. Kobayashi[1], N. Miyashita[1], Y. Shimizu[1], Y. Okada[1] and M. Yamaguchi[2], *[1]Univ. of Tsukuba and [2]Univ. of Toyota Technological Inst., Japan*	**17:15 F-6-2** Study of the transient electroluminescence process using organic light-emitting diodes with a partial doping layer H. Kajii, K. Takahashi, J. S. Kim and Y. Ohmori, *Osaka Univ., Japan*			**17:15 I-6-2** High-Temperature Operation Over 500°C of Pnp AlGaN/GaN HBTs K. Kumakura and T. Makimoto, *NTT Basic Research Labs., Japan*
17:30 E-6-3 Quick Response Observed in Solid-State Electrochromic Device with an Interfacial Barrier Structure H. Yoshimura and N. Koshida, *Tokyo Univ. of Agriculture and Technology, Japan*	**17:30 F-6-3** Surface Plasmon Excitation and Emitted Light Properties in Otto/Kretschmann Configuration K. Shinbo, T. Yamamoto, Y. Shimizu, Y. Ohdaira, K. Kato and F. Kaneko, *Niigata Univ., Japan*	**17:30 G-6-2** Velocity Measurements of Magnetic Domain Wall by Local Hall Effect Y. Sekine[1] and J. Nitta[1,2], *[1]NTT Basic Research Labs. and [2]CREST-JST, Japan*	**17:30 H-6-2** Intelligent Neural Implant Microsystem Fabricated Using Multi-Chip Bonding Technique T. Watanabe, K. Motonami, K. Sakamoto, J. Deguchi, R. Kobayashi, K. Komiya, K. Okumura, T. Fukushima, H. Kurino, H. Mushiake and M. Koyanagi, *Tohoku Univ., Japan*	**17:30 I-6-3** Influence of Lattice Constants of GaN and InGaN on Npn-type GaN/InGaN Heterojunction Bipolar Transistors T. Makimoto[1], T. Kido[2], K. Kumakura[1], Y. Taniyasu[1], M. Kasu[1] and N. Matsumoto[2], *[1]NTT Basic Research Labs. and [2]Shonan Inst. of Technology, Japan*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
			17:50 D-6-3 A stochastic computing chip for measurement of Manhattan distance M. Hori[1], M. Ueda[2] and A. Iwata[1], *[1]Hiroshima Univ. and [2]Matsushita Electric, Japan*

18:30–20:30 Rump Session (Room 501, Room 502)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
	17:45 F-6-4 Fabrication and Photoelectrochemical Properties of Porphyrin-Fullerene Assemblies by Self-assembly and Surface Sol-Gel Processes T. Akiyama, K. Matsuoka, K. Kakutani and S. Yamada, *Kyushu Univ., Japan*	**17:45 G-6-3** Magnetic and Microstructural Properties of FePt $L1_0$ Nanoparticle Films Fabricated by Self-Assembled Deposition Method J. C. Bea[2], C. K. Yin[1], M. Nishijima[1], T. Fukushima[1], T. Sadoh[3], M. Miyao[3] and M. Koyanagi[1], *[1]Tohoku Univ., [2]JST and [3]Kyushu Univ., Japan*	**17:45 H-6-3** Evaluation of Electrical Stimulus Current to Retina Cells for Retinal Prosthesis K. Motonami, T. Watanabe, J. Deguchi, T. Fukushima, H. Tomita, E. Sugano, M. Sato, H. Kurino, M. Tamai and M. Koyanagi, *Tohoku Univ., Japan*	**17:45 I-6-4** p-InGaN/n-GaN Vertical Conducting Diodes on n^+-SiC Substrate for High Power Electronic Device Applications A. Nishikawa, K. Kumakura and T. Makimoto, *NTT Basic Research Labs., Japan*
	18:00 F-6-5 Electrochemical Behavior and Electronic Characteristics of Self-Assembled Viologen Monolayers using QCM and Au(111) surface D. Y. Lee[1], S. H. Park[1], D. J. Qian[2] and Y. S. Kwon[1], *[1]Dong-A Univ. and [2]Fudan Univ., Korea*		**18:00 H-6-4** Integration of Superparamagnetic Polymer Composites into Microfluidic Devices for the Feasible Control of Magnetic Beads in Microchannels T. Akagi[1], N. Ichikawa[2] and T. Ichiki[1,3], *[1]Univ. of Tokyo, [2]Toyo Univ. and [3]PRESTO-JST, Japan*	

18:30–20:30 Rump Session (Room 501, Room 502)

POSTER SESSION (13:00-15:00, Exhibition Hall)

P1
Advanced Gate Stack / Si Processing Science
(28 Papers)

P1-1
Microscopic Effect of Nitrogen Doping on Dielectric Constant of Hf-silicate
H. Momida[1], T. Hamada[1], T. Yamamoto[2], T. Uda[2], N. Umezawa[3], K. Shiraishi[4], T. Chikyow[3] and T. Ohno[3,1], *[1]Univ. of Tokyo, [2]AdvanceSoft Corp., [3]NIMS and [4]Univ. of Tsukuba, Japan*

P1-2
Effect of SiO_2 Underneath Layer on $LaAlO_3$ High Dielectric Constant Material for Gate Oxide Application
M. Hasan and H. Hwang, *Gwangju Inst. of Science and Technology, Korea*

P1-3
Thermal Stability of the Yttrium Aluminate Film and the Suppression of its structural change and electrical properties degradation
T. Yamamoto[1], Y. Izumi[1], T. Miyamoto[1], H. Seki[1], H. Hashimoto[1], M. Inoue[2], M. Oosawa[2], S. Hasaka[2], Y. Sugita[3] and K. Ikeda[3], *[1]Toray Research Center, [2]Taiyo Nippon Sanso Corp. and [3]Fujitsu Labs. Ltd., Japan*

P1-4
Effect of Starting Interface in Scalability/Device Performance of Ultra-Scaled ALD HfSiON/TiN Gate Stacks
M. A. Quevedo-Lopez[1], S. A. Krishnan[1], P. D. Kirsch[1], J. Peterson[1], H. J. Li[1], M. Kim[2] and C. Huffman[1], *[1]International Sematech and [2]Univ. of Texas at Dallas, USA*

P1-5
A New Method to Correct Capacitance of High-leakage Ultra-thin Gate Dielectric
B. Y. Tsui[1,2], Y. P. Huang[1], F. C. Hsieh[1] and W. H. Wu[1], *[1]National Chiao-Tung Univ. and [2]National Nano Device Labs., Taiwan*

P1-6
Threshold Voltage Instability in nMOSFETs with $HfSiO/SiO_2$ High-κ Gate Stacks
W. H. Wu[1], Y. T. Hou[2], Y. Jin[2], H. J. Tao[2], S. C. Chen[2], M. S. Liang[2], B. Y. Tsui[1] and M. C. Chen[1], *[1]National Chiao-Tung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P1-7
A Novel Explanation of Substrate Bias Dependent Dielectric Breakdown Behavior with Channel Quantization Effect in Ultrathin Oxide pMOSFETs
S. Chaing, J. W. You, C. T. Lu, M. F. Lu, S. Huang-Lu and S. C. Chien, *United Microelectronics Corp., Taiwan*

P1-8
Improving high-κ gate dielectrics properties by high pressure water vapor annealing
P. Punchaipetch[1], H. Nakamura[1], Y. Uraoka[1], T. Fuyuki[1], T. Sameshima[2] and S. Horii[3], *[1]Nara Inst. of Science and Technology, [2]Tokyo Univ. of Agriculture and Technology and [3]Hitachi Kokusai Electric Inc., Japan*

P1-9
Reduction of accumulation thickness in metal gate
H. Watanabe[1], K. Nakajima[2], K. Matsuo[2], T. Saito[2] and T. Kobayashi[2], *[1]Toshiba Corp. and [2]Semiconductor Company, Toshiba Corp., Japan*

P1-10
Analysis of NiSi Fully-silicided Gate on SiO_2 and HfO_2 for CMOS Application
C. F. Huang and B. Y. Tsui, *National Chiao-Tung Univ., Taiwan*

P1-11
Composition control of Ni-silicide by CVD using $Ni(PF_3)_4$ and Si_3H_8
M. Ishikawa[1], I. Muramoto[1], H. Machida[1], Y. Ohshita[2], S. Imai[3] and A. Ogura[3], *[1]Tri Chemical Labs. Inc., [2]Toyota Technological Inst. and [3]Meiji Univ., Japan*

P1-12
Work Function Adjustment by Nitrogen Incorporation in HfN Gate Electrode
C. S. Lai[1], S. K. Peng[1], J. C. Wang[2], T. M. Pan[1], K. M. Fan[1] and J. Y. Wong[1], *[1]Chang Gung Univ. and [2]Nanya Technology Corp., Taiwan*

P1-13
Overcoming Challenges in Metal Gate Etching for Sub-45 nm Technology Node
V. Bliznetsov, R. Kumar, L. K. Bera, W. Y. Loh, C. H. Tung, N. Balasubramanian and D. L. Kwong, *Inst. of Microelectronics, Singapore*

P1-14
Germanium Out-Diffusion in HfO_2 and its Impact on Electrical Properties
Q. Zhang[1], N. Wu[1], C. Zhu[1] and L. K. Bera[2], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*

P1-15
Gate Stack Integration of Germanium Oxynitride for Germanium MOSFETs
Y. L. Chao[1], R. Scholz[2] and J. C. S. Woo[1], *[1]Univ. of California Los Angeles and [2]Max Planck Inst. of Microstructure Physics, USA*

P1-16
Atomistic Modeling of Boron Diffusion with Germanium Pre-amorphization for Ultra Shallow S/D Junction in nanometer-scale PMOS Devices
B. J. Kim, J. H. Yoo and T. Won, *Inha Univ., Korea*

P1-17
Influences of Ion Implantation Damages on Elevated Source/Drain Formation for Ultra-Thin Body SOI MOSFET
H. Oh[1], T. Sakaguchi[1], J. Bea[2], T. Fukushima[1] and M. Koyanagi[1], *[1]Tohoku Univ. and [2]JST, Japan*

P1-18
Ion-Implanted p/n Junction Characteristics in p- and n-type Germanium
T. Nishimura, M. Toyama, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

P1-19
Impact of Annealing Methods and Sequences on Dopant Activation and Diffusion of Ultra-shallow Implanted Silicon
W. S. Yoo and K. Kang, *WaferMasters, Inc., USA*

P1-20
Effect of Hydrogen on Helium implant-induced Nanocavities
A. Vengurlekar[1], S. Ashok[1], E. Ntsoenzok[2] and N. D. Theodore[3], *[1]Pennsylvania State Univ., [2]CERI/CNRS and [3]Freescale Semiconductor, USA*

P1-21
Development of Hybrid Tight-Binding Quantum Chemical Molecular Dynamics Method and Its Application to Boron Implantation Process into Pre-amorphized Silicon Substrate
T. Masuda[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], M. Kubo[1, 2], E. Broclawik[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO-JST, Japan*

P1-22
Ultra-Shallow p+/n Junction Prepared by Low Energy BF_3 Plasma Doping (PLAD) and KrF Excimer Laser Annealing
D. K. Lee, S. K. Baek, C. H. Cho, S. H. Heo and H. S. Hwang, *Gwangju Inst. of Science and Technology, Korea*

P1-23
Dopant Activation Enhancement in Silicon by Hydrogen Treatment
S. Ashok and A. Vengurlekar, *The Pennsylvania State Univ., USA*

P1-24
Application of Microwave Plasma Gate Oxidation to Strained-Si on SiGe and SGOI
M. Nishisaka and T. Asano, *Kyushu Inst. of Technology, Japan*

P1-25
Damage-Free Microwave-Excited Plasma Contact Hole Etching without Carrier Deactivation at the Interface between Silicide and Heavily-Doped Si
T. Goto, M. Terasaki, H. Asahara, H. Nakazawa, A. Inokuchi, J. Yamanaka, A. Teramoto, M. Hirayama, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P1-26
Characterization of Crystalline Defects and Stress in Shallow Trench Isolation by Cathodoluminescence and Raman Spectroscopies
R. Sugie[1], K. Matsuda[1], N. Nagai[1], T. Ajioka[1], M. Yoshikawa[1], T. Mizukoshi[2], K. Shibusawa[2] and S. Yo[3], *[1]Toray Research Center, [2]Miyagi Oki Electric Co., Ltd. and [3]Oki Electric Industry Co., Ltd., Japan*

P1-27
Depth Profile of Various Bonding Configration of Nitrogen Atoms in Silicon Oxynitrides formed by Plasma Nitridation
H. Nohira[1], S. Shinagawa[1], T. Ikuta[2], M. Hori[2], M. Kase[2], H. Okamoto[1] and T. Hattori[1], *[1]Musashi Inst. of Technology and [2]Fujitsu Ltd., Japan*

P1-28
A new landing plug formation in a submicron self-aligned contact etching
M. S. Lee, S. K. Lee, T. W. Jung, D. D. Lee and S. C. Moon, *Hynix Corp., Korea*

P2
Characterization and Materials Engineering for Device Integration
(13 Papers)

P2-1
Hydrocarbon Groups and Film Properties of SiOCH Dielectrics: Theoretical Investigations using Molecular Models
N. Tajima[1], T. Hamada[2], T. Ohno[1], K. Yoneda[3], N. Kobayashi[3], S. Hasaka[4] and M. Inoue[4], *[1]NIMS, [2]Univ. of Tokyo, [3]SELETE and [4]Taiyo Nippon Sanso Corp., Japan*

P2-2
High frequency dielectric mapping using un-contact probe for dielectric materials
H. Kakemoto, S. M. Nam, S. Wada and T. Tsurumi, *Tokyo Tech, Japan*

P2-3
Infrared Complex Dielectric Function Analysis for Chemical Bonding Structure of Porous Silica Low Dielectric Constant Films
S. Takada[1], N. Hata[1,2], S. Hishiya[3], N. Fujii[3], T. Nakayama[3] and T. Kikkawa[2,4], *[1]AIST, [2]MIRAI-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*

P2-4
Effect of Pore Generating Materials on the Electrical and Mechanical Properties of Porous Low-k Films
S. Kim[1], J. Hahn[2] and K. Char[1], *[1]Seoul National Univ. and [2]Korea Research Inst. of Standards and Science, Korea*

P2-5
Grating Metal Structure with Low-K BCB and Electroplated Copper for High-Q Spiral Inductors
S. K. Yeo, S. H. Shin, J. H. Lee and Y. S. Kwon, *KAIST, Korea*

P2-6
UV-Raman Spectroscopy System for Local and Global Strain Measurement in Si
I. Chiba[1], R. Shimidzu[1], K. Yamasaki[2], D. Kosemura[2], S. Tanaka[2] and A. Ogura[2], *[1]PHOTON Design Corp. and [2]Meiji Univ., Japan*

P2-7
Characterization of Self Assembled Monolayers for Ultra Low-k Films
B. R. Murthy[1], W. M. Yee[2], A. Krishnamoorthy[1], V. Anand[2], K. Y. Yong[3], S. F. Choy[1], K. Prasad[2], R. Kumar[1] and D. C. Frye[4], *[1]Inst. of Microelectronics, [2]Nanyang Technological Univ., [3]National Univ. of Singapore and [4]The Dow Chemical Company, Singapore*

P2-8
Deep Trench Etching for Chip-to-Chip Three-Dimensional Integration
H. Kikuchi, Y. Yamada, H. Kijima, T. Fukushima and M. Koyanagi, *Tohoku Univ., Japan*

P2-9
High Aspect-Ratio Through-Wafer Interconnections with Thick Oxidized Porous Silicon Sidewall Via
B. J. Kim, M. L. Ha and Y. S. Kwon, *KAIST, Korea*

P2-10
Numerical Study of the Self-Interconnection Assembly Method Using Resin Containing Solder Fillers
K. Ohta, K. Yasuda, M. Matsushima and K. Fujimoto, *Osaka Univ., Japan*

P2-11
The annealing effects of GaN MIS capacitors with photo-CVD oxide layers
Y. Z. Chiou[1], Y. K. Su[2], S. J. Chang[2], C. K. Wang[2] and J. J. Tang[1], *[1]Southern Taiwan Univ. of Technology and [2]National Cheng Kung Univ., Taiwan*

P2-12
AC Power Loss and Signal Coupling in VLSI backend Interconnects
C. C. Chen[1], C. C. Liao[1], H. L. Kao[1], A. Chin[1], S. P. McAlister[2] and C. C. Chi[3], *[1]National Chiao Tung Univ., [2]National Research Council of Canada and [3]National Tsing-Hua Univ., Taiwan*

P2-13
Nickel Germanide Formation on Condensed Ge Layer for Ge-on-Insulator Device Application
H. Choi[1], M. Park[1,2], T. Fukushima[1] and M. Koyanagi[1], *[1]Tohoku Univ. and [2]Samsung Electronics Co. Ltd., Japan*

P3
CMOS Devices / Device Physics
(20 Papers)

P3-1
3D Device Simulation for Neutron-induced Latch-up in CMOS Devices
H. Yamaguchi[1], E. Ibe[1], Y. Yahagi[1] and H. Kameyama[2], *[1]Production Engineering Research Lab., Hitachi Ltd. and [2]Renesas Kodaira Semiconductor Co. Ltd, Japan*

P3-2
Characterization of Embedded Poly-Heater PMOSFETs and its Application on In-Line Wafer Level NBTI Monitor
C. S. Wang[1,2], W. C. Chang[1], W. S. Ke[1], C. T. Chiang[1], C. F. Lee[1], K. C. Su[1] and M. J. Chen[2], *[1]United Microelectronics Corp. and [2]National Chiao Tung Univ., Taiwan*

P3-3
DC Hot Carrier Reliability at Elevated Temperatures for nMOSFETs Using 0.13µm Technology
J. C. Lin[1, 3], S. Y. Chen[2], H. W. Chen[2], Z. W. Jhou[2], H. C. Lin[2], S. Chou[1], J. Ko[1], T. F. Lei[3] and H. S. Haung[2], *[1]United Microelectronics Corp., [2]National Taipei Univ. of Technology and [3]National Chiao Tung Univ., Taiwan*

P3-4
The Impact of Body-Potential on Hot-Carrier-Induced Device Degradation for 90nm Partially-Depleted SOI nMOSFETs
C. M. Lai[1], C. T. Lin[1], Y. K. Fang[1], W. K. Yeh[2], J. W. Syu[2] and W. T. Shiau[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P3-5
Investigation of Accumulation-mode Vertical Double-gate MOSFET
M. Masahara, K. Endo, Y. X. Liu, T. Matsukawa, S. O'uchi, K. Ishii, H. Takashima, E. Sugimata and E. Suzuki, *AIST, Japan*

P3-6
Characteristics of Metal Gate GOI-MOSFET with High-*k* Gate Dielectric Fabricated by Ge Condensation Method
M. Park[1,2], H. Choi[1], J. Bea[1], T. Fukushima[1] and M. Koyanagi[1], *[1]Tohoku Univ. and [2]Samsung Electronics Co. Ltd., Japan*

P3-7
Experimental study on Improving Unclamped Inductive Switching Characteristics of the New Power MOSFET Employing Deep Body Contact
I. H. Ji, Y. H. Choi, S. S. Kim, Y. I. Choi and M. K. Han, *Seoul National Univ., Korea*

P3-8
Analytical Solutions to Quantum Drift-Diffusion Equations for Quantum Mechanical Modeling of MOS Structures
S. Uno[1], H. Abebe[2] and E. Cumberbatch[1], *[1]Claremont Graduate Univ. and [2]Univ. of Southern California, USA*

P3-9
Comparison of Random Dopant-Induced Threshold Voltage Fluctuations in Nanoscale Single-, Double-, and Surrounding-Gate Field Effect Transistors
Y. Li, S. M. Yu and C. F. Hsiao, *National Chiao Tung Univ., Taiwan*

P3-10
Impact of Oxide Thickness Fluctuation on MOSFETs Gate Tunnelling
B. Cheng, S. Roy, A. Martinez and A. Asenov, *Univ. of Glasgow, UK*

P3-11
Carrier Mobility in Multi-FinFETs with a (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching
Y. X. Liu, E. Sugimata, K. Ishii, M. Masahara, K. Endo, T. Matsukawa, H. Takashima, H. Yamauchi and E. Suzuki, *AIST, Japan*

P3-12
Accurate Evaluation of Inversion-Layer Mobility and Experimental Extraction of Local Strain Effect in Sub-µm Si MOSFETs
C. Tanaka, K. Ohuchi and J. Koga, *Toshiba Corp., Japan*

P3-13
Electron and Hole Mobilities in Orthorhombically Strained Silicon
S. T. Chang, *National Chung Hsing Univ., Taiwan*

P3-14
Investigation and Modeling of Stress Interactions on 90 nm SOI CMOS with Various Mobility Enhancement Approaches
C. T. Lin[1], Y. K. Fang[1], W. K. Yeh[2], H. C. Chang[3], C. H. Hsu[3], L. W. Chen[3], M. L. Lee[3], C. T. Tsai[3] and W. T. Shiau[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P3-15
MEMS 3-D Stacked RF Transformers Fabricated by 0.18 µm MS/RF CMOS technology With Improved Power Loss and Noise Figure Performances
Y. S. Lin[1], H. B. Liang[1], T. Wang[2] and S. S. Lu[2], *[1]National Chi-Nan Univ. and [2]National Taiwan Univ., Taiwan*

P3-16
Mobility Modulation Technology Impact on Device Performance and Reliability for <100> sub-90nm SOI CMOSFETs
C. M. Lai[1], C. T. Lin[1], W. K. Yea[2], Y. K. Fang[1] and W. T. Shiau[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P3-17
The DC Performance of Nanometer MOSFETs: Targets Versus Reality
F. Schwierz, *Techn. Univ., Germany*

P3-18
A High Performance Embedded 60nm Gate Length CMOSFET with Novel Strained Silicon Process
C. J. Huang[1], K. Y. Chang[2], S. Chou[1], J. Koe[1], J. H. Huang[2], H. Liao[2] and C. Y. Lim[2], *[1]United Microelectronics Corp. and [2]United Microelectronics-Singapore Corp., Taiwan*

P3-19
A Novel Simplified Process for Self Aligned Planar Wrapping Gate FET's with Directionally Crystallized Si Channel Processed via Sequential Lateral Solidification
Y. W. Park and J. C. S. Woo, *Univ. of California Los Angeles, USA*

P3-20
The Characteristics and Reliability of Multi-channel Poly-Si TFTs
M. S. Shieh, J. Y. Sang, C. Y. Chen, S. D. Wang and T. F. Lei, *National Chiao Tung Univ., Taiwan*

P4 Advanced Memory Technology
(11 Papers)

P4-1
The New Technology for DRAM Cell Transistor with S-RCAT and its Size Effect
S. G. Park[1], J. Y. Kim[1], Y. I. Kim[1], H. J. Oh[1], J. H. Kim[1], S. E. Kim[1], W. S. Lee[1], M. S. Shim[1], K. P. Lee[1], Y. J. Park[1], W. S. Lee[1], B. I. Ryu[1] and Y. H. Rho[2], *[1]Samsung Electronics Co. Ltd. and [2]Sungkyunkwan Univ., Korea*

P4-2
Improvement of Cell Stability at Low Voltage Operation on 6T-SRAM Cell with 0.1µm Channel Width
H. C. Jung, S. An, Y. Son, Y. Cho, J. Nam, K. Koh, K. Kim and W. S. Lee, *Samsung Electronics Co. Ltd., Korea*

P4-3
Abnormal Disturb Mechanism of sub 100nm NAND Flash
S. J. Joo, H. J. Yang, H. S. Kim and K. H. Noh, *Hynix Corp., Korea*

P4-4
Characteristics of Band-to-Band Hot Hole Injection for Erasing Operation in Charge Trapping Memory
L. Sun[1], L. Pan[1], H. Pang[1], Y. Zeng[1], Z. Zhang[1], J. Chen[2] and J. Zhu[1], *[1]Tsing-hua Univ. and [2]Semiconductor Manufacturing International Corp., China*

P4-5
Thorough Diagnoses of the Impact of Flash Memory Cell UV-State Threshold Voltage on the Cell Reliability and Program/Erase Cycling Endurance Performance
V. C. W. Kuo[1], H. P. Hwang[1], C. T. Huang[2], C. W. Chou[2], S. M. Tzeng[1], C. P. Lai[1], T. W. Tzeng[1], Y. E. Huang[1], W. Z. Wong[1], C. S. Yang[1] and S. Pittikoun[1], *[1]Powerchip Semiconductor Corp. and [2]not with PSC anymore, Taiwan*

P4-6
Effect of Compensation Implant in SONOS Flash EEPROMs
P. B. Kumar[1], E. Murakami[2], S. Kamohara[2] and S. Mahapatra[1], *[1]Indian Inst. of Technology Bombay and [2]Renesas Technology Corp., India*

P4-7
Non-volatile Al_2O_3 memory using an Al-rich structure as a charge storage layer
S. Nakata[1], K. Saito[2] and M. Shimada[1], *[1]NTT and [2]NTT AFTY Corp., Japan*

P4-8
A new low temperature APM cleaning process to improve ONO integrity in 0.18 µm stacked-gate EEPROM memory
J. Zhao, J. S. Ng, K. F. Wong, W. Zhang, M. Mukhopadhyay and D. Shukla, *Systems on Silicon Manufacturing Corp., Singapore*

P4-9
Effects of Voltage Cycling on Polarization and Reliability of 3D SBT Ferroelectric Capacitors Integrated in 0.18µm CMOS Technology
D. Wouters[1], L. Goux[1], J. Lisoni[1], D. Maes[1], H. Vander Meeren[1], V. Paraschiv[1], L. Haspeslagh[1], C. Artoni[2], G. Corallo[2] and R. Zambrano[2], *[1]IMEC and [2]STMicroelectronics, Belgium*

P4-10
Fabrication and Evaluation of Magnetic Tunnel Junction with MgO Tunneling Barrier
T. Sakaguchi, H. Choi and T. Sugimura, *Tohoku Univ., Japan*

P4-11
Annealing effect of phase change and current control in phase change channel transistor memory
Y. Yin, D. Niida, H. Sone and S. Hosaka, *Gunma Univ., Japan*

P5 Advanced Circuits and Systems
(9 Papers)

P5-1
A Large Variable Ratio On-Chip Inductor with Spider Legs Shield
T. Yammouch, H. Sugawara, K. Okada and K. Masu, *Tokyo Tech, Japan*

P5-2
Systematic Analysis and Modeling of On-Chip Spiral Inductors for CMOS RFIC Application
M. C. Tang[1], Y. K. Fang[1], C. M. Lai[1], W. K. Yeh[2] and T. H. Yeh[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]Realtek Semiconductor Corp., Taiwan*

P5-3
An Intelligent Simulation-Based Optimization Technique for Integrated Circuit Design Automation: A Case Study of LNA Circuit Design
Y. Li and H. M. Chou, *National Chiao Tung Univ., Taiwan*

P5-4
A Novel Fast Lock-in PLL Frequency Synthesizer with Direct Frequency Presetting Circuit
X. Kuang[1], N. Wu[1] and G. Shou[2], *[1]Chinese Academy of Sciences and [2]Liuhewangtong Microelectronics Ltd., China*

P5-5
Estimation of Wire Length Distribution for Evaluating Performance Improvement of Three-Dimensional LSI
J. Deguchi, Y. Nakatani, T. Sugimura, T. Fukushima and M. Koyanagi, *Tohoku Univ., Japan*

P5-6
No Feedback ΔΣ ADC for High Frequency Operation Using Frequency ΔΣ Modulator
W. Matsubara, M. Sakou, K. Maezawa and T. Mizutani, *Nagoya Univ., Japan*

P5-7
THD Measurement and Compensation for Analog Circuits with Fine CMOS Devices
T. Komuro[1,3], S. Sobukawa[2], H. Kobayashi[3] and H. Sakayori[1], *[1]Agilent Technologies International Japan, Ltd., [2]NF Corp. and [3]Gunma Univ., Japan*

P5-8
A Novel Operation Scheme for Realizing Combined Linear-Logarithmic Response in Photodiode-Type Active Pixel Sensor Cells
A. Hamasaki, M. Terauchi and K. Horii, *Hiroshima City Univ., Japan*

P5-9
New TxID sequence and Matched Filter implementation for ATSC DTV
J. S. Cha[1], B. Yoon[1], N. Hur[2], Y. Lee[3] and S. Kim[3], *[1]Univ. of Seokyeong, [2]Sungkyunkwan Univ., [3]ETRI, Korea*

P6 Compound Semiconductor Circuits, Electron Devices and Device Physics
(13 Papers)

P6-1
Extremely Low Noise Characteristics of 0.15 µm Power Metamorphic HEMT
J. Y. Shim, H. S. Yoon, D. M. Kang, J. Y. Hong and K. H. Lee, *ETRI, Korea*

P6-2
$In_{0.49}GaP/Al_{0.45}GaAs$ E-pHEMT with High Gate Forward Turn-on Voltage & High Transconductance Linearity
K. Jang, Juyong Lee, Jaehak Lee, K. Seo, *Seoul National Univ., Korea*

P6-3
Origin of Frequency Dependence in Drain Conductance of InAlAs/InGaAs HEMTs
H. Taguchi, M. Hayakawa, Y. Nakamura, T. Iida and Y. Takanashi, *Tokyo Univ. of Science, Japan*

P6-4
Improvement of Linearity in Novel InGaAsN-based HEMTs
Y. K. Su, S. H. Hsu, S. J. Chang and J. D. Wu, *National Cheng Kung Univ., Taiwan*

P6-5
Double-Transconductance-Plateau Characteristics in InGaAs/GaAs Real-Space Transfer High Electron Mobility Transistor
C. S. Lee[1], W. C. Hsu[2], Y. J. Chen[2], J. C. Huang[2] and D. H. Huang[2], *[1]Feng Chia Univ. and [2]National Cheng Kung Univ., Taiwan*

P6-6
A Comparative Study on the DC, Microwave Characteristics of 0.12 μm Double-Recessed Gate AlGaAs/InGaAs/GaAs PHEMTs Using a Dielectric Assisted Process
J. W. Lim, H. K. Ahn, H. G. Ji, W. J. Chang, J. K. Mun and H. Kim, *ETRI Korea*

P6-7
Novel $In_{0.425}Al_{0.575}As/In_xGa_{1-x}As$ Metamorphic δ-HEMT's on GaAs Substrate with Various Channel Designs
W. C. Hsu[1], C. S. Lee[2], Y. J. Chen[1], J. C. Huang[1] and C. L. Wu[3], *[1]National Cheng Kung Univ., [2]Feng Chia Univ. and [3]Transcom, Inc., Taiwan*

P6-8
Compact RF Switches Using Dielectric Overhang Gate Process & Stacked Inductor
K. Jang, J. Lee, S. Kim and K. Seo, *Seoul National Univ., Korea*

P6-9
P-type doping for Be/C co-implantation in GaN
K. T. Liu[1], Y. K. Su[2], S. J. Chang[2] and Y. Horikoshi[3], *[1]Cheng Shiu Univ., [2]National Cheng Kung Univ. and [3]Waseda Univ., Taiwan*

P6-10
Enhanced f_{max} and low base resistance in Ni silicided SiGe HBT
H. C. Bae, S. H. Kim, Y. J. Song, S. W. Yoo, S. H. Lee and B. W. Kim, *ETRI, Korea*

P6-11
Enhancement-Mode High Electron Mobility Transistors Lattice-Matched to InP Substrates Utilizing Ti/Pt/Au Gate Metallization
J. H. Jang[1], S. Kim[2] and I. Adesida[2], *[1]Gwangju Inst. of Science and Technology and [2]Univ. of Illinois at Urbana Champaign, Korea*

P6-12
HEMT Yield Improvement with Ultrasonic-assisted recess for High speed Integrated Circuit
S. J. Yeon, H. Kim, J. Lee and K. Seo, *Seoul National Univ., Korea*

P6-13
Temperature-Dependent Characteristics of an Sulfur-Passivated AlGaAs/InGaAs/GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT)
P. H. Lai, S. I. Fu, Y. Y. Tsai, C. I. Kao, C. W. Chen, C. H. Yen and W. C. Liu, *National Cheng Kung Univ., China*

P7
Photonic Devices and Device Physics
(20 Papers)

P7-1
Effect of Surface Treatment on the Performances of Vertical-structure GaN-based High-power LEDs with Electroplating Metallic Substrate
K. M. Uang[1,2], S. J. Wang[1], S. L. Chen[1], Y. C. Yang[1], T. M. Chen[2] and B. W. Liou[2], *[1]National Cheng Kung Univ and [2]Wu-Feng Inst. of Technology, Taiwan*

P7-2
Fabrication and characteristics of GaN-based Microcavity LEDs with high reflectivity A1N/GaN DBRs
Y. C. Peng[1], C. C. Kao[1], J. Y. Tsai[1], T. C. Lu[1], H. H. Yao[1], T. T. Kao[1], C. F. Lin[2], H. C. Kuo and S. C. Wang, *[1]National Chiao Tung Univ and [2]National Chung Hsing Univ., Taiwan*

P7-3
GaN-Based Green Resonant Cavity Light Emitting Diodes
W. K. Wang[1], R. H. Horng[1], S. Y. Huang[2], J. M. Chen[2], Y. J. Tsai[1] and D. S. Wuu[1], *[1]National Chung-Hsing Univ., and [2]Da-Yeh Univ., China*

P7-4
Light-output Enhanced of GaN-based Light-emitting Diodes by Photoelectro-chemical oxidation in H_2O
F. I. Lai, W. Y. Chen, C. C. Kao, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ., Taiwan*

P7-5
High Brightness InGaN/GaN LEDs with ESD Protection
S. C. Shei[1] and C. S. Chang[2], *[1]South Epitaxy Corp. and [2]Inst. of Microelectronics, National Cheng Kung Univ., Taiwan*

P7-6
Enhanced Light Output of InGaN/GaN Light Emitting Diode with Excimer Laser Etching on Nano-roughened P-GaN Surface
H. W. Huang, J. T. Chu, C. C. Kao, T. H. Hsueh, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ., Taiwan*

P7-7
Nitride-based flip-chip LEDs with transparent ohmic contacts and reflective mirrors
W. S. Chen[1], S. J. Chang[1], Y. K. Su[1], Y. C. Lin[1], C. S. Chang[1], T. K. Ke[1], C. F. Shen[1] and S. C. Shei[2], *[1]National Cheng Kung Univ. and [2]South Epitaxy Corp., Taiwan*

P7-8
Relative Intensity Noise of Vertical Cavity Surface Emitting Lasers (VCSELs) with Polarization-Selective Feedback
Y. H. Chang, *National Chiao Tung Univ., Taiwan*

P7-9
A Theoretical Study: Effect of Eu and Er ion Dopant on the Electronic Excitations of Yttrium Oxide and Yttrium Oxy-Sulphide.
A. Govindasamy[1], C. Lv[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], M. Kubo[1,2], E. Broclawik[1] and A. Miyamoto[1], *[1]Tohoku Univ., [2]PRESTO-JST, Japan*

P7-10
A Theoretical Study on Influence of Oxygen Vacancies on the Electronic Properties of Indium Oxide and Indium Tin Oxide
C. Lv[1], X. Wang[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], M. Kubo[1, 2], E. Broclawik[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO-JST, Japan*

P7-11
Theoretical Design of MgO Protecting Layer in Plasma Display by New Kinetic Monte Carlo Simulator
M. Kubo[1,2], H. Kikuchi[1], T. Masuda[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Kajiyama[3] and A. Miyamoto[1], *[1]Tohoku Univ., [2]PRESTO-JST and [3]Univ. of Tokyo Japan*

P7-12
Photoluminescence and Electroluminescence Properties of The Er-doped Silicon-Rich Silicon Oxide Films deposited by Pulsed Laser Deposition Technique
Y. Lim[1], C. Ko[1], M. Han[1], C. H. Bae[2], S. M. Park[2] and K. Park[1], *[1]Univ. of Seoul and [2]Kyung Hee Univ., Korea*

P7-13
Structural and Optical Properties of Electro-Optic Material: Sputtered $(Ba,Sr)TiO_3$
M. Suzuki, Z. Xu, Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*

P7-14
Photodetector Characteristics of Metal-Oxide-Semiconductor Tunneling Structures with Transparent Conductive Tin Oxide Gate
M. Chikamoto, H. Hashimoto, K. Horikoshi, A. Shinozaki, S. Morita, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ., Japan*

P7-15
Novel Fabrication Technique of Optical Waveguides using Low Density Silicon Nitride Films Deposited by Plasma-Enhanced Chemical Vapor Deposition
S. Yokoyama and T. Kakite, *Hiroshima Univ., Japan*

P7-16
Groove-Buried Optical Waveguides Based on Metal Organic Solution-Derived $Ba_{0.7}Sr_{0.3}TiO_3$ Thin Films
Z. Xu, M. Suzuki, Y. Tanushi, K. Wakushima and S. Yokoyama, *Hiroshima Univ., Japan*

P7-17
InP/InGaAs Partially p-Doped Photodiode with Leaky Optical Waveguide and Distributed Bragg Reflectors for High-Saturation-Current and High-Bandwidth-Responsivity Product
W. Y. Chiu, W. K. Wang, Y. S. Wu, F. H. Huang, D. M. Lin, Y. J. Chan and J. W. Shi, *National Central Univ., Taiwan*

P7-18
Control of Spectral Photosensitivity in Stacked Color Sensors: Proposal and Theoretical Analysis
N. Kakimoto and T. Numai, *Ritsumeikan Univ., Japan*

P7-19
Fabrication of Si thin-film solar cells by hot-wire chemical vapor deposition and laser doping techniques
S. Y. Lien[1], D. S. Wuu[1,2], Y. C. Lin[1], I. C. Hsieh[3] and H. Y. Mao[1], *[1]National Chung Hsing Univ., [2]National Formosa Univ. and [3]Da-Yeh Univ., Taiwan*

P7-20
Homoepitaxial ZnSe MIS Photodetectors Using SiO_2 and BST Insulator
T. K. Lin[1], S. J. Chang[1], Y. K. Su[1], Y. Z. Chiou[2], C. K. Wang[1], S. P. Chang[1], J. J. Tang[2] and B. R. Huang[3], *[1]National Cheng Kung Univ., [2]Southern Taiwan Univ. of Technology and [3]National Yunlin Univ. of Science and Technology, Taiwan*

P8
Advanced Material Synthesis and Crystal Growth Technology
(9 Papers)

P8-1
Constraining the Direction of Carbon Nanotubes by Oxide Capping Layer
K. C. Lin, R. L. Lai, Y. R. Chang, C. P. Juan, T. Y. Chuang, J. K. Shiu, H. C. Tai and H. C. Cheng, *National Chiao Tung Univ., Taiwan*

P8-2
Crystal Growth Mechanism of Spherical Silicon Fabricated by Dropping Method
S. Omae[1], T. Minemoto[1], M. Murozono[2], H. Takakura[1] and Y. Hamakawa[1], *[1]Ritsumeikan Univ. and [2]Clean Venture 21 Co., Japan*

P8-3
High-Rate Growth of Defect-Free Epitaxial Si at Low Temperatures by Atmospheric Pressure Plasma CVD
T. Wakamiya, H. Ohmi, H. Kakiuchi, H. Watanabe, K. Yasutake, K. Yoshii and Y. Mori, *Osaka Univ., Japan*

P8-4
High-Rate Deposition of Intrinsic Amorphous Silicon Layers for Solar Cells using Very High Frequency Plasma at Atmospheric Pressure
H. Kakiuchi[1], H. Ohmi[1], Y. Kuwahara[1], M. Matsumoto[2], Y. Ebata[3], K. Yasutake[1], K. Yoshii[1] and Y. Mori[1], *[1]Osaka Univ., [2]Sanyo Electric Company and [3]Sharp, Japan*

P8-5
Study of Effects of Metal Layer on Hydrogen Desorption from Hydrogenated Amorphous Silicon Using Temperature-Programmed Desorption
Y. Hamaoka, H. Ohmi, H. Kakiuchi and K. Yasutake, *Osaka Univ., Japan*

P8-6
Fabrication of InP and InGaAs air-hole type Two-dimensional Photonic Crystals by Selective Area MOVPE
S. Hashimoto, J. Takeda, A. Tarumi, S. Hara, J. Motohisa and T. Fukui, *Univ. of Hokkaido, Japan*

P8-7
Precise Control of Growth of VCSEL Structure by using MBE *in-situ* Reflectance Monitor
M. Mizutani, F. Teramae, K. Takeuchi, T. Murase, S. Naritsuka and T. Maruyama, *Meijo Univ., Japan*

P8-8
Interface states of AlSb/InAs heterointerface with AlAs-like interface
S. Gozu[1], K. Akahane[1], N. Yamamoto[1], A. Ueta[1], T. Ando[2] and N. Ohtani[3], *[1]National Inst. of Information and Communications Technology, [2]Hamamatsu Photonics K. K. and [3]Doshisha Univ., Japan*

P8-9
X-ray Resonant/Off-Resonant Scattering of Fractional Monolayer AlAs/GaAs Superlattices
H. Miyagawa[1], K. Takao[1], K. Fujii[1], M. Mizumaki[2], O. Sakata[2], S. Kimura[2], A. Kitano[2], R. Ueji[1], N. Sumida[1] and S. Koshiba[1], *[1]Kagawa Univ. and [2]JASRI, Japan*

P9
Physics and Applications of Novel Functional Materials and Devices
(10 Papers)

P9-1
A novel method to convert metallic-type CNTs to semiconducting-type CNT-FETs
B. H. Chen[1,2], J. H. Wei[3], P. Y. Lo[1], M. J. Tsai[1], T. S. Chao[2], H. C. Lin[2] and T. Y. Huang[2], *[1]ERSO, [2]National Chiao Tung Univ and [3]Ching Yun Univ., Taiwan*

P9-2
Synthesis of Inorganic-Compounded Nanowires using Carbon Nanotube Templates
H. Konishi[1], M. Kishida[1], Y. Murata[1], T. Yasuda[1], D. Maeda[1], K. Tomita[1], K. Motoyoshi[1], S. Honda[1], J. G. Lee[1], H. Mori[1], S. Yoshimoto[2], R. Hobara[2], I. Matsuda[2], S. Hasegawa[2], K. Oura[1] and M. Katayama[1], *[1]Osaka Univ., and [2]Univ. of Tokyo, Japan*

P9-3
Metal-coated Carbon Nanotube Tips for Nanoscale Electrical Measurements
Y. Murata[1], M. Kishida[1], H. Konishi[1], D. Maeda[1], T. Yasuda[1], K. Motoyoshi[1], K. Tomita[1], S. Honda[1], H. Okado[1], S. Yoshimoto[2], R. Hobara[2], I. Matsuda[2], S. Hasegawa[2], K. Oura[1] and M. Katayama[1], *[1]Osaka Univ., and [2]Univ. of Tokyo, Japan*

P9-4
Fabrication of nanoscaled-schottky diodes based on metal silicide/silicon nanowire with scanning probe lithography and Wet etching and its electrical characterization
J. T. Sheu[1], S. P. Yeh[2], S. T. Tsai[3] and C. H. Lien[2], *[1]National Chiao Tung Univ., [2]National Tsing-Hua Univ. and [3]National Chi-Nan Univ.*

P9-5
Quantum Simulation of Nanoscale Metal/Insulator Tunnel Transistors
M. Shin, *Information and Communications Univ., Korea*

P9-6
Selective deposition of gold particles on DPN patterns on silicon dioxide surface
J. T. Sheu[1, 2], C. H. Wu[1,2] and T. S. Chao[1], *[1]National Chiao Tung Univ. and [2]National Synchrotron Radiation Research Center, Taiwan*

P9-7
Feasibility of Observing a Spin Drag Effect in the Electronic Transport
Y. Takahashi[1], Y. Sato[2], F. Hirose[1] and H. Kawaguchi[1,2], *[1]Yamagata Univ. and [2]CREST-JST, Japan*

P9-8
Dynamic Analyses of Thermally Induced Ultrasonic Emission from Nanocrystalline Silicon
Y. Watabe[1], Y. Honda[1] and N. Koshida[2], *[1]Matsushita Electric and [2]Tokyo Univ. of Agriculture and Technology, Japan*

P9-9
Exciton dephasing in $(AlAs)_m/(GaAs)_n$ various period superlattices
S. Takizawa, H. Hari, Y. Miyaoka, K. Fujii, H. Yamada, H. Miyagawa, N. Tsurumachi, S. Koshiba, S. Nakanishi and H. Itoh, *Kagawa Univ., Japan*

P9-10
Ultraviolet Lasing of Sol-Gel Derived Zinc Oxide Polycrystalline Films
S. Y. Kuo[1], F. I. Lai[2], W. C. Chen[3], C. P. Cheng[3], H. C. Kuo[2] and S. C. Wang[2], *[1]Instrument Technology Research Center, [2]National Chiao Tung Univ. and [3]National Taiwan Normal Univ., Taiwan*

P10
Organic Materials Science, Device Physics, and Applications
(11 Papers)

P10-1
Fabrication of Electrically conductive Chemically adsorbed monomolecular layer with polypyrrolyl groups
S. Yamamoto[1] and K. Ogawa[2], *[1]Kobe City College of Technology and [2]Kagawa Univ., Japan*

P10-2
Electronic and Transport Properties of Ferrocene Molecule: Theoretical Study
T. Uehara, H. Baba, R. V. Belosludov, A. A. Farajian, H. Mizuseki and Y. Kawazoe, *Tohoku Univ., Japan*

P10-3
Structure and Properties Due to NO_2 Gas in Copper Phthalocyanine Films Prepared by Oblique Vacuum Evaporation Method
T. Wakasa, K. Shinbo, Y. Ohdaira, K. Kato and F. Kaneko, *Niigata Univ., Japan*

P10-4
Organic Multi-Function Diodes Operable for Emission and Photo detection Modes
H. Shimada[1], J. Yanagi[1], Y. Matsushita[1], S. Naka[1,2], H. Okada[1,2] and H. Onnagawa[1,2], *[1]Toyama Univ. and [2]Innovation Plaza Tokai JST, Japan*

P10-5
The Influence of the Conductive Layer on the Organic Electroluminescent Device
H. H. Yu[1], S. J. Hwang[2] and M. C. Tsen[1], *[1]National Formosa Univ. and [2]National United Univ., Taiwan*

P10-6
Characteristics of polymer light emitting diodes with the LiF anode interfacial layer
S. Sohn, J. Yang, H. Chae, J. Boo and D. Jung, *Sungkyunkwan Univ., Korea*

P10-7
Air-stable Ambipolar Organic Thin Film Transistors Based on Copper Pthalocyanince Composites
R. Ye[1], M. Baba[1], T. Suzuki[2] and K. Mori[1], *[1]Iwate Univ. and [2]Iwate Industrial Research Inst., Japan*

P10-8
Improvement of on/off ratio of pentacene static induction transistor with ultra-thin CuPc layer
Y. Watanabe[1], H. Iechi[1,2] and K. Kudo[1,3], *[1]Optoelectronic Industry and Technology Development Association, [2]Ricoh Co. Ltd and [3]Chiba Univ., Japan*

P10-9
Organic thin-film transistors with N2 treatment
B. T. Wu[1], Y. K. Su[1], Y. S. Chen[1], M. L. Tu[1], Y. T. Chiou[2] and C. H. Chu[2], *[1]National Cheng Kung Univ. and [2]Inst. of Industrial Technology Research, Taiwan*

P10-10
Analysis of Interface trap between pentacene active layer and gate insulator of OTFTs.
C. K. Han, T. H. Kim and C. K. Song, *Dong-A Univ., Korea*

P10-11
SPICE model of Pentacene Thin Film Transistor
H. Jung, Y. X. Xu and C. K. Song, *Dong-A Univ., Korea*

P11
Micro / Nano Electromechanical and Bio-Systems
(9 Papers)

P11-1
Vibration Characteristics of PZT Actuator by Fluid Flow in Intravascular Oxygenator
G. B. Kim[1], T. K. Kwon[1], S. J. Kim[2], C. U. Hong[1] and N. G. Kim[1], *[1]Univ. of Chonbuk and [2]College of Iksan, Korea*

P11-2
Ion Polarity Dependent Voltage Shifts of SiGe Membrane for pH Sensor
C. S. Lai, C. M. Yang, C. Y. Wang and T. C. Wang, *Chang Gung Univ., Taiwan*

P11-3
Development of DNA chip nanoarray by Fluidic Self-assembly method for Detection of DNA Hybridization
D. K. Kim[1], Y. S. Kwon[2], Y. Takamura[1] and E. Tamiya[1], *[1]JAIST and [2]Dong-A Univ., Japan*

P11-4
Development of Nano-Gap Device for Biosensor
S. Morita, T. Hirokane, T. Takegawa, S. Urabe, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ., Japan*

P11-5
Vacuum Pressure Sensors Using Carbon Nanotubes as Electron Emitters
S. J. Kim[1], N. K. Choi[1], J. O. Jeon[1], S. H. Lee[1] and C. J. Lee[2], *[1]Kyungnam Univ. and [2]Hanyang Univ., Korea*

P11-6
Improvement of Breakdown Field of Carbon Nanotubes by a Ti-Capping Layer on Catalyst Nanopaticles
R. L. Lai[1], Y. R. Chang[1], C. P. Juan[1], T. Y. Chuang[1], K. C. Lin[1], J. K. Shiu[1], H. C. Tai[1], K. H. Chen[2], L. C. Cheng[3] and H. C. CHENG[1], *[1]National Chiao Tung Univ., [2]Inst. of Atomic and Molecular Sciences, Academia Sinica and [3]National Taiwan Univ., Taiwan*

P11-7
Fabrication InGaN Nano-disk Structure in GaN Reverse Hexagonal Pyramid
C. F. Lin, J. J. Dai, Z. J. Yang and J. H. Zheng, *National Chung Hsing Univ., Taiwan*

P11-8
Fabrication the Nanoporous InGaN-based Light-Emitting Diodes
C. F. Lin, J. H. Zheng, Z. J. Yang and J. J. Dai, *National Chung Hsing Univ., Taiwan*

P11-9
Fast and Accurate Simulation for Topography in Nanometer Semiconductor Process
J. G. Lee and T. Won, *Inha Univ., Korea*

Thursday, September 15

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-7: Metal Gates I
(9:15-10:25)
Chairs: Y. Tsunashima (Toshiba)
R. M. Wallace (Univ. of Texas at Dallas)

9:15 A-7-1 (Invited)
Metal Gate Electodes Formed by Atomic Layer Deposition
G. Parsons, *North Carolina State Univ., USA*

9:45 A-7-2
Material Characterization of Metal-germanide Gate Electrodes Formed by FUGE (Fully Germanided) Process
Y. Tsuchiya, M. Koyama, J. Koga and A. Nishiyama, *Toshiba Corp., Japan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-7: Carrier Transport II
(9:15-10:15)
Chairs: Y. Momiyama (Fujitsu)
H. Oda (Renesas)

9:15 B-7-1
Advanced split-CV technique for accurate extraction of inversion layer mobility in short channel MOSFETs
H. Irie and A. Toriumi, *Univ. of Tokyo, Japan*

9:35 B-7-2
Improved oxidation-induced Ge condensation technique by using H^+ irradiation and post-annealing for highly stress-relaxed ultrathin SGOI
M. Ikishima[1], I. Tsunoda[1], T. Sadoh[1], T. Enokida[2], M. Ninomiya[3], M. Nakamae[3] and M. Miyao[1], *[1]Kyushu Univ., [2]Fukuryo Semicon and [3]SUMCO, Japan*

Room 502 (C)

Joint Area 1, 2 and 3

C-7: Germanide and Defects
(9:15-10:15)
Chairs: M. Kodera (Toshiba)
M. Matsuura (Renesas)

9:15 C-7-1
Material and Electrical Characterization of Nickel Germanide for p-channel Germanium Schottky Source/Drain Transistors
R. T. P. Lee[1,2], S. L. Liew[1], B. Balakrisnan[1], K. Y. Lee[1], Y. C. Yeo[2] and D. Z. Chi[1], *[1]Inst. of Materials Research and Engineering and [2]National Univ. of Singapore, Singapore*

9:35 C-7-2
Highly Thermal Immune Ni GermanoSilicide with Nitrogen-Doped Ni and Co/TiN Double Capping Layer for Nano-Scale CMOS Applications
S. Y. Oh[1], J. G. Yun[1], Y. J. Kim[1], W. J. Lee[1], H. H. Ji[1], T. Agchbayar[1], U. S. Kim[2], H. S. Cha[2], S. B. Heo[2], Y. J. Cho[3], K. J. Han[3], Y. C. Kim[3], J. S. Wang[4] and H. D. Lee[1], *[1]Chungnam National Univ., [2]MagnaChip Semiconductor Ltd. and [3]Korea Univ. of Technology and Education, Korea*

Room 503 (D)

Area 5: Advanced Circuits and Systems

D-7: Mixed-Signal Design
(9:15-10:25)
Chairs: H. Yamauchi (Sanyo Electric)
T. Komuro (Agilent Technologies International Japan)

9:15 D-7-1 (Invited)
Issues of Mixed-Signal Circuit Design in 90nm CMOS LSI Technology
T. Iida[1], H. Ishii[2], T. Nakao[2] and N. Hamanishi[2], *[1]STARC and [2]Semiconductor Company, Toshiba Corp., Japan*

9:45 D-7-2
A 6-bit A/D Converter for MEMS-control circuit
J. Terada, M. Urano, J. Kodate, S. Mutoh and K. Machida, *NTT, Japan*

Room 504 (E)

Room 505 (F)

Area 10: Organic Materials Science, Device Physics, and Applications

F-7: Organic Light Emitting Devices I
(9:15-10:30)
Chairs: T. Kamata (AIST)
T. Sano (Sanyo Electric)

9:15 F-7-1 (Invited)
Tetrabenzoporphyrin Organic Semiconductors for Flexible Organic Thin Film Transistors and Circuits
J. Kanicki[1], P. B. Shea[1] and N. Ono[2], *[1]Univ. of Michigan and [2]Ehime Univ., USA*

9:45 F-7-2
Top-Emission Inverted Organic Light Emitting Diode Using Aluminum Nitride Buffer Layer
C. C. Tseng, F. S. Juang and T. S. Liu, *National Formosa Univ., Taiwan*

Room 401 (G)

Joint Area 8 and 9

G-7: Joint Session Nanotubes and Nanowires I
(9:15-10:45)
Chairs: K. Matsumoto (Osaka Univ.)
M. Nihei (Fujitsu Labs.)

9:15 G-7-1 (Invited)
Revolution in Carbon Nanotube Synthesis - "Super Growth"
D. N. Futaba, K. Hata, K. Mizuno, T. Yamada, T. Namai, Y. Hayamizu, M. Yumura and S. Iijima, *National Inst. of Advanced Industrial Science and Technology, Japan"*

9:45 G-7-2
Single Walled Carbon Nanotubes Grown by Chemical Vapour Deposition: Structures and Devices for Transport and Optics
D. G. Austing, P. Finnie and J. Lefebvre, *National Research Council of Canada, Canada*

Room 402 (H)

Area 4: Advanced Memory Technology

H-7: FeRAM I
(9:15-10:25)
Chairs: H. S. Jeong (Samsung Electronics)
T. Eshita (Fujitsu)

9:15 H-7-1 (Invited)
Current Development Status and Future Challenge of FeRAM Technologies
S. Y. Lee and K. Kim, *Samsung Electronics Co. Ltd., Korea*

9:45 H-7-2
Highly Reliable 0.15μm/14F^2 Cell FRAM Capacitor using $SrRuO_3$ Buffer Layer
J. E. Heo, B. J. Bae, D. C. Yoo, S. D. Nam, J. E. Lim, D. H. Im, S. O. Park, H. S. Kim, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*

Room 403 (I)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

I-7: Modeling and Simulation
(9:15-10:30)
Chairs: K. Maezawa (Nagoya Univ.)
S. Tanaka (NEC)

9:15 I-7-1 (Invited)
Simulation of AlGaN/GaN Heterostructure Field Effect Transistors
N. Braga[1], R. Mickevicius[1], W. Fichtner[1], R. Gaska[2], M. S. Shur[3], G. Simin[4] and M. A. Khan[4], *[1]Synopsys, Inc., [2]Sensor Electronic Technology Inc., [3]Rensselaer Polytechnic Inst. and [4]Univ. of South Carolina, USA*

9:45 I-7-2
Characterization and Modeling of Microwave Noise in InP/InGaAs Composite Channel High Electron Mobility Transistors (HEMTs)
Y. Liu, H. Wang and R. Zeng, *Nanyang Technological Univ., Singapore*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
10:05 A-7-3 Area Selective Flash Lamp Post-Deposition Annealing of High-k Film Using Si Photo Absorber for Metal Gate MISFETs with NiSi Source/Drain T. Matsuki, I. Nishimura, Y. Akasaka, K. Hayashi, M. Noguchi, K. Yamashita, K. Torii, N. Kasai and Y. Nara, *SELETE, Japan*	**9:55 B-7-3** High Mobility Fully-Depleted Germanium-on-Insulator pMOSFET with 32-nm-Thick Ge Channel Layer Formed by Ge-Condensation Technique S. Nakaharai[1], T. Tezuka[1], E. Toyoda[2], N. Hirashita[1], Y. Moriyama[1], T. Maeda[3], T. Numata[1], N. Sugiyama[1] and S. Takagi[3,4], *[1]MIRAI-ASET, [2]Toshiba Ceramics, [3]MIRAI-AIST and [4]Univ. of Tokyo, Japan*	**9:55 C-7-3** Theoretical Investigation of Neutral Point Defects in $CoSi_2$ T. Wang, Y. H. Son, H. S. Joo, Y. J. Kim, I. S. Han and H. D. Lee, *Chungnam National Univ., Korea*	**10:05 D-7-3** Low Power and High Sensitivity MRAM Sensing Scheme with Body Biased Preamplifier T. Sugimura, J. Deguchi, H. Choi, T. Sakaguchi, H. Oh, T. Fukushima and M. Koyanagi, *Tohoku Univ., Japan*

Break

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
	10:00 F-7-3 Improvements in the Characteristics of Blue Polymer Light-emitting Diodes by Polymer Hole Transport Layer J. Li, T. Sano, Y. Hirayama, T. Tomita, H. Fujii and K. Wakisaka, *Sanyo Electric Company, Japan*	**10:00 G-7-3** Air-Stable p-Type and n-Type Carbon Nanotube Field-Effect Transistors with Top-Gate Structure on SiN_x Passivation Films Formed by Catalytic Chemical Vapor Deposition D. Kaminishi[1], H. Ozaki[1], Y. Ohno[1], K. Maehashi[1], K. Inoue[1], K. Matsumoto[1], Y. Seri[2], A. Masuda[2], H. Matsumura[2] and T. Niki[3], *[1]Osaka Univ., [2]JAIST and [3]Ishikawa Seisakusho, Ltd., Japan*	**10:05 H-7-3** Bit Distribution and Reliability of High Density 1.5V FRAM Embedded with 130nm, 5LM Copper CMOS Logic K. R. Udayakumar, K. Boku, K. A. Remack, J. Rodriguez, S. R. Summerfelt, F. G. Celii, S. Aggarwal, J. S. Martin, L. Hall, L. Matz, B. Rathsack, H. McAdams and T. S. Moise, *Texas Instruments, USA*	**10:00 I-7-3** Low-Field Electron Mobility Models for Bulk GaN and AlGaN/GaN 2DEGs F. Schwierz, *Techn. Univ., Germany*
	10:15 F-7-4 The Improvement of Luminance Efficiency by the Insertion of Buffer layers in Flexible Organic Light-Emitting Diodes T. H. Yang[1], F. S. Juang[1], Y. S. Tsai[1] and M. Yokoyama[2], *[1]National Formosa Univ., [2]I-Shou Univ., Taiwan*	**10:15 G-7-4** Topographic and Conductive AFM Measurements on Carbon Nanotube Field-Effect Transistors Fabricated by In-situ Chemical Vapor Deposition L. Rispal, Y. Stefanov, R. Heller, G. Tzschöckel, G. Hess, K. Haberle and U. Schwalke, *Darmstadt Univ. of Technology, Germany*		**10:15 I-7-4** Theoretical Analysis of Breakdown Characteristics for Recessed Gate GaAs MESFETs T. Shugo, D. Macarambon Jr. and M. Kuzuhara, *Univ. of Fukui, Japan*
		10:30 G-7-5 Fermi Level Modulation of n-type Doped Single Walled Carbon Nanotube using Buried Local-Gate FET Structure by Oxygen Ion Implantation with Ultra-low Energy Ion Beam of 25eV T. Kamimura[1,2], K. Yamamoto[2,3], and K. Matsumoto[1,2,3], *[1]Osaka Univ., [2]CREST-JST and [3]AIST, Japan*		

Break

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-8: Metal Gates II
(10:45-12:05)
Chairs: T. Aoyama (Fujitsu Labs.)
G. Parsons (North Carolina State Univ.)

10:45 A-8-1
$Mo_xSi_yN_z$ Metal Gate Electrode with Tunable Work Function for Advanced CMOS
P. Zhao[1], J. Kim[2], M. J. Kim[1], B. E. Gnade[1] and R. M. Wallace[1], *[1]Univ. of Texas at Dallas and [2]Kookmin Univ., USA*

11:05 A-8-2
Ta-based metal gates (Ta, TaB_x, TaN_x and TaC_x) -Modulated Work Function and Improved Thermal Stability-
R. Ichiahra, Y. Tsuchiya, Y. Kamimuta, M. Koyama and A. Nishiyama, *Toshiba Corp., Japan*

11:25 A-8-3
Gate Depletion Effect Reduction and Flat-band Voltage Control in Poly-Si/$HfAlO_x$ MOSFETs with Nanometer TaN Dots at the Top Interface
H. Fujiwara[1], M. Kadoshima[1], H. Ota[2], H. Takaba[1], N. Mise[1], H. Satake[1], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC-AIST and [3]Univ. of Tokyo, Japan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-8: Device Reliability
(10:45-12:15)
Chairs: D. Hisamoto (Hitachi)
K. Kurimoto (Matsushita Electric)

10:45 B-8-1 (Invited)
Explanation of Negative Bias Temperature Instability Mechanism in p-MOSFETs by Reaction-Diffusion Model
S. Mahapatra, S. Sharma P. B. Kumar, D. Varghese, D. Saha, *IIT Bombay, India*

11:15 B-8-2
Influence of bulk bias on NBTI of pMOSFETs with ultra-thin SiON gate dielectric
S. Zhu[1], A. Nakajima[1], T. Ohashi[2] and H. Miyake[2], *[1]Hiroshima Univ. and [2]Elpida Memory, Inc., Japan*

11:35 B-8-3
Devices Characteristics and Aggravated Negative Bias Temperature Instability in PMOSFETs with Uniaxial Compressive Strain
C. Y. Lu, H. C. Lin, Y. F. Chang and T. Y. Huang, *National Chiao Tung Univ., Taiwan*

Room 502 (C)

Joint Area 1, 2 and 3

C-8: Advanced Source/Drain Technology
(10:45-12:15)
Chairs: K. Ohuchi (Toshiba)
Y. Nara (Selete)

10:45 C-8-1 (Invited)
Current Status and Forecast in High-Performance CMOS Device Technology
T. Sugii, *Fujitsu Ltd., Japan*

11:15 C-8-2
Buried Epitaxial, $Si_{1-y}C_y$ (y = 0.07%) for the Suppression of Leakage in SPER (550°C 10 mins) Activated Junctions and Current Drive Enhancement in nMOSFET
C. F. Tan[1], E. F. Chor[1], H. Lee[2], J. Liu[2], E. Quek[2] and L. Chan[2], *[1]National Univ. of Singapore and [2]Chartered Semiconductor Manufacturing, Singapore*

11:35 C-8-3
Gate Overlapped Raised Extension Structure (GORES) MOSFET by Using In-situ Doped Selective Si Epitaxy
Y. Tateshita[1], T. Imoto[1], Y. Kikuchi[1], J. Wang[1], T. Kataoka[1], Y. Miyanami[1], H. Ikeda[1], S. Fujita[1], T. Landin[2], C. Arena[2], H. Iwamoto[1], T. Ohno[1], T. Kobayashi[1], M. Saito[1], S. Kadomura[1] and N. Nagashima[1], *[1]Sony Corp. and [2]ASM America Inc., Japan*

Room 503 (D)

Area 5: Advanced Circuits and Systems

D-8: High-Frequency Circuits
(10:45-12:05)
Chairs: R. Fujimoto (Toshiba)
M. Mizuno (NEC)

10:45 D-8-1
A Spurious Suppression Technique for Fractional-N Frequency Synthesizers
R. Tachibana, Y. Shimizu, S. Ishizuka and H. Masuoka, *Toshiba Corp., Japan*

11:05 D-8-2
Design of Differential Transformer Balun and Its Application to CMOS LNA
Y. J. Lee[1], J. J. Kim[2] and H. K. Yu[1], *[1]ETRI and [2]MagnaChip Semiconductor Ltd., Korea*

11:25 D-8-3
Design of I-Q down-converter in CMOS for wireless network application
T. H. Teo, Y. Z. Xiong, *Inst. of Microelectronics, Singapore*

Room 504 (E)

Room 505 (F)

Area 10: Organic Materials Science, Device Physics, and Applications

F-8: Organic Light Emitting Devices II
(10:45-12:15)
Chairs: H. Usui (Tokyo Univ. of Agri. & Tech.)
T. Sano (Sanyo Electric)

10:45 F-8-1
Experimental Study of Chemical Reaction between LiF and Polyflourene Interface During Sputtering ITO Cathode for Top Emission PLED Devices
C. W. Teng, C. C. Lee and K. C. Liu, *Chang Gung Univ., Taiwan*

11:00 F-8-2
Effects of thickness of organic and multi-layer anode on luminance efficiency in top-emission oraganic light-emitting diodes
S. J. Lin[1], H. Y. Ueng[1] and F. S. Juang[2], *[1]Univ. of Sun Yat-Sen and [2]Univ. of Formosa, Taiwan*

11:15 F-8-3
Transparent barrier coatings for flexible organic light-emitting diode applications
D. S. Wuu[1], T. N. Chen[1], C. C. Chiang[1], C. C. Wu[1], H. B. Lin[1], Y. P. Chen[1], W. C. Chen[1] and F. S. Juang[2], *[1]National Chung Hsing Univ. and [2]National Formosa Univ., Taiwan*

Room 401 (G)

Joint Area 8 and 9

G-8: Joint Session Nanotubes and Nanowires II
(10:00-12:30)
Chairs: K. Ishibashi (RIKEN)
Z. K. Tang (Hong Kong Univ. of Science)

11:00 G-8-1 (Invited)
to be announced
Z. K. Tang, *Hong Kong Univ. of Science & Technology, China*

Room 402 (H)

Area 4: Advanced Memory Technology

H-8: FeRAM II
(10:45-12:05)
Chairs: T. Eshita (Fujitsu)
N. Ishiwata (NEC)

10:45 H-8-1
Fabrication and Characterization of Ferroelectric Gate Field Effect Transistor Memory Based on Ferroelectric-Insulator Interface Conduction
B. Y. Lee, S. Ikemori, M. Noda and M. Okuyama, *Osaka Univ., Japan*

11:05 H-8-2
Study of the Metal-Ferroelectric-Insulator-Si Structure Device Formation by Controlling Properties of High Frequency and Microwave Excited Plasma
I. Takahashi, H. Sakurai, T. Isogai, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

Room 403 (I)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

I-8: Modeling and Simulation
(10:45-11:30)
Chairs: K. Maezawa (Nagoya Univ.)
S. Tanaka (NEC)

10:45 I-8-1
Analysis of Trap-Parameter Dependence of Lag Phenomena and Current Collapse in GaN FETs
H. Takayanagi, H. Nakano, K. Itagaki and K. Horio, *Shibaura Inst. of Tech., Japan*

11:00 I-8-2
Extraction of an Empirical Temperature-Dependence InGaP/GaAs HBT Large-Signal Model
D. M. Lin, F. H. Hang, M. W. Hsieh, H. P. Wang and Y. J. Chan, *National Central Univ., Taiwan*

11:15 I-8-3
Noise Analysis of Nitride-based MOS-HFETs with Photo-chemical Vapor Deposition SiO_2 Gate Oxide in the Linear and Saturation Region
C. K. Wang[1], S. J. Chang[1], Y. K. Su[1], Y. Z. Chiou[2], T. K. Lin[1], T. K. Ko[1], H. L. Liu[1] and J. J. Tang[2], *[1]National Cheng Kung Univ. and [2]Southern Taiwan Univ. of Technology, Taiwan*

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
11:45 A-8-4 Low temperature divided CVD technique for TiN metal gate electrodes of p-MISFETs S. Sakashita[1], K. Mori[1], K. Tanaka[2], M. Mizutani[1], M. Inoue[1], S. Yamanari[1], J. Yugami[1], H. Miyatake[1] and M. Yoneda[1], *[1]Renesas Technology Corp. and [2]Renesas Semiconductor Engineering, Japan*	**11:55 B-8-4** A Comprehensive Study of Hot-Carrier Effects in Body-Tied FinFETs J. W. Han[1], C. H. Lee[2], D. Park[2] and Y. K. Choi[1], *[1]KAIST and [2]Samsung Electronics Co. Ltd., Korea*	**11:55 C-8-4** A Double-Gate device architecture optimization for sub-45nm digital CMOS technologies using cell-based timing analysis R. Surdeanu, G. Doornbos, R. Ng, P. Christie, V. H. Nguyen, B. J. Pawlak, J. J. G. P. Leo, M. J. H. vanDal and Y. L. Ponomarev, *Philips Research Leuven, Belgium*	**11:45 D-8-4** Zero-Crosstalk Bus Line Structure for Global Interconnects in Si ULSI M. Kimura, H. Ito, H. Sugita, K. Okada and K. Masu, *Tokyo Tech, Japan*

12:30–13:30 SSDM 2005 Luncheon (PORTOPIA HOTEL Room KAIRAKU, B1F)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
	11:30 F-8-4 Microscopic EL spectral imaging in polymer-blend light emitting diodes N. Takada and T. Kamata, *AIST, Japan*	**11:30 G-8-2** Electronic and Structural Properties of Organic Molecules inside Carbon Nanotube R. V. Belosludov, H. Mizuseki, T. Takenobu, Y. Iwasa and Y. Kawazoe, *Tohoku Univ., Japan*	**11:25 H-8-3** Bismuth Ferrite Thin Films for Advanced FeRAM Devices S. K. Singh and H. Ishiwara, *Tokyo Tech, Japan*	
	11:45 F-8-5 White Light-Emitting Device on Flexible Plastic Substrates H. Lee and J. Kanicki, *Univ. of Michigan, USA*	**11:45 G-8-3** Direct Ultrasensitive DNA Sensors Based on Carbon Nanotube Field-Effect Transistors K. Maehashi[1], K. Matsumoto[1], K. Kerman[2], Y. Takamura[2] and E. Tamiya[2], *[1]Osaka Univ. and [2]JAIST, Japan*	**11:45 H-8-4** Multi-bit Programming for 1T-FeRAM by Local Polarization Method Y. Tabuchi[1], S. Hasegawa[1], T. Tamura[2], H. Hoko[2], K. Kato[3], Y. Arimoto[2] and H. Ishiwara[1], *[1]Tokyo Tech, [2]Fujitsu Labs. Ltd. and [3]AIST, Japan*	
	12:00 F-8-6 Study on characteristics of electroluminescence based on Zn complexes O. K. Kwon[1], Y. K. Jang[1], B. J. Lee[2] and Y. S. Kwon[1], *[1]Dong-A Univ. and [2]Inje Univ., Korea*	**12:00 G-8-4** Development of an Ultrasensitive Gas Sensor Based on Single-Walled Carbon Nanotubes W. Wongwiriyapan[1], S. Honda[1], H. Konishi[1], T. Mizuta[1], T. Ohmori[1], T. Ito[2], T. Maekawa[2], K. Suzuki[2], H. Ishikawa[2], T. Murakami[3], K. Kisoda[4], H. Harima[3], K. Oura[1] and M. Katayama[1], *[1]Osaka Univ., [2]New Cosmos Electric Co., Ltd., [3]Kyoto Inst. of Technology and [4]Wakayama Univ., Japan* **12:15 G-8-5** Precise Control of Island Size for Carbon Nanotube Single Electron Transistor operating at Room Temperature by AFM Electrical Manipulation C. K. Hyon[1,2], T. Kamimura[1,4], M. Maeda[1,3] and K. Matsumoto[1,2,4], *[1]CREST-JST, [2]AIST, [3]Univ. of Tsukuba and [4]Osaka Univ., Japan*		

12:30–13:30 SSDM 2005 Luncheon (PORTOPIA HOTEL Room KAIRAKU, B1F)

Room 301 (A)

Area 1: Advanced Gate Stack / Si Processing Science

A-9: GeFETs & Simulation
(13:30-14:50)
Chairs: K. Shiraishi (Univ. of Tsukuba)
J. Yugami (Renesas)

13:30 A-9-1
Influences of Activation Annealing on Characteristics of Ge p-MOSFET with ZrO_2 Gate Dielectric
Y. Kamata, Y. Kamimuta, T. Ino, R. Iijima, M. Koyama and A. Nishiyama, *Toshiba Corp., Japan*

13:50 A-9-2
Thermally Robust Y_2O_3/Ge MOS Capacitors
H. Nomura, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

14:10 A-9-3
First-principles studies on metal induced gap states (MIGS) at metal/high-*k* HfO_2 interfaces
T. Nakaoka[1], K. Shiraishi[1,2], Y. Akasaka[3], T. Chikyow[2], K. Yamada[4,2] and Y. Nara[3], *[1]Univ. of Tsukuba, [2]NIMS, [3]SELETE and [4]Waseda Univ., Japan*

Room 501 (B)

Area 3: CMOS Devices / Device Physics

B-9: Device Technology I
(13:30-14:50)
Chairs: K. Takeuchi (NEC)
K. Shibahara (Hiroshima Univ.)

13:30 B-9-1
Efficient Reduction of Standby Leakage Current in LSIs for Use in Mobile Devices
H. Kudo[1], K. Ishikawa[1], Y. Mishima[1], S. Satou[1], F. Kihare[2], M. Okamoto[2], T. Ito[2], Y. Suzuki[2], T. Nomura[2], M. Kawano[2], K. Nishikawa[2] and Y. Ozaki[2], *[1]Fujitsu Labs. Ltd. and [2]Fujitsu Ltd., Japan*

13:50 B-9-2
Reliability and Memory Characteristics of Sequential Laterally Solidified LTPS Poly-Si TFT with a ONO Stack Gate Dielectric
S. I. Hsieh[1], Y. C. King[1], H. T. Chen[2], Y. C. Chen[2], C. L. Chen[2] and J. X. Lin[2], *[1]National Tsing-Hua Univ. and [2]Industrial Technology Research Inst., Taiwan*

14:10 B-9-3
Direct measurement of the offset spacer effect on the carrier profiles in sub-50 nm p-MOSFETs
H. Fukutome[1], T. Saiki[2], R. Nakamura[2], A. Usujima[2] and T. Aoyama[1], *[1]Fujitsu Labs. Ltd. and [2]Fujitsu Ltd., Japan*

Room 502 (C)

Joint Area 1, 2 and 3

C-9: Shallow Junction
(13:30-14:50)
Chairs: H. Hwang (Gwangju Inst. of Sci. & Tech.)
B. Mizuno (UJT Lab.)

13:30 C-9-1
Dopant Redistribution at Nickel Silicide/Silicon Interface
T. Yamauchi[1], A. Kinoshita[1], K. Ohuchi[2] and K. Kato[1], *[1]Toshiba Corp. and [2]Semiconductor Company, Toshiba Corp., Japan*

13:50 C-9-2
Integration of ultra shallow junctions in PVD TaN nMOS transistors with Flash Lamp Annealing
S. Severi[1,2], K. De Meyer[1,2], B. J. Pawlak[3], R. Duffy[3], C. Kerner[1], S. McCoy[4], J. Gelpey[4], T. Salinger[4], L. A. Ragnasson[1], P. P. Absil[1], M. Jurczak[1] and S. Biesemans[1], *[1]IMEC, [2]Katholieke Univ. Leuven, [3]Philips and [4]Vortek Industries, Belgium*

14:10 C-9-3
Ultra Shallow Junction Formation Using Plasma Doping and Laser Annealing for Sub-65 nm Technology Nodes
G. H. Yon, S. J. Hong, G. H. Buh, T. S. Park, Y. G. Shin, U. I. Chung and J. T. Moon, *Samsung Electronics Co. Ltd., Korea*

Room 503 (D)

Area 5: Advanced Circuits and Systems

D-9: Device Characteristics and Circuits
(13:30-14:50)
Chairs: T. Hamasaki (Texas Instruments Japan)
K. Masu (Tokyo Tech)

13:30 D-9-1
Development of an Integrated RF Impedance Matching Device with LPF Function using a CoFeB Magnetic/Polyimide Dielectric Hybrid Thin-Film Coplanar-Line
H. Nakayama[1,2], T. Yamamoto[2], Y. Mizoguchi[2], T. Sato[2], K. Yamasawa[2], Y. Miura[2], Y. Miyake[3], M. Akie[3], Y. Uehara[3], M. Munakata[4] and M. Yagi[4], *[1]Nagano National College of Technology, [2]Shinshu Univ., [3]Fujitsu Ltd. and [4]Sojo Univ., Japan*

13:50 D-9-2
A Logarithmic Response CMOS Image Sensor with Parasitic PNP BJT
C. H. Lai, L. W. Lai and Y. C. King, *National Tsing-Hua Univ., Taiwan*

14:10 D-9-3
Neutron-induced Soft-Error Simulation Technology for Logic Circuits
T. Uemura, Y. Tosaka and S. Satoh, *Fujitsu Labs. Ltd., Japan*

Room 504 (E)

Room 505 (F)

Area 10: Organic Materials Science, Device Physics, and Applications

F-9: Organic Transistors I
(13:30-15:00)
Chairs: K. Kudo (Chiba Univ.)
H. Usui (Tokyo Univ. of Agri. & Tech.)

13:30 F-9-1 (Invited)
Organic Thin-film Transistors Based on n-type Organic Semiconductors
S. Tokito, *NHK, Japan*

14:00 F-9-2
Pentacene thickness dependence of FET properties in bottom contact structure; Estimation of the effective channel thickness
E. Lim, T. Manaka, R. Tamura and M. Iwamoto, *Tokyo Tech, Japan*

14:15 F-9-3
Field-assisted Electron Injection Current in Submicron Pentacene Transistors
J. Jo[1,2], J. J. Heremans[2], F. Bradbury[2], H. Chen[2] and V. Soghomonian[2], *[1]Ajou Univ. and [2]Ohio Univ., Korea*

Room 401 (G)

Joint Area 8 and 9

G-9: Joint Session Nanotubes and Nanowires III
(13:30-15:00)
Chairs: T. Fukui (Hokkaido Univ.)
K. Yamaguchi (Univ. of Electro-Communications)

13:30 G-9-1
Multi-quantum structures of GaAs/AlGaAs Free-standing Nanowires
K. Tateno[1], H. Gotoh[1] and Y. Watanabe[2], *[1]NTT Basic Research Labs. and [2]NTT Advanced Technology, Japan*

13:45 G-9-2
Analysis of Structure and Orientation of Vertical Germanium Single Crystal Nanowires on Silicon Substrates
H. Jagannathan[1], H. Kim[2], M. Deal[1], P. C. McIntyre[1] and Y. Nishi[1], *[1]Stanford Univ. and [2]Sungkyunkwan Univ., USA*

14:00 G-9-3
Photocurrent of Single Silicon Nanowire synthesized by Thermal Chemical Vapor Deposition
K. H. Kim[1], K. Keem[1], J. Kang[1], C. Yoon[1], D. Y. Jeong[1], B. Min[1], K. Cho[1], S. Kim[1] and M. Suh[2], *[1]Korea Univ. and [2]Samsung Electronics Co. Ltd., Korea*

Room 402 (H)

Area 4: Advanced Memory Technology

H-9: MRAM
(13:30-15:00)
Chairs: N. Ishiwata (NEC)
Y. Ohji (Renesas)

13:30 H-9-1 (Invited)
Overview and Future Challenge of MRAM Technologies
S. Tehrani, J. M. Slaughter, B. Engel, M. Durlam, N. Rizzo, R. Dave, J. Sun and J. Janesky, *Freescale Semiconductor, USA*

14:00 H-9-2
A Novel MTJ Shape with Large Write Operation Margin for High Density MRAM
Y. Sato, S. Yagaki, C. Yoshida, K. Kobayasi, M. Aoki and H. Tanaka, *Fujitsu Labs. Ltd., Japan*

Room 403 (I)

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
14:30 A-9-4 Theoretical analysis of the Fermi level pinning in HfO_2/Si system induced by the interface defect states M. Ikeda[1], G. Kresse[2], T. Nabatame[1] and A. Toriumi[3,4], *[1]MIRAI-ASET, [2]Univ. of Vienna, [3]MIRAI-AIST and [4]Univ. of Tokyo, Japan*	**14:30 B-9-4** Degradation of Current Drivability of Schottky Source/Drain Transistors with High-k Gate Dielectrics and Possible Measures to Suppress the Phenomenon M. Ono, A. Nishiyama and M. Koyama, *Toshiba Corp., Japan*	**14:30 C-9-4** Function of Phase Switch Layer for Ultra Shallow Junction Formation by Green Laser Annealing A. Matsuno[1,2] and K. Shibahara[1], *[1]Hiroshima Univ. and [2]Phoeton Corp., Japan*	**14:30 D-9-4** Mismatches under the Impact of Hot Carrier Stress in 0.15 μm Technology J. C. Lin[1,3], S. Y. Chen[2], H. W. Chen[2], H. C. Lin[2], Z. W. Jhou[2], S. Chou[1], J. Ko[1], T. F. Lei[3] and H. S. Haung[2], *[1]United Microelectronics Corp., [2]National Taipei Univ. of Technology and [3]National Chiao Tung Univ., Taiwan*

Break

Area 3: CMOS Devices / Device Physics	Area 1: Advanced Gate Stack / Si Processing Science	Area 5: Advanced Circuits and Systems
B-10: Device Technology II (15:15-16:15) Chairs: H. Oda (Renesas) K. Takeuchi (NEC)	C-10: Metal Gates III (15:15-16:35) Chairs: R. M. Wallace (Univ. of Texas at Dallas) T. Aoyama (Fujitsu Labs.)	D-10: Power Devices and Packaging Technologies (15:15-16:25) Chairs: T. Komuro (Agilent Technologies International Japan) T. Hamasaki (Texas Instruments Japan)

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
	14:30 F-9-4 Study on the Carrier Transport of Pentacene Thin Film Transistor at High Temperatures P. Y. Lo, Z. Pei, J. J. Hwang and Y. J. Chan, *INST., Taiwan*	**14:15 G-9-4** Transport and Back-Gated Field Effect Characteristics of Si Nanowires formed by Stress-Limited Oxidation A. Agarwal[1], T. Y. Liow[1,2], R. Kumar[1], C. H. Tung[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore, Singapore*	**14:20 H-9-3** Self-aligned MTJ etching technique using side walls for high-density $8F^2$ MRAMs M. Yoshikawa[1], M. Amano[1], T. Ueda[1], E. Kitagawa[1], S. Takahashi[1], T. Kai[1], T. Kishi[1], N. Shimomura[1], H. Aikawa[1], T. Kajiyama[1], K. Hosotani[1], Y. Asao[1], K. Suemitsu[2], H. Hada[2], S. Tahara[2] and H. Yada[1], *[1]Toshiba Corp. and [2]NEC Corp., Japan*	
	14:45 F-9-5 Device Characteristics of FETs Made From a p-doped Polythiophene Solution S. Hoshino, M. Yoshida, S. Uemura, T. Kodzasa and T. Kamata, *AIST, Japan*	**14:30 G-9-5** The Influence of Oxygen Concentration in the Sputtering Gas on the Self-synthesis of Tungsten Oxide Nanowires on Sputter-deposited Tungsten Films S. J. Wang, C. H. Chen, R. M. Ko, Y. C. Kuo and Y. Y. Wang, *National Cheng Kung Univ., Taiwan*	**14:40 H-9-4** New Magnetic Flash Memory with FePt Magnetic Floating Gate C. K. Yin[1], J. C. Bea[2], Y. G. Hong[1], M. Miyao[3], K. Natori[4] and M. Koyanagi[1], *[1]Tohoku Univ., [2]JST, [3]Kyushu Univ. and [4]Univ. of Tsukuba, Japan*	
		14:45 G-9-6 Photoresponse of a single ZnO nanowire illuminated by modulated light K. Keem, K. H. Kim, J. Kang, C. Yoon, D. Y. Jeong, B. Min, K. Cho and S. Kim, *Korea Univ., Korea*		

Break

Area 10: Organic Materials Science, Device Physics, and Applications	Area 4: Advanced Memory Technology
F-10: Organic Transistors II (15:15-16:15) Chairs: M. Iwamoto (Tokyo Tech) T. Kamata (AIST)	H-10: PRAM (15:15-16:15) Chairs: Y. Ohji (Renesas) I. Asano (Elpida)

Room 301 (A)	Room 501 (B)	Room 502 (C)	Room 503 (D)
	15:15 B-10-1 Impact of Body Bias Controlling in Partially Depleted SOI Devices with Hybrid Trench Isolation Technology T. Iwamatsu[1], M. Tsujiuchi[1], Y. Hirano[1], T. Ikeda[1], F. Komatsu[2], T. Ipposhi[1], S. Maegawa[1] and Y. Ohji[1], *[1]Renesas Technology Corp. and [2]Renesas Semiconductor Engineering, Japan*	**15:15 C-10-1** Analysis of the Origin of the Threshold Voltage Change Induced by Impurity in Fully Silicided NiSi/SiO_2 gate stacks K. Manabe, K. Takahashi, T. Hase, N. Ikarashi, M. Oshida, T. Tatsumi and H. Watanabe, *NEC Corp., Japan*	**15:15 D-10-1 (Invited)** The High Voltage Anti-Trend C. Mangelsdorf, *Analog Devices Inc., Japan*
	15:35 B-10-2 A High Gain (25%) Strained Silicon Scheme for 65nm High Performance nMOSFETs T. Y. Chang, J. W. Pan, Y. C. Liu, P. W. Liu B. C. Lan, C. H. Tsai, T. F. Chen, C. H. Tung, C. T. Huang, C. T. Tsai and W. T. Shiau, *United Microelectronics Corp., Taiwan*	**15:35 C-10-2** Realization of A Metal Split Gate By Gate Full Ni-Silicidation Process for MOSFET RF/Analog Applications J. Yuan and J. C. S. Woo, *Univ. of California Los Angeles, USA*	**15:45 D-10-2** A New Protection Circuit for improving Short-Circuit Withstanding Capability of Lateral Emitter Switched Thyristor (LEST) Y. H. Choi[1], I. H. Ji[1], B. C. Jeon[1], Y. I. Choi[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Ajou Univ., Korea*
	15:55 B-10-3 Advanced I/O Technology using Laterally Modulated Channel MOSFET for 65-nm Node SoC E. Yoshida[1], Y. Momiyama[2], N. Hasegawa[1], M. Kojima[2], S. Satoh[1], and T. Sugii[1], *[1]Fujitsu Labs. Ltd. and [2]Fujitsu Ltd., Japan*	**15:55 C-10-3** Stress voltage polarity dependent threshold voltage shift behavior of ultrathin Hafnium oxide gated pMOSFET with TiN electrode H. Park[1,4], R. Choi[2], B. H. Lee[3], C. D. Young[2], M. Chang[1], J. C. Lee[4] and H. Hwang[1], *[1]Gwangju Inst. of Science and Technology, [2]International Sematech, [3]IBM and [4]AMRC, UT Asutin, Korea*	**16:05 D-10-3** Wafer-level Fabrication of Compliant Bump N. Watanabe and T. Asano, *Kyushu Inst. Of Technology, Japan*
		16:15 C-10-4 Highly Manufacturable Hf-silicate Technology with Optimized Composition for Gate-First Metal Gate CMOSFET S. C. Song[1], S. H. Bae[1], J. H. Sim[1], G. Bersuker[1], Z. Zhang[2], P. Kirsch[3], P. Majhi[4], N. Moumen[3], P. Zeitzoff[3] and B. H. Lee[3], *[1]Sematech, [2]Texas Instruments, [3]IBM and [4]Intel, USA*	

Room 504 (E)	Room 505 (F)	Room 401 (G)	Room 402 (H)	Room 403 (I)
	15:15 F-10-1 Fabrication of the low operating voltage Poly(3-hexylthiophene) transistor using sputtering $A1_2O_3/HfO_2/A1_2O_3$ stacking insulator C. H. Lin[1], K. C. Li[1], K. C. Liu[1] and J. P. Hu[2], *[1]Chang Gung Univ. and [2]Industrial Technology Research Inst., Taiwan*		**15:15 H-10-1** Highly Reliable Ring Type Contact Scheme for High Density PRAM C. W. Jeong, S. J. Ahn, Y. N. Hwang, Y. J. Song, J. H. Oh, S. H. Lee, K. C. Ryoo, J. H. Park, J. M. Shin, J. H. Park, W. C. Jeong, K. H. Koh, G. T. Jeong, H. S. Jeong and K. N. Kim, *Samsung Electronics Co. Ltd., Korea*	
	15:30 F-10-2 Performance Recovery of n-channel Perfluoropentacene Thin Film Transistors by High Vacuum Annealing T. Yokoyama, T. Nishimura, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*		**15:35 H-10-2** Lower Power and Higher Speed Operations of Phase-Change Memory Device Using Antimony Selenide (Sb_xSe_{1-x}) S. M. Yoon[1], N. Y. Lee[1], S. O. Ryu[1], K. J. Choi[1], Y. S. Park[1], S. Y. Lee[1], B. G. Yu[1], M. J. Kang[2], S. Y. Choi[2] and M. Wuttig[3], *[1]ETRI, [2]Yonsei Univ. and [3]Physikalisches Inst. der RWTH Aachen, Korea*	
	15:45 F-10-3 A pixel circuit for AMOLED consisting of OTFTs and OLED K. B. Choe, H. Jung, G. S. Ryu and C. K. Song, *Dong-A Univ., Korea*		**15:55 H-10-3** Temperature Dependence of Phase Change Random Access Memory Cell X. S. Miao, L. P. Shi, R. Zhao, P. K. Tan, K. G. Lim, J. M. Li and T. C. Chong, *Data Storage Inst., Singapore*	
	16:00 F-10-4 Single Grain and Single Grain Boundary Resistance of Pentacene Thin Film Characterized by Nano-scale Electrode Array T. Edura[1], M. Nakata[1], H. Takahashi[1], H. Onozato[1], J. Mizuno[1], K. Tsutsui[1], M. Haemori[2], K. Itaka[2,3], H. Koinuma[2,3] and Y. Wada[1-3], *[1]Waseda Univ., [2]Tokyo Tech and [3]CREST-JST, Japan*			

ORGANIZING COMMITTEE

Chair: K. Taniguchi (Osaka Univ.)
Vice-Chair: H. Sakaki (Univ. of Tokyo)
Members:

Y. Aoyagi (Tokyo Tech)
T. Asano (Kyusyu Inst. of Tech.)
H. Hasegawa (Hokkaido Univ.)
T. Hattori (Sony)
S. Hiraki (Toshiba)
M. Hirose (AIST)
Y. Horiike (NIMS)
S. Hosaka (Tokyo Electron)
A. Ibaraki (Sanyo Electric)
T. Ikoma (Hitotsubashi Univ.)
H. Ishiwara (Tokyo Tech)
T. Kamiya (National Inst. for Academic Degrees and Univ. Evaluation)
T. Kanayama (AIST)
M. Kanazawa (ASET)
A. Kita (Oki Electric)
M. Nakamura (Hitachi)
K. Natori (Univ. of Tsukuba)
T. Nishimura (Renesas)
M. Ogura (Matsushita Electric)
T. Ohmi (Tohoku Univ.)
F. Sato (NHK)
Y. Shiraki (Musashi Inst. of Tech.)
J. Sone (NEC)
T. Suga (Univ. of Tokyo)
K. Tada (Kanazawa Inst. of Tech.)
A. Takahashi (Sharp)
H. Takasu (ROHM)
H. Takayanagi (NTT)
E. Takeda (Hitachi)
K. Tsubouchi (Tohoku Univ.)
H. Tsuchikawa (Fujitsu Labs.)
J. Ueda (Semiconductor Industry Res. Inst. Japan)
H. Watanabe (Selete)
Y. Yasuda (Kochi Univ. of Tech.)

INTERNATIONAL ADVISORY COMMITTEE

D. Antoniadis (MIT)
C. Y. Chang (National Chiao Tung Univ.)
G. Declerck (IMEC)
L. Eaves (Univ. of Nottingham)
L. Esaki (Shibaura Inst. of Tech.)
J. S. Harris (Stanford Univ.)
K. v. Klitzing (Max-Planck-Inst.)
Z. J. Li (Tsinghua Univ.)
S. Namba (Nagasaki Inst. of Applied Science)
Y. Nishi (Stanford Univ.)
K. H. Ploog (Paul-Drude-Inst.)
T. Sugano (Toyo Univ.)
K. Takahashi (Teikyo Univ. of Sci. & Tech.)
S. Tanaka (SRL)

STEERING COMMITTEE

Chair: M. Morita (Osaka Univ.)
Vice-Chair: T. Hiramoto (Univ. of Tokyo)
Secretary: Y. Fujiwara (Osaka Univ.)
Members:
K. Eriguchi (Kyoto Univ.)
Y. Kamakura (Osaka Univ.)
S. Maekawa (Renesas)
M. Nagata (Kobe Univ.)
A. Sakai (Nagoya Univ.)
Y. Setsuhara (Osaka Univ.)
H. Tabata (Osaka Univ.)
T. Takahashi (Univ. of Tokyo)
Y. Uraoka (NAIST)

PROGRAM COMMITTEE

Chair: A. Toriumi (Univ. of Tokyo)
Vice-Chair: Y. Hirayama (NTT), H. Matsuoka (Hitachi), K. Kim (Samsung Electronics)
Secretary: T. Ichiki (Univ. of Tokyo)

Subcommittee Members:

[1] Advanced Gate Stack / Si Processing Science
Chair: Y. Nara (Selete)
Members: T. Aoyama (Fujitsu Labs.), H. Hwang (Gwangju Inst. of Sci. & Tech.), S. Miyazaki (Hiroshima Univ.), B. Mizuno (UJT Lab.), A. Sakai (Nagoya Univ.), H. Satake (ASET), K. Shiraishi (Univ. of Tsukuba), Y. Tsunashima (Toshiba), R. M. Wallace (Univ. of Texas at Dallas), J. Yugami (Renesas)

[2] Characterization and Materials Engineering for Device Integration
Chair: S. Ogawa (Matsushita Electric)
Members: K. Char (Seoul National Univ.), S. C. Chen (TSMC), N. Hata (AIST), M. Kodera (Toshiba), M. Matsuura (Renesas), F. Mizuno (Meisei Univ.), M. Nihei (Fujitsu Labs.), T. Tatsumi (Sony), K. Ueno (NEC), T. Yoda (Toshiba)

[3] CMOS Devices / Device Physics
Chair: K. Shibahara (Hiroshima Univ.)
Members: D. Hisamoto (Hitachi), K. Kurimoto (Matsushita Electric), H. C. Lin (National Chiao Tung Univ.), Y. Momiyama (Fujitsu), H. Oda (Renesas), M. Ogawa (Kobe Univ.), K. Ohuchi (Toshiba), K. Takeuchi (NEC), J. C. S. Woo (UCLA), C. C. Wu (TSMC)

[4] Advanced Memory Technology
Chair: A. Nitayama (Toshiba)
Members: I. Asano (Elpida), T. Eshita (Fujitsu), C. Hsu (eMemory Tech.), N. Ishiwata (NEC), H. S. Jeong (Samsung Electronics), T. Kobayashi (Hitachi), Y. Ohji (Renesas), Y. Yamauchi (Sharp)

[5] Advanced Circuits and Systems
Chair: H. Kobayashi (Gunma Univ.)
Members: R. Fujimoto (Toshiba), T. Hamasaki (Texas Instruments Japan), W. H. Ki (Hong Kong Univ. of Sci. & Tech.), T. Komuro (Agilent Technologies International Japan), K. Masu (Tokyo Tech), M. Mizuno (NEC), H. Yamauchi (Sanyo Electric)

[6] Compound Semiconductor Circuits, Electron Devices and Device Physics

Chair: M. Kuzuhara (Univ. of Fukui)

Members:
Y.-J. Chan (National Central Univ.)
T. Enoki (NTT)
T. Hashizume (Hokkaido Univ.)
R. Hattori (Mitsubishi Electric)
S. Kuroda (Eudina Devices)
K. Maezawa (Nagoya Univ.)
A. Nakagawa (New Japan Radio)
Y. Ohno (Univ. of Tokushima)
S. Tanaka (NEC)
T. Tanaka (Matsushita Electric)

[7] Photonic Devices and Device Physics

Chair: M. Sugawara (Fujitsu Labs.)

Members:
C. Chang-Hasnain (Univ. of California, Berkeley)
M. Ezaki (Toshiba)
T. Hatta (Mitsubishi Electric)
K. Komori (AIST)
Y. Lee (Hitachi)
L. Lester (Univ. of New Mexico)
S. Noda (Kyoto Univ.)
M. Tokushima (NEC)
O. Wada (Kobe Univ.)

[8] Advanced Material Synthesis and Crystal Growth Technology

Chair: H. Yamaguchi (NTT)

Members:
H. Asahi (Osaka Univ.)
Y. Awano (Fujitsu)
T. Fukui (Hokkaido Univ.)
Y. Nanishi (Ritsumeikan Univ.)
R. Nötzel (Eindhoven Univ. of Tech.)
Y. Ochiai (NEC)
S. Shimomura (Osaka Univ.)
M. Tanaka (Univ. of Tokyo)
K. Yamaguchi (Univ. of Electro-Communications)

[9] Physics and Applications of Novel Functional Materials and Devices

Chair: Y. Takahashi (Hokkaido Univ.)

Members:
T. Fujisawa (NTT)
K. Ishibashi (RIKEN)
K. Matsumoto (Osaka Univ.)
H. Mizuta (Tokyo Tech)
J. Motohisa (Hokkaido Univ.)
Y. Nakamura (NEC)
Y. Ohno (Tohoku Univ.)
B. G. Park (Seoul National Univ.)
M. Tabe (Shizuoka Univ.)
T. Usuki (Fujitsu)

[10] Organic Materials Science, Device Physics, and Applications

Chair: K. Kudo (Chiba Univ.)

Members:
M. Iwamoto (Tokyo Tech)
T. Kamata (AIST)
K. Kato (Niigata Univ.)
Y. Ohmori (Osaka Univ.)
Y. W. Park (Seoul National Univ.)
T. Sano (Sanyo Electric)
A. Sugimura (Osaka Sangyo Univ.)
H. Usui (Tokyo Univ. of Agri. & Tech.)

[11] Micro / Nano Electromechanical and Bio-Systems

Chair: H. Tabata (Osaka Univ.)

Members:
S. A. Contera (Univ. of Oxford)
T. Nishimoto (Shimadzu)
H. Oana (Univ. of Tokyo)
T. Ono (Tohoku Univ.)
K. Sawada (Toyohashi Univ. of Tech.)
H. Sugihara (Matsushita Electric)
Y. Takamura (JAIST)
Y. Yoshino (Murata Mfg.)

Persons in charge of online paper submission and registration:

M. Nagata (Kobe Univ.) Y. Kamakura (Osaka Univ.)

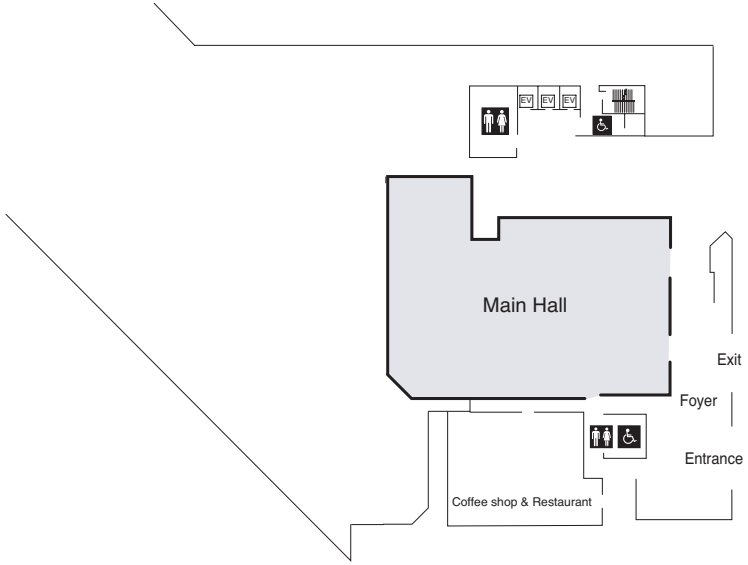
SECRETARIAT

c/o Inter Group Corp.
Toranomon Takagi Bldg., 1-7-2,
Nishishinbashi, Minato-ku,
Tokyo 105-0003, Japan
TEL: +81-3-3597-1108
FAX: +81-3-3597-1097
E-mail: ssdm@intergroup.co.jp

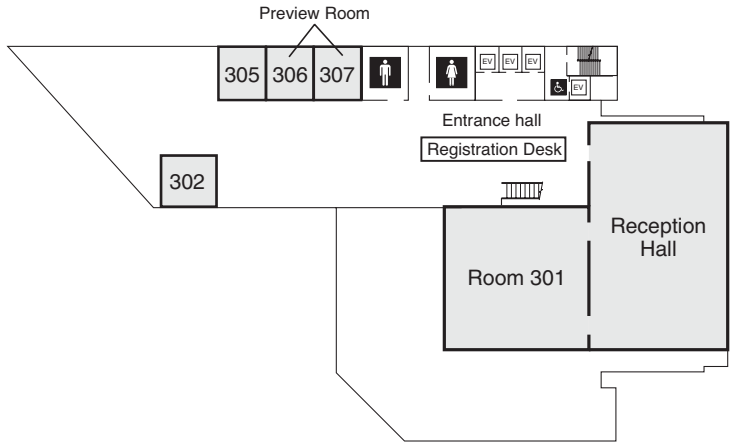
SSDM 2005 is subsidized by the following organizations:
* The Ministry of Education, Culture, Sports, Science and Technology
* Commemorative Organization for the Japan World Exposition (’70)

SSDM 2005 Floor Map, International Conference Center Kobe

1F



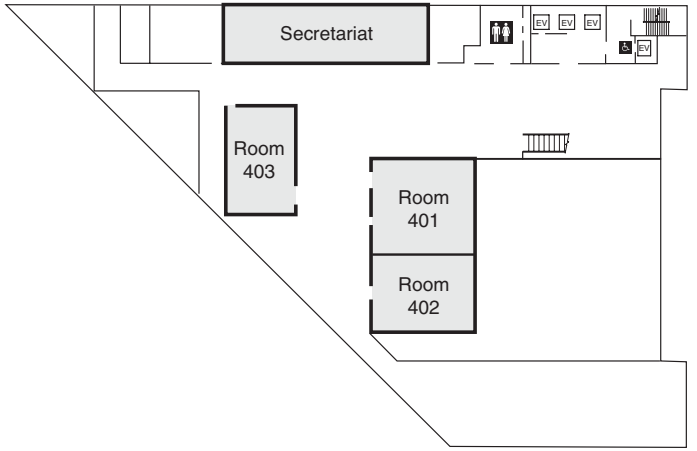
3F



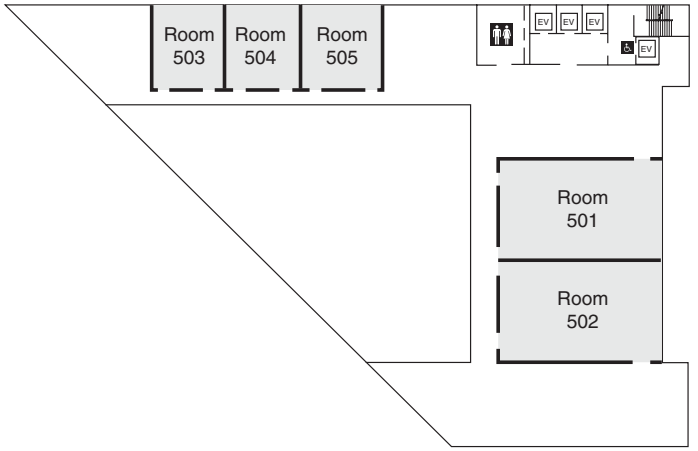
Shimin-Hiroba Station and the second floor of International Conference Center Kobe are connected by roofed pedestrian walkways. Please go up to the third floor for registration.

SSDM 2005 Floor Map, International Conference Center Kobe

4F



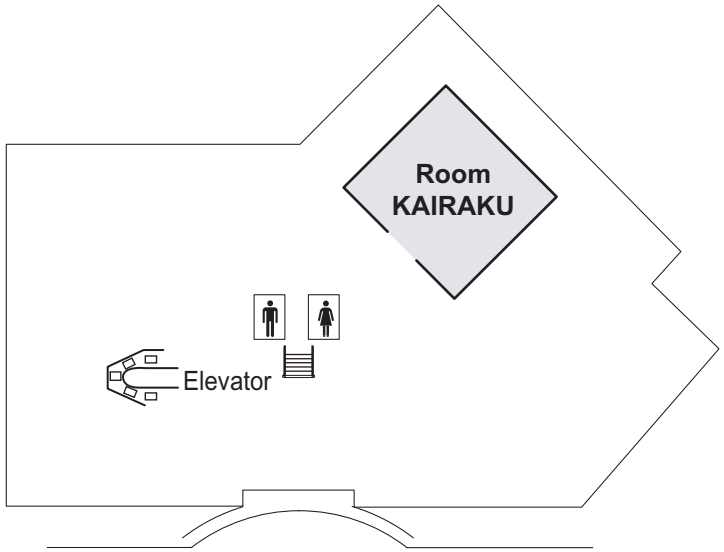
5F



SSDM 2005 Floor Map, Portopia Hotel

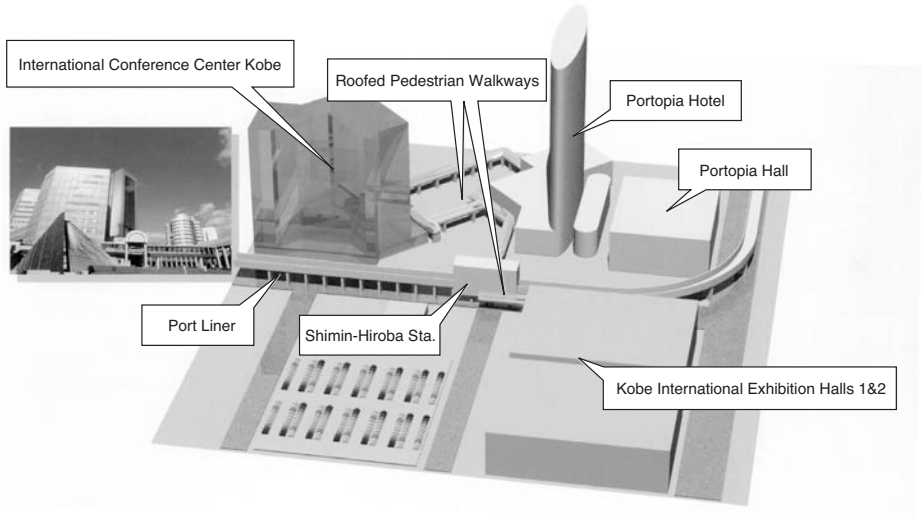
KAIRAKU banquet & luncheon room

B1F



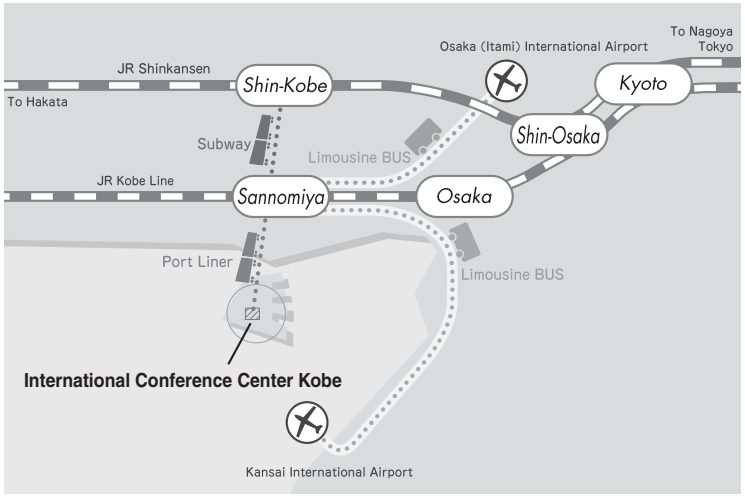
The second floor of the Portopia Hotel and International Conference Center Kobe are connected by roofed pedestrian walkways. Please go down to B1 floor for the banquet (September 13) and the luncheon (September 15).

Access to International Conference Center Kobe



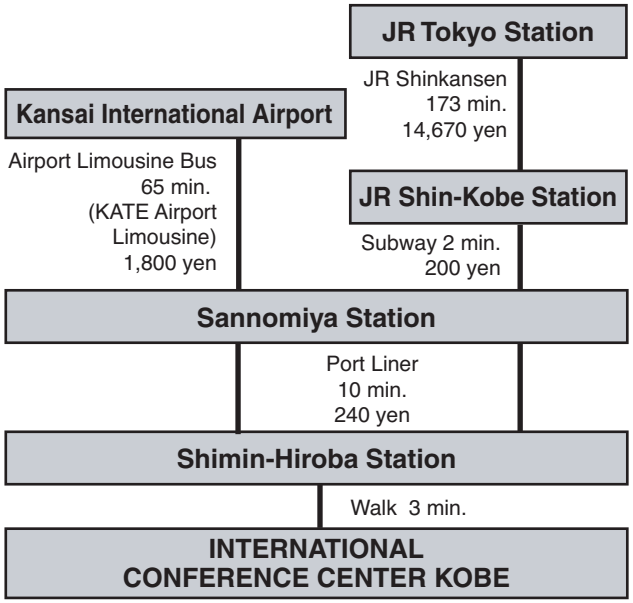
After getting out of the ticket gate of Shimin-Hiroba Sta., please walk to the right through roofed pedestrian walkways, which lead to the second floor of International Conference Center Kobe and the Portopia Hotel.

Rail Map



Access to International Conference Center Kobe

Transportation to the Venue of SSDM 2005



CAUTION

A taxi from Kansai International Airport direct to International Conference Center Kobe would cost you more than 20,000 yen.