ADVANCE PROGRAM

2006 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS

Conference — September 13-15, 2006
Short Course — September 12, 2006
Place — Pacifico Yokohama (Kanagawa, Japan)

2006 International Conference on Solid State Devices and Materials (SSDM 2006)

SECRETARIAT
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The Institute of Image Information and Television Engineers
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Web Site : http://www.ssdm.jp

SSDM 2006 Time Table

Wednesday, September 13

MAIN HALL

10:00-12:20 PL: Opening Session/SSDM & Paper Award

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
14:00-15:45 **Area 9: Physics and Applications of Novel Functional Materials and Devices** A-1: Novel Devices and Characterization	**14:00-16:00** **Area 7: Photonic Devices and Device Physics** B-1: Special Session : Photonic Crystals and Si Photonics I	**14:00-16:20** **Area 5: Advanced Circuits and Systems** C-1: MEMS and Modeling	**14:00-15:30** **Area 10: Organic Materials Science, Device Physics, and Applications** D-1: Organic Light Emitting Diodes	**14:00-15:45** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-1: High-Speed Devices and ICs	**14:00-15:50** **Area 4: Advanced Memory Technology** F-1: FeRAM	**14:00-15:50** **Area 2: Characterization and Materials Engineering for Interconnect Integration** G-1: Advanced Metallization	**14:00-16:00** **Area 3: CMOS Devices /Device Physics** H-1: CMOS Performance Enhancement Technology I	**14:00-15:45** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** I-1: Nanostructure Fabrication	**14:00-16:00** **Area 1: Advanced Gate Stack /Si Processing Science** J-1: Metal/High-k Gate Stack
16:15-18:00 **Area 9: Physics and Applications of Novel Functional Materials and Devices** A-2: Novel Optical Devices	**16:15-18:00** **Area 7: Photonic Devices and Device Physics** B-2: Special Session : Photonic Crystals and Si Photonics II	**16:30-18:10** **Area 5: Advanced Circuits and Systems** C-2: Wireless Interconnect	**16:00-17:45** **Area 10: Organic Materials Science, Device Physics, and Applications** D-2: Organic Light Emitting Diodes and Solar Cells	**16:15-17:45** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-2: Wide-Bandgap Devices	**16:15-18:00** **Area 4: Advanced Memory Technology** F-2: DRAM	**16:15-18:00** **Area 2: Characterization and Materials Engineering for Interconnect Integration** G-2: Characterization I	**16:15-18:00** **Area 3: CMOS Devices /Device Physics** H-2: CMOS Performance Enhancement Technology II	**16:15-18:00** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** I-2: Compound Semiconductors	**16:15-18:00** **Area 1: Advanced Gate Stack /Si Processing Science** J-2: FUSI Gate Electrode

18:30-20:30 Banquet/Young Award (Intercontinental Hotel, Pacific 3F)

Thursday, September 14

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
9:00-10:30 **Area 11: Micro/nano Electromechanical and Bio-Systems (Devices)** A-3 : MEMS and NEMS : Fabrication	**9:00-10:30** **Area 7: Photonic Devices and Device Physics** B-3 : LEDs and Lasers	**9:00-10:20** **Area 5: Advanced Circuits and Systems** C-3: Toward Next Generation Systems	**9:00-10:30** **Area 10: Organic Materials Science, Device Physics, and Applications** D-3: Organic Materials and Device Physics I	**9:00-10:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-3: Sensors and Interface Physics	**9:00-10:40** **Area 3: CMOS Devices /Device Physics** F-3: Quasi-Ballistic Transport	(Poster setting)	(Poster setting)	(Poster setting)	**9:10-10:40** **Area 1: Advanced Gate Stack /Si Processing Science** J-3: Characterization of Gate Stack
10:45-12:15 **Short Presentation** **Area 11 and Area 8**	**10:45-12:15** **Short Presentation** **Area 7 and Area 4**	**10:45-12:15** **Short Presentation** **Area 5 and Area 2**	**10:45-11:30** **Area 10:Organic Materials Science, Device Physics, and Applications** D-4: Organic Materials and Device Physics II **11:30-12:30** **Short Presentation** **Area 10**	**10:45-12:15** **Short Presentation** **Area 6 and Area 9**	**10:45-12:15** **Short Presentation** **Area 3**	(Poster setting)	(Poster setting)	(Poster setting)	**10:45-12:15** **Short Presentation** **Area 1**

13:00-15:00 Poster Session

15:15-16:15 **Joint Area 8 and 9** A-5: Nanowires and Nanotubes I	**15:15-16:30** **Area 7: Photonic Devices and Device Physics** B-5: Quantum-dot Lasers	**15:15-16:25** **Area 4: Advanced Memory Technology** C-5: ReRAM	**15:15-16:15** **Area 2: Characterization and Materials Engineering for Interconnect Integration** D-5: Emerging Interconnect	**15:15-16:35** **Area 1: Advanced Gate Stack/ Si Processing Science** E-5: Junction I	**15:15-16:35** **Area 3: CMOS Devices /Device Physics** F-5: Device Reliability and Characterization	(Poster removed by 15:30 and Preparation for Rump Session)	(Poster removed by 15:30 and Preparation for Rump Session)	(Poster removed)	**15:15-16:35** **Area 1: Advanced Gate Stack /Si Processing Science** J-5: High-k Dielectrics I
16:30-18:00 **Joint Area 8 and 9** A-6: Nanowires and Nanotubes II	**16:45-18:00** **Area 7: Photonic Devices and Device Physics** B-6: Quantum Optical Devices	**16:45-17:55** **Area 4: Advanced Memory Technology** C-6: Flash Memory I	**16:25-17:45** **Area 2: Characterization and Materials Engineering for Interconnect Integration** D-6: Assembly and Packaging	**16:45-17:45** **Area 1: Advanced Gate Stack/ Si Processing Science** E-6: Junction II	**16:45-18:05** **Area 3: CMOS Devices /Device Physics** F-6: Device Fluctuation Analysis			**16:45-18:05** **Area 5: Advanced Memory Technology** I-6: Analog Circuit Techniques	**16:45-17:45** **Area 1: Advanced Gate Stack /Si Processing Science** J-6: Interface Properties of Ge

18:30-20:30 Rump Session **Room 501 "Challenges of New Non-Volatile Memories : Innovative Strategies to catch up with FLASH"**
Room 502 "Nanotechnology - Impact on Electronics, Photonics and Biology-"

Friday, September 15

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
9:00-10:30 **Area 9: Physics and Applications of Novel Functional Materials and Devices** A-7: Novel Devices and Materials I	**9:00-10:30** **Area 7: Photonic Devices and Device Physics** B-7: Micro-Optics and Optical Waveguids	**9:00-10:30** **Area 11: Micro/nano Electromechanical and Bio-Systems (Devices)** C-7: Micro and Nano Fluidics for Biosensing	**9:45-10:30** **Area 10: Organic Materials Science, Device Physics, and Applications** D-7: Molecular Electronics		**9:00-10:20** **Area 4: Advanced Memory Technology** F-7: Flash Memory II	**9:00-10:40** **Area 2: Characterization and Materials Engineering for Interconnect Integration** G-7: Characterization II	**9:00-10:40** **Area 3: CMOS Devices /Device Physics** H-7: Compact Modeling	**9:00-10:15** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** I-7: Novel Materials	**9:00-10:40** **Area 1: Advanced Gate Stack /Si Processing Science** J-7: High-k Dielectrics II
10:45-12:15 **Area 9: Physics and Applications of Novel Functional Materials and Devices** A-8: Novel Devices and Materials II	**10:45-12:00** **Area 7: Photonic Devices and Device Physics** B-8: All-Optical Switches	**10:45-12:15** **Area 11: Micro/nano Electromechanical and Bio-Systems (Devices)** C-8: Nano and Bio Sensors I	**10:45-12:00** **Area 10: Organic Materials Science, Device Physics, and Applications** D-8: Organic Transistor I	**10:45-12:15** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-8: GaAs FETs and Process Technologies	**10:45-12:25** **Area 4: Advanced Memory Technology** F-8: MRAM/PRAM	**10:45-12:25** **Area 2: Characterization and Materials Engineering for Interconnect Integration** G-8: Special Session I ; Reliability	**10:45-12:25** **Area 3: CMOS Devices /Device Physics** H-8: Advanced Channel and Substrate Technology	**10:45-11:45** **Area 8: Advanced Material Synthesis and Crystal Growth Technology** I-8: New Materials	**10:45-12:25** **Area 1: Advanced Gate Stack /Si Processing Science** J-8: Metal/High-k CMOS
13:15-14:45 **Area 9: Physics and Applications of Novel Functional Materials and Devices** A-9: Novel Devices and Materials III	**13:15-15:00** **Area 7: Photonic Devices and Device Physics** B-9: Detectors and Sensors	**13:15-15:00** **Area 11: Micro/nano Electromechanical and Bio-Systems (Devices)** C-9: Nano and Bio Sensors II	**13:30-15:00** **Area 10: Organic Materials Science, Device Physics, and Applications** D-9: Organic Transistor II	**13:15-15:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-9: GaN FETs and Process Technologies	**13:15-14:55** **Area 3: CMOS Devices /Device Physics** F-9: Schottky S/D and Carrier Transport	**13:15-15:35** **Area 2: Characterization and Materials Engineering for Interconnect Integration** G-9: Special SessionII ; Metallization Challenges	**13:15-14:55** **Area 3: CMOS Devices /Device Physics** H-9: Carrier Transport		**13:15-15:05** **Area 1: Advanced Gate Stack /Si Processing Science** J-9: Reliability
		15:15-16:30 **Area 11: Micro/nano Electromechanical and Bio-Systems (Devices)** C-10: MEMS and NEMS : Application	**15:15-16:15** **Area 10: Organic Materials Science, Device Physics, and Applications** D-10: Organic Transistor III	**15:15-17:00** **Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics** E-10: High-Voltage GaN Devices			**15:15-16:55** **Area 3: CMOS Devices /Device Physics** H-10: Advanced Device Technology		**15:15-16:35** **Area 1: Advanced Gate Stack /Si Processing Science** J-10: Metal Gate Electrode

SSDM 2006 Advance Program
General Information

DATE
Conference: **September 13-15, 2006 (Official language is English)**
Short Course: **September 12, 2006 (in Japanese)**

LOCATION
Pacifico Yokohama
1-1-1 Minatomirai, Nishi-ku, Yokohama 220-0012, Japan
Phone: +81-45-221-2155 Fax: +81-45-221-2136
Pacifico Yokohama, located in Yokohama's new and growing waterfront development Minato Mirai 21 area, is an integrated convention center on a world class scale. Since its opening in 1991, Pacifico Yokohama has hosted a variety of gatherings amid the magnificent surroundings of the international port city of Yokohama, Japan's historic window to the outside world.
It takes less than 2 hours from Tokyo international airport to Pacifico in limousine bus or train. From central Tokyo area, a 30 minutes ride on train will take you to Pacifico.
For further information, see
http://www.pacifico.co.jp/english/

REGISTRATION
The registration desk will be open from September 12 to 15 in the entrance hall on the third floor (conference site). The registration hours are as follows:

September 12	11:00-17:00	Foyer (5F)
13	9:00-17:00	Entrance Hall (2F)
14	9:00-17:00	Foyer (5F)
15	9:00-15:30	Foyer (5F)

Early registration will be accepted only through the conference website until August 12, 2006, 24:00 Japan time. (http://www.ssdm.jp)
Advanced registration through the conference website will be closed September 5, 2006, 17:00 Japan time. After the date, registration can be made at the conference site as on-site registration. Early registration is recommended.

	Registration Fee		Short Course (in Japanese)	Banquet
	On or Before 24:00, August 12 (Japan time)	On or After August 13		
Regular	¥40,000	¥45,000	¥15,000	¥7,000
Student	¥5,000		¥3,000	¥4,000
Accompanied person(s)				¥4,000/person

* Fees include tax.

1) The registration fee includes one copy of the abstract book and a CD-ROM. However, it does not include the banquet, and an additional payment is required to attend the banquet (Regular: ¥7,000, Student/Accompanied person: ¥4,000).
2) Those who register as students are required to fax a copy of their current student ID to Kinki Nippon Tourist Co., Ltd. (KNT) (Fax: +81-3-5256-1588) at the time of registration and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of the online registration of individual information.
3) Registration is complete only after payment is made in full.

Payment Procedure
Payment can be made by:
- One of the following credit cards:
  1. VISA 2. MasterCard 3. Diners Club 4. American Express 5. JCB
- A bank transfer to KNT Co., Ltd. (Message: SSDM)
  Account at Sumitomo Mitsui Banking Corp., Suzuran Branch, 1-3-12 Nishishimbashi, Minato-ku, Tokyo 105-0003, Japan (SWIFT Code: SMBCJPJT, Ordinary Account: 6103515, Account Name: Kinki Nippon Tourist Co., Ltd.)

* Personal checks are not acceptable.

Confirmation of Pre-Registration
Upon receipt of your online registration, a written confirmation will be faxed or e-mailed to you after your payment is confirmed.
Please bring this confirmation slip with you and present it to the registration desk.

Registration Cancellation
Conference:
Cancellation fee of ¥3,000 will be deducted from the refund. Cancellation should be made in writing to KNT Co., Ltd. No cancellation will be accepted after August 17, 2006. Extended Abstracts will be sent to absent registrants after the conference.

Short Course:
Cancellation fee of ¥2,000 will be deducted from the refund. Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be accepted after August 17. Short-course textbooks will be sent to the absent registrants after the conference.

Banquet:
Cancellation fee of ¥1,000 will be deducted from the refund, Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be acccepted after August. 17.

Inquiries for Registration
Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho
Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2006-gb@or.knt.co.jp
Office hours: 9:30-17:30 (weekdays only)

On-site Registration
Registration fees should be paid in Japanese Yen or credit cards. VISA, MasterCard, Diners Club, American Express and JCB are acceptable. No personal checks are acceptable.

BANQUET
The conference banquet will be held on the evening of Wednesday, September 13. The banquet fee (Regular: ¥7,000, Student/Accompanied person: ¥4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

LATE NEWS PAPERS
Submission of Late News Papers has been already closed on July 31, 2006. The accepted papers will be on "Advance Program Part II" which will be distributed at the venue during the conference.

SPECIAL Issue of JJAP
Authors of papers presented at SSDM 2006 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April 2007.

RUMP SESSIONS - September 14 (Thursday) 18:30-20:30

Session A (Room 501, 5F)

"Challenges of New Non-Volatile Memories: Innovative Strategies to catch up with FLASH"

Non-Volatile Memories (NVMs), in particular Flash, are playing an important role in the semiconductor market with usage in mobile phones and other types of mobile equipment. In the coming years mobile systems will demand even more NVM with high density and very high writing throughput for data storage application, or with fast random access for code execution. DRAM and NAND Flash, both of which occupy more than 70% of whole current memory market are expected to keep their fast technology evolution until 2015 and will reach at 20-30 nm technology node by the early of 2010s. If alternative NVMs such as FeRAM, MRAM, ReRAM and PRAM continue their technology evolution with the same speed as was done during last decade, there will be no chance to compete with NAND Flash in the future main memory market. Now as the scaling speeds of Flash and DRAM become slightly slow down, alternative NVMs might have a chance for the market. In this session, the material innovation of NVMs for catching up with the Flash Memories will be discussed.

Organizers/Moderators: N. Fujimura (Osaka Pref. Univ., Japan)
T. Sakata (Hitachi, Japan)
S. Zaima (Nagoya Univ., Japan)

Panelists: R. Bez/P. Cappelletti (STMicroelectronics, Italy)
T. Ohta (Ovonic Phase Change Inst., Japan)
Y. S. Park (Samsung Electronics, Korea)
T. Shimoda (Seiko Epson, Japan) tentative
H. Yoda (Toshiba, Japan) tentative

A couple of additional panelists will be invited.

Session B (Room 502, 5F)

"Nanotechnology–Impact on Electronics, Photonics and Biology–"

Nanotechnology research is expanding its field rapidly, ranging from electronics, photonics, and mechanics to biology, and so on. However, it is still uncertain how it can be used and give real impacts on the fields, except some limited examples. From the fabrication point of view, the bottom-up technology and the top-down technology appear to be still separated, although a technology to make a bridge between them is highly required. From the functionality point of view, the single electronics, spintronics and quantum computing, et al., those discussed in terms of emerging research devices need nanotechnology to fabricate elemental devices for them. What are the new functionality of them? Can these new functional devices be fabricated in reality? Do they help the difficulty that the present silicon devices are facing? What are the biological application, and how it relates to electronics? There are many questions, most of which are difficult to answer. The rump session will begin with presentations from some panelists, followed by free discussions on these issues. We are grateful if audience may find their own answer through the session.

Organizers/Moderators: T. Ichiki (Univ. of Tokyo, Japan)
K. Ishibashi (RIKEN, Japan)

Panelists: T. Fujisawa (NTT Corp., Japan)
P. Hadley (Graz Univ. of Technology, Austria)
T. Hiramoto (Univ. of Tokyo, Japan)
J. Ohta (NAIST, Japan)
M. Sugawara (Fujitsu Labs., Japan)
H. Tabata (Osaka Univ., Japan)
B. Yu (NASA Ames Research Center, USA)

SHORT COURSE

Short Course entitled “Understanding Basic Physics of Scaled MOSFETs” will be held on Tuesday, September 12. All lectures are given in Japanese.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

AWARDS

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 2000.

SSDM Paper Award

Given for the best paper presented at SSDM 2005.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at SSDM 2005.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted, and who have applied for the grant. Submitting an application form does not guarantee that the grant will be awarded. Each related area chair will choose one candidate from the applicants. Late news papers are not eligible for travel grant.

The grant is authorized by the Marubun Research Promotion Foundation (MRPF), which is one of the cooperation organizations. The grant covers part of the recipient’s travel costs, but does not necessarily cover all their expenses. Successful candidates must attend the ceremony which will be held during the conference (details of which will be given later) to receive the grant. Failure to attend will result in forfeiture of the grant.

VISA REQUIREMENT

All foreign participants must have a valid passport. Participants from countries where a visa is required to enter Japan are advised to apply at the nearest Japanese Embassy or Consulate as soon as possible.

Concerning visa applications, generally, in applying for a visa each applicant is requested to submit the documents listed below:

(1) an invitation letter (an optional document written in English)
(2) a letter of guarantee (written in Japanese)
(3) documents certifying the purpose of the visit (written in Japanese)
(4) the applicant’s schedule in Japan (written in Japanese)

Please ask the nearest Japanese Embassy to make sure what documents are required to obtain a visa first, and then contact the SSDM Secretariat. The Secretariat will send the Reply Form for Visa Application in order to obtain the required documents. Please complete the Reply Form for Visa Application and submit it to the Secretariat. We will send you all the requested documents as soon as we receive the Reply Form.

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F, 19-2 Kanda-Matsunaga-cho, Chiyoda-ku
Tokyo 101-8641, JAPAN
Phone: +81-3-5256-1581 Fax: +81-3-5256-1588
E-mail: ssdm2006-gb@or.knt.co.jp

Hotel Accommodations

KNT has blocked rooms at following hotels in Yokohama for the conference period. Reservations can be made through the conference website.

Hotel Name	**Yokohama Grand Inter-continental Hotel**
Room Rates	Single: JPY23,100 Twin: JPY11,550 (per person, per night) *JPY2,100 will be added to the above rates on Sep. 15 (Fri.).
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	Minato Mirai 1-1-1 Nishi-ku, Yokohama-shi, Kanagawa 220-8522 Japan
Phone	+81-45-223-2222
Access to Hotel	2 min. walk from Minato Mirai Line Minato Miirai Sta.
To Conference site	Next to the site

Hotel Name	**Pan Pacific Hotel Yokohama**
Room Rates	Single: JPY21,000 Twin: JPY12,600 (per person, per night) *JPY3,150 for a single and JPY2,100 for a twin will be added to the above rates on Sep. 15 (Fri.)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	Minato Mirai 2-3-7 Nishi-ku, Yokohama-shi, Kanagawa 220-8543 Japan
Phone	+81-45-682-2222
Access to Hotel	1 min. walk from Minato Mirai Line Minato Mirai Sta.
To Conference site	1 min. walk to the site

Hotel Name	**Navios Yokohama**
Room Rates	Single: JPY11,445 (per person, per night) *JPY1,050 will be added to the above rates on Sep. 15 (Fri.).
Hotel Deposit	JPY10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	Shinko 2-1-1 Naka-ku, Yokohama-shi, Kanagawa 231-0001 Japan
Phone	+81-45-633-6000
Access to Hotel	3 min. walk from Minato Mirai Line? Bashamichi Sta.
To Conference site	7 min. walk to the site

Hotel Name	**Yokohama Sakuragicho Washington Hotel**
Room Rates	Single: JPY11,550 Twin: JPY8,925 (per person, per night)
Hotel Deposit	JPY10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	Sakuragicho 1-1-67 Naka-ku, Yokohama-shi, Kanagawa 231-0062
Phone	+81-45-683-3111
Access to Hotel	3 min. walk from Minato Mirai Line Bashamichi Sta.
To Conference site	10 min. walk to the site

Hotel Name	**San-ai Yokohama Hotel**
Room Rates	Single: JPY9,240 (per person, per night)
Hotel Deposit	JPY10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	Hanasakicho 3-95 Naka-ku, Yokohama-shi, Kanagawa 231-0063
Phone	+81-45-242-4411
Access to Hotel	5 min. walk from JR Sakuragicho sta.
To Conference site	15 min. walk to the site

Notes: 1) All room rates are per person per night including breakfast, 10% service charge, and 5% consumption tax.
2) The above rates are valid only during the period of the SSDM 2006 meeting.
3) Communication fee of 500 JPY is required for per reservation and this is charged as handling charge for KNT.
4) The deposit will be deducted from your hotel bill. Please settle the balance with the hotel cashier.
5) The above rates and information are subject to change without notice.

Application and Payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website. Reservations should be made by no later than August 18, 2006 (Japan time). (A confirmation sheet will be sent by KNT)
Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment. All payment must be paid only in Japanese yen by one of the following methods.

1) Credit Card:
(VISA, MasterCard, Diners Club, AMEX or JCB only)
* Please fill in the necessary items with your signature in the credit card section of the application form.
2) Bank Transfer:
Sumitomo Mitsui Banking Corp.
Suzuran Branch
SWIFT Code: SMBCJPJT
Ordinary Account: 6103515
Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation Policy for Accommodations

In case of cancellation, a written notification should be sent to KNT by e-mail (ssdm2006-gb@or.knt.co.jp) or by FAX (+81-3-5256-1588) to avoid any trouble.
Hotels: Up to 14 days before the arrival date.No Charge
13–7 days before.....10 % of daily room charge
6–2 days before.....40 % of daily room charge
Less than 2 days, or no notice given..100 % of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Yokohama is warm and sometimes humid in September. The temperature range is 18-30˚C.

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Yokohama (conference site) and Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

SSDM 2006 INSTRUCTION for SPEAKERS
Oral Presentation

Time Schedule

	Session Time	Presentation	Discussion
Plenary	50 min.	45 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	15 min.	5 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of presentation , Third: End of discussion.

Audio-Visual Equipment

The meeting rooms will contain the following audiovisual equipment:
• LCD projector **(PC itself is not provided)**
• Overhead projector
• Microphone
• Projection laser pointer
Speakers wishing to present their papers using the LCD projector are requested to verify their PC's compatibility with the LCD projector at the conference room during a break time prior to their presentations.

Poster Presentation

Poster sessions are scheduled for Thursday, September 14, from 13:00 to 15:00. Poster boards will be available with identifying labels at the Room 501,502,511,512 on the fifth floor. Authors are requested to prepare their posters between 9:00 and 12:00 on September 14 and remove them by 15:30 on September 14. Any posters remaining after 15:30 will be disposed of by the secretariat. Usable space on each poster board will be approximately 900mm wide and 1,500mm high. Pushpins will be available. Each presentation will be assigned a board, labeled with the paper number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are asked to give a short oral presentation in the morning of September 14. The presentation time should be kept strictly to two minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations be held in a quick, successive sequence. While one speaker is giving his/her presentation, the next several speakers should wait nearby in line for their turn in order to move on to the next presentation. Note that any absent speakers will be skipped and each presentation will be automatically stopped after two minutes have elapsed. Only a PC projector will be made available. You should send your presentation file to the secretariat (ssdm@intergroup.co.jp) by e-mail by August 24. The file must be an exact "2-page" landscape PDF. Because the presentation time is limited, please describe your research objective and results clearly and do NOT show the author list or the title on your file, those of which will be prepared by the SSDM Secretariat.

Short oral presentations will be held, as follows. Please check your poster number. (P# means the poster presentation of Area #.)

Room 411/412	P11, P8
Room 413	P7, P4
Room 414/415	P5, P2
Room 416/417	P10
Room 418	P6, P9
Room 419	P3
Small Auditorium	P1

Wednesday, September 13

MAIN HALL, 1F

PL: Opening Session (10:00–12:20)
Chairpersons: T. Hiramoto, Univ. of Tokyo and Y. Hirayama, Tohoku Univ.

10:00 Pl-0
Welcome Address and Award Presentation
H. Sakaki, Univ. of Tokyo

10:40 PL-1 (Plenary)
Nano-CMOS & Emerging Technologies–Myths and Hopes
T. Skotnicki, STMicroelectronics, France

11:30 PL-2 (Plenary)
MEMS as Key Components for Systems
M. Esashi, Tohoku Univ., Japan

12:20-14:00 Lunch

Room 411/412 (A)

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-1: Novel Devices and Characterization
(14:00-15:45)
Chairs: J. Motohisa (Hokkaido Univ.)
Y. Nakamura (NEC)

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-1: Special Session ; Photonic Crystals and Si Photonics I
(14:00-16:00)
Chairs: S. Noda (Kyoto Univ.)
M. Tokushima (NEC)

Room 414/415 (C)

Area 5: Advanced Circuits and Systems

C-1: MEMS and Modeling
(14:00-15:20)
Chairs: T. Komuro (Agilent Technologies International Japan)
K. Masu (Tokyo Tech)

C-1: MEMS and Modeling
(15:20-16:20)
Chairs: T. Hamasaki (Texas Instruments Japan)
M. Horiguchi (Renesas)

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-1: Organic Light Emitting Diodes
(14:00-15:45)
Chairs: Y. Ohmori (Osaka Univ.)
T. Sano (Sanyo Electric)

Room 418 (E)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

E-1: High-Speed Devices and Ics
(14:00-15:45)
Chairs: K. Maezawa (Nagoya Univ.)
S. Yamahata (NTT)

Room 419 (F)

Area 4: Advanced Memory Technology

F-1: FeRAM
(14:00-15:50)
Chairs: T. Eshita (Fujitsu)
H. S. Jeong (Samsung Electronics)

Room 501 (G)

Area 2: Characterization and Materials Engineering for Interconnect Integration

G-1: Advanced Metallization
(14:00-15:50)
Chairs: S. Ogawa (Selete/ Matsushita)
K. Ueno (Shibaura Institute of Technology)

Room 502 (H)

Area 3: CMOS Devices/Device Physics

H-1: CMOS Performance Enhancement Technology I
(14:00-16:00)
Chairs: K. Shibahara (Hiroshima Univ.)
D. Hisasmoto (Hitachi)

Room 511/512 (I)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

I-1: Nanostructure Fabrication
(14:00-15:45)
Chairs: T. Sogawa (NTT)
H. Yamaguchi (NTT)

Small Auditorium (J)

Area 1: Advanced Gate Stack / Si Processing Science

J-1: Metal/High-k Gate Stack
(14:00-16:00)
Chairs: Y. Nara (Selete)
J. Yugami (Renesas)

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
14:00 A-1-1 (Invited) Nanowire Field Effect Transistor L. E. Wernersson, *Lund Univ., Sweden*	**14:00 B-1-1 (Invited)** Control of Light Emission and Propagation in Semiconductor Photonic Nanostructures T. Baba, *Yokohama National Univ., Japan*	**14:00 C-1-1 (Invited)** Low-Voltage Operated Piezoelectric Tunable Capacitor for Reconfigurable RF Systems T. Kawakubo, T. Nagano, M. Nishigaki and K. Itaya, *Toshiba Corp., Japan*	**14:00 D-1-1 (Invited)** Highly Efficient Carrier Injection and Transport in Organic Light Emitting Diodes C. Adachi, *Kyushu Univ., Japan*	**14:00 E-1-1 (Invited)** InP-based High-speed Transistors and their IC Applications K. Murata, K. Sano, H. Fukuyama, T. Kosugi, M. Nakamura, K. Kurishima, M. Tokumitsu and T. Enoki, *NTT Corp., Japan*
14:30 A-1-2 Infrared detection with silicon nano transistors K. Nishiguchi[1], Y. Ono[1], A. Fujiwara[1], H. Yamaguchi[1], H. Inokawa[2] and Y. Takahashi[3], *[1]NTT Corp., [2]Shizuoka Univ. and [3]Hokkaido Univ., Japan*	**14:30 B-1-2 (Invited)** All-Optical Switching and Control of Si Photonic Crystal Nanocavities M. Notomi, *NTT Corp., Japan*	**14:30 C-1-2 (Invited)** MEMS Packaging for RF Switch T. Seki, *OMRON, Japan*	**14:30 D-1-2** Top emission organic light emitting diodes with double metal layer anode C. R. Tsai, F. S. Juang, L. W. Ji, Y. S. Tsai and C. C. Liu, *National Formosa Univ., Taiwan*	**14:30 E-1-2** High Power and Stable Oscillations in the RTD Pair Oscillator ICs Fabricated with Metamorphic RTDs K. Maezawa[1], Y. Ookawa[1], S. Kishimoto[1], T. Mizutani[1], M. Takakusaki[2] and H. Nakata[2], *[1]Nagoya Univ. and [2]Nippon Mining & Metals Co., Ltd., Japan*
14:45 A-1-3 High-Resolution Measurement of Ultra-Shallow Structures by Scanning Spreading Resistance Microscopy L. Zhang, K. Ohuchi, K. Adachi, M. Tomita, K. Ishimaru, M. Takayanagi and A. Nishiyama, *Toshiba Corp., Japan*			**14:45 D-1-3** The Experiment and Simulation Study Top Emission PLEDs Using LiF/Ag/ITO Cathode C. W. Teng[1], Y. H. Lu[1], Y. C. Tsai[1], K. Y. Chang[1], S. H. Chou[1], K. C. Liu[1], L. C. Chen[2], Y. C. Fang[3] and H. E. Huang[3], *[1]Chang Gung Univ., [2]DELTA OPTOELECTRONICS and [3]CSIST, Taiwan*	**14:45 E-1-3** High-speed and Low-Power NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology H. Kim, S. Yeon and K. Seo, *Seoul National Univ., Korea*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
14:00 F-1-1 (Invited) Overview and Future Challenge of FeRAM Technologies Y. Kato, H, Tanaka, K. Isogai, K. Kaibara, Y. Kaneko and Y. Shimada, *Matsushita Electric, Japan*	**14:00 G-1-1 (Invited)** Carbon Nanotube via Technologies for Advanced Interconnect Integration M. Nihei[1,2], A. Kawabata[1,2], T. Hyakushima[1], S. Sato[1,2], T. Nozue[1], D. Kondo[1,2], H. Shioya[1,2], T. Iwai[2,3], M. Ohfuti[1,2] and Y. Awano[1,2], *[1]Selete, [2]Fujitsu Ltd. and [3]Fujitsu Labs., Japan*	**14:00 H-1-1 (Invited)** Direct Silicon Bonded (DSB) Mixed Orientation Substrate for High Performance Bulk CMOS Technology C. Y. Sung, H. Yin, H. Ng, K. L. Saenger, G. Pfeiffer, V. Chan, R. Zhang, J. Li, J. A. Ott, R. Bendernagel, S. B. Ko, Z. Ren, X. Chen, V. Ku, Z. J. Luo, N. Rovedo, K. Fogel, M. Khare, G. Shahidi and S. Crowder, *IBM, USA*	**14:00 I-1-1 (Invited)** GaN-based Quantum Wires, Discs, and Dots with Novel Electronic Properties K. H. Ploog, *Paul Drude Inst. for Solid State Electronics, Germany*	**14:00 J-1-1 (Invited)** Towards Metal-gate/high-k Integration for High Performance CMOS Technology E. Cartier, *IBM, USA*
14:30 F-1-2 Full-Bit Functional, High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process K. R. Udayakumar[1], T. S. Moise[1], S. R. Summerfelt[1], F. G. Celii[1], G. Shinn[1], K. Boku[1], K. Remack[1], A. Haider[1], D. Anderson[1], J. Gertas[1], Y. Obeng[1], G. Albrecht[1], J. S. Martin [1], J. Rodriguez[1], B. Khan[1], S. Aggarwal[1], N. Schaver[1], H. McAdams[1], and A. Mckerrow[1] J. Eliason[2], J. Groat[2], R. Bailey[2], G. R. Fox[2], E. Jabillo[2] and J. Walbert[2], *[1]Texas Instruments Inc. and [2]Ramtron International Corp., USA*	**14:30 G-1-2** Ti-barrier Metal for Robust and Reliable 45nm Node Porous Low-k/Copper Interconnects K. Higashi[1], H. Yamaguchi[1], T. Yosho[1], A. Sakata[1], S. Omoto[1], S. Yamashita[1], T. Fujimaki[1], Y. Enomoto[2], N. Matsunaga[1] and H. Shibata[1], *[1]Toshiba Corp. and [2]Sony Corp., Japan*	**14:30 H-1-2 (Invited)** Strained-Silicon Transistors with Silicon-Carbon Source/Drain Y. C. Yeo, *National Univ. of Singapore, Singapore*	**14:30 I-1-2 (Invited)** Functions and Device Applications of Quantum-sized Silicon N. Koshida, *Tokyo Univ. o f Agriculture and Technology, Japan*	
14:50 F-1-3 Formation of Ferroelectric $Sr_2(Ta_{1-x}, Nb_x)_2O_7$ Thin Film on Amorphous SiO_2 by Microwave-Excited Plasma Enhanced Metalorganic Chemical Vapor Deposition I. Takahashi, K. Funaiwa, K. Azumi, S. Yamashita, Y. Shirai, M. Hirayama, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*	**14:50 G-1-3** Key mechanisms for improved EM lifetime of CoWP capped Cu interconnects Y. Kakuhara[1], N. Kawahara[1], K. Ueno[2] and N. Oda[1], *[1]NEC Corp. and [2]Shibaura Inst. of Tech., Japan*		**14:40 J-1-2** Demonstration of Low Vt NMOSFETs Using Thin HfLaO in ALD TiN/HfSiO Gate Stack C. S. Park[1], S. C. Song[1], G. Bersuker[1], H. N. Alshareef[2], B. S. Ju[1], P. Majhi[3], B. H. Lee[4], R. Jammy[4], H. K. Park[5], M. S. Joo[6], J. Pu[6] and B. J. Cho[6], *[1]SEMATECH, [2]Texas Instruments, [3]Intel, [4]IBM Assignee, [5]GIST and [6]NUS, USA*	

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
15:00 A-1-4 Imaging of interference between incident and reflected electron waves at an InAs/GaSb heterointerface by low-temperature scanning tunneling spectroscopy K. Suzuki[1], K. Kanisawa[1], S. Perraud[1,2], M. Ueki[3], K. Takashina[1] and Y. Hirayama[1,4,5], *[1]NTT Corp., [2]CNRS, [3]NTT Electronics Techno Corp., [4]SORST-JST and [5]Tohoku Univ., Japan*	**15:00 B-1-3** Photonic Crystal Nanocavity Continuous-wave Laser Operation at Room Temperature M. Nomura, S. Iwamoto, K. Watanabe, N. Kumagai, Y. Nakata, S. Ishida and Y. Arakawa, *Univ. of Tokyo, Japan*	**15:00 C-1-3** A Capacitive-Sensing Scheme for Control of Adaptive MEMS Device Stacked on CMOS LSI T. Shimamura[1], H. Morimura[1], K. Kuwabara[1], N. Sato[1], J. Terada[1], M. Ugajin[1], S. Shigematsu[1], K. Machida[2], M. Nakanishi[1] and H. Ishii[1], *[1]NTT Microsystem Integration Labs. and [2]NTT Advanced Technology Corp., Japan*	**15:00 D-1-4** Simulation for double ultra-thin separately doped red organic light-emitting diode S. H. Wang[1], T. S. Li[1], F. S. Juang[2] and Y. S. Tsai[2], *[1]Kun-Shan Univ. and [2]National Formosa Univ., Taiwan*	**15:00 E-1-4** Effect of flatness of heterointerfaces on device performance of InP-based HEMTs I. Watanabe[1], K. Shinohara[1], T. Kitada[2], S. Shimomura[2], A. Endoh[3], Y. Yamashita[3], T. Mimura[3], S. Hiyamizu[2] and T. Matsui[1], *[1]National Inst. of Information and Communications Technology, [2]Osaka Univ. and [3]Fujitsu Labs. Ltd., Japan*
		15:20 C-1-4 Equivalent Circuit Model for On-Chip Variable Inductor T. Yammouch, K. Ishida, K. Okada and K. Masu, *Tokyo Tech, Japan*		
15:15 A-1-5 Magnetopiezoresistance effects in an InAs/AlGaSb nanomechanical resonator with extremely small power consumption I. Mahboob[1], H. Okamoto[1], M. Ueki[1] and H. Yamaguchi[1,2], *[1]NTT Corp. and [2]Tohoku Univ., Japan*	**15:15 B-1-4** Modified Luminescence from Germanium Self-assembled Quantum Dots in Photonic Crystal Cavity at Room Temperature J. Xia[1], N. Usami[2], Y. Ikegami[1], Y. Nakata[3] and Y. Shiraki[1], *[1]Musashi Inst. of Technology, [2]Tohoku Univ. and [3]Horiba Ltd., Japan*	**15:40 C-1-5** On-Chip Asymmetric Coaxial Waveguide Structure for Chip Area Reduction I. C. H. Lai, H. Tanimoto and M. Fujishima, *Univ. of Tokyo, Japan*	**15:15 D-1-5** Black film improving the contrast ratio of organic light emitting diodes Y. L. Wu [1], Y. C. Lin[1], F. S. Juang[2] and Y. K. Su[3], *[1]National Changhua Univ. of Education, [2]National Formosa Univ. and [3]National Cheng Kung Univ., Taiwan*	**15:15 E-1-5** Thermally-stable gate technologies for InAlAs/InGaAs/InP HEMTs L. Wang, W. Zhao and I. Adesida, *Univ. of Illinois at Urbama Champaign, USA*
15:30 A-1-6 Structure, strength and conductance of palladium wires of single atom width T. Matsuda[1] and T. Kizuka[1,2], *[1]Univ. of Tsukuba and [2]JST, Japan*	**15:30 B-1-5** Highly Efficient and Stable Photoluminescence of Nanocrystalline Porous Silicon with Fully Annealed and Passivated Surfaces B. Gelloz[1] and N. Koshida[1,2], *[1]Tokyo Univ. of Agriculture and Technology and [2]Quantum14 Co., Japan*	**16:00 C-1-6** On-Die Monitoring of Substrate Coupling for Mixed-Signal Circuit Isolation D. Kosaka, M. Fujiwara, T. Danjo and M. Nagata, *Kobe Univ., Japan*		**15:30 E-1-6** The Gate Length Reducing Process for Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs S. J. Yeon, J. Lee, G. Seol and K. Seo, *Seoul National Univ., Korea*
Break				

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
15:10 F-1-4 Robust 2-D Stack Capacitor Technologies for 64Mb 1T1C FRAM J. Y. Jung, H. J. Joo, J. H. Park, S. K. Kang, H. S. Kim, D. Y. Choi, J. H. Kim, Y. S. Lee, Y. M. Kang, S. Y. Lee, H. S. Jeong and K. Kim, *Samsung Electronics Co., Ltd., Korea*	**15:10 G-1-4** A MOCVD TiSiN/Ta Barrier Metal for Improved EM Performance and Low Via/line Resistance using Direct Contact Via (DCV) Process for Sub-65 nm Technology H. C. Lee[1], S. J. Joo[1], I. C. Baek[1], C. Shim[1], J. H. Hong[1], J. W. Han[1], K. H. Kim[1] and Y. M. Kim[2], *[1]Dongbu Electronics and [2]Hongik Univ., Korea*	**15:00 H-1-3** Effect of Tensile Strain on Gate and Substrate Currents of strained-Si n-MOSFETs T. Hoshii, S. Sugahara and S. Takagi, *Univ. of Tokyo, Japan*	**15:00 I-1-3** Uniform Self-Formation of High-Density InAs Quantum Dots by InGaAs Embedding Growth S. Tonomura[1], M. Tomita[1] and K. Yamaguchi[1], *Univ. of Electro-Communications, Japan*	**15:00 J-1-3** Wide Controllability of Flatband Voltage in La_2O_3 Gate Stack Structures - Remarkable Advantages of La_2O_3 over HfO_2 - K. Ohmori[1], P. Ahmet[2], K. Shiraishi[3], K. Yamabe[3], H. Watanabe[4], Y. Akasaka[5], N. Umezawa[1], K. Nakajima[1], M. Yoshitake[1], T. Nakayama[6], K. S. Chang[7], K. Kakushima[2], Y. Nara[5], M. L. Green[7], H. Iwai[2], K. Yamada[8] and T. Chikyow[1], *[1]National Inst. for Materials Science, [2]Tokyo Tech, [3]Univ. of Tsukuba, [4]Osaka Univ., [5]Selete, [6]Chiba Univ., [7]National Inst. of Standards and Technology and [8]Waseda Univ., Japan*
		15:20 H-1-4 Sub-30 nm Strained P-Channel FinFETs with Condensed SiGe Source/Drain Stressors K. M. Tan[1], T. Y. Liow[1,2], R. T. Lee[1], K. J. Chui[1], C. H. Tung[2], N. Balasubramanian[2], G. S. Samudra[1], W. J. Yoo[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*	**15:15 I-1-4** Individual cathode luminescence spectroscopy of zinc oxide particles based on in situ transmission electron microscopy M. Ohyama[1] and T. Kizuka[1,2], *[1]Univ. of Tsukuba and [2]JST, Japan*	**15:20 J-1-4** Study of La Concentration Dependent V_{FB} Shift in Metal/HfLaOx/Si Capacitors Y. Yamamoto, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*
15:30 F-1-5 Impact of (111)-Oriented $SrRuO_3$/Pt Tailored Electrode for Highly Reproducible Preparation of MOCVD-PZT Film for High Density FeRAM N. Menou, H. Kuwabara and H. Funakubo, *Tokyo Tech, Japan*	**15:30 G-1-5** Modeling and Characterization of the On-chip Interconnects R. Kumar[1], S. C. Rustagi[1], S. Sun[1], K. Mouthaan[2] and T. K. S. Wong[3], *[1]Inst. of Microelectronics, [2]National Univ. of Singapore and [3]Nanyang Technological Univ., Singapore*	**15:40 H-1-5** Evaluating Strained/Relaxed-Ge, Strained-Si, Strained-SiGe For Future Nanoscale p-MOSFETs. T. Krishnamohan[1], D. Kim[1], C. Jungemann[2], Y. Nishi[1] and K. C. Saraswat[1], *[1]Stanford Univ. and [2]Univ. of the Armed Forces, USA*	**15:30 I-1-5** Facile Fabrication of Gold Nanoparticle-Titanium Oxide Alternate Assemblies by Surface Sol-Gel Process and Their Photoresponsive Properties T. Arakawa, T. Kawahara, T. Akiyama and S. Yamada, *Kyushu Univ., Japan*	**15:40 J-1-5** High quality La aluminates/Si (100) interface realized by passivation of Si dangling bonds with 1monolayer epitaxial $SrSi_2$ A. Takashima, Y. Nishikawa, T. Schimizu, D. Matsushita, M. Suzuki, T. Yamaguchi and N. Fukushima, *Toshiba Corp., Japan*
Break				

Room 411/412 (A)

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-2: Novel Optical Devices
(16:15-18:00)
Chairs: T. Usuki (Fujitsu Labs.)
Y. Ohno (Tohoku Univ.)

16:15 A-2-1 (Invited)
Single Photon Detectors based on Quantum Dot Devices-from Principle of Operation to Single Photon Counting
B. E. Kardynal[1], S. S. Hees[1,2], P. See[1], A. J. Shields[1], I. Farrer[2] and D. A. Ritchie[2], *[1]Toshiba Research Europe and [2]Univ. of Cambridge, UK*

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-2: Special Session ; Photonic Crystals and Si Photonics II
(16:15-18:00)
Chairs: O. Wada (Kobe Univ.)
H. Yamada (NEC)

16:15 B-2-1 (Invited)
Integrated Photonic Network Node-Chip with Photonic Crystals
H. Yamada[1,2], T. Chu[2], A. Gomyo[1,2], J. Uchida[1,2], S. Ishida[3] and Y. Arakawa[3], *[1]NEC Corp., [2]OITDA and [3]Univ. of Tokyo, Japan*

Room 414/415 (C)

Area 5: Advanced Circuits and Systems

C-2: Wireless Interconnect
(16:30-17:30)
Chairs: M. Horiguchi (Renesas)
R. Fujimoto (Toshiba)

C-2: Wireless Interconnect
(17:30-18:10)
Chairs: R. Fujimoto (Toshiba)
T. Hamasaki (Texas Instruments Japan)

16:30 C-2-1
60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique
K. Niitsu[1], N. Miura[1], M. Inoue[1], Y. Nakagawa[2], M. Tago[2], M. Fukaishi[2], H. Ishikuro[1] and T. Kuroda[1], *[1]Keio Univ. and [2]NEC Corp., Japan*

16:50 C-2-2
Inter-chip Transmission Characteristics of Meander Dipole Antennas Integrated in 0.18 μm CMOS UWB Transceiver Chips
K. Kimoto, N. Sasaki, M. Nitta, M. Fukuda and T. Kikkawa, *Hiroshima Univ., Japan*

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-2: Organic Light Emitting Diodes and Solar Cells
(16:00-17:15)
Chairs: Y. Ohmori (Osaka Univ.)
T. Sano (Sanyo Electric)
T. Someya (Univ. of Tokyo)

16:00 D-2-1 (Invited)
TFT Technologies for Flexible Displays
J. Jang, *Kyung Hee Univ., Korea*

16:30 D-2-2
Efficient Red Electrophosphorescent Devices Based on Iridium Complexes of Fluorinated 1-phenylisoquinoline
G. Y. Park, J. H. Seo, D. I. Yoo, Y. K. Kim, Y. S. Kim and Y. Ha, *Hongik Univ., Korea*

Room 418 (E)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

E-2: Wide-Bandgap Devices
(16:15-17:45)
Chairs: Y. Ohno (Univ. of Tokushima)
S. Kuroda (Eudina Devices Inc.)

16:15 E-2-1 (Invited)
Diamond Electronics-Will it be able to compete with III-Nitrides?-
E. Kohn, *Univ. of Ulm, Germany*

Room 419 (F)

Area 4: Advanced Memory Technology

F-2: DRAM
(16:15-18:00)
Chairs: I. Asano (Elpida)
H. S. Jeong (Samsung Electronics)

16:15 F-2-1 (Invited)
Overview and Future Challenges eDRAM Technologies
H. Sugimura, T. Wake, K. Inoue, M, Hamada, H. Shirai, S. Arai, M. Takeuchi, T. Sakoh, M. Sakao and T. Tanigawa, *NEC Corp., Japan*

Room 501 (G)

Area 2: Characterization and Materials Engineering for Interconnect Integration

G-2: Characterization I
(16:15-18:00)
Chairs: N. Hata (AIST)
F. Mizuno (Meisei Univ.)

16:15 G-2-1 (Invited)
Ultralow-dielectric Polysilsesquioxane Films with High Modulus and Closed-pore Morphology
D. Y. Yoon, *Seoul National Univ., Korea*

Room 502 (H)

Area 3: CMOS Devices/Device Physics

H-2: CMOS Performance Enhancement Technology II
(16:15-18:00)
Chairs: F. Boeuf (STMicroelectronics)
H. Oda (Renesas)

16:15 H-2-1
Potential of and Issues with Multiple-Stressor Technology (MST) in High-Performance 45nm Generation Devices
T. Miyashita[1], A. Hatada[1], Y. Shimamune[1], T. Owada[2], N. Tamura[1], T. Aoyama[1] and S. Satoh[1], *[1]Fujitsu Labs., Ltd. and [2]Fujitsu Ltd., Japan*

16:35 H-2-2
Large Reduction in Standby Power Consumption Achieved with Stress-controlled SRAM Cell Layout
H. Kudo[1], K. Ishikawa[1], R. Tanabe[1], H. Fukutome[1], Y. Mishima[1], S. Satou[1], T. Sugii[1], F. Kihara[2], M. Okamoto[2], M. Yoshimura[2], T. Sugimachi[2], H. Hashimoto[2] and M. Ohtsuki[2], *[1]Fujitsu Labs., Ltd. and [2]Fujitsu Ltd., Japan*

Room 511/512 (I)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

I-2: Compound Semiconductors
(16:15-18:00)
Chairs: K.H. Ploog (Paul Drude Inst.)
D. Iwai (Fujitsu Labs.)

16:15 I-2-1
Electrical Properties of Ge-Doped InSb and InAs on GaAs(111)A Substrate
J. Nishinaga, R. Harada, T. Takada, A. Kawaharazuka and Y. Horikoshi, *Waseda Univ., Japan*

16:30 I-2-2
A method for suppressing deep-level emission in ZnSe/Ge/Ge_xSi_{1-x}/Si structure
J. T. Ku[1], T. H. Yang[1], G. Luo[2], W. C. Chou[1], T. Y. Yang[3] and C. Y. Chang[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]Academia Sinica, Taiwan*

Small Auditorium (J)

Area 1: Advanced Gate Stack / Si Processing Science

J-2: FUSI Gate Electrode
(16:15-18:00)
Chairs: K. Shiraishi (Univ. of Tsukuba)
E. Cartier (IBM)

16:15 J-2-1
Evaluation of Chemical Structures and Work Function of NiSi near the Interface between Nickel Silicide and SiO_2
A. Ohta[1], H. Yoshinaga[1], H. Murakami[1], D. Azuma[1], Y. Munetaka[1], S. Higashi[1], S. Miyazaki[1], T. Aoyama[2], K. Kosaka[2] and K. Shibahara[1], *[1]Hiroshima Univ., [2]Fujitsu Labs. and, Japan*

16:35 J-2-2
Pd_2Si Fully-Silicided Gate: Kinetics of Silicide Formation and Workfunction Tuning
T. Hosoi, K. Sano, K. Hosawa and K. Shibahara, *Hiroshima Univ., Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
16:45 A-2-2 Optical Properties of Dynamically-Modulated Dots and Wires Formed by Surface Acoustic Waves T. Sogawa[1], H. Gotoh[1], Y. Hirayama[1], T. Saku[1], S. Miyashita[2], P. V. Santos[3] and K. H. Ploog[3], *[1]NTT Corp., [2]NTT Advanced Technology Corp. and [3]Paul Drude Inst., Japan*	**16:45 B-2-2** Compact Multi-Mode Optical Ring Resonators for Interconnection on Si Chips Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*		**16:45 D-2-3** Efficiency improvement in flexible phosphorescent organic light-emitting diode S. Y. Su[1], Y. S. Tsai[1], F. S. Juang[1], L. W. Ji[1], S. H. Wang[2] and Y. K. Su[3], *[1]National Formosa Univ., [2]Kun-Shan Univ. and [3]National Cheng Kung Univ., Taiwan*	**16:45 E-2-2** C-band GaN-FET Power Amplifiers with 160-W Output Power Y. Okamoto, A. Wakejima, K. Matsunaga, Y. Ando, T. Nakayama, K. Ota and H. Miyamoto, *NEC Corp., Japan*
17:00 A-2-3 Photon Statistics in a Thick Barrier Coupled Quantum Dot S. Yamauchi[1,2], A. Shikanai[1,2], I. Morohashi[1,2], S. Furue[1,2], K. Komori[1,2], T. Sugaya[1,2] and T. Takagahara[3], *[1]AIST, [2]CREST and [3]Kyoto Inst. of Technology, Japan*	**17:00 B-2-3** Silicon Optical Modulators in Silicon-on-Insulator (SOI) Substrate Based on the p-i-n Waveguide Structure M. T. Hsu and R. W. Chuang, *National Cheng Kung Univ., Taiwan*	**17:10 C-2-3** On-Chip Yagi Antenna for Wireless Signal Transmission in Stacked MCP K. Ohashi[1], T. Yammouch[1], M. Kimura[1], H. Ito[1], K. Okada[1], K. Ishida[1], K. Itoi[2], M. Sato[2], T. Ito[2] and K. Masu[1], *[1]Tokyo Tech and [2]Fujikura Ltd., Japan*	**17:00 D-2-4** Energy Transfer Employing Europium Complex and Blue Phosphorescent Dye and Application for White Organic Light-Emitting Diodes Y. Hino, H. Kajii and Y. Ohmori, *Osaka Univ., Japan*	**17:00 E-2-3** GaN-based Direct-coupled FET Logic (DCFL) Digital Circuits Operating at 375ºC Y. Cai, Z. Cheng, Z. Yang, C.W. Tang, K.M. Lau, K.J. Chen, *Hong Kong University of Science and Technology, Hong Kong*
17:15 A-2-4 Exciton Rabi Oscillation in InAs/GaAs Coupled Quantum Dot K. Goshima[1,2], K. Komori[1,2], S. Yamauchi[1,2], I. Morohashi[1,2] and T. Sugaya[1, 2, *[1]AIST and [2]CREST, Japan*	**17:15 B-2-4** Low Temperature Fabrication of Monolithic Mach-Zehnder Optical Modulator on Silicon using Sputtered (Ba,Sr)TiO_3 and Mechanism of Transient Response M. Suzuki, K. Nagata, Y. Tanushi and S. Yokoyama, *Hiroshima Univ., Japan*		**17:15 D-2-5** Formation of bulk-heterojunction structure in organic bilayer solar cells by heat treatment T. Osasa, S. Yamamoto and M. Matsumura, *Osaka Univ., Japan*	**17:15 E-2-4** Effects of Growth Temperature of a GaN Cap Layer on Electrical Properties of AlGaN/GaN HFETs T. Deguchi[1], M. Yamashita[1], E. Waki[1], A. Nakagawa[1], H. Ishikawa[2] and T. Egawa[2], *[1]New Japan Radio Co., Ltd. and [2]Nagoya Inst. of Technology, Japan*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
16:45 F-2-2 A Highly Reliable MIM Technology with non-Crystallized HfOx Dielectrics Using Novel MOCVD Stacked TiN Bottom Electrodes T. Ohtsuka[2], Y. Shibata[1], H. Arai[1], H. Ichimura[1], S. Matsuyama[1], K. Uchiyama[1], J. Suzuki[1], A. Tsuzumitani[1], K. Yoneda[1], Y. Hashimoto[1], T. Nakabayashi[1] and E. Fujii[1], *[1]Matsushita Electric and [2]Panasonic Semiconductor Engineering Co., Ltd., Japan*	**16:45 G-2-2** SiOCH Films with Hydrocarbon Network Bonds: First-Principles Investigation N. Tajima[1], T. Hamada[2], T. Ohno[1], K. Yoneda[3], S. Kondo[3], N. Kobayashi[3], M. Shinriki[4], K. Miyazawa[4], K. Sakota[4], S. Hasaka[4] and M. Inoue[4], *[1]NIMS, [2]Univ. of Tokyo, [3]Selete and [4]Taiyo Nippon Sanso Corp., Japan*	**16:55 H-2-3** Layout Independent Transistor with Stress-controlled and Highly Manufacturable STI Process K. Horita, M. Ishibashi, H. Umeda, T. Kawahara, T. Ikeda, T. Yamashita, T. Kuroi and Y. Inoue, *Renesas Technology Corp., Japan*	**16:45 I-2-3** Effect of Hydrogen in Zinc Oxide Thin-Film Transistor grown by MOCVD J. Jo[1], O. Seo[2], E. Jeong[1], H. Seo[1], B. Lee[3] and Y. I. Choi[1], *[1]Ajou Univ., [2]NFC and [3]CDA Co., Ltd., Korea*	**16:55 J-2-3** Workfunction Adjustment Using Thin Metal Film (Ti, Pd) under FUSI Gate Electrode and Laser Annealing Y. Huang [1,2,3], K. L. Pey[1], D. Z. Chi[3], K. K. Ong[1], P. S. Lee[1] and I. S. Goh[2], *[1]Nanyang Technological Univ., [2]Systems on Silicon Manufacturing Co. Pte. Ltd. and [3]Inst. of Material Research & Engineering, Singapore*
17:05 F-2-3 Robust and Cost-Effective MIS-Al_2O_3/SiON Double-Layered Capacitor Technology for Sub-90 nm DRAMs O. Tonomura, H. Hamamura and H. Miki, *Hitahchi Ltd., Japan*	**17:05 G-2-3** Nondestructive characterization of temperature-dependent backbone Si-O-Si structure in porous silica films by in-situ Fourier-transform infrared spectroscopy S. Takada[1], N. Hata[1,2], X. Li[1], N. Fujii[3], T. Nakayama[3] and T. Kikkawa[2,4], *[1]ASRC-AIST, [2]MIRAI-ASRC-AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*		**17:00 I-2-4** The Effect of As_2 and As_4 Molecule Beam Species on MBE Grown GaN_xAs_{1-x} /GaAs MQW by Modulated N Radical Beam Source M. Kakino[1], K. Fujii[1], K. Takao[1], H. Miyagawa[1], N. Tsurumachi[1], H. Itoh[1], S. Nakanishi[1], H. Akiyama[2] and S. Koshiba[1], *[1]Kagawa Univ. and [2]Univ. of Tokyo, Japan*	
17:25 F-2-4 Diffusion Barrier Characteristics of TiSix/TiN for Tungsten Dual Poly Gate in DRAM M. G. Sung, K. Y. Lim, H. J. Cho, S. R. Lee, S. A. Jang, Y. S. Kim, M. S. Joo, J. H. Lee, T. Y. Kim, H. S. Yang, S. H. Pyi and J. W. Kim, *Hynix Corp., Korea*	**17:25 G-2-4** Characterization of Low-k Interconnect Dielectrics by EELS Y. Otsuka[1], M. Shimada[2], N. Kawasaki[1] and S. Ogawa[2], *[1]Toray Research Center Inc. and [2]Selete, Japan*	**17:15 H-2-4** A Full Analytical Model to evaluate Strain Induced by CESL on MOSFET Performances F. Payet[1], F. Boeuf[1], C. Ortolland[2] and T. Skotnicki[1], *[1]STMicroelectronics and [2]Philips Semiconductors, France*	**17:15 I-2-5** GaN Heteroepitaxy on Si(111) substrates Using AlN/AlGaN Superlattice Buffer Layers T. Akasaka, Y. Kobayashi and T. Makimoto, *NTT Corp., Japan*	**17:15 J-2-4** The first principles calculations of fermi level pinning in FUSI-PtSi/HfO_2/Si system induced by local distortion of HfO_2 M. Ikeda[1], G. Kresse[2], M. Kadoshima[1], T. Nabatame[1], H. Satake[1] and A. Toriumi[3,4], *[1]MIRAI-ASET, [2]Univ. Wien, [3]MIRAI-AIST and [4]Univ. of Tokyo, Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
17:30 A-2-5 Study of Basic Characteristics of Spin - Photodiode Consisting of III-V p-n Heterojunction J. Hayafuji, T. Kondo and H. Munekata, *Tokyo Tech, Japan*	**17:30 B-2-5** Light emission from two junction Si CMOS LED's (450nm - 750nm) with two order increase in emission intensity-Applications for next generation silicon-based optoelectronics L. W. Snyman[1], M. du Plessis[2] and H. Aharoni[3], *[1]Tshwane Univ. of Technology, [2]Univ. of Pretoria and [3]Ben Gurion Univ. of the Negev, South Africa*	**17:30 C-2-4** On-chip Ultra-Wideband Receiver using Silicon Integrated Antennas for Inter-chip Wireless Interconnection N. Sasaki, M. Fukuda, M. Nitta, K. Kimoto and T. Kikkawa, *Hiroshima Univ., Japan*	**17:30 D-2-6** Build-on Technology of Bi-Directional Optical Communication System using Bi-Functional Organic Diodes H. Okada, Y. Matsushita, S. Naka and H. Onnagawa, *Univ. of Toyama, Japan*	**17:30 E-2-5** The High Temperature Thermally Treated SiNx Passivation of AlGaN/GaN HEMT using Remote PECVD J. C. Her[1], D. H. Kim[1], S. W. Kim[1], K. C. Jang[1], J. H. Lee[2] and J. E. Oh[3], *[1]Seoul National Univ., [2]THELEDS Co., LTD. and [3]Hanyang Univ., Korea*
17:45 A-2-6 Resonant Terahertz Detection Based on High-electron-mobility Transistor with Schottky Source/Drain Contact A. Satou[1], V. Ryzhii[1], T. Otsuji[2] and M. S. Shur[3], *[1]Univ. of Aizu, [2]Tohoku Univ. and [3]Rensselaer Polytechnic Inst., Japan*		**17:50 C-2-5** A 0.18 μm CMOS Impulse Radio Based UWB Transmitter for Global Wireless Interconnections of 3D Stacked-Chip System M. Fukuda, P. K. Saha, N. Sasaki, M. Nitta and T. Kikkawa, *Hiroshima Univ., Japan*		

18:30-20:30 Bauquet/Young Award (Intercontinental Hotel, Pacific 3F)

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
		17:35 H-2-5 56% pMOSFETs Drive Current Enhancement from Optimized Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS K. H. Lee, C. T. Huang, W. H. Hung, L. S. Jeng, S. F. Ting, M. L. Tseng, J. C. Wu, T. M. Shen, O. Cheng and C. W. Liang, *United Microelectronics Corp., Taiwan*	**17:30 I-2-6** Strong Ultraviolet Emission from InGaN/AlGaN Multi Quantum Well Grown by Multi-step Process H. G. Chen, H. H. Yao, J. T. Chu, N. F. Hsu, T. C. Lu, H. C. Kuo and S. C. Wang, *National Chiao Tung Univ., Taiwan*	**17:35 J-2-5** Si-Capped Annealing of HfO_2-based Dielectrics for Suppressing Interface Layer Growth and Oxygen Out-Diffusion M. Takahashi[1], H. Satake[1], M. Kadoshima[1], A. Ogawa[1], K. Iwamoto[1], H. Ota[2], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC and [3]Univ. of Tokyo, Japan*
17:45 F-2-5 Gate Workfunction Engineering of Bulk FinFETs for Sub-50 nm DRAM Cell Transistors K. H. Park, K. R. Han, Y. M. Kim and J. H. Lee, *Kyungpook National Univ., Korea*	**17:45 G-2-5** Local Bonding Structure of High-Stress Silicon Nitride Film modified by UV Curing for Strained-Silicon Technology beyond 45nm Node SoC Devices Y. Miyagawa[1], T. Murata[1], Y. Nishida[1], T. Nakai[1], A. Uedono[2], N. Hattori[1], M. Matsuura[1], K. Asai[1] and M. Yoneda[1], *[1]Renesas Technology Corp. and [2]Univ. of Tsukuba, Japan*		**17:45 I-2-7** Hexagonal Boron Nitride Heteroepitaxial Layers on Graphitized 6H-SiC Substrate Grown by Metalorganic Vapor Phase Epitaxy Y. Kobayashi[1], H. Hibino[1], T. Nakamura[2], T. Akasaka[1], T. Makimoto[1] and N. Matsumoto[2], *[1]NTT Corp. and [2]Shonan Inst. of Technology, Japan*	

18:30-20:30 Bauquet/Young Award (Intercontinental Hotel, Pacific 3F)

Room 411/412 (A)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

A-3: MEMS and NEMS : Fabrication
(9:00-10:30)
Chairs: T. Nishimoto (Shimadzu)
T. Ono (Tohoku Univ.)

9:00 A-3-1 (Invited)
New Approach to Experimental Nanomechanics Using MEMS Technology
Y. Isono, *Ritsumeikan Univ., Japan*

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-3: LEDs and Lasers
(9:00-10:30)
Chairs: M. Ezaki (Toshiba)
M. Sugawara (Fujitsu Labs.)

9:00 B-3-1
High Brightness and Crack-free InGaN/GaN Light Emitting Diode With AlGaN Buffer Layer On Si (111)
Y. P. Hsu[1], S. J. Chang[1], Y. K. Su[1], W. S. Chen[1], J. K. Sheu[1], J. Y. Chu[1] and C. T. Kuo[2], *[1]National Cheng Kung Univ. and [2]Epitech Technology Corp., Taiwan*

9:15 B-3-2
Improved light output and electrical performance of InGaN/GaN light-emitting diode by surface texturing of the n-type GaN
S. H. Su, C. C. Hou, R. S. Shieh and M. Yokoyama, *I-Shou Univ., Taiwan*

Room 414/415 (C)

Area 5: Advanced Circuits and Systems

C-3: Toward Next Generation Systems
(9:00-9:40)
Chairs: H. Yamauchi (Sanyo Electric)
H. Kobayashi (Gunma Univ.)

C-3: Toward Next Generation Systems
(9:40-10:20)
Chairs: K. Masu (Tokyo Tech)
H. Yamauchi (Sanyo Electric)

9:00 C-3-1
Large-Scale Quantum Computing Emulation Based on Unitary Macro-Operations
Y. Goto and M. Fujishima, *Univ. of Tokyo, Japan*

9:20 C-3-2
Random Number Generator with 0.3MHz Generation Rate using Non-Stoichiometric Si_xN MOSFET
M. Matsumoto, R. Ohba, S. Yasuda, K. Uchida, T. Tanamoto and S. Fujita, *Toshiba Corp., Japan*

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-3: Organic Materials and Device Physics I
(9:00-10:30)
Chairs: K. Kato (Niigata Univ.)
K. Kudo (Chiba Univ.)

9:00 D-3-1 (Invited)
Organic Single Crystal Transistors and Interface Control
Y. Iwasa, *Tohoku Univ., Japan*

Room 418 (E)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

E-3: Sensors and Interface Physics
(9:00-10:00)
Chairs: T. Hashizume (Hokkaido Univ.)
K. Kumakura (NTT)

9:00 E-3-1
Performance of open-gate AlGaN/GaN HFET in various kinds of liquids
T. Kokawa, T. Sato and T. Hashizume, *Hokkaido Univ., Japan*

9:15 E-3-2
Characteristics of a New Resistive-Type Hydrogen Sensor
C. W. Hung, H. L. Lin, H. I. Chen, Y. Y. Tsai, P. H. Lai, S. I. Fu and W. C. Liu, *National Cheng Kung Univ., Taiwan*

Room 419 (F)

Area 3: CMOS Devices/Device Physics

F-3: Quasi-Ballistic Transport
(9:00-10:40)
Chairs: Y. Kamakura (Osaka Univ.)
K. Kurimoto (Matsushita Electric)

9:00 F-3-1
Ohm's Law from a Transmission Viewpoint
K. Natori[1,2] and T. Shimizu[1], *[1]Univ. of Tsukuba and [2]CREST-JST, Japan*

9:20 F-3-2
A Picture of Quasi-Ballistic Transport in Nanoscale MOSFETs
H. Tsuchiya, K. Fujii, T. Mori and T. Miyoshi, *Kobe Univ., Japan*

Room 501 (G)

Room 502 (H)

Room 511/512 (I)

Small Auditorium (J)

Area 1: Advanced Gate Stack / Si Processing Science

J-3: Characterization of Gate Stack
(9:10-10:40)
Chairs: S. Miyazaki (Hiroshima Univ.)
A. Sakai (Nagoya Univ.)

9:10 J-3-1 (Invited)
High-resolution RBS Analysis of Si-dielectrics Interfaces
K. Kimura[1], Z. Ming[1], K. Nakajima[1], M. Suzuki[1], M. Uematsu[2], K. Torii[3], S. Kamiyama[3], Y. Nara[3], H. Watanabe[4], K. Shiraishi[5], T. Chikyow[6] and K. Yamada[7], *[1]Kyoto Univ., [2]NTT Corp., [3]Selete, [4]Osaka Univ., [5]Univ. of Tsukuba, [6]NIMS and [7]Waseda Univ., Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
9:30 A-3-2 CMOS-Compatible Suspended Square Inductors on Silicon Wafers for RF ICs C. M. Tai and C. N. Liao, *National Tsing Hua Univ., Taiwan*	**9:30 B-3-3** Fabrication of High Light-Extraction Efficiency LED Using Nanostructures by UV Nanoimprint Lithography and Electrodeposition H. Ono[1], Y. Ono[2], K. Kasahara[2], J. Mizuno[1] and S. Shoji[1], *[1]Waseda Univ. and [2]Sumitomo Chemical Co., Ltd, Japan*	**9:40 C-3-3** Nearest-Euclidean-Distance Search Associative Memory Architecture with Fully Parallel Mixed Digital-Analog Match Circuitry M. A. Abedin, Y. Tanaka, A. Ahmadi, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan*	**9:30 D-3-2** Decay process of a large surface potential of as-deposited Alq3 films N. Kajimoto, T. Manaka and M. Iwamoto, *Tokyo Tech, Japan*	**9:30 E-3-3** Modulation of Resistivity of Two-Dimensional Electron Gas in AlGaN/GaN Structure Y. C. Chang[1], J. K. Sheu[1] and Y. L. Li[2], *[1]National Cheng Kung Univ. and [2]National Taiwan Univ., Taiwan*
9:45 A-3-3 Ultra high aspect ratio sub-micron silicon micromachining by double-passivation deep reactive ion etching R. Nagarajan and B. R. Murthy, *Inst. of Microelectronics, Singapore*	**9:45 B-3-4** Light Emitting Diode Array Prepared by Epitaxial Film Bonding T. Suzuki, H. Fujiwara, M. Mutoh, T. Sagimori, H. Kurokawa, T. Igari, T. Kaneto, H. Furuta, I. Abiko, M. Sakuta and M. Ogihara, *Oki Digital Imaging Corp., Japan*		**9:45 D-3-3** Electronic structure of bathocuproine on metal studied by ultraviolet photoemission spectroscopy S. Toyoshima[1,2], K. Kuwabara[1], T. Sakurai[1], T. Taima[2], K. Saito[2], H. Kato[3] and K. Akimoto[1], *[1]Tsukuba Univ., [2]AIST and [3]Hirosaki Univ., Japan*	**9:45 E-3-4** Electrical and Optical Properties of an n-Channel GaN Schottky Barrier MISFET H. B. Lee, H. I. Cho, H. S. An, J. H. Lee and S. H. Hahm, *Kyungpook National Univ., Korea*
10:00 A-3-4 Room Temperature Vacuum Sealing with Au Thin Films Using Ar Beam Surface Activation H. Okada, T. Itoh and T. Suga, *Univ. of Tokyo, Japan*	**10:00 B-3-5** High Performances of 650 nm Resonant Cavity Light Emitting Diodes for Plastic Optical Fiber Applications Y. C. Lee[1], C. E. Lee[1], S. W. Chiou[2], H. C. Kuo[1], T. C. Lu[1] and S. C. Wang[1], *[1]National Chiao Tung Univ. and [2]United Epitaxy Co., Taiwan*	**10:00 C-3-4** Scaling Trends and Mitigation Techniques for Soft Errors in Flip-Flops T. Uemura[1], Y. Tosaka[1], S. Satoh[1], K. Takahisa[2] and K. Hatanaka[2], *[1]Fujitsu Labs. Ltd. and [2]Osaka Univ., Japan*	**10:00 D-3-4** Spin injection from magnetic electrodes to organic semiconductors studied by transport and spectroscopic measurements T. Shimada, *Univ. of Tokyo, Japan*	

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
9:40 F-3-3 Intrinsic Delay of Nanoscale MOSFETs under Ballistic Transport A. Tsuda, T. Kunikiyo, T. Okagaki, T. Watanabe, M. Tanizawa, K. Ishikawa, H. Nunogami and A. Uchida, *Renesas Technology Corp., Japan*				**9:40 J-3-2** Real-Time Observation of Initial Thermal Oxidation on Si(110)-16x2 Surfaces by O1s Photoemission Spectroscopy Using Synchrotron Radiation M. Suemitsu[1], A. Kato[1], H. Togashi[1], A. Konno[1], Y. Yamamoto[1], Y. Teraoka[2], A. Yoshigoe[2] and Y. Narita[3], *[1]Tohoku Univ., [2]Japan Atomic Energy Agency and [3]Kyushu Inst. of Technology, Japan*
10:00 F-3-4 The effect of side-traps on ballistic transistor in Kondo regime T. Tanamoto, K. Uchida and S. Fujita, *Toshiba Corp., Japan*				**10:00 J-3-3** Nonlinear Al Concentration Dependence of the HfAlOx/Si Conduction Band Offset Studied by Internal Photoemission Spectroscopy T. Horikawa[1], A. Ogawa[2], K. Iwamoto[2], K. Okada[2], H. Ota[1], T. Nabatame[2] and A. Toriumi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
10:15 A-3-5 MEMS Wafer Level Packaging by Using Surface Activated Bonding Y. Takegawa, T. Baba, T. Okudo and Y. Suzuki, *Matsushita Electric Works, Ltd., Japan*	**10:15 B-3-6** InP-Based Quantum Cascade Lateral Grating Distributed Feedback Lasers K. Kennedy, D. G. Revin, A. B. Krysa, K. M. Groom, L. R. Wilson, J. W. Cockburn and R. Hogg, *Univ. of Sheffield, UK*		**10:15 D-3-5** Dependence of Memory Characteristics of Organic Bi-stable Device on Structural Parameters J. J. Lee and C. K. Song, *Dong-A Univ., Korea*	

Break

Short Presentation P11 and P8 (10:45-12:15) Chair: H. Tabata (Osaka Univ.)	Short Presentation P7 and P4 (10:45-12:15) Chair: M. Sugawara (Fujitsu Labs.)	Short Presentation P5 and P2 (10:45-12:15) Chair: H. Kobayashi (Gunma Univ.)	**Area 10: Organic Materials Science, Device Physics, and Applications** D-4: Organic Materials and Device Physics II (10:45-11:30) Chairs: M. Iwamoto (Tokyo Tech) K. Kato (Niigata Univ.)	Short Presentation P6 and P9 (10:45-12:15) Chair: M. Kuzuhara (Univ. of Fukui)

10:45 D-4-1
Self Assembled Viologen Modified Electrode as Mediator of Glucose Sensor
D. Y. Lee[1], A. K. M. Kafi[1], S. H. Park[1], D. J. Qian[2] and S. Kwon[1], *[1]Dong-A Univ. and [2]Fudan Univ., Korea*

11:00 D-4-2
Orientation and Electrical Conduction of Poly(3-hexylethiophene) Thin Film Prepared by Using a Different Solution-process Method
S. Mototani, S. Ochiai, S. Tanabe, A. Ohashi, Y. Uchida, K. Kojima and T. Mizutani, *Aichi Inst. of Tech., Japan*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
				10:20 J-3-4 Electric characteristics of Si_3N_4 films formed by directly radical nitridation on Si (110) and Si (100) surfaces M. Higuchi[1], T. Aratani[1], T. Hamada[1], A. Teramoto[1], T. Hattori[1,2], S. Sugawa[1], T. Ohmi[1], S. Shinagawa[2], H. Nohira[2], E. Ikenaga[3] and K. Kobayashi[3], *[1]Tohoku Univ., [2]Musashi Inst. of Technology and [3]JASRI/SPring8, Japan*

Break

Short Presentation P3 (10:45-12:15) Chair: H. Oda (Renesas)	Short Presentation P1 (10:45-12:15) Chair: Y. Nara (Selete)

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
			11:15 D-4-3 Theoretical Investigation of Electrical and Electronic Properties of Carbon Materials A. Chutia[1], Z. Zhu[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], M. Kubo[1,2], C. A. Del Carpio[1], P. Selvam[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*	
			Short Presentation P10 (11:30-12:30) **Chair: K. Kubo (Chiba Univ.)**	

Lunch

13:00-15:00 Poster Session (Room 501, 502, 511/512, 5F)

Area 8: Advanced Material Synthesis and Crystal Growth Technology Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 7: Photonic Devices and Device Physics	Area 4: Advanced Memory Technology	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 1: Advanced Gate Stack/Si Processing Science
A-5: Nanowires and Nanotubes I (15:15-16:15) Chairs: T. Fukui (Hokkaido Univ.) Y. L. Foo (Inst. of Materials Research & Engineering)	B-5: Quantum-dot Lasers (15:15-16:30) Chairs: M. Sugawara (Fujitsu Labs.) K. Komori (AIST)	C-5: ReRAM (15:15-16:25) Chairs: Y. Ohji (Renesas) I. Asano (Elpida)	D-5: Emerging Interconnect (15:15-16:15) Chairs: T. Yoda (Toshiba) T. Tatsumi (SONY)	E-5: Junction I (15:15-16:35) Chairs: B. Mizuno (UJT Inc.) H. Hwang (Gwangju Inst. of Sci. & Tech.)
15:15 A-5-1 (Invited) ZnO Nanorods for Electronic Nanodevice Applications G. C. Yi, W. I. Park, J. Yoo, H. J. Kim and C. H. Lee, *POSTECH, Korea*	**15:15 B-5-1 (Invited)** Self-Assembled Quantum Dots: Engineered Gain Medium S. Oktyabrsky, M. Yakimov, J. Van Eisden and V. Tokranov, *State Univ. of New York at Albany, USA*	**15:15 C-5-1 (Invited)** Mechanisms of Resistance Switching Memory Effect in Oxides M. Kawasaki, *Tohoku Univ., Japan*	**15:15 D-5-1 (Invited)** Si Nano-photonics for LSI on-chip Optical Interconnection K. Nishi, J. Fujikata, H. Yamada, T. Ishi, M. Nakada, K. Nose, M. Mizuno, M. Fukaishi, Y. Urino and K. Ohashi, *NEC Corp., Japan*	**15:15 E-5-1** Atmospheric In-situ Arsenic-Doped SiGe Selective Epitaxial Growth for Raised Extension NMOSFET T. Ikuta, Y. Miyanami, S. Fujita, H. Iwamoto and S. Kadomura, *Sony Corp., Japan*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)

Lunch

13:00-15:00 Poster Session (Room 501, 502, 511/512, 5F)

Area 3: CMOS Devices/Device Physics	Area 1: Advanced Gate Stack/Si Processing Science
F-5: Device Reliability and Characterization (15:15-16:35) Chairs: Y. Kamakura (Osaka Univ.) J. C. S. Woo (UCLA)	J-5: High-k Dielectrics I (15:15-16:35) Chairs: Y. Tsunashima (Toshiba) T. Nabatame (ASET)
15:15 F-5-1 (Invited) Simulation of Atomic Scale Effects and Fluctuations in Nano-Scale CMOS A. Asenov, A. R. Brown, G. Roy, C. Alexander and A. Martinez, *Univ. of Glasgow, UK*	**15:15 J-5-1** Plasma Nitridation of HfO_2 Enabling a 0.9 nm EOT with High Mobility for a Gate First MOSFET P. D. Kirsch[1], M. Quevedo-lopez[2], S. A. Krishnan[3], C. Krug[3], F. S. Aguirre[4], R. M. Wallace[4], B. H. Lee[1] and R. Jammy[1], *[1]IBM, [2]Texas Instruments, [3]SEMATECH and [4]UT-Dallas, Usa*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
15:45 A-5-2 Arrangement of Catalyst Islands at Surface Atomic Steps toward Position Control of Nanowires H. Hibino, K. Tateno and Y. Watanabe, *NTT Corp., Japan*	**15:45 B-5-2 (Invited)** Fabrication of Sb-based QDs for Long-wavelength VCSELs N.Yamamoto[1], K. Akahane[1], S. Gozu[1], A. Ueta[1], N. Ohtani[2] and M. Tsuchiya[1], *[1]NICT and [2]Doshisha Univ., Japan*	**15:45 C-5-2** Low Power Operation of Non-volatile Hafnium Oxide Resistive Memory H. Y. Lee[1], P. S. Chen[2], C. C. Wang[1], S. Maikap[1], P. J. Tzeng[1], C. H. Lin[1], L. S. Lee[1] and M. J. Tsai[1], *[1]Industrial Technology Research Inst. and [2]Ming Shin Univ. of Science & Technology, Taiwan*	**15:45 D-5-2 (Invited)** 3D System Integration: Enabling Technologies and Applications P. Ramm, *Fraunhofer IZM, Germany*	**15:35 E-5-2** Self-Heating Induced Germanium Outdiffusion and Non-Local Channel Degradation in the Strained-Si/SiGe N-MOSFET subjected to Channel Hot-Electron Stress T. W. H. Phua[1], D. S. Ang[2], C. H. Tung[3] and C. H. Ling[1], *[1]National Univ. of Singapore, [2]Nanyang Technological Univ. and [3]Inst. of Microelectronics, Singapore*
16:00 A-5-3 Exciton and biexciton emissions from single GaAs quantum dots in (Al,Ga)As nanowires H. Sanada, H. Gotoh, K. Tateno and H. Nakano, *NTT Corp., Japan*		**16:05 C-5-3** SiOx/ß-SiC/Si MIS Resistive Memory Devices Formed by One- and Two-Stage Oxidation of ß-SiC M. Shouji, T. Nagashima and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan*		**15:55 E-5-3** Ni(alloy)-germanosilicide contact technology for Si1-xGex (x=0.20-0.5) junctions K. L. Pey[1,2], L. Jin[1], W. K. Choi[1,3], H. P. Yu[1], D. A. Antoniadis[1,4], E. A. Fitzgerald[1,4], D. Z. Chi[5] and D. M. Isaacson[1,4], *[1]SMA, [2]Nanyang Technological Univ., [3]National Univ. of Singapore, [4]MIT and [5]IMRE, Singapore* **16:15 E-5-4** Impacts of Si Crystal Orientation on NiSi Silicided Junction Leakage Induced by Anisotropic Ni Migration M. Tsuchiaki[1] and A. Nishiyama[1], *Toshiba Corp., Japan*
Break				

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
15:45 F-5-2 Improvement of Device Characteristics Variation by using a Body-Bias Controlling Technology Based on a Hybrid Trench Isolated SOI Y. Maki, Y. Hirano, M. Tsujiuchi, T. Iwamatsu, O. Ozawa, T. Ipposhi and Y. Inoue, *Renesas Technology Corp., Japan*				**15:35 J-5-2** Excellent Leakage Current of Crystallized Silicon-Doped HfO_2 Films Down to Sub-nm EOT K. Tomida, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*
16:05 F-5-3 3D Statistical Simulation of Gate Leakage Fluctuations Due to Combined Interface Roughness and Random Dopants S. Markov[1], A. R. Brown[1], B. Cheng[1], G. Roy[1], S. Roy[1] and A. Asenov[1], *Univ. of Glasgow, UK*				**15:55 J-5-3** Spatial Fluctuation of Electrical properties in Hf-Silicate Film Observed with Scanning Capacitance Microscopy Y. Naitou[1,4], A. Ando[1], H. Ogiso[2], S. Kamiyama[3], Y. Nara[3], H. Watanabe[4] and K. Yasutake[4], *[1]AIST NeRI, [2]AIST-Advanced Manufacturing Research Inst., [3]Selete and [4]Osaka Univ., Japan* **16:15 J-5-4** Mechanism of Threshold Voltage Reduction and Hole Mobility Enhancement in pMOSFETs Employing Sub-1nm EOT HfSiON by Use of Substrate Fluorine Ion Implantation S. Inumiya[1], A. Uedono[2], S. Miyazaki[3], S. Ohtsuka[1], T. Matsuki[1], T. Wada[1], T. Aoyama[1], K. Yamada[4] and Y. Nara[1], *[1]Selete, [2]Univ. of Tsukuba, [3]Hiroshima Univ. and [4]Waseda Univ., Japan*
Break				

Room 411/412 (A)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-6: Nanowires and Nanotubes II
(16:30-18:00)
Chairs: K. Matsumoto (Osaka Univ.)
Y. Awano (Fujitsu Labs.)

16:30 A-6-1 (Invited)
Probing Carbon Nanostructures Growth Mechanism Using an in-situ UHVTEM
Y. L. Foo, *Inst. of Materials Research and Engineering, Singapore*

17:00 A-6-2
High-Sensitive and Label-Free Detection of Biomolecules Using Single-Walled Carbon Nanotube Modified Microelectrodes
J. Okuno[1], K. Maehashi[1], K. Matsumoto[1], K. Kerman[2], Y. Takamura[2] and E. Tamiya[2], *[1]Osaka Univ. and [2]JAIST, Japan*

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-6: Quantum Optical Devices
(16:45-18:00)
Chairs: L. Lester (Univ. of New Mexico)
T. Usuki (Univ. of Tokyo)

16:45 B-6-1 (Invited)
Single-photon Generator for Telecom Applications
T. Usuki[1], K. Takemoto[2], S. Hirose[2], M. Takatsu[2], T. Miyazawa[1], Y. Sakuma[3], N. Yokoyama[2] and Y. Arakawa[1], *[1]Univ. of Tokyo, [2]Fujitsu Labs. and [3]NIMS, Japan*

Room 414/415 (C)

Area 4: Advanced Memory Technology

C-6: Flash Memory I
(16:45-17:55)
Chairs: Y. Yamauchi (Sharp)
Y. Shimamoto (Hitachi Ltd.)

16:45 C-6-1 (Invited)
Future Outlook of Floating Gate Flash Memory
F. Arai, *Toshiba Corp., Japan*

Room 416/417 (D)

Area 2: Characterization and Materials Engineering for Interconnect Integration

D-6: Assembly and Packaging
(16:25-17:45)
Chairs: S. H. Brongersma (IMEC)
D. Y. Yoon (Seoul National Univ.)

16:25 D-6-1
Real-time observation of Hydrogen Plasma Reflow Process with Lead-free Solder Pastes
S. Nishi[1], E. Higurashi[1], T. Suga[1], T. Hagihara[2], T. Takeuchi[2], Y. Shingai[2], S. Yamagata[3], R. Katoh[3] and K. Arase[3], *[1]Univ. of Tokyo, [2]Shinko Seiki Co., Ltd. and [3]Senju Metal Industry Co., Ltd., Japan*

16:45 D-6-2
The Reliability Characteristics of Wafer-Level Chip-Scale Package under Various Current Stressing
H. Y. Kung[1,3], S. H. Chen[2], Y. S. Lai[3], E. Jahja[1] and W. K. Yeh[1], *[1]National Univ. of KaoHsiung, [2]Tung Fang Inst. of Technology and [3]Advanced Semiconductor Engineering, Inc., Taiwan*

Room 418 (E)

Area 1: Advanced Gate Stack/Si Processing Science

E-6: Junction II
(16:45-17:45)
Chairs: B. Mizuno (UJT Inc.)
H. Fukutome (Fujitsu Labs.)

16:45 E-6-1
Reduction in PN Junction Leakage for Ni-silicided Small Si Islands by Using Thermal Conduction Heating with Stacked Hot Plates
H. Itokawa[1], H. Akutsu[1], A. Nomachi[1], H. Oono[2], T. Iinuma[1] and K. Suguro[1], *[1]Semiconductor Company, Toshiba Corp. and [2]Toshiba Corp., Japan*

17:05 E-6-2
A Novel Laser Annealing Process for Advanced CMOS with Suppressed Gate Depletion and Ultra-shallow Junctions
A. Shima[1], T. Mine[1], L. Feng[2], X. Wang[2], Y. Wang[2] and K. Torii[1], *[1]Hitachi, Ltd. and [2]Ultratech Inc., Japan*

Room 419 (F)

Area 3: CMOS Devices/Device Physics

F-6: Device Fluctuation Analysis
(16:45-18:05)
Chairs: D. Hisamoto (Hitachi Ltd.)
Y. Momiyama (Fujitsu)

16:45 F-6-1
NBTI Improvement under Highly Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS and Beyond
C. T. Huang, L. S. Jeng, W. H. Hung, S. F. Ting, K. H. Lee, M. L. Tseng, O. Cheng and C. W. Liang, *United Microelectronics Corp., Taiwan*

17:05 F-6-2
NBT Stress Induced Anomalous Drain Current Instability in HfSiON pMOSFETs Arising from Bipolar Charge Trapping
C. J. Tang[1], H. C. Ma[1], C. T. Chan[1], T. Wang[1] and H. C. Wang[2], *[1]National Chiao Tung Univ. and [2]TSMC, Taiwan*

Room 501 (G)

Room 502 (H)

Room 511/512 (I)

Area 5: Advanced Circuits and Systems

I-6: Analog Circuit Techniques
(16:45-18:05)
Chairs: H. Kobayashi (Gunma Univ.)
T. Komuro (Agilent Technologies International Japan)

16:45 I-6-1 (Invited)
A Practical, Systematic, Simple Method to Evaluate Speed/Bandwidth Potential of CMOS Processes for Analog Design and Related Practical Considerations
K. Hadidi, *Urmia Univ., Iran*

Small Auditorium (J)

Area 1: Advanced Gate Stack / Si Processing Science

J-6: Interface Properties of Ge
(16:45-17:45)
Chairs: K. Shiraishi (Univ. of Tsukuba)
A. Sakai (Nagoya Univ.)

16:45 J-6-1
Quantitative Evaluation of Interface Trap Density in Ge-MIS Interfaces
N. Taoka[1], K. Ikeda[2], Y. Yamashita[2], N. Sugiyama[2] and S. Takagi[1,3], *[1]MIRAI-ASRC, [2]MIRAI-ASET and [3]Univ. of Tokyo, Japan*

17:05 J-6-2
Fabrication of SiO_2/Ge MIS structures by plasma oxidation of ultrathin Si films grown on Ge
H. Kumagai[1], M. Shichijo[1], H. Ishikawa[1], T. Hoshii[1], S. Sugahara[1], Y. Uchida[2] and S. Takagi[1], *[1]Univ. of Tokyo and [2]Teikyo Univ. of Science and Technology, Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
17:15 A-6-3 Electric properties of single-walled carbon nanotube film field effect transistors with various work function electrodes: a comparison between pristine and potassium-encapsulated nanotubes H. Maki[1], S. Suzuki[2], T. Sato[1] and K. Ishibashi[3], *[1]Keio Univ., [2]NTT Corp. and [3]RIKEN, Japan*	**17:15 B-6-2** Wavelength Tunable (1.55 µm Region) InAs/InGaAsP/InP (100) Quantum Dots in Telecom Laser Applications R. Nötzel, S. Anantathanasarn, P. J. van Veldhoven, F. W. M. van Otten, T. J. Eijkemans, Y. Barbarin, E. A. J. M. Bente, T. du. Vries, E. Smalbrugge, E. J. Geluk, Y. S. Oei, M. K. Smit and J. H. Wolter, *Eindhoven Univ. of Technology, The Netherlands*	**17:15 C-6-2** An Advanced Air Gap Process for MLC flash memories reducing Vth interference and realizing high reliability. K. Tsukamoto, T. Murata, T. Fukumura, F. Ohta, T. Yoshitake, S. Shimizu, Y. Ikeda, K. Asai, M. Shimizu and O. Tsuchiya, *Renesas Technology Corp., Japan*	**17:05 D-6-3** 65nm Node Transistor Characteristic Evaluation Technology for Assembly Stress and Assembly Stress Relaxation Design K. Takemura, M. Takahashi, H. Sano, K. Koike, Y. Itoh and H. Hirano, *Matsushita Electric, Japan*	
17:30 A-6-4 DNA Aptamer-Based Biosensing of Immunoglobulin E Using Carbon Nanotube Field-Effect Transistors T. Katsura[1], K. Maehashi[1], K. Matsumoto[1], K. Kerman[2], Y. Takamura[2] and E. Tamiya[2], *[1]Osaka Univ. and [2]JAIST, Japan*	**17:30 B-6-3** Novel Quantum Dot 3-section Super-luminescent Diode Y.C. Xin[1], A. Martinez[1], T. A. Saiz[1], T. Nilsen[1,2], A. L. Moscho[1], Y. Li[1], A. Gray[4], A. Vahktin[3] and L. F. Lester[1], *[1]Univ.of New Mexico, [2]Univ. of Science and Technology, [3]Southwest Sciences, Inc. and [4]Zia Laser, Inc., USA*	**17:35 C-6-3** Very Low Bit Error Rate in Flash Memory using Tunnel Dielectrics formed by Kr/O_2/NO Plasma Oxynitridation T. Suwa[1], H. Takahashi[1], Y. Kumagai[1], G. Fujita[1], A. Teramoto[1], S. Sugawa[1] and T. Ohmi[1], *Tohoku Univ., Japan*	**17:25 D-6-4** Millions-Pins Direct Bonding of Cu Electrodes and Feasibility of SAB Method with Ultrathin Adhesive Layer for Wafer-Scale Bumpless Interconnect A. Shigetou, T. Itoh and T. Suga, *Univ. of Tokyo, Japan*	**17:25 E-6-3** Dopant-atom distribution measurement at p-n junctions on wet-prepared Si(111): H surfaces by scanning tunneling microscopy M. Nishizawa, L. Bolotov and T. Kanayama, *MIRAI-ASRC-AIST, Japan*
17:45 A-6-5 Surface Potential Measurement of Carbon Nanotube FETs using Kelvin Probe Force Microscopy T. Umesaka[1], H. Ohnaka[1], Y. Ohno[1,2], S. Kishimoto[1], K. Maezawa[1] and T. Mizutani[1], *[1]Nagoya Univ. and [2]PRESTO, Japan*	**17:45 B-6-4** MBE Growth of High Power Quantum Dot Superluminescent LEDs S. K. Ray, T. L. Choi, K. M. Groom, H. Y. Liu, M. Hopkinson and R. A. Hogg, *Univ. of Sheffield, UK*			

18:30-20:30 Rump Session (Room 501, Room 502)

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
			17:15 I-6-2 A 0.6V Supply CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization Y. Masui, T. Yoshida, M. Sasaki and A. Iwata, *Hiroshima Univ., Japan*	
17:25 F-6-3 Impact of Silicon Film Thickness on LF Noise in SOI Devices L. Zafari, J. Jomaah and G. Ghibaudo, *IMEP, France*			**17:35 I-6-3** Low-Voltage, Low-Phase-Noise Ring-VCO using 1/f-Noise Reduction Techniques T. Yoshida, N. Ishida, M. Sasaki and A. Iwata, *Hiroshima Univ., Japan*	**17:25 J-6-3** Strong Fermi-level Pinning of Wide Range of Work-function Metals at Valence Band Edge of Germanium T. Nishimura, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*

18:30-20:30 Rump Session (Room 501, Room 502)

POSTER SESSION (13:00-15:00, Room 501, 502, 511/512)

P1
Advanced Gate Stack / Si Processing Science
(28 Papers)

P-1-1
Suppression of Leakage Current and Moisture Absorption of La_2O_3 films with Ultraviolet Ozone Post Treatment
Y. Zhao, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*

P-1-2
Dielectric Constant Behavior of Oriented Tetragonal Zr-Si-O System
T. Ino, Y. Kamimuta, M. Koyama and A. Nishiyama, *Toshiba Corp. Japan*

P-1-3
Interface Layer Control at Y_2O_3/Ge by N_2 and O_2 Annealing on Ge(100) and Ge(111) Surfaces
H. Nomura, K. Kita, T. Nishimura and A. Toriumi, *Univ. of Tokyo, Japan*

P-1-4
Non-crystalline Stable Gate Dielectrics for Advanced Nano-Cmos Devices
G. Lucovsky[1], S. Lee[1] and J. Lüning[2], *[1]North Carolina State Univ. and [2]Stanford Synchrotron Radiation Lab., USA*

P-1-5
Hf and N Release from HfSiON in High-Temperature Annealing Induced by Oxygen Incorporation
T. Matsuki, S. Inumiya, N. Mise, T. Eimori and Y. Nara, *Semiconductor Leading Edge Techonologies, Inc., Japan*

P-1-6
Epitaxial High-K Oxide Metal Gate MOSFETs: Damascene CMP Process Integration and Electrical Results
R. Endres, Y. Stefanov and U. Schwalke, *Darmstadt Univ. of Technology, Germany*

P-1-7
Impact of PVD-based In-situ Fabrication Method for Metal/High-k Gate Stacks
S. Horie[1], T. Minami[2], N. Kitano[2], M. Kosuda[2], H. Watanabe[1] and K. Yasutake[1], *[1]Osaka Univ. and [2]Canon ANELVA Corp., Japan*

P-1-8
Investigation of Inversion C-V Reconstruction for Long-Channel MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach
W. Lee[1], P. Su[1], K. W. Su[2], C. S. Chiang[2] and S. Liu[2], *[1]National Chiao Tung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P-1-9
Behavior of Local Charge Trapping Sites in La_2O_3-Al_2O_3 Composite Films under Constant Voltage Stress
T. Sago, A. Seko, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*

P-1-10
Improvement of mobility and NBTI reliability in MOSFETs with ALD-Si-nitride/SiO_2 stack dielectrics and P^+-poly Si gate
S. Zhu[1], A. Nakajima[1], T. Ohashi[2] and H. Miyake[2], *[1]Hiroshima Univ. and [2]Elpida Memory Inc., Japan*

P-1-11
Near Surface Oxide Trap Density Profiling in NO and Remote Plasma Nitrided Oxides in Nano-Scale MOSFETs, Using Multi-Temperature Charge Pumping Technique: No+ vs. Oxide Processing
Y. Son[1], C. K. Baek[2], B. Kim[2], I. S. Han[1], T. G. Goo[1], H. D. Lee[1] and D. M. Kim[2], *[1]Chungnam National Univ. and [2]Korea Inst. for Advanced Study, Korea*

P-1-12
Ultra-thin Oxide Lifetime Projection and Comparison of nFET and pFET for 90nm/65nm Application
C. L. Lin, T. Kao, J. P. Chen, J. Shieh and K. C. Su, *United Microelectronics Corp. (UMC), Taiwan*

P-1-13
Theoretical Simulation of Dielectric Breakdown by Molecular Dynamics and Tight-Binding Quantum Chemistry Method
Z. Zhu[1], A. Chutia[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. Del Carpio[1], P. Selvam[3] and A. Miyamoto[1,3], *[1]Tohoku Univ., [2]PRESTO-JST and [3]NICHe, Tohoku Univ., Japan*

P-1-14
Electrical characteristic improvement of high-k gated MOS device by nitridation treatment using plasma immersion ion implantation (PIII)
K. S. Chang-Liao[1], P. H. Tsai[1], H. Y. Kao[1], T. K. Wang[1], S. F. Huang[2], W. F. Tsai[2] and C. F. Ai[2], *[1]National Tsing Hue Univ. and [2]Inst. of Nuclear Energy Research, Taiwan*

P-1-15
Effect of Gate Oxide Thickness Uniformity on the Characteristics of Three-dimensional Transistors
H. J. Cho, T. Y. Kim, Y. S. Kim, S. A. Jang, S. R. Lee, K. Y. Lim, M. G. Sung, J. H. Kim, S. W. Oh, T. W. Jung, T. K. Oh, Y. T. Hwang, Y. H. Kim, H. S. Yang and J. W. Kim, *Hynix Semiconductor Inc., Korea*

P-1-16
Precise Extraction of Metal Gate Work Function from Bevel Structures
A. Kuriyama[1,3,4], O. Faynot[1], L. Brévard[1], A. Tozzo[1], L. Clerc[1], J. Mitard[1,2], V. Vidal[1,2], S. Deleonibus[1], S. Cristoloveanu[3] and H. Iwai[4], *[1]CEA-LETI, [2]STMicroelectronics, [3]IMEP and [4]Tokyo Tech, France*

P-1-17
Work Function Modulation Using Thin Interdiffused Metal Layers for Dual Metal-Gate Technology
A. E. Lim[1], W. S. Hwang [1], X. P. Wang[1], D. L. Kwong[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore and [2]Inst. of Microelectronics, Singapore*

P-1-18
Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes
T. Matsukawa, Y. X. Liu, K. Endo, M. Masahara, K. Ishii, H. Yamauchi, J. Tsukada and E. Suzuki, *National Inst. Adv. Ind. Sci. and Technol., Japan*

P-1-19
Nitrogen Induced Extrinsic States (NIES) in Effective Work Function Instability of TiNx/SiO_2 and TiNx/HfO_2 Gate Stacks
C. S. Lai[1], J. C. Wang[2], S. C. Yang[1], J. Y. Wong[1] and S. K. Peng[1], *[1]Univ. of Chang Gung and [2]Nanya Technology Corp. Taiwan*

P-1-20
Physical and Electrical Characteristics of HfN Metal Gate Electrode Synthesized by Post-Rapid Thermal Annealing-assisted MOCVD
W. Wang[1], T. Nabatame[2] and Y. Shimogaki[1], *[1]Univ. of Tokyo and [2]MIRAI-ASET, Japan*

P-1-21
Composition Dependence of Work Function in Metal (Ni, Pt)-Germanide Gate Electrodes
D. Ikeno, K. Furumai, H. Kondo, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, *Nagoya Univ., Japan*

P-1-22
Stress-Relaxation Process during Post-Annealing in SGOI Formed by H^+ Irradiation and Oxidation-Induced Ge Condensation
M. Tanaka[1], T. Sadoh[1], K. Matsumoto[2], T. Enokida[3] and M. Miyao[1], *[1]Kyushu Univ., [2]SUMCO Corp. and [3]Fukuryo Semicon Engineering Corp., Japan*

P-1-23
Microscopic Mechanism of Oxygen Transport during Thermal Silicon Oxidation
H. Kageshima[1], M. Uematsu[1], T. Akiyama[2] and T. Ito[2], *[1]NTT Basic Research Labs. and [2]Mie Univ., Japan*

P-1-24
Low-Leakage-Current Ultra-thin SiO_2 Film by Low-Temperature Neutral Beam Oxidation
T. Ikoma[1], C. Taguchi[1], S. Fukuda[1], K. Endo[2], H. Watanabe[3] and S. Samukawa[1], *[1]Tohoku Univ., [2]AIST and [3]Osaka Univ., Japan*

P-1-25
Rate-Limiting Reaction of Layer-by-Layer Oxidation on Si(001) Surfaces: Dependence on the First Oxide Layer Growth Kinetics
S. Ogawa and Y. Takakuwa, *Tohoku Univ., Japan*

P-1-26
Xe Preamorphization Implantation for Transient Enhanced Diffusion Suppression of As in Ge Substrate
T. Fukunaga, K. Hosawa, T. Hosoi and K. Shibahara, *Hiroshima Univ. , Japan*

P-1-27
Low Leakage Current and Low Resistivity p^+n Diodes on Si(110) Fabricated by Ga^+/B^+ Combination I/I and Low Temperature Annealing
H. Imai, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P-1-28
Effects of CF_3I Plasma for Reducing UV Irradiation Damage in Dielectric Film Etching Processes
Y. Ichihashi[1,2], Y. Ishikawa[1], R. Shimizu[2], H. Mizuhara[2], M. Okigawa[2] and S. Samukawa[1], *[1]Tohoku Univ. and [2]Sanyo Electric Co., Ltd., Japan*

P2
Characterization and Materials Engineering for Interconnect Integration
(19 Papers)

P-2-1
Formation of Mesoporous Pure Silica Zeolite Film
T. Seo[1], T. Yoshino[2], N. Hata[2] and T. Kikkawa[1,2], *[1]Hiroshima Univ. and [2]National Inst. of Advanced Industrial Science and Technology, Japan*

P-2-2
Pure-Silica Zeolite Films Prepared by a Vapor Phase Transport Method
Y. Cho[1], K. Kohmura[2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Mitsui Chem., Japan*

P-2-3
Thermally Stable Carbon-Doped Silicon Oxide Films Deposited at Room Temperature
K. Yamaoka, H. Kato, D. Tsukiyama, Y. Yoshizako, Y. Terai and Y. Fujiwara, *Osaka Univ., Japan*

P-2-4
Comparison of the Planarization Technologies for the Next Generation
I. Kobata[1], Y. Wada[1], Y. Toma[2], T. Suzuki[2], A. Kodera[2], K. Tokushige[1], A. Fukunaga[1] and M. Tsujimura[1], *[1]Ebara Corporation and [2]Ebara Research Co., Ltd., Japan*

P-2-5
Application of Double Polishing Pad for Shallow Trench Isolation Chemical Mechanical Polishing Process
Y. J. Seo and S. W. Park, *Daebul Univ., South korea*

P-2-6
Analyses of Interface Adhesion between Cu and SiCN Etch Stop Layers by Nanoindentation and Nanoscratch Tests
S. Y. Chang and Y. S. Lee, *National Chung Hsing Univ., Taiwan*

P-2-7
Characterization of pore sealing effect on trench sidewalls in porous low-k films by vapor adsorption in-situ spectroscopic ellipsometry
N. Hata[1], K. Koga[2], K. Sumiya[2], S. Takada[1], M. Tada[2], Y. Kawamoto[2] and T. Kanayama[1], *[1]MIRAI-ASRC-AIST and [2]CASMAT, Japan*

P-2-8
Anisotropic mechanical characterization of Cu single crystals and thin films
S. Shimizu, N. Kojima and J. Ye, *NISSAN ARC, Ltd., Japan*

P-2-9
Ag diffusion in Low-K material (SiOC and BCN) and its challenges using as an interconnection
M. K. Mazumder, R. Moriyama, C. Kimura, H. Aoki and T. Sugino, *Osaka Univ., Japan*

P-2-10
Relationship between structure and conductance of nanometer-sized iridium contacts
M. Ryu[1] and T. Kizuka[1,2], *Univ. of Tsukuba and [2]JST, Japan*

P-2-11
Effectiveness of Titanium and Carbon capping layer in NiSi formation with Ni film deposited by Atomic Layer Deposition
C. M. Yang, S. W. Yun, J. B. Ha, K. I. Na, H. I. Cho, H. B. Lee, J. H. Jeong, S. H. Hahm, S. H. Kong and J. H. Lee, *Kyungpook National Univ. Korea*

P-2-12
A Study of Relationship of Wafer Breakage vs. Wafer Edge Analysis
S. H. Chen[1], S. L. Chen[2] and W. K. Yeh[3], *[1]Tung Fang Institute of Technology, [2]National United Univ. and [3]National Univ. of Kaohsiung, Taiwan*

P-2-13
Characterization of Void in Bonded SOI Wafers by Controlling Coherence Length of Near-Infrared Microscope
N. Ajari, J. Uchikosi, T. Hirokane, K. Arima and M. Morita, *Osaka Univ., Japan*

P-2-14
Evaluation of Alignment Accuracy for Wafer Bonding Using Moiré Technique
C. Wang and T. Suga, *Univ. of Tokyo, Japan*

P-2-15
Sub-Atmospheric Chemical Vapor Deposition Process for Chip-to-Wafer 3-Dimensional Integration
H. Kikuchi, Y. Yamada, A. M. Ali, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. Japan*

P-2-16
A Low Temperature Process of Bonding Fine Pitch Au/Sn Bumps in Air
Y. H. Wang[1], K. Nishida[2], M. Hutter[3], T. Kimura[2] and T. Suga[1], *[1]Univ. of Tokyo, [2]National Inst. for Materials Science and [3]Fraunhofer IZM, Japan*

P-2-17
Finite element analysis of nanometer-scale contact for low temperature bonding
T. Higashino and T. Suga, *Univ. of Tokyo, Japan*

P-2-18
Low Temperature Interconnection of Cu Micro-bump on Polyimide and Ni/Au Film by Surface Activated Flip Chip Method
Z. Xu and T. Suga, *Univ. of Tokyo, Japan*

P-2-19
Impacts of Layout Dimensions and Ambient Temperatures on Silicon Based On-Chip RF Interconnects
M. C. Tang[1], Y. K. Fang[1], W. K. Yeh[2] and R. L. Wang[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]National Kaohsiung Marine Univ., Taiwan*

P3
CMOS Devices / Device Physics
(26 Papers)

P-3-1
An Efficient Mobility Enhancement Engineering on 65nm FUSI CMOSFETs using a Second CESL Process
C. M. Lai[1], Y. K. Fang[1], C. T. Lin[1], W. K. Yeh[2], C. W. Hsu[2], C. H. Hsu[3], L. W. Chen[3] and M. Ma[3], *[1]National Cheng Kung Univ. [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P-3-2
Monte Carlo Simulation of Band-to-band Tunneling in Silicon Devices
Z. L. Xia, G. Du, Y. C. Song, J. Wang, X. Y. Liu, J. F. Kang and R. Q. Han, *Peking Univ., China*

P-3-3
Local Strained Channel nMOSFETs by Different Poly-Si Gate and SiN Capping Layer Thicknesses: Mobility, Simulation, Size Dependence, and Hot Carrier Stress
Y. J. Lee[1], C. H. Fan[2], W. Y. Lin[3], C. C. Wan[2], B. R. Huang[3], W. L. Yang[2], T. S. Chao[4] and D. S. Chuu[2], *[1]National Nano Device Lab., [2]Feng Chia Univ. and [3]Department of Electronic Engineering, National Yunlin Univ. of Science and Technology, Taiwan*

P-3-4
Characterization of Subthreshold Behavior of Narrow-Channel SOI nMOSFET with Additional Side-Gate Electrodes
K. Okuyama, K. Yoshikawa and H. Sunami, *Hiroshima Univ. Japan*

P-3-5
Gate Capacitance Analysis of Multi-finger MOSFETs for RF Applications
H. Aoki and M. Shimasue, *MODECH Inc., Japan*

P-3-6
Characteristics of Poly-Si Nanowire Thin Film Transistors with Double-Gated Structures
C. J. Su[1], H. C. Lin[1,2], C. C. Hung[1], H. H. Tsai[1], Y. J. Lee[2] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P-3-7
A New 1200V PT-IGBT with Protection Circuit employing the Lateral IGBT and Floating p-well Voltage Sensing Scheme
I. H. Ji[1], Y. H. Choi[1], B. C. Jeon[1], S. C. Lee[2], S. S. Kim[2], K. H. Oh[2], C. M. Yun[2] and M. K. Han[1], *[1]Seoul National Univ. and [2]Fairchild Semiconductor Korea, Korea*

P-3-8
Efficient Improvement on Device Performance for sub-90nm SOI CMOSFETs
C. T. Lin[1], Y. K. Fang[1], C. M. Lai[1], W. K. Yeh[2], C. W. Hsu[2], C. H. Hsu[3], L. W. Chen[3] and M. Ma[3], *[1]National Cheng Kung Univ., [2]National Univ. of Kaohsiung and [3]United Microelectronics Corp., Taiwan*

P-3-9
Multiband Simulation of Quantum Electron Transport in Nano-Scale Devices Based on Non-Equilibrium Green's Function
H. Fitriawan, S. Souma, M. Ogawa and T. Miyoshi, *Kobe University, Japan*

P-3-10
Effect of Mobility Degradation and Supply Voltage on NBTI Induced Drain Current Degradation
J. F. Chen[1], D. H. Yang[1], C. Y. Lin[2] and S. Y. Wu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P-3-11
Impact of Source/Drain $Si_{1-y}Cy$ Stressors on the Silicon-on-Insulator NMOSFETs
J. Huang, W. C. Wang, J. W. Fan and S. T. Chang, *National Chung Hsing Univ. Taiwan*

P-3-12
An Analysis of Layout and Temperature Effects on Magnetic-Coupling Factor, Resistive-Coupling Factor, and Power Gain Performances of RF Transformers for RFIC Applications
Y. S. Lin, C. C. Chen, Y. R. Tzeng and H. B. Liang, *National Chi-Nan Univ. Taiwan*

P-3-13
Modeling of Drain Bias Dependence on Threshold Voltage Shift Under Negative Gate Bias Stress of a-Si: H TFTs
H. Y. Tseng, K. Y. Chiang and C. P. Kung, *Industrial Technology Research Institute (ITRI), Taiwan*

P-3-14
A New SOI Lateral Insulated Gate Bipolar Transistor and Lateral Diode employing the Separated Schottky Anode for a Power Integrated Circuit
I. H. Ji, Y. H. Choi, M. W. Ha and M. K. Han, *Seoul National Univ., Korea*

P-3-15
Impacts of LP-SiN Capping Layer and Lateral Diffusion of interface Trap on Hot Carrier Stress of NMOSFETs
C. Y. Lu[1], C. S. Lu[1], Y. L. Hsieh[1], Y. J. Lee[2], H. C. Lin[1,2] and T. Y. Huang[1], *[1]National Chiao Tung Univ. and [2]National Nano Device Labs., Taiwan*

P-3-16
Effects of Strained Layers on Zener Tunneling in Silicon Nanostructures
H. Minari and N. Mori, *Osaka Univ., Japan*

P-3-17
A New Statistical Evaluation Method for the Variation of MOSFETs
S. Watabe, S. Sugawa, A. Teramoto and T. Ohmi, *Tohoku Univ., Japan*

P-3-18
A Novel Self Aligned Design Adapted Gate All Around (SADAGAA) MOSFET including two stacked Channels : A High Co-Integration Potential
R. Wacquez[1,2,3], R. Cerutti[1], P. Coronel[1], A. Cros[1], D. Fleury[1], A. Pouydebasque[4], J. Bustos[1], S. Harrison[4], N. Loubet[1], S. Borel[3], D. Lenoble[1], D. Delille[4], F. Leverd[1], F. Judong[1], MP. Samson[1,3], N. Vuillet[1,3], B. Guillaumot[1,3], T. Ernst[3], P. Masson[2] and T. Skotnicki[1], *[1]ST Microelectronics, [2]IMT Technipôle Château Gombert and [3]LETI, France*

P-3-19
Characterization of RF LDMOS Transistors with Different Layout Structures
H. H. Hu[1], K. M. Chen[2], G. W. Huang[2], C. Y. Chang[1], Y. C. Lu[3], Y. C. Yang[3] and E. Cheng[3], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]United Microelectronics Corp., Taiwan*

P-3-20
Combined Negative Bias Temperature Instability and Hot Carrier Stress Effects in Low Temperature Poly-Si Thin Film Transistors
C. Y. Chen[1], J. W. Lee[2], W. C. Chen[3], H. Y. Lin[3], K. L. Yeh[3], P. H. Lee[1], M. S. Shieh[1], S. D. Wang[1] and T. F. Lei[1], *[1]National Chiao Tung Univ., [2]National Nano Device Labs. and [3]Toppoly Optoelectronics Corp., Taiwan*

P-3-21
N-Type Extended Drain Silicon Controlled Rectifier ESD Protection Device with High Latchup Immunity for High Voltage Operating I/O Application
Y. J. Seo[1] and K. H. Kim[2], *[1]Daebul Univ. and [2]MagnaChip Semiconductor Ltd., Korea*

P-3-22
Strain Efficiency Enhancement with Stress Intermedium Engineering (SIE) for Sub-65nm CMOS Scaling
H. M. Chen, C. C. Huang, J. R. Hwang, C. Y. Chang, Y. M. Sheu, M. Y. Yang, C. K. Wen, S. C. Chen, H. J. Tao and F. L. Yang, *Taiwan Semiconductor Manufacturing Company , Taiwan*

P-3-23
Empirical Model of Phonon-Limited Electron Mobility for Ultra-Thin Body SOI MOS-FET
T. Yamamura, S. Sato and Y. Omura, *Kansai Univ., Japan*

P-3-24
Re-examination of 1/f Noise in FD-SOI for Practical Usage of Analog Circuits
A. Kumar, Y. Domae, N. Miura, T. Okamura, H. Komatsubara, Y. Kita and J. Ida, *Oki Electric Industry Co. Ltd., Japan*

P-3-25
Ultra-Narrow Silicon Nanowire (~ 3 nm) Gate-All-Around MOSFETs
N. Singh, Y. F. Lim, S. C. Rustagi, L. K. Bera, A. Agarwal, G. Q. Lo, N. Balasub and D. L. Kwong, *Inst. of Microelectronics, Singapore*

P-3-26
Hot-Carrier Reliability Improvement in Submicron High-Voltage DMOS Transistors
J. F. Chen[1], J. R. Lee[1], K. M. Wu[1], Y. K. Su[1], H. C. Wang[1], Y. C. Lin[2] and S. L. Hsu[2], *[1]National Cheng Kung Univ. and [2]Taiwan Semiconductor Manufacturing Company, Taiwan*

P4
Advanced Memory Technology
(12 Papers)

P-4-1
Technology of Ferroelectric Thin Film Formation with Large Coercive Field for Future Scaling Down of Ferroelectric Gate FET Memory Device
I. Takahashi, T. Isogai, K. Azumi, M. Hirayama, A. Teramoto, S. Sugawa and T. Ohmi, *Tohoku Univ., Japan*

P-4-2
FinFET NAND Flash with Nitride/Si Nanocrystal/Nitride Hybrid Trap Layer
J. D. Choe[1], S. H. Lee[1], J. J. Lee[1], E. S. Cho[1], Y. Ahn[1], B. Y. Choi[1], S. K. Sung[1], J. No[1], I. Chung[2], K. Park[1] and D. Park[1], *[1]Samsung Electronics Co. and [2]Sungkyunkwan Univ., Korea*

P-4-3
2-Bit Lanthanum Oxide Trapping Layer Nonvolatile Flash Memory
Y. H. Lin, T. Y. Yang, C. H. Chien and T. F. Lei, *National Chiao Tung Univ., Taiwan*

P-4-4
A Novel NAND Flash Technology with Selective Epitaixial Growth Plug Structure for the Improvement in HV Transistor Breakdown Voltage
S. Jeon, C. Kang, U. Roh, C. Lee, Y. Shin, J. Sim, J. Kim, J. Sel, Y. Jeong, W. Jung, J. Choi and K. Kim, *Samsung Electronic Co., Ltd., Korea*

P-4-5
Ultra Low Operation Current Lateral Phase-Change Memory
Y. Yin, D. Niida, N. Higano, A. Miyachi, H. Sone and S. Hosaka, *Gunma Univ., Japan*

P-4-6
Lateral and vertical magnetic interaction in a submicron-sized Fe monolayer and a Fe/Au/Fe trilayer ring structure
M. Kohda[1], K. Takagi[1], T. Miyawaki[1], K. Toyoda[1], A. Fujita[1] and J. Nitta[1,2], *[1]Tohoku Univ. and [2]CREST-JST, Japan*

P-4-7
Low Current Reversible Resistive Switching in Bismuth Titanate Deposited by Electron Cyclotron Resonance Sputtering
Y. Jin, H. Shinojima and M. Shimada, *NTT Microsystem Integration Labs., Japan*

P-4-8
Resistive Switching Properties of $SrZrO_3$-based Memory Films
C. C. Lin[1], B. C. Tu[1], C. C. Lin[1], C. H. Lin[2] and T. Y. Tseng[1], *[1]National Chiao Tung Univ. and [2]Winbond Electronics Corp., Taiwan*

P-4-9
Thermal properties of NiO_y resistor practically free from the 'forming' process
K. Kinoshita, C. Yoshida, H. Aso, M. Aoki and Y. Sugiyama, *Fujitsu Labs. Ltd., Japan*

P-4-10
Resistance Switching Characteristics of Binary Metal Oxides
I. S. Park, K. R. Kim and J. Ahn, *Hanyang Univ., Korea*

P-4-11
Capacitorless DRAM Cell with Highly Scalable Surrounding Gate Structure
H. Jeong, Y. S. Lee, S. Kang, I. H. Park, W. Y. Choi, H. Shin, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*

P-4-12
Cost-Effective and Highly Reliable 6F2 Multi-Gigabit DRAM in 60nm Technology Node for Low Power and High Performance Applications
D. Ha, J. H. Kim, T. H. An, S. S. Lee, S. H. Jang, S. H. Kim, M. S. Kang, H. T. Kim, S. H. Lee, M. Y. Sim, W. T. Park, D. H. Han, S. M. Jeon, J. W. Park, S. H. Kim, S. H. Kwon, Y. G. Kim, Y. J. Choi, M. S. Sim, C. H. Cho, M. M. Jeong, T. W. Lee, G. Jin, W. S. Lee and B. I. Ryu, *Samsung Electronics Co., Ltd., Korea*

P5 Advanced Circuits and Systems
(10 Papers)

P-5-1
Hardware Architecture for Pseudo-2D Hidden-Markov-Model-Based Face Recognition System Employing Laplace Distribution Functions
Y. Suzuki and T. Shibata, *Univ. of Tokyo, Japan*

P-5-2
Binocular Range Image Sensor LSI with Fully Parallel Stereo Correlation Processing
T. Yoshida, K. Ono and Y. Arima, *Kyushu Inst. of Technology, Japan*

P-5-3
A Novel Vision Chip for High-Speed Target Tracking
W. Miao, Q. Lin and N. Wu, *Chinese Academy of Sciences, China*

P-5-4
Image-Scan Video Segmentation Architecture and FPGA Implementation
T. Morimoto, H. Adachi, K. Yamaoka, K. Awane, T. Koide and H. J. Mattausch, *Hiroshima Univ., Japan*

P-5-5
An Edge Cache Memory Arhcitecture for Early Visual Processing VLSIs
Ö. Özturk and T. Shibata, *Univ. of Tokyo, Japan*

P-5-6
A Hardware-Implementation-Friendly PCNN for Analog Image-Feature-Generation Circuits
J. Chen and T. Shibata, *Univ. of Tokyo, Japan*

P-5-7
A Double-Feedback Voltage-Control-Oscillator
H. M. Chen[1], S. H. Lee[2] and S. L. Jang[2], *[1]Lunghwa Univ. of Science and Technology and [2]National Taiwan Univ. of Science and Technology, Taiwan*

P-5-8
Design of Cartesian Feedback Loop Linearization Chip for UHF band Using 0.6μm Bi-CMOS Technology
M. S. Kang, Y. J. Chong, S. J. You and T. J. Chung, *ETRI, Korea*

P-5-9
Optimization on Layout Structures of LTPS TFTs for On-Panel ESD Protection Design
C. K. Deng[1], M. D. Ker[1], J. Y. Chung[1] and W. T. Sun[2], *[1]National Chiao-Tung Univ. and [2]AU Optronics Corp., Taiwan*

P-5-10
Low Power Spin-Transfer MRAM Writing Scheme with Selective Word Line Bootstrap
T. Sugimura, T. Sakaguchi, T. Fukushima, T. Tanaka and M. Koyanagi, *Tohoku Univ. Japan*

P6 Compound Semiconductor Circuits, Electron Devices and Device Physics
(9 Papers)

P-6-1
A 77GHz T/R MMIC One-Chip Set Fabricated by a 0.15μm GaAs mHEMT Technology
D. M. Kang, J. Y. Hong, J. Y. Shim, H. S. Yoon and K. H. Lee, *ETRI, Korea*

P-6-2
Broadband 60 GHz Power Amplifier MMIC with Excellent Gain-Flatness
W. J. Chang[1], H. G. Ji[1], J. W. Lim[1], H. K. Ahn[1], H. Kim[1] and S. H. Oh[2], *[1]ETRI and [2]Chungnam National Univ., Korea*

P-6-3
Influence of T-gate shape on the device characteristics in SiN-assisted 0.12um AlGaAs/InGaAs PHEMT
H. Ahn, J. W. Lim, H. G. Ji, W. J. Chang, J. K. Mun and H. Kim, *ETRI, Korea*

P-6-4
Auger Effect of Hole Accumulation on Characteristics of InAlAs/InGaAs HEMTs
H. Taguchi, H. Murakami, M. Oura, T. Iida and Y. Takanashi, *Tokyo Univ. of Science, Japan*

P-6-5
Pt Buried Gate E-pHEMT with High $V_{G,ON}$ and Reduced Surface Trap Effects
K. Jang[1], G. Seol[1], S. Kim[1], J. Her[1], J. Lee[2] and K. Seo[1], *[1]Seoul National Univ. and [2]Theleds Co., Ltd., Korea*

P-6-6
Direct Calculation of Source Parasitic Resistance in AlGaAs/GaAs HEMTs
H. Saito, S. Ito and M. Kuzuhara, *Univ. of Fukui, Japan*

P-6-7
Highly-Stable Thermal Characteristics of a High Electron-Mobility Transistor with a Novel $In_{0.3}Ga_{0.7}As_{0.99}N_{0.01}$(Sb) Dilute Channel
K. H. Su[1], W. C. Hsu[1], C. S. Lee[2], Y. S. Lin[3], P. J. Hu[1], R. S. Hsiao[4,5], T. W. Chi[4] and J. Y. Chi[4], *[1]National Cheng-Kung Univ. [2]Feng Chia Univ. [3]National Dong Hwa Univ. [4]National Chiao-Tung Univ. and [5]Industrial Technology Research Inst., Taiwan*

P-6-8
The GaN based HEMT and Schottky diode with filed plate technology for DC/DC converter
W. K. Wang, Y. J. Chang, C. K. Lin, C. H. Lin and Y. J. Chan, *National Central Univ. Taiwan*

P-6-9
A Size-Dependent Equivalent-Circuit Model of High Performance Near-Ballistic-Transport Photodiode
Y. S. Wu, D. M. Lin, F. H. Huang, W. Y. Chiu, J. W. Shi and Y. J. Chan, *Natonal Central Univ., Taiwan*

P7 Photonic Devices and Device Physics
(20 Papers)

P-7-1
Lock-in pixel using a Current-assisted photonic demodulator Implemented in 0.6μm Standard CMOS
W. Van der Tempel, D. Van Nieuwenhove, R. Grootjans and M. Kuijk, *Vrije Univ. Brussel, Belgium*

P-7-2
AlGaN UV-B Photodetectors on AlN/sapphire template
H. Jiang and T. Egawa, *Nagoya Inst. of Technology, Japan*

P-7-3
Development of Flexible Electrochromic Device with Thin Film Configuration
H. Yoshimura, T. Sakaguchi and N. Koshida, *Tokyo Univ. of Agriculture and Technology, Japan*

P-7-4
Effect of Temperature on the Bandwidth and Responsivity of Uni-Traveling-Carrier and Modified Uni-Traveling-Carrier Photodiodes
D. H. Jun, J. H. Jang and J. I. Song, *GIST, Korea*

P-7-5
The Fabrication of the Double Ring Resonators Semiconductor Laser
M. C. Shih[1], S. C. Wang[1], C. W. Liang[1] and M. H. Weng[2], *[1]National Univ. of Kaohsiung and [2]National Nano Device Labs., Taiwan*

P-7-6
AlGaN Ultraviolet Metal-Semiconductor-Metal Photodetectors with Low-Temperature-Grown Cap Layers
S. J. Chang[1], M. H. Wu[1], H. Hung[1], Y. C. Lin[1], H. Kuan[2], R. M. Lin[3] and C. H. Chen[4], *[1]National Cheng Kung Univ., [2]Far East College, [3]Chang Gung Univ. and [4]Cheng Shiu Univ., Taiwan*

P-7-7
Inverted GaN p-i-n photodiodes with a buried p^+/n^{++} tunneling junction
M. L. Lee[2], J. K. Sheu[2], W. C. Lai[2], S. C. Shei[3] and S. J. Chang[2], *[1]Southern Taiwan Univ. of Technology, [2]National Cheng Kung Univ. and [3]National Univ. of Tainan, Taiwan*

P-7-8
Optical constants of beta-$FeSi_2$ film on Si substrate obtained from transmittance and reflectance data and origin of Urbach-tail
H. Kakemoto[1], T. Higuchi[2], H. Shibata[3], S. Wada[1] and T. Tsurumi[1], *[1]Tokyo Tech, [2]Tokyo Univ. of Science and [3]National Inst. of Advanced Industrial Science and Technology, Japan*

P-7-9
Improved Device Characteristocs of InGaAsN Photodetectors Using MIMS Structure
Y. K. Su, W. C. Chen, R. W. Chuang, S. H. Hsu and B. Y. Chen, *National Cheng Kung Univ., Taiwan*

P-7-10
Effects of Transparent Conductive Layers on Characteristics of InGaN-Based Green Resonant-Cavity Light-Emitting Diodes
S. Y. Huang[1], R. H. Horng[1], W. K. Wang[1], T. E. Yu[1], P. R. Lin[1] and D. S. Wuu[1,2], *[1]National Chung Hsing Univ. and [2]National Formosa Univ., Taiwan*

P-7-11
High Reliable Nitride Based LEDs with Internal ESD Protection
C. F. Shen[1], S. J. Chang[1], S. C. Shei[2], C. S. Chang[3], W. S. Chen[1], T. K. Ko[1] and Y. Z. Chiou[4], *[1]National Cheng Kung Univ., [2]National Univ. of Tainan, [3]Epitech Technology Corp. and [4]Southern Taiwan Univ. of Technology, Taiwan*

P-7-12
Design and Characterization of 1 by 128 Linear Arrays of Sensitivity Improved InGaAs/InP NIR Photodetector
Y. C. Jo[1], H. J. Song[1], H. Kim[1] and P. Choi[2], *[1]KETI and [2]Kyungpook National Univ., Korea*

P-7-13
Junction Temperature and Thermal Resistance Measurement in High-Power Light Emitting Diodes Using A Real-Time Diode Forward Voltage Sampling Technique
S. J. Wang[1], T. M. Chen[1,2], K. M. Uang[2], S. L. Chen[1], D. M. Kuo[1], H. Y. Kuo[1], B. W. Liou[2] and S. H. Yang[3], *[1]National Cheng Kung Univ., [2]Wu-Feng Inst. of Technology, and [3]National Kaohsiung Univ., Taiwan*

P-7-14
Enhancement of Carrier Confinement by the Multiquantum Barriers in Blue InGaN/GaN Multiple Quantum Well Light-emitting Diodes
J. C. Wang, H. T. Shen and T. E. Nee, *Chang Gung Univ., Taiwan*

P-7-15
Effect of Residual Stress in Thin Films on the Radiation Spectrum of a Semiconductor Laser
H. Miura, T. Kawauchi, K. Suzuki and M. Sasaki, *Tohoku Univ., Japan*

P-7-16
Photodiode Model for CMOS Image Sensor SPICE Simulation
W. J. Chiang, H. C. Chen and Y. C. King, *National Tsing Hua Univ., Taiwan*

P-7-17
Characterization of the ZnO metal-semiconductor-metal ultraviolet photodetectors with Au contact electrodes
S. J. Young[1], L. W. Ji[2], S. J. Chang[1], Y. K. Su[1] and X. L. Du[3], *[1]National Cheng Kung Univ., [2]National Formosa Univ. and [3]Chinese Academy of Sciences, Taiwan*

P-7-18
High electrical stress influence on reliability characteristics of polarization-induced GaN-InGaN MQW LEDs
J. S. Jang[1] and H. H. Lee[2], *[1]Korea Univ. and [2]PAL, Korea*

P-7-19
Ultraviolet Random Laser Action of Nano-structured Zinc Oxide
F. I. Lai[1], W. C. Chen[2], S. Y. Kuo[2] and C. P. Cheng[3], *[1]Ching Yun Univ., [2]National Applied Research Labs. and [3]National Taiwan Normal Univ., Taiwan*

P-7-20
Mechanism investigation of chlorine-treated InGaN/GaN light-emitting diodes
P. S. Chen and C. T. Lee, *National Cheng Kung Univ., Taiwan*

P8 Advanced Material Synthesis and Crystal Growth Technology (21 Papers)

P-8-1
Optical Properties of InGaN/GaN Light Emitting Diodes Grown by Pulsed-Trimethylindium-Flow Process
T. H. Hsueh[1], J. K. Sheu[1], W. C. Lai[1], Y. T. Wang[2], H. C. Kuo[2] and S. C. Wang[2], *[1]National Cheng Kung Univ. and [2]National Chiao Tung Univ., Taiwan*

P-8-2
Polarization field effect on the electrical and electronic band characteristics at the interface between metal and strained GaN/InGaN layer
J. S. Jang[1], S. R. Jeon[2], M. C. Jung[3], H. J. Shin[3] and H. H. Lee[3], *[1]Korea Univ., [2]KOPTI and [3]PAL, Korea*

P-8-3
Characteristic comparison of GaN grown on patterned sapphire substrates following growth time
D. H. Kang, J. C. Song, B. Y. Shim, E. A. Ko, D. W. Kim and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-4
Efficient stress relief in GaN heteroepitaxy on Si(111) using various metal buffer
E. A. Ko, D. W. Kim, B. Y. Shim, I. W. Lee and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-5
Electroabsorptive Properties of InGaAs/InAlAs Five-Layer Asymmetric Coupled Quantum Well (FACQW)
T. Arakawa[1], K. Takimoto[1], S. Miyazaki[1], K. Yamaguchi[1], N. Haneji[1], J. H. Noh[2] and K. Tada[3], *[1]Yokohama National Univ., [2]Yokogawa Electric Corp. and [3]Kanazawa Inst. of Technology, Japan*

P-8-6
Photoluminescence characterization of type II $Zn_{0.97}Mn_{0.03}Se/ZnSe_{0.92}Te_{0.08}$ multiple-quantum-well structures
J. J. Shiu[1], W. L. Chen[1], D. Y. Lin[1], C. S. Yang[2] and W. C. Chou[2], *[1]National Changhua Univ. of Education and [2]National Chiao Tung Univ., Taiwan*

P-8-7
Growth of III-V epitaxial material on Si Substrates for high-speed electronic applications
G. L. Luo[1], Y. C. Hsieh[2], T. H. Yang [2] and E. Y. Chang[2], *[1] National Nano Devices Labs. and [2]National Chiao Tung Univ., Taiwan*

P-8-8
Self-assembled GaN nano-column grown on Si (111) substrate using Au+Ga alloy seeding method by MOCVD
B. Y. Shim, E. A. Ko, J. C. Song, D. H. Kang, D. W. Kim, I. H. Lee and C. R. Lee, *Chonbuk National Univ., Korea*

P-8-9
The Influence of Carbon Content on Material and Field Emission Properties of Nanowires Self-synthesized from Sputter-deposited WCx Films
R. M. Ko, S. J. Wang, C. H. Chen, W. C. Tsai, Y. C. Kuo, C. L. Chang and Z. F. Wen, *National Cheng Kung Univ., Taiwan*

P-8-10
A Novel Method for the Preparation of Si Nanowires
R. Lin[1], H. C. Lin[1,2], J. Y. Yang[1], S. W. Shen[1] and C. J. Su[2], *[1]National Nano Device Labs. and [2]National Chiao Tung Univ., Taiwan*

P-8-11
In situ High-Resolution Transmission Electron Microscopy of Deformation of Multi-walled Carbon Nanometer-sized capsules
R. Kato[1], K. Asaka[1], K. Miyazawa[2] and T. Kizuka[1,3], *[1]Univ. of Tsukuba , [2]National Inst for Materials Science and [3]JST, Japan*

P-8-12
Enlargement of Crystal-Grains in Thin Silicon Films Using Continuous-Wave Laser Irradiation
S. Fujii, S. Kuroki, K. Kotani and T. Ito, *Tohoku Univ., Japan*

P-8-13
Kinetic Monte Carlo (KMC) Modeling for Boron Diffusion in Strained Silicon
Y. K. Kim, K. S. Yoon and T. Won, *Inha Univ., Korea*

P-8-14
Ab-initio Study on Energy Barrier for Neutral Indium Migration in a Silicon Substrate
K. S. Yoon, C. O. Hwang and T. Won, *Inha univ., Korea*

P-8-15
Moisture-Barrier Properties of Carbon-coated Silicon Oxide Films
W. R. Chen[1], H. M. Guo[2], T. H. Meen[1], K. H. Wu[2], F. S. Juang[1] and C. J. Huang[3], *[1]National Formosa Univ., [2]Southern Taiwan Univ. of Technology and [3]National Univ. of Kaohsiung, Taiwan*

P-8-16
TiO_2 nanocrystal prepared by ALD system at elevated temperature
C. H. Lin, C. C. Wang, P. J. Tzeng, S. Maikap, H. Y. Lee, L. S. Lee and M. J. Tsai, *Industrial Technology Research Inst., Taiwan*

P-8-17
Synthesis of Au/TiO_2 Core-Shell Nanoparticles from TTIP and Thermal Resistance Effect of TiO_2 Shell
H. Kwon, Y. Lim and Y. Yu, *Chonbuk National Univ., Korea*

P-8-18
Electrical Characteristics and Preparation of $(Ba_{0.5}Sr_{0.5})TiO_3$ Ferroelectric Films by Spray Pyrolysis and Rapid Thermal Annealing
H. S. Koo[1], M. Chen[2], H. K. Ku[3] and T. Kawai[1], *[1]Osaka Univ., [2]Ming Hsin Univ. of Science and Technology and [3]Fortune Inst. of Technology, Japan*

P-8-19
Photoluminescence Characteristics of YAG:Ce Phosphor by Sol-Gel Method
H. W. Choi, S. K. Lee, J. H. Cha[1] and K. H. Kim, *Univ. of Kyungwon, Korea*

P-8-20
Development of Accelerated Large-Scale Electronic Structure Calculation Program for Designing of Rare Earth Phosphors
A. Endou[1], H. Onuma[1], C. Lv[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], H. Takaba[1], M. Kubo[2], C. A. del Carpio[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P-8-21
Study of the Improved Conductivity of Indium-tin Oxide Films Cosputtered with Zinc Oxide at Room Temperature from Thermal Degradations
D. S. Liu[1], C. H. Lin[1], C. S. Sheu[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*

P9 Physics and Applications of Novel Functional Materials and Devices (13 Papers)

P-9-1
Effects of Thermal Effusivity in Nanocrystalline Porous Silicon on Long-Term Operation of Thermally Induced Ultrasonic Emission
Y. Watabe[1], Y. Honda[1] and N. Koshida[2], *[1]Matsushita Electric and [2]Tokyo Univ. of Agriculture and Technology, Japan*

P-9-2
Mechanical Properties of Nanometer-sized Fullerene C_{60} Whiskers Studied by In situ High-Resolution Transmission Electron Microscopy
R. Kato[1], K. Asaka[1], K. Miyazawa[2] and T. Kizuka[1,3], *[1]Univ. of Tsukuba, [2]National Inst. for Materials Science and [3]JST, Japan*

P-9-3
Theoretical Study on the Electronic and Structural Properties of p-Type Transparent Conducting Metal Oxides
C. Lv[1], X. Wang[1], A. Govindasamy[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. del Carpio[1], P. Selvam[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P-9-4
Field Emission Improvement from Pillar Array of Aligned Carbon Nanotubes
C. P. Juan[1,2], K. C. Lin[2], R. L. Lai[2], J. Y. Yang[3] and H. C. Cheng[2], *[1]St. John's Univ., [2]National Chiao Tung Univ. and [3]National Nano Device Lab., Taiwan*

P-9-5
Macroscopic Model of Current-induced Magnetic Switching Effect in Pseudo-spin-valve Structure
M. Ren, L. Zhang, J. Hu, N. Deng and P. Chen, *Tsinghua Univ., China*

P-9-6
Electrical Characterization of Carbon Nanowalls
M. Ura[1], W. Takeuchi[2], Y. Tokuda[2], M. Hiramatsu[3], H. Kano[4] and M. Hori[1], *[1]Nagoya Univ., [2]Aichi Inst. of Technology, [3]Meijo Univ. and [4]NU Eco-Engineering Corp., Japan*

P-9-7
Optical Properties of Size-Controlled Porous Nanostructures Formed on n-InP (001) Substrates by Electrochemical Process
T. Fujino, T. Sato and T. Hashizume, *Hokkaido Univ., Japan*

P-9-8
Development of a Thermal Conductivity Prediction Simulator of Lattice Vibration for Semiconductor, Insulator and Conduction Electron for Metal
H. Tsuboi[1], C. Arunabhirun[1], Z. Zhu[1], C. Lv[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. del Carpio[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*

P-9-9
Local Characterization of Photovoltage on Polycrystalline Silicon Solar Cells by KFM with Piezo-resistive Cantilever
M. Takihara[1], T. Igarashi[1], T. Ujihara[2] and T. Takahashi[1], *[1]Univ. of Tokyo and [2]Nagoya Univ., Japan*

P-9-10
A Spin Drag Effect in Temperature Dependence of Spin-Polarized Electron Mobilities
Y. Takahashi[1], Y. Sato[2], F. Hirose[1] and H. Kawaguchi[2,3], *[1]Yamagata Univ., [2]CREST and [3]Nara Inst. of Science and Technology, Japan*

P-9-11
Hybrid simulation of the RF-SET and its charge sensitivity analysis
M. Manoharan[1], H. Mizuta[1,2] and S. Oda[1,2], *[1]Tokyo Tech and [2]SORST-JST, Japan*

P-9-12
Electrical Characteristics and Preparation of Nanostructured $Pb(Zr_{0.5}Ti_{0.5})O_3$ Ferroelectric Films by Spray Pyrolysis
M. Chen[1], H. S. Koo[2], Y. Hotta[2] and T. Kawai[2], *[1]Ming-Hsin Univ. of Science and Technology and [2]Osaka Univ., Taiwan*

P-9-13
A transmission-type radio-frequency single-electron transistor (RF-SET) with an in-plane-gate SET (IPG-SET)
Y. S. Yu[1], E. S. Kim[1], C. H. Lee[1], S. H. Kim[1], S. H. Son[2,3], S. W. Hwang[2,3] and D. Ahn[3], *[1]Hankyong National Univ., [2]Korea Univ. and [3]Univ. of Seoul, Korea*

P10
Organic Materials Science, Device Physics, and Applications
(20 Papers)

P-10-1
High Efficiency White Organic Light-Emitting Diodes with Double-Doped in a Single Emissive Layer
S. H. Su [1], C. C. Hou[1], W. C. Cheng[1], J. F. Li[2], R. S. Shieh[1] and M. Yokoyama[1], *[1]I-Shou Univ. and [2]National Chung Cheng Univ., Taiwan*

P-10-2
Fabrication of color-stable organic light-emitting devices by utilizing incomplete energy transform
C. S. Huang, Y. K. Su and B. T. Wu, *National Cheng Kung Univ., Taiwan*

P-10-3
Effect of $SnDP(HPB)_2$ as Hole Blocking Layer in OLED
D. E. Kim[1], B. S. Kim[1], W. S. Kim[2], O. K. Kwon[1], B. J. Lee[2] and Y. S. Kwon[1], *[1]Dong-A Univ. and [2]Inje Univ., Korea*

P-10-4
Theoretical Study on the Photophyscial Properties of an Efficient Sensitizer for Nanocrystalline TiO_2-Based Solar Cells
A. Govindasamy[1], C. Lv[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], C. A. Del Carpio [1], M. Kubo[1,2] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]JST-PRESTO, Japan*

P-10-5
Dye Sensitization Effect on Photocurrent Generation of Porphyrin-Polythiophene Composite Films
K. Sugawa[1], K. Kakutani[1], T. Akiyama[1], S. Yamada[1], K. Takechi[2], T. Shiga[2], M. Motohiro[2], H. Nakayama[3] and K. Kohama[3], *[1]Kyushu Univ., [2]Toyota Central R&D Labs., Inc. and [3]Toyota Motor Corp., Japan*

P-10-6
Thermo Effects on the Novel Soft Electronic Substrates
H. H. Yu[1], M. C. Tseng[1], K. C. Hwang[1] and S. J. Hwang[2], *[1]National Formosa Univ. and [2]National United Univ., Taiwan*

P-10-7
A Low Voltage Memory (~2V) Based on Polystyrene for Printable Electronics
C. C. Chang, H. T. Lin, Z. Pei, W. M. Lou, C. A. Jong and Y. J. Chan, *ITRI, Taiwan*

P-10-8
The Measurement of Electrical Conduction of Self-Assembled Viologen Derivatives Using Scanning Tunneling Microscopy
N. S. Lee[1], H. K. Shin[2], D. J. Qian[3] and Y. S. Kwon[1], *[1]Dong-A Univ., [2]Pohang Univ. of Science and Technology and [3]Fudan Univ., Korea*

P-10-9
Effect of Oxygen Contents on the Property of Hydrophobic Thin Films Deposited on Flexible Substrates Using Plasma-enhanced CVD
D. S. Liu[1], C. Y. Wu[1], B. W. Huang[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*

P-10-10
Synchrotron Radiation Studies of the Orientation of Thin Silicon Phthalocyanine Dichloride Film on HOPG Substrate
D. Juzhi[1,2], T. Sekiguchi[1], Y. Baba[1] and N. Hirao[1], *[1]Japan Atomic Energy Agency and [2]China Univ. of Tech., Japan*

P-10-11
Reduction of Electrical Damage due to Au/Pentacene Contact Formation by Introducing Ar Gas during Au Evaporation
T. Sawabe[1], K. Okamura[1], T. Miyamoto[2], M. Nakamura[1] and K. Kudo[1], *[1]Chiba Univ. and [2]Toray Research Center, Inc, Japan*

P-10-12
Elemental analysis of novel organic semiconductor materials for molecular electronics
S. Shcherbyna[1], V. Baranov[2] and D. K. Bohme[1], *[1]York Univ. and [2]IBBME, Univ. of Toronto, Canada*

P-10-13
Fabrication of Nano-gate Structure Organic Static Induction Transistor using Electron Beam Lithography
M. Fukuda, H. Yamaguchi, M. Iizuka and K. Kudo, *Chiba Univ., Japan*

P-10-14
A Simple Method for Extraction of Contact Resistance in Organic Thin Film Transistor
B. C. Jung and C. K. Song, *Dong-A Univ., Korea*

P-10-15
Analysis of pentacene FET characteristics using a Maxwell-Wagner model
R. Tamura, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech, Japan*

P-10-16
Fabrication and Ethanol Vapor Treatment of Magnesium Phthalocyanine Field Effect Transistor
K. Shinbo, T. Akazawa, H. Ikarashi, Y. Ohdaira, K. Kato and F. Kaneko, *Niigata Univ., Japan*

P-10-17
Full-swing Pentacene Organic Inverter with Long-channel Driver and Short-channel Load
C. A. Lee, D. W. Park, K. D. Jung, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*

P-10-18
Physical Properties and Fabricating Technology of Novel Type Resist for Color Filter in TFT LCD
P. C. Pan, H. C. Wu, H. S. Koo and T. Kawai, *Osaka Univ., Japan*

P-10-19
Fabrication of vertical organic light emitting transistor using thin-film ZnO
H. Yamauchi, M. Iizuka and K. Kudo, *Chiba Univ., Japan*

P-10-20
Significantly Enhancing Luminance of Organic Light-Emitting Diodes (OLEDs) with Doping Iodine and Nitrogen Treatment
S. F. Chen, Y. K. Fang, S. C. Hou, F. S. Lin, C. Y. Lin, S. H. Chang and T. H. Chou, *National Cheng Kung Univ., Taiwan*

P11
Micro/Nano Electromechanical and Bio-Systems (Devices)
(9 Papers)

P-11-1
High Performance RF Passive Devices on Plastic Substrates for RFIC Application
B. F. Hung, C. C. Chen, H. L. Kao and A. Chin, *National Chiao Tung Univ., Taiwan*

P-11-2
Development of a Functional Chromosome Nano-Dissection System Using Porous Anodic Alumina Pattern Chip and AFM Cantilever
D. K. Kim[1], M. Saito[1], Y. S. Kwon[2] and E. Tamiya[1], *[1]JAIST and [2]Dong-A Univ., Japan*

P-11-3
Effect of Chemical Modification of the Substrate Surface on Lipid Bilayer Formation
T. Isono, H. Tanaka and T. Ogino, *Yokohama National Univ., Japan*

P-11-4
Biosensing with CNx multi-wall carbon nanotubes
H. J. Burch, S. A. Contera, C. N. Toldeo, M. R. Planque, N. Grobert, K. Voitchovsky and J. F. Ryan, *Univ. of Oxford, UK*

P-11-5
Novel process techniques for ISFET/REFET micro chip based on common Si_3N_4 sensing membrane
C. S. Lai, C. E. Lue, C. M. Yang and J. H. Jao, *Chang Gung Univ., Taiwan*

P-11-6
Modulation of the Density of Assembled Gold Nanoparticles and Local Plasmon Coupling Effect on SPR Spectrum Response
X. Li, K. Tamada and M. Hara, *Tokyo Tech, Japan*

P-11-7
Electric Properties in Biofilms Studied by Resonant Auger Electron Spectroscopy
Y. Baba[1], T. Sekiguchi[1], I. Shimoyama[1], K. G. Nath[2] and N. Hirao[1], *[1]Japan Atomic Energy Agency and [2]Univ. of Quebec, Japan*

P-11-8
Micro molding of three-dimensional metal structure by non-electro plating of photopolymerized resin
T. Yoshimura, S. Maruo and K. Mukai, *Yokohama National Univ., Japan*

P-11-9
High-Quality-Factor and Low-Power-Loss Micromachined RF Bifilar Transformer for UWB RFIC Applications
Y. S. Lin[1], C. C. Chen[1], H. B. Liang[1], T. Wang[2] and S. S. Lu[2], *National Chi Nan Univ. and [2]National Taiwan Univ., Taiwan*

Friday, September 15

Room 411/412 (A)

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-7: Novel Devices and Materials I
(9:00-10:30)
Chairs: H. Mizuta (Tokyo Tech)
Y. Suda (Tokyo Univ. of Agriculture & Technology)

9:00 A-7-1 (Invited)
Semiconductor Nanowire Devices for Future Logic and Memory
B. Yu and M. Meyyappan, *NASA Ames Research Center, USA*

9:30 A-7-2
Charge Polarity Dependence of Negative Differential Conductance in Room-Temperature Operating Silicon Single-Charge Transistor
M. Kobayashi, K. Miyaji and T. Hiramoto, *Univ. of Tokyo, Japan*

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-7: Micro-Optics and Optical Waveguides
(9:00-10:30)
Chairs: L. Young (Hitachi)
S. Nishikawa (Mitsubishi Electric)

9:00 B-7-1 (Invited)
Optoelectronic Tweezers: Optical Manipulation Using LEDs and Spatial Light Modulators
M. C. Wu, *Univ. of California Berkeley, USA*

9:30 B-7-2
Novel Opto-Electro Printed Circuit Board with Polynorbornene Optical Waveguide
M. Fujiwara[1,2], Y. Shirato[1], H. Owari[1], K. Watanabe[1], M. Matsuyama[1], K. Takahama[1], T. Mori[1], K. Miyao[1], K. Choki[1], T. Fukushima[2], T. Tanaka[2] and M. Koyanagi[2], *[1]Sumitomo Bakelite Co., Ltd. and [2]Tohoku Univ., Japan*

Room 414/415 (C)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

C-7: Micro and Nano Fluidics for Biosensing
(9:00-10:30)
Chairs: Y. Takamura (JAIST)
H. Oana (Univ. of Tokyo)

9:00 C-7-1 (Invited)
Digital Microfluidics for Chemical and Biological Applications
R. L. Garrell, *Univ. of California Los Angeles, USA*

9:30 C-7-2
DNA Size Separation Employing Quartz Nano-Pillars with Different Allocations
R. Ogawa[1], N. Kaji[2], S. Hashioka[1], Y. Baba[2,3] and Y. Horiike[1], *[1]NIMS, [2]Nagoya Univ. and [3]AIST, Japan*

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-7: Molecular Electronics
(9:15-10:30)
Chairs: T. Someya (Univ. of Tokyo)
K. Kato (Niigata Univ.)

Room 418 (E)

Room 419 (F)

Area 4: Advanced Memory Technology

F-7: Flash Memory II
(9:00-10:20)
Chairs: C. Hsu (eMemory Tech.)
Y. Yamauchi (Sharp)

9:00 F-7-1
The incorporation effect of thin Al_2O_3 layers on ZrO_2-Al_2O_3 nanolaminates in the composite oxide-high-K-oxide stack for the floating gate flash memory devices
M. S. Joo, S. R. Lee, H. Yang, K. Hong, S. A. Jang, J. Koo, J. Kim, S. Shin, M. Kim, S. Pyi, N. Kwak and J. W. Kim, *Hynix Semiconductor Inc., Korea*

9:20 F-7-2
High-k HfO_2/Al_2O_3 nanolaminated charge trapping layers for high performance flash memory device applications
S. Maikap[1], P. J. Tzeng[1], T. Y. Wang[2], C. H. Lin[1], H. Y. Lee[1], C. C. Wang[1], L. S. Lee[1], J. R. Yang[2] and M. J. Tsai[1], *[1]Industrial Technology Research Inst. and [2]National Taiwan Univ., Taiwan*

Room 501 (G)

Area 2: Characterization and Materials Engineering for Interconnect Integration

G-7: Characterization II
(9:00-10:40)
Chairs: M. Kodera (Toshiba)
M. Matsuura (Renesas)

9:00 G-7-1
Late News

9:20 G-7-2
CuAl Alloy Interconnects as a Solution to the Trade-off between Reliability and Defect Density
T. Furusawa[1], D. Kodama[1], H. Miyazaki[1], M. Matsumoto[1], J. Izumitani[1], H. Matsumoto[2], S. Fukui[1], K. Hashimoto[1], S. Tawa[1], Y. Nagaki[2], M. Okada[1], K. Tomita[1], A. Ishii[1], N. Amou[2], K. Mori[1], K. Maekawa[1], Y. Minoura[3], N. Suzumura[1], K. Honda[1], Y. Hirose[1] and A. Osaki[1], *[1]Renesas Technology Corp., [2]Renesas Semiconductor Engineering Corp. and [3]Ltec Corp., Japan*

Room 502 (H)

Area 3: CMOS Devices/Device Physics

H-7: Compact Modeling
(9:00-10:40)
Chairs: A. Asenov (Univ. of Glasgow)
K. Kurimoto (Matsushita Electric)

9:00 H-7-1
Suppressed short-channel effect of DG-MOSFET and its modeling
H. Oka[1], R. Tanabe[1], N. Sadachika[2], A. Yumisaki[2] and M. Miura-Mattausch[2], *[1]Fujitsu Labs., Ltd. and [2]Hiroshima Univ., Japan*

9:20 H-7-2
A Continuous, Explicit Drain-Current Model for Asymmetric Undoped Double-Gate MOSFETs
Z. M. Zhu[1], X. Zhou[1], K. Chandrasekaran[1], G. H. See[1] and S. C. Rustagi[2], *[1]Nanyang Technological Univ. and [2]Inst. of Microelectronics, Singapore*

Room 511/512 (I)

Area 8: Advanced Material Synthesis and Crystal Growth Technology

I-7: Novel Materials
(9:00-10:15)
Chairs: S. Shimomura (Osaka Univ.)
D. Iwai (Fujitsu Labs.)

9:00 I-7-1
Epitaxial growth of $La_{0.7}Ba_{0.3}MnO_3$ thin films on $SrTiO_3$ and $LaAlO_3$ substrates by metal-organic deposition process
K. Daoudi, T. Tsuchiya, T. Nakajima, I. Yamaguchi, T. Manabe and T. Kumagai, *AIST, Japan*

9:15 I-7-2
Molecular Dynamics and Quantum Chemical Molecular Dynamics Approach to Design of MgO Protecting Layer in Plasma Display
M. Kubo[1,2], H. Kikuchi[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], C. A. del Carpio[1], H. Kajiyama[3] and A. Miyamoto[1], *[1]Tohoku Univ., [2]JST-PRESTO and [3]Univ. of Tokyo, Japan*

Small Auditorium (J)

Area 1: Advanced Gate Stack/Si Processing Science

J-7: High-k Dielectrics II
(9:00-10:40)
Chairs: Y. Nara (Selete)
A. Toriumi (Univ. of Tokyo)

9:00 J-7-1
Optimization of Hafnium Zirconate (HfZrOx) Gate Dielectric for Device Performance and Reliability
R. I. Hegde, D. H. Triyoso, S. Kalpat, S. B. Samavedam, J. K. Schaeffer, E. Luckowski, C. Capasso, D. C. Gilmer, M. Raymond, D. Roan, J. Nguyen, L. La, E. Hebert, X. D. Wang, R. Gregory, R. S. Rai, J. Jiang, T. Y. Luo and B. E. White Jr
Jr.White, *ASTS, USA*

9:20 J-7-2
Current Transportation Mechanism and Interface States Characterization of Sputtered Gd_2O_3 Gate Dielectrics for ULSI Application
W. C. Wu[1], C. S. Lai[2], K. T. Wang[1], J. C. Wang[3] and T. S. Chao[1], *[1]National Chiao Tung Univ., [2]Chang Gung Univ. and [3]Nanya Technology Corp., Taiwan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
9:45 A-7-3 High-PVCR Si/Si_{1-x} Gex Planer-Type Resonant Tunneling Diode Formed with Phosphorous doped Quadruple-layer Buffer H. Maekawa, Y. Sano and Y. Suda, *Tokyo Univ. of Agriculture and Technology, Japan*	**9:45 B-7-3** Micro-Racetrack Notch Filters Based on InGaAsP/InP High Mesa Optical Waveguides W. S. Choi[1], D. H. Kim[1], S. Khisa[1], W. Zhao[2], J. W. Bae[2], I. Adesida[2] and J. H. Jang[1], *[1]Gwangju Inst. of Science and Technology and [2]Univ. of Illinois at Urbana Campaign, Korea*	**9:45 C-7-3** Integrated DNA Purification and Detection Device for Diagnosis of Infection Diseases S. Hashioka[1], R. Ogawa[1], H. Ogawa[2] and Y. Horiike[1], *[1]NIMS and [2]Adbic Incorp., Japan*	**9:45 D-7-2** Fowler-Nordheim Tunneling in Electromigrated Break Junctions with Porphyrin Derivatives Y. Noguchi, T. Nagase, R. Ueda, T. Kamikado, T. Kubota and S. Mashiko, *National Inst. of Information and Communications Technology, Japan*	
10:00 A-7-4 High-Density Floating Nanodots Memory Produced by Cage-Shaped Protein K. Yamada[1], S. Yoshii[1], S. Kumagai[1], A. Miura[2], Y. Uraoka[2], T. Fuyuki[2] and I. Yamashita[1,2,3], *[1]Matsushita Electric, [2]Nara Inst. of Science and Technology and [3]CREST, Japan*	**10:00 B-7-4** Fabrication Method of Microlens Array Using Oxidized Porous Silicon Bulk Micromachining and PDMS Replication Molding S. K. Yeo, M. L. Ha and Y. S. Kwon, *KAIST, Korea*	**10:00 C-7-4** RNA Trap using Microfluidic Chip with Taper Shaped Channel K. Ueno[1], W. Nagasaka[1], Y. Tomizawa[1], Y. Nakamori[1], E. Tamiya[1] and Y. Takamura[1,2], *[1]JAIST, and [2]PRESTO, Japan*	**10:00 D-7-3** Effect of UV/ozone Treatment on Nanogap Electrodes for Molecular Devices T. Goto[1], H. Inokawa[2], K. Sumitomo[1], M. Nagase[1], Y. Ono[1] and K. Torimitsu[1], *[1]NTT Corp. and [2]Shizuoka Univ., Japan*	
10:15 A-7-5 Tunnel-coupled double nanocrystalline Si quantum dots integrated into a single-electron transistor Y. Kawata[1], M. Khalafalla[1], K. Usami[1], Y. Tsuchiya[1,2], H. Mizuta[1,2] and S. Oda[1,2], *[1]Tokyo Tech and [2]SORST-JST, Japan*	**10:15 B-7-5** Photocell system driven by Mechanoluminescence N. Terasaki, C. N. Xu, Y. Imai and H. Yamada, *AIST, Japan*	**10:15 C-7-5** Manipulation of DNA Molecules in Nanopores by Electric Field for Porous Silicon Based DNA Microarray Applications R. Yamaguchi[1], K. Ishibashi[1], K. Miyamoto[1], Y. Kimura[1, 2] and M. Niwano[1, 2], *[1]Tohoku Univ. and [2]CREST, Japan*	**10:15 D-7-4** Analysis of hole trapping into pentacene FET by Optical Second Harmonic Generation and C-V measurements E. Lim, T. Manaka, R. Tamura and M. Iwamoto, *Tokyo Tech, Japan*	

Break

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
9:40 F-7-3 P-SONOS and N-SONOS Transient Current and Field Modeling for Program and Erase P. Y. Du and J. C. Guo, *National Chiao Tung Univ., Taiwan*	**9:40 G-7-3** Shear Stress Analyses in Chemical Mechanical Planarization Processing with Cu/porous low-k Structure M. Kodera[1], Y. Mochizuki[2], A. Fukuda[2], H. Hiyama[2] and M. Tsujimura[3], *[1]Semiconductor Company, Toshiba Corp, [2]Ebara Research Corp. and [3]Ebara Corp., Japan*	**9:40 H-7-3** Surface-Potential-Based MOS-Varactor Model for RF Applications M. Miyake[1], N. Sadachika[1], D. Navarro[1], Y. Mizukane[1], T. Ezaki[1], M. Miura-Mattausch[1], H. J. Mattausch[1], T. Ohguro[2], T. Iizuka[2], M. Taguchi[2], S. Kumashiro[2] and S. Miyamoto[2], *[1]Hiroshima Univ. and [2]Semiconductor Technology Academic Research Center, Japan*	**9:30 I-7-3** Amorphous $CuxGa_{1-x}O$ film deposition by ultrahigh vacuum radio frequency magnetron sputtering H. Ishikwa, N. Takeuchi, N. Okuda, T. Takeuchi and Y. Horikoshi, *Waseda Univ., Japan*	**9:40 J-7-3** The Effect of Nitrogen on Thermal Diffusion in HfO_2-based Gate Dielectrics N. Takahashi, T. Yamasaki and C. Kaneta, *Fujitsu Labs. Ltd., Japan*
10:00 F-7-4 Lateral Redistribution and Interactive Impacts of Localized Trapped Charges during Retention Baking in SONOS Memory H. Pang, L. Pan, L. Sun, D. Wu and J. Zhu, *Tsinghua Univ., China*	**10:00 G-7-4** Effects of Oxidizer in Metal CMP Slurry on Open Circuit Potential Change during Metal Polishing S. Shima, S. Kamioka, S. Yasuda, H. Nagano, Y. Wada, K. Tokushige, A. Fukunaga and M. Tsujimura, *Ebara Corp., Japan*	**10:00 H-7-4** Using MASTAR as a Pre-SPICE Model Generator for Early Technology Assessment and Circuit Simulation F. Boeuf[1], M. Sellier[1], B. Duriez[2], E. Josse[1], A. Pouydebasque[2], M. Müller[2], F. Payet[1], B. Borot[1] and T. Skotnicki[1], *[1]STMicroelectronics and [2]Philips Semiconductor, France*	**9:45 I-7-4** Development of New Calculation Method for Rare Earth Element and Large Scale Electronic Structure Calculation of Blue Phosphor $BaMgAl_{10}O_{17}:Eu^{2+}$ H. Onuma[1], H. Tsuboi[1], M. Koyama[1], A. Endou[1], H. Takaba[1], M. Kubo[1,2], C. A. del Carpio[1], P. Selvam[1] and A. Miyamoto[1], *[1]Tohoku Univ. and [2]PRESTO, Japan*	**10:00 J-7-4** The Highly Reliable Evaluation of Mobility in an Ultra Thin High-k Gate Stack with an Advanced Pulse Measurement Method R. Iijima[1], M. Takayanagi[2], M. Koyama[1] and A. Nishiyama[1], *[1]Toshiba Corp. and [2]Semiconductor Company, Toshiba Corp., Japan*
	10:20 G-7-5 Ionic Conduction Leakage Current in Porous Silica Films Y. Kayaba[1], K. Kohmura[2] and T. Kikkawa[1], *[1]Hiroshima Univ. and [2]Mitsui Chemicals, Inc., Japan*		**10:00 I-7-5** MBE Growth of Gd/Fe Multilayer on GaAs(001) H. Miyagawa, S. Koshiba, N. Takahashi, N. Tsurumachi, H. Shiraoka, K. Matsushita, S. Nakanishi and H. Itoh, *Kagawa Univ., Japan*	**10:20 J-7-5** Intrinsic Electronically-Active Defects in Transition Metal Elemental Oxides G. Lucovsky[1], H. Seo[1], L. B. Fleming[1], M. D. Ulrich[1] and J. Luning[2], *[1]North Carolina Strate Univ. and [2]Stanford Synchrotron Radiation Lab., USA*

Break

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
Area 9: Physics and Applications of Novel Functional Materials and Devices	**Area 7: Photonic Devices and Device Physics**	**Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)**	**Area 10: Organic Materials Science, Device Physics, and Applications**	**Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics**
A-8: Novel Devices and Materials II (10:45-12:15) Chairs: Y. Takahashi (Hokkaido Univ.) M. Tabe (Shizuoka Univ.)	B-8: All-Optical Switches (10:45-12:00) Chairs: M. Sugawara (Fujitsu Labs.) M. Tokushima (NEC)	C-8: Nano and Bio Sensors I (10:45-12:15) Chairs: K. Sawada (Toyohashi Univ. of Tech.) S. A. Contera (Univ. of Oxford)	D-8: Organic Transistor I (10:45-12:00) Chairs: K. Kudo (Chiba Univ.) M. Iwamoto (Tokyo Tech)	E-8: GaAs FETs and Process Technologies (10:45-12:15) Chairs: Y. J. Chan (National Chiao Tung Univ.) S. Tanaka (NEC)
10:45 A-8-1 Electrostatic coupling between two double-quantum dots studied by resonant tunneling current G. Shinkai[1,2], T. Fujisawa[1,2], T. Hayashi[1] and Y. Hirayama[1,3,4], *[1]NTT Corp., [2]Tokyo Tech, [3]Tohoku Univ. and [4]SORST-JST, Japan*	**10:45 B-8-1** 40G bit/s NRZ wavelength converter with narrow active waveguides and inverted operation T. Hatta[1,2,3], T. Miyahara[1,2], Y. Miyazaki[1,2], K. Takagi[1,2], K. Matsumoto[1,2], T. Aoyagi[1,2], K. Mishina[3], A. Maruta[3] and K. Kitayama[3], *[1]OITDA, [2]Mitsubishi Electric Corp. and [3]Osaka Univ. Japan*	**10:45 C-8-1 (Invited)** Microchip based Fabrication of Curved Microstructures like Spider in Nature S. H. Lee, *Korea Univ., Korea*	**10:45 D-8-1** Combined Impact of Field and Carrier Concentration on Charge Carrier Mobilities in Amorphous Organic Thin Films C. Madigan and V. Bulović, *MIT, USA*	**10:45 E-8-1** Enhancement Mode GaAs n-MOSFET with High-k Dielectric M. Yakimov[1], V. Tokranov[1], R. Kambhampati[1], S. Koveshnikov[2], W. Tsai[2], F. Zhu[3], J. Lee[3] and S. Oktyabrsky[1], *[1]State Univ. of New York at Albany, [2]Intel Corp. and [3]Univ. of Texas at Austin, USA*
11:00 A-8-2 Photo Illumination Effect on Single-Electron-Tunneling Current Through a Thin Bicrystal SOI FET R. Nuryadi[1], Z. A. Burhanudin[1], R. Yamano[1], T. Ishino[1], Y. Ishikawa[2] and M. Tabe[1], *[1]Shizuoka Univ. and [2]Univ. of Tokyo, Japan*	**11:00 B-8-2** Improved Waveguide Structure for All Optical Switches based on Intersubband Transition in II-VI Quantum Wells K. Akita[1,2], R. Akimoto[1], T. Hasama[1], H. Ishikawa[1] and Y. Takanashi[2], *[1]National Inst. of Advanced Industrial Science and Technology and [2]Tokyo Univ. of Science, Japan*		**11:00 D-8-2** Electric field distribution in organic field effect transistor evaluated by microscopic second harmonic generation T. Manaka, E. Lim, R. Tamura, D. Yamada and M. Iwamoto, *Tokyo Tech, Japan*	**11:00 E-8-2** Investigation of GaAs MOSFETs with Gate Oxide Grown Using Photoelectrochemical Oxidation Method H. Y. Lee[1], Y. F. Lin[1], M. Y. Wang[1] and C. T. Lee[2], *[1]National Formosa Univ. and [2]National Cheng Kung Univ., Taiwan*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
Area 4: Advanced Memory Technology	**Area 2: Characterization and Materials Engineering for Interconnect Integration**	**Area 3: CMOS Devices/Device Physics**	**Area 8: Advanced Material Synthesis and Crystal Growth Technology**	**Area 1: Advanced Gate Stack/Si Processing Science**
F-8: MRAM/PRAM (10:45-12:25) Chairs: Y. Ohji (Renesas) N. Ishiwata (NEC)	G-8: Special Session I ; Reliability (10:45-12:25) Chairs: S. Ogawa (Selete/ Matsushita) Y. Hayashi (NEC)	H-8: Advanced Channel and Substrate Technology (10:45-12:25) Chairs: Y. Momiyama (Fujitsu) K. Takeuchi (NEC)	I-8: New Materials (10:45-11:45) Chairs: K. Nishi (NEC) H. Yamaguchi (NTT)	J-8: Metal/High-k CMOS (10:45-12:25) Chairs: Y. Tsunashima (Toshiba) O. Faynot (LETI)
10:45 F-8-1 Process Integration of Low-Power and High-Speed 16Mb MRAM using Multi-Layer Yoke Wiring Technology T. Kajiyama[1], S. Miura[2], Y. Asao[1], T. Ueda[1], H. Aikawa[1], M. Iwayama[1], K. Hosotani[1], M. Amano[1], M. Yoshikawa[1], K. Tsuchida[1], S. Ikegawa[1], T. Kishi[1], M. Shimomura[1], K. Shimura[2], N. Ohshima[2], H. Hada[2], A. Nitayama[1], S. Tahara[2] and H. Yoda[1], *[1]Toshiba Corp. and [2]NEC Corp., Japan*	**10:45 G-8-1 (Invited)** Challenges of Cu Metallization for 45nm and beyond M. H. Tsai, *TSMC, Taiwan*	**10:45 H-8-1** Strained SiGe-On-Insulator N-MOSFET with Silicon Source/Drain for Drive Current Enhancement G. H. Wang[1], E. H. Toh[1], K. W. Ang[1], C. H. Tung[2], A. Du[2], Y. L. Foo[3], G. Q. Lo[2], G. Samudra[1] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Inst. of Microelectronics and [3]Inst. of Materials Research & Engineering, Singapore*	**10:45 I-8-1** Fabrication of III-V-O-I (III-V on Insulator) structures on Si using micro-channel epitaxy with a two-step growth technique M. Shichijo, R. Nakane, S. Sugahara and S. Takagi, *Univ. of Tokyo, Japan*	**10:45 J-8-1** Highly scalable and WF-tunable Ni(Pt)Si/SiON TOSI-gate CMOS devices obtained in a CMP-less integration scheme M. Muller[1], G. Bidal[2], A. Mondot[2], S. Denorme[2], C. Fenouillet-Beranger[4], F. Boeuf[2], D. Aime[2], M. Rafik[2], P. Gouraud[2], T. Kormann[1], G. Chabanne[3], A. Zauner[1], G. Braeckelmann[3], S. Bonnetier[3], D. Barge[1], C. Laviron[4], A. Toffoli[4], A. Tarnowka[1], S. Pokrant[1] and T. Skotnicki[2], *[1]Philips Semiconductors, [2]STMicroelectronics, [3]Freescale Conductors and [4]CEA-LETI, France*
11:05 F-8-2 New Magnetic Nano-Dots Memory with FePt Nano-Dots C. K. Yin[1], J. C. Bea[2], M. Murugesan[2], M. Oogane[1], T. Fukushima[1], T. Tanaka[1], K. Natori[3], M. Miyao[4] and M. Koyanagi[1], *[1]Tohoku Univ., [2]JST, [3]Univ. of Tsukuba and [4]Kyusyu Univ., Japan*		**11:05 H-8-2** Ultra-thin Ge-on-Insulator (GOI) Metal S/D p-channel MOSFETs fabricated by low temperature MBE growth T. Uehara, H. Matsubara, S. Sugahara and S. Takagi, *Univ. of Tokyo, Japan*	**11:00 I-8-2** Dynamics of Defects in Strained Silicon, Strained SiGe and Strained Germanium A. Reznicek, S. W. Bedell, J. P. de Souza, K. W. Schwarz, K. E. Fogel, J. A. Ott, H. J. Hovel and D. K. Sadana, *IBM Research, USA*	**11:05 J-8-2** Sub-30 nm P-channel Schottky Source/Drain FinFETs: Integration of Pt_3Si FUSI Metal Gate and High-k Dielectric R. T. P. Lee[1], K. M. Tan[1], A. E. J. Lim[1], T. Y. Liow[1], G. Q. Lo[3], G. Samudra[1], D. Z. Chi[2] and Y. C. Yeo[1], *[1]National Univ. of Singapore, [2]Inst. of Materials Research and Engineering and [3]Inst. of Microelectronics, Singapore*

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11:15 A-8-3 Fabrication of Ge Quantum-dots by Oxidation of $Si_{1-x}Ge_x$-on-insulator Nanowires and its Applications to Resonant Tunneling Diodes and Single-electron/Single-hole Transistors W. T. Lai and P. W. Li, *National Central Univ. , Taiwan*		**11:15 C-8-2** First Selective Detection of Proteins Using Top-Gate Carbon Nanotube Field Effect Transistor M. Abe[1, 2], K. Murata[1, 2, 3], A. Kojima[3, 4], Y. Ifuku[4], M. Shimizu[5], T. Ataka[1, 2] and K. Matsumoto[2, 3, 5, 6], *[1]Olympus Corp., [2]NEDO, [3]CREST-JST, [4]Mitsubishi Kagaku, [5]AIST and [6]Osaka Univ., Japan*	**11:15 D-8-3** Organic Static Induction Transistors Based on Pentacene Thin Films with Various Source Electrodes Y. Watanabe[1], H. Iechi[1,2] and K. Kudo[1], *[1]Chiba Univ. and [2]Ricoh Co., Ltd. Japan*	**11:15 E-8-3** Passivation Effects of 100 nm $In_{0.4}AlAs/In_{0.35}GaAs$ Metamorphic HEMT With Remote PECVD Grown Si_3N_4 Layer S. Kim, K. Jang, J. Lee, J. Her and K. Seo, *Seoul National Univ., Korea*	**11:25 F-8-3** Optimization of Ring Type Electrode Process for High Density PRAM K. C. Ryoo, Y. J. Song, D. H. Kang, C. W. Jeong, J. H. Kong, J. H. Oh, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, J. H. Park, Y. T. Oh, J. S. Kim, J. M. Shin, J. H. Park, K. W. Lee, Y. Fai, G. H. Koh, G. T. Jeong, H. S. Jeong and K. Kim, *Samsung Electronics Co., Ltd, Korea*	**11:15 G-8-2 (Invited)** Defects in Electroplated Cu and their Impact on Stress Migration Reliability A. Uedono[1], T. Suzuki[2], T. Nakamura[2], T. Ohdaira[3] and R. Suzuki[3], *[1]Univ. of Tsukuba, [2]STARC and [3]AIST, Japan*	**11:25 H-8-3** Reduction of Parasitic Resistance of Self-Aligned Copper Germanide for Germanium p-MOSFETs Y. L. Chao and J. C. Woo, *Univ. of California Los Angeles, USA*	**11:15 I-8-3** Inhomogeneous strain in thin silicon films analyzed by grazing incidence x-ray diffraction H. Omi[1], T. Kawamura[1], Y. Kobayashi[1], S. Fujikawa[2], Y. Tsusaka[2], Y. Kagoshima[2] and J. Matsui[3], *[1]NTT Corp., [2]Univ. of Hyogo and [3]CAST, Japan*	**11:25 J-8-3** Effects of Optimization of Gate Edge Profile on sub-45nm Metal Gate High-k Dielectric Metal-Oxide-Semiconductor Field Effect Transistors Characteristics C. Y. Kang[1], R. Choi[1], S. H. Bae[2], S. C. Song[1], M. M. Hussain[1], C. Young[1], D. Heh[1], G. Bersuker[1] and B. H. Lee[3], *[1]SEMATECH, [2]Univ. of Texas at Austin and [3]IBM Assignee, USA*
11:30 A-8-4 Observation of single-electron pump operation with one ac gate bias in phosphorous-doped Si wires D. Moraru[1], Y. Ono[2], H. Inokawa[1], K. Yokoi[1], R. Nuryadi[1], H. Ikeda[1] and M. Tabe[1], *[1]Shizuoka Univ. and [2]NTT Corp., Japan*		**11:30 C-8-3** High-efficiency cell membrane perforation technique based on self-organized ZnO nanorods M. Seki, T. Saito and H. Tabata, *Osaka Univ., Japan*	**11:30 D-8-4** Investigation for hafnium oxide as an insulator layer of organic thin film transistor C. W. Lin, J. H. Lin and K. C. Liu, *Chang Gung Univ., Taiwan*	**11:30 E-8-4** Microwave Performance of Pseudomorphic HEMT with Tunable Field-Plate Voltage H. C. Chiu and F. T. Chien, *Chang Gung Univ. Taiwan*				**11:30 I-8-4** Characterization of Epitaxial Silicon Films Grown by Atmosheric Pressure Plasma Chemical Vapor Deposition at Low Temperatures (450-600˚C) N. Tawara, H. Ohmi, Y. Terai, H. Kakiuchi, H. Watanabe, Y. Fujiwara and K. Yasutake, *Osaka Univ., Japan*	
11:45 A-8-5 SET-based Flexible Multi-valued NAND and NOR Gates for Half-Adder C. K. Lee[1], S. J. Kim[1], S. J. Choi[1], J. H. Hwang[1], R. S. Chung[1], J. J. Lee[1], M. S. Kim[1], S. J. Shin[1], J. B. Choi[1], Y. S. Yu[2], H. W. Kye[3] and B. N. Song[3], *[1]Chungbuk National Univ., [2]Hankyong National Univ. and [3]EXCEL Semiconductor Inc., Korea*		**11:45 C-8-4** In-situ Monitoring of DNA Hybridization Using Surface Infrared Spectroscopy K. Miyamoto[1], R. Yamaguchi[1], K. Ishibashi[1], Y. Kimura[1,2] and M. Niwano[1,2], *[1]Tohoku Univ. and [2]CREST-JST, Japan*	**11:45 D-8-5** Reduction of Bias-Induced Threshold Voltage Shift in Pentacene Field Effect Transistors by Interface Modification and Molecular Ordering C. B. Park, T. Nishimura, T. Yokoyama, K. Kita and A. Toriumi, *Univ. of Tokyo, Japan*	**11:45 E-8-5** 80nm T-Shaped Gate Metamorphic HEMTs fabricated Using Two-Step Gate Recess Process H. S. Yoon, J. Y. Shim, D. M. Kang, J. Y. Hong and K. H. Lee, *ETRI, Korea*	**11:45 F-8-4** Characteristics Improvement of Phase Change Memory with Programming Pulse Width D. S. Chao[1,3], C. M. Lee[1], Y. C. Chen[1], P. H. Yen[1], D. Y. Wang[1], M. J. Chen[1], S. C. Lo[2], H. H. Hsu[1], W. H. Wang[1], F. Chen[1], Y. Chuo[1], C. Lien[3], M. J. Kao[1] and M. J. Tsai[1], *[1]EOL, [2]MCL and [3]National Tsing Hua Univ., Taiwan*	**11:45 G-8-3** Nondestructive characterization of dielectric stack structures by laser-pulse-generated surface acoustic wave analysis T. Takimura[1], N. Hata[1,2], Y. Shishida[3], S. Chikaki[3] and T. Kikkawa[2,4], *[1]ASRC, AIST, [2]MIRAI-ASRC, AIST, [3]MIRAI-ASET and [4]Hiroshima Univ., Japan*	**11:45 H-8-4** Bendable High-Performance Electronic Devices (Active Transistor, High-Density Interconnect and Passive-MIM Capacitors) on Flexible Organic-Substrate H. Y. Li [1], L. H. Guo[1], W. Y. Loh[1], L. K. Bera[1], Q. X. Zhang[1], N. Hwang[1], E. B. Liao[1], K. W. Teoh[1], H. M. Chua[1], Z. X. Shen[2], G. Q. Lo[1], N. Balasubramanian[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]Nanyang Technological Univ., Singapore*		**11:45 J-8-4** Compatibility of ALD Hafnium Silicate with Dual Metal Gate CMOS Integration M. M. Hussain[1], S. -. Song[1], C. Y. Kang[1], M. Quevedo-lopez[2], H. Alshareef[2], B. Sassman[1], R. Choi[1] and B. H. Lee[3], *[1]SEMATECH, [2]Texas Instruments and [3]IBM, USA*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
12:00 A-8-6 Multi-Functionality of Novel Structured Tunneling Devices W. Y. Choi, J. Y. Song, J. P. Kim, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*		**12:00 C-8-5** Si-Based Planer Type Ion-channel Biosensors H. Uno[1], Z. L. Zhang[1], T. Y. Chiang[1], K. Suzui[1], R. Tero[1], S. Nakao[1], S. Seki[2], S. Tagawa[2] and T. Urisu[1], *[1]Inst. for Molecular Science and [2]Osaka Univ., Japan*		**12:00 E-8-6** Comparative Study of DC and Microwave Characteristics of 0.12 μm T-Shaped Gate AlGaAs/InGaAs/GaAs PHEMTs Using a Hybrid and Conventional E-beam Lithography Process J. W. Lim, S. W. Yoon, H. K. Ahn, H. G. Ji, W. J. Chang, J. K. Mun and H. Kim, *ETRI, Korea*

Lunch

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
12:05 F-8-5 Thickness Dependent Nano-Crystallization in $Ge_2Sb_2Te_5$ films and Its Effect on Devices X. Wei [1,2], L. Shi[1] and C. T. Chong[1,2], *[1]Data Storage Inst. and [2]National Univ. of Singapore, Singapore*	**12:05 G-8-4** High Performance SiN-MIM Decoupling Capacitors with Surface-smoothed Bottom Electrodes for High-speed MPUs I. Kume[1], N. Inoue[1], H. Ohtake[1], S. Saitoh[1], N. Furutake[1], J. Kawahara[1], T. Toda[2], T. Shinmura[2], K. Matsui[2], T. Iwaki[2], K. Ohto[2], M. Furuyama[2] and Y. Hayashi[1], *[1]NEC Corp. and [2]NEC Electronics, Japan*			**12:05 J-8-5** Full-Metal-Gate Integration of Dual-Metal-Gate HfSiON CMOS Transistors by Using Oxidation-Free Dummy-Mask Process F. Ootsuka, Y. Tamura, Y. Akasaka, S. Inumiya, H. Nakata, M. Ohtsuka, T. Watanabe, M. Kitajima, Y. Nara and K. Nakamura, *Selete , Japan*

Lunch

Room 411/412 (A)

Area 9: Physics and Applications of Novel Functional Materials and Devices

A-9: Novel Devices and Materials III
(13:15-14:45)
Chairs: K. Ishibashi (RIKEN)
T. Fujisawa (NTT)

13:15 A-9-1 (Invited)
Organic Molecular Wires
P. Hadley and M. Durkut, *Graz Univ. of Technology, Austria*

Room 413 (B)

Area 7: Photonic Devices and Device Physics

B-9: Detectors and Sensors
(13:15-15:00)
Chairs: M. Tokushima (NEC)
M. Sugawara (Fujitsu Labs.)

13:15 B-9-1
InP/InGaAs Leaky Waveguide Photodiode with a Partially p-Doped Absorption Layer and a Distributed-Bragg-Reflector (DBR) for High-Power and High-Bandwidth-Responsivity Product Performance
W. Y. Chiu, W. K. Wang, Y. S. Wu, F. H. Huang, D. M. Lin, Y. J. Chan and J. W. Shi, *National Central Univ., Taiwan*

13:30 B-9-2
Deep Trench Isolation for Pixel Crosstalk Suppression in Active Pixel Sensor with 1.7μm pixel pitch
B. J. Park[1], C. R. Moon[1], Y. W. Lee[1], D. W. Kim[1], K. H. Paik[1], J. R. Yoo[1], Y. S. Yoo[1], Y. Jon[1], C. H. Koo[1], S. C. Bang[1], Y. K. Lee[1], Y. J. Cho[1], S. H. Hwang[1], D. C. Park[1], H. G. Jung[1], J. C. Shin[1], J. Jung[2], K. B. Lee[1], H. P. Noh[1], D. H. Lee[1] and K. Kim[1], *[1]Samsung Electronics Co. and [2]Sejong Univ., Korea*

Room 414/415 (C)

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

C-9: Nano and Bio Sensors II
(13:15-15:00)
Chairs: H. Tabata (Osaka Univ.)
H. Sugihara (Matsushita Electric)

13:15 C-9-1
Membranes as Self-Assembling Coating of Solid State Device Components: Integration of Submicron Electrical Circuitry with Biological Systems
M. R. R. de Planque, N. C. Toledo, S. A. Contera and J. F. Ryan, *Univ. of Oxford, UK*

13:30 C-9-2
Evaluation of Electrical Stimulus Current to Retina Cells for Retinal Prosthesis by Using Platinum-Black (Pt-b) Stimulus Electrode Array
T. Watanabe, K. Komiya, T. Kobayashi, R. Kobayashi, T. Fukushima, H. Tomita, E. Sugano, M. Sato, H. Kurino, T. Tanaka, M. Tamai and M. Koyanagi, *Tohoku Univ., Japan*

Room 416/417 (D)

Area 10: Organic Materials Science, Device Physics, and Applications

D-9: Organic Transistor II
(13:30-15:00)
Chairs: M. Iwamoto (Tokyo Tech)
T. Someya (Univ. of Tokyo)

13:30 D-9-1 (Invited)
Development of a Printed Dielectric Layer for Organic Transistors
T. Kamata, S. Uemura, M. Yoshida, K. Suemori, S. Hoshino, N. Takada and T. Kozasa, *AIST, Japan*

Room 418 (E)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

E-9: GaN FETs and Process Technologies
(13:15-15:00)
Chairs: M. Kuzuhara (Univ. of Fukui)
R. Hattori (Mitsubishi Electric)

13:15 E-9-1 (Invited)
Methods and Mechanisms for Ohmic Contacts on AlGaN/GaN HEMTs
I. Adesida, F. M. Mohammed, L. Wang, A. Basu and V. Kumar, *Univ. of Illinois at Urbana-Champaign, USA*

Room 419 (F)

Area 3: CMOS Devices/Device Physics

F-9: Schottky S/D and Carrier Transport
(13:15-14:55)
Chairs: A. Hokazono (Toshiba)
J. C. S. Woo (UCLA)

13:15 F-9-1
Dopant Segregated Pt-Germanide Schottky S/D p-MOSFET with HfO_2/TaN gate on Strained Si-SiGe channel
W. Y. Loh[1], Y. Chen[1,2], S. J. Lee[2], L. K. Bera[1], R. Yang[1], G. Q. Lo[1] and D. L. Kwong[1], *[1]Inst. of Microelectronics and [2]National Univ. of Singapore, Singapore*

13:35 F-9-2
Improved Performance of Schottky Barrier Source/Drain Transistors with High-K Gate Dielectrics by Adopting Recessed Channel and/or Buried Source/Drain Structures
M. Ono, M. Koyama and A. Nishiyama, *Toshiba Corp., Japan*

Room 501 (G)

Area 2: Characterization and Materials Engineering for Interconnect Integration

G-9: Special Session II : Metallization Challenges
(13:15-15:35)
Chairs: J. Koike (Tohoku Univ.)
M. Nihei (Selete/Fujitsu)

13:15 G-9-1 (Invited)
Reliability Challenges for Advanced Copper Low-k Interconnects
Z. Tokei[1], C. Bruynseraede[1], Y. L. Li[1,2], I. Ciofi[1] and G. P. Beyer[1], *[1]IMEC and [2]Katholieke Univ. Leuven, Belgium*

Room 502 (H)

Area 3: CMOS Devices/Device Physics

H-9: Carrier Transport
(13:15-14:55)
Chairs: H. C. Lin (National Chiao Tung Univ.)
K. Takeuchi (NEC)

13:15 H-9-1
Comparative Study on Influence of Subband Structures on Electrical Characteristics of III-V Semiconductor, Ge and Si Channel n-MISFETs
S. Takagi and S. Sugahara, *Univ. of Tokyo , Japan*

13:35 H-9-2
Influence of High Dielectric Constant in Gate Insulator on Remote Coulomb Scattering due to Gate Impurities in Si MOS Inversion Layer
Y. Nakabayashi[1], T. Ishihara[1], T. Shimizu[2] and J. Koga[1], *[1]Toshiba Corp. and [2]Semiconductor Co., Toshiba Corp., Japan*

Room 511/512 (I)

Small Auditorium (J)

Area 1: Advanced Gate Stack/Si Processing Science J-9-1

J-9: Reliability
(13:15-15:05)
Chairs: J. Yugami (Renesas)
S. Miyazaki (Hiroshima Univ.)

13:15 J-9-1 (Invited)
Degradation and Breakdown of Sub-1nm EOT HfO_2/Metal Gate Stacks
G. Groeseneken[1,2], R. Degraeve[1], T. Kauerauf[1,2], M. Cho[1,3], M. Zahid[4], L. A. Ragnarsson[1], D. P. Brunco[5], B. Kaczer[1], P. Roussel[1] and S. De Gendt[1,2], *[1]IMEC, [2]KU Leuven, [3]Seoul National Univ., [4]John Moores Univ. and [5]Intel assignee at IMEC, Belgium*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
13:45 A-9-2 Possible Non-equilibrium Kondo Effect in a Nanocrystalline Silicon Point-Contact Transistor M. A. H.Khalafalla[1], H. Mizuta[1], S. Oda[1] and Z. A. K. Durrani[2], *[1]Tokyo Tech and [2]Univ. of Cambridge, Japan*	**13:45 B-9-3** Pseudo 2-Transistor Active Pixel Sensor Using a High Responsivity PMOSFET-Type Photodetector with a Transfer Gate S. H. Seo[1], S. H. Lee[1], K. D. Kim[1], J. K. Shin[1], P. Choi[1], J. H. Park[2] and H. Kim[2], *[1]Kyungpook National Univ. and [2]Korea Electronics Technology Inst., Korea*	**13:45 C-9-3** Development of a CMOS Image Sensor for Real Time In Vivo Imaging of the Protease Activity Inside the Mouse Hippocampus D. C. Ng, T. Nakagawa, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, *Nara Inst. of Science and Technology, Japan*		**13:45 E-9-2** High-temperature and UV-assisted C-V characterization of GaN MIS structures H. Kato, M. Miczek and T. Hashizume, *Hokkaido Univ., Japan*	**13:55 F-9-3** Examination of Performance Improvement in Dopant Segregated Schottky MOSFETs; Short Channel Effects, Carrier Velocity and Parasitic Resistance Y. Nishi, A. Kinoshita and J. Koga, *Toshiba Corp., Japan*	**13:45 G-9-2** Diffusion Barrier Property of an Interface Layer Formed with Cu-Mn, Al and Mg Alloy Films on SiO_2 J. Iijima[1,2], M. Haneda[1] and J. Koike[1], *[1]Tohoku Univ. and [2]JST, Japan*	**13:55 H-9-3** Experimental Evidence for Invalidity of Matthiessen's Rule for MOS Inversion Layer Mobility Analysis through Hall Factor Measurement K. Kita, H. Irie and A. Toriumi, *Univ. of Tokyo, Japan*		**13:45 J-9-2** Impact of Captured-Carrier Distribution on Recovery Characteristics of Positive- and Negative-Bias Temperature Instability in HfSiON/SiO_2 Gate Stack I. Hirano, T. Yamaguchi, Y. Mitani, K. Sekine, M. Takayanagi, K. Eguchi and H. Satake, *Toshiba Corp., Japan*
14:00 A-9-3 Low Temperature Characteristics of Ambipolar SiO_2/Si/SiO_2 Hall-bar Devices K. Takashina[1], B. Gaillard[1], Y. Ono[1] and Y. Hirayama[1,2], *[1]NTT Corp. and [2]SORST-JST, Japan*	**14:00 B-9-4** Photodetective Characteristics of Metal-Oxide-Semiconductor Tunneling Structure with Aluminum Grid Gate H. Hashimoto, R. Yamada, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ., Japan*	**14:00 C-9-4** An Optical/Potential/Voltammetric Multifunctional CMOS Image Sensor for On-chip Biomolecular/Neural Sensing Applications T. Tokuda, I. Kadowaki, K. Kagawa, M. Nunoshita and J. Ohta, *Nara Inst. of Science and Technology, Japan*	**14:00 D-9-2** Low Hysteresis Organic Thin-Film Transistors and Inverters with Hybrid Gate Dielectric D. W. Park, C. A. Lee, K. D. Jung, B. G. Park, H. Shin and J. D. Lee, *Seoul National Univ., Korea*	**14:00 E-9-3** Device Isolation by Plasma Treatment for Planar Integration of E/D-mode AlGaN/GaN HEMTs R. Wang, Y. Cai, W. C. W. Tang, K. M. Lau and K. J. Chen, Hong Kong Univ. of Science and Technology, Hong Kong		**14:05 G-9-3** Self-Formation of Ti-rich Interfacial Layers in Cu(Ti) Alloy Films S. Tsukimoto, K. Ito and M. Murakami, *Kyoto Univ., Japan*			**14:05 J-9-3** Reliability of thick oxides integrated with HfSiOx gate dielectric B. H. Lee[1,2], C. Y. Kang[1], T. H. Lee[3], J. Barnett[1], R. Choi[1], S. C. Song[1] and R. Jammy[2], *[1]SEMATECH, [2]IBM Assignee and [3]Univ. of Texas at Austin, USA*
14:15 A-9-4 Detection of Magnetic Domain Wall in a Permalloy Wire by the Local Hall Effect Y. Sekine[1], T. Akazaki[1] and J. Nitta[2,3], *[1]NTT Corp., [2]Tohoku Univ. and [3]CREST-JST, Japan*	**14:15 B-9-5** A Compact Single-Photon Avalanche Diode in a Deep-Submicron CMOS Technology H. Finkelstein, M. J. Hsu and S. Esener, *Univ. of California San Diego, USA*	**14:15 C-9-5** Large scale electrode array based on distributed microchip architecture for retinal prosthesis J. Ohta[1], T. Tokuda[1], S. Sugitani[1], M. Taniyama[1], M. Nunoshita[1], A. Uehara[2], Y. Terasawa[2] and Y. Tano[3], *[1]Nara Inst. of Science and Technology, [2]NIDEK Co., Ltd. and [3]Osaka Univ., Japan*	**14:15 D-9-3** Performance enhancement of Organic TFT by low-energy Ar ion beam treatment onto gate dielectric surface S. Kang[1], J. Park[1], S. Jung[1], H. J. Lee[2] and M. Yi[1], *[1]Pusan National Univ. and [2]SungKyunKwan Univ., Korea*	**14:15 E-9-4** Phosphorus Implantation Effects in Mg Doped GaN Epilayers K. T. Liu[1], Y. K. Su[2], S. J. Chang[2] and Y. Horikoshi[3], *[1]Cheng Shiu Univ., [2]National Cheng Kung Univ. and [3]Waseda Univ., Taiwan*	**14:15 F-9-4** Study on Carrier Transport Limited by Coulomb Scattering due to Charged Centers in HfSiON MISFETs T. Ishihara, R. Iijima, M. Takayanagi, H. Tanimoto and M. Koyama, *Toshiba Corp., Japan*	**14:25 G-9-4 (Invited)** New Method of Probing Barrier Integrity and Low-k Stability C. U. Kim[1], D. M. Meng[1], N. Michael[1], Y. J. Park[2] and L. Matz[2], *[1]Univ. of Texas at Arlington and [2]Texas Instruments, USA*	**14:15 H-9-4** Analytical Model for Phonon-Limited Mobility in n-MOS Inversion Layers on Arbitrarily Oriented and Strained Si Surfaces M. Szczap[1,2], N. Cavassilas[1], F. Boeuf[2], F. Payet[2] and T. Skotnicki[2], *[1]L2MP and [2]STMicroelectronics, France*		**14:25 J-9-4** Impact of Initial Traps on TDDB and NBTI Reliabilities in High-k Gate Dielectrics K. Okada[1], H. Ota[2], T. Horikawa[2], M. Kadoshima[1], A. Ogawa[1], T. Nabatame[1] and A. Toriumi[2,3], *[1]MIRAI-ASET, [2]MIRAI-ASRC-AIST and [3]Univ. of Tokyo, Japan*
14:30 A-9-5 A Field-Effect Transistor with a Deposited Graphite Thin Film H. Inokawa[1], M. Nagase[2], S. Hirono[3], T. Goto[2], H. Yamaguchi[2] and K. Torimitsu[2], *[1]Shizuoka Univ., [2]NTT Corp. and [3]NTT Afty Engineering Corp., Japan*	**14:30 B-9-6** Threshold Behavior of Photoresponse of Plasma Waves by New Photomixer Devices Y. M. Meziani[1], M. Hanabe[1], T. Otsuji[1] and E. Sano[2], *[1]Tohoku Univ. and [2]Hokkaido Univ., Japan*	**14:30 C-9-6** Development of Si Long Microprobe (SiLM) for Platform of Intelligent Neural Implant Microsystem R. Kobayashi, T. Watanabe, K. Komiya, T. Fukushima, K. Sakamoto, H. Kurino, T. Tanaka, N. Katayama, H. Mushiake and M. Koyanagi, *Tohoku Univ., Japan*	**14:30 D-9-4** Stable Polymer Dielectric Film for P3HT TFT by Modified Poly-(Vinyl Phenol) with Polar Functional Gourp P. Y. Lo[1, 2], Z. Pei[1], F. Y. Yang[1], Y. R. Peng[1], Y. C. Lin[1] and Y. J. Chan[2], *[1]Industrial Technology Research Inst. and [2]National Central Univ., Taiwan*	**14:30 E-9-5** ICP Reactive Ion Etching with $SiCl_4$ Gas for Recessed Gate AlGaN/GaN HFET K. Matsuura[1], D. Kikuta[1], J. P. Ao[1], H. Ogiya[2], M. Hiramoto[2], H. Kawai[3] and Y. Ohno[1], *[1]Univ. of Tokushima, [2]SAMCO Inc. and [3]POWDEC K. K., Japan*			**14:35 H-9-5** Energy relaxation of two-dimensional electrons in Si-MOSFETs : determination of deformation potential constant of conduction band of Si K. H. Park, K. Hirakawa and S. Takagi, *Univ. of Tokyo, Japan*		

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)
	14:45 B-9-7 Optical Responses of Josephson Vortex flow Transistor under irradiation of femtosecond laser pulses I. Kawayama[1,2], Y. Doda[1,2], H. Murakami[1] and M. Tonouchi[1,2], *[1]Osaka Univ. and [2]CREST-JST, Japan*	**14:45 C-9-7** Liquid Sensing by Nano-gap Device with Treated Surface T. Hirokane, H. Hashimoto, D. Kanzaki, T. Takegawa, S. Morita, S. Urabe, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ., Japan*	**14:45 D-9-5** Fabrication of Low-Voltage Pentacene Thin Film Transistors with Al_2O_3 gate dielectric grown by oxygen plasma process K. D. Kim and C. K. Song, *Dong-A Univ., Korea*	**14:45 E-9-6** SiO_2 Passivation Effects on the Leakage Current in Dual-Gate AlGaN/GaN High Electron Mobility Transistors M. W. Ha, J. Lim, Y. H. Choi, J. C. Her, K. S. Seo and M. K. Han, *Seoul National Univ., Korea*

Break

	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 10: Organic Materials Science, Device Physics, and Applications	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics
	C-10: MEMS and NEMS : Application (15:15-16:30) Chairs: Y. Yoshino (Murata Mfg.) T. Ono (Tohoku Univ.)	D-10: Organic Transistor III (15:15-16:15) Chairs: K. Kudo (Chiba Univ.) T. Someya (Univ. of Tokyo)	E-10: High-Voltage GaN Devices (15:15-17:00) Chairs: A. Nakagawa (New Japan Radio) T. Tanaka (Matsushita Electric)
	15:15 C-10-1 **(Invited)** Physical Sensors in MEMS Technology K. Maenaka, *Univ. of Hyogo, Japan*	**15:15 D-10-1** Threshold Voltage Control in Pentacene TFTs by Perfluoropentacene Stack T. Yokoyama, T. Nishimura, K. Kita, K. Kyuno and A. Toriumi, *Univ. of Tokyo, Japan*	**15:15 E-10-1** **(Invited)** Recent Advances in GaN Power Devices T. Kachi, *Toyota Central R&D Labs., Japan*

Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
	14:55 G-9-5 An Excellent Cu Diffusion Barrier for Next Generation Multi-level Cu-interconnect C. J. Lee, C. F. Huang and B. Y. Tsui, *National Chiao Tung Univ., Taiwan*			**14:45 J-9-5** Leakage mechanism of ultrathin SiON gate dielectric H. Watanabe, D. Matsushita, K. Muraoka and K. Kato, *Toshiba Corp. , Japan*

Break

	Area 3: CMOS Devices/Device Physics	Area 1: Advanced Gate Stack/Si Processing Science
	H-10: Advanced Device Technology (15:15-16:55) Chairs: K. Shibahara (Hiroshima Univ.) A. Hokazono (Toshiba)	J-10: Metal Gate Electrode (15:15-16:35) Chairs: T. Nabatame (ASET) H. Fukutome (Fujitsu Labs.)
15:15 G-9-6 Plasma-enhanced polymerization thin films as a drift barrier for Cu interconnects T. Yoshino[1], J. Kawahara[2], N. Hata[1], Y. Shishida[2] and T. Kikkawa[1,3], *[1]MIRAI-ASRC, AIST, [2]MIRAI-ASET and [3]Hiroshima Univ., Japan*	**15:15 H-10-1** Novel Elevated Source/Drain Technology for FinFET Overcoming Agglomeration and Facet Problems Utilizing Solid Phase Epitaxy K. Miyano, A. Kaneko, I. Mizushima, A. Yagishita, K. Suguro, Y. Saito, K. Eguchi and Y. Tsunashima, *Toshiba Corp., Japan*	**15:15 J-10-1** Work Function Modulation by Segregation of Indium through Tungsten Gate For Dual-Metal Gate CMOS Applications K. Nakajima, M. Koyama, T. Aoyama, A. Nishiyama, K. Eguchi and K. Suguro, *Toshiba Corp., Japan*

Room 411/412 (A)	Room 413 (B)	Room 414/415 (C)	Room 416/417 (D)	Room 418 (E)	Room 419 (F)	Room 501 (G)	Room 502 (H)	Room 511/512 (I)	Small Auditorium (J)
			15:30 D-10-2 Organic Field-Effect Transistor Integrated Circuits using Self-Alignment Process Technology H. Okada, T. Nagai, T. Kimura, S. Naka and H. Onnagawa, *Univ. of Toyama, Japan*				**15:35 H-10-2** Threshold Voltage Instability of 45-nm-node Poly-Si- or FUSI-Gated SRAM Transistors Caused by Dopant Lateral Diffusion in Poly-Si K. Hosaka, T. Aoyama, K. Suzuki, *Fujitsu Labs., Japan*		**15:35 J-10-2** Diffusion control technique in TiN stacked metal gate electrodes for p-MISFETs S. Sakashita, T. Kawahara, M. Mizutani, M. Inoue, K. Mori, S. Yamanari, M. Higashi, Y. Nishida, K. Honda, N. Murata, J. Tsuchimoto, J. Yugami, K. Fujiwara and M. Yoneda, *Renesas Technology Corp., Japan*
		15:45 C-10-2 Piezoelectric Optical Micro Scanner with Built-in Torsion Sensor T. Kobayashi and R. Maeda, *National Inst. of Advanced Industrial Science and Technology, Japan*	**15:45 D-10-3** Alignment-Free Printable Organic Thin-Film Transistors on the Flexible Substrate T. Arai[1], N. Sato[2], K. Yamaguchi[2], M. Kawasaki[1], M. Fujimori[1], T. Shiba[1], M. Ando[1] and K. Torii[1], *[1]Hitachi, Ltd. and [2]Kanagawa Univ., Japan*	**15:45 E-10-2** Improvement of Breakdown Voltages in GaN Schottky Barrier Diodes by Pseudo-Superjunction Structures K. Nakazawa, H. Ueno, H. Matsuo, M. Yanagihara, Y. Uemoto, T. Ueda and T. Tanaka, *Matsushita Electric, Japan*			**15:55 H-10-3** Novel threshold voltage fine control method for FETs within a wafer using LDSi (Locally Differentiated Scanning ion implant) K. B. Rouh, M. Y. Lee, S. W. Jin, Y. S. Sohn, Y. S. Joung, Y. J. Ki, I. K. Han, Y. W. Song and S. W. Park, *Hynix Semiconductor Inc., Korea*		**15:55 J-10-3** Work Function Instability at pMOS Metal/HfSiON Interfaces Y. Tsuchiya and M. Koyama, *Toshiba Corp., Japan*
		16:00 C-10-3 High-Q Piezoelectrically Actuated RF MEMS Tunable Capacitor M. Nishigaki[1], T. Nagano[1], T. Miyazaki[1], T. Kawakubo[2] and K. Itaya[1], *[1]Toshiba Corp. and [2]Toshiba Research Consulting Corp., Japan*	**16:00 D-10-4** Hall effect of polycrystalline pentacene field-effect transistors on plastic films Y. Takamatsu, T. Sekitani, S. Nakano, T. Sakurai and T. Someya, *Univ. of Tokyo, Japan*	**16:00 E-10-3** High Critical Electric Field Exceeding 8 MV/cm Measured Using AlGaN p-i-n Vertical Conducting Diode on n-SiC Substrate A. Nishikawa, K. Kumakura and T. Makimoto, *NTT Corp., Japan*					

16:15 C-10-4
Solenoid RF Transformer and Balun
J. M. Yook, J. H. Ko and Y. S. Kwon, *KAIST, Korea*

16:15 E-10-4
High Breakdown Voltage AlGaN/GaN MIS-HEMT with TiO_2/Si_3N_4 Gate Insulator
S. Yagi[1], M. Shimizu[1], M. Inada[1], H. Okumura[1], H. Ohashi[1], Y. Yano[2] and N. Akutsu[2], *[1]National Inst. of Advanced Industrial Science and Technology and [2]Taiyo Nippon Sanso Corp., Japan*

16:30 E-10-5
Pnp AlGaN/InGaN/GaN Double Heterojunction Bipolar Transistors with Low-Base-Resistance (<100Ω/sq)
K. Kumakura and T. Makimoto, *NTT Corp., Japan*

16:45 E-10-6
A New Field Plate Structure for Suppression of Leakage Current of AlGaN/GaN HEMTs
Y. H. Choi, M. W. Ha, J. Lim and M. K. Han, *Seoul National Univ., Korea*

16:15 H-10-4
Novel Gate-All-Around MOSFETs with Self-Aligned Structure
J. Y. Song, W. Y. Choi, J. P. Kim, S. W. Kim, J. D. Lee and B. G. Park, *Seoul National Univ., Korea*

16:35 H-10-5
Improvement of Bulk CMOS Electrostatic Integrity using Germanium and Carbon co-implantation
B. Dumont[1,2], A. Pouydebasque[3], F. Milesi [4,5], S. Kader[2], F. Boeuf[1] and T. Skotnicki[1], *[1]STMicroelectronics, [2]LPM - INSA Lyon, [3]Philips Semiconductors, [4]Ion Beam Services and [5]CEA-LETI, France*

16:15 J-10-4
Thermal stability of metal electrodes and its impact on gate dielectric characteristics
H. Park[1,4], H. C. Wen[2], M. Chang[1], M. Jo[1], R. Choi[2], B. H. Lee[2,3], S. C. Song[2], C. Y. Kang[2,4], T. Lee[4], G. Brown[2], J. C. Lee[4] and H. Hwang[1], *[1]Gwangju Inst. of Science and Technology, [2]SEMATECH, [3]IBM Assignee and [4]The Univ. of Texas at Austin, Korea*

ORGANIZING COMMITTEE

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SSDM 2006 is subsidized by the following organization:
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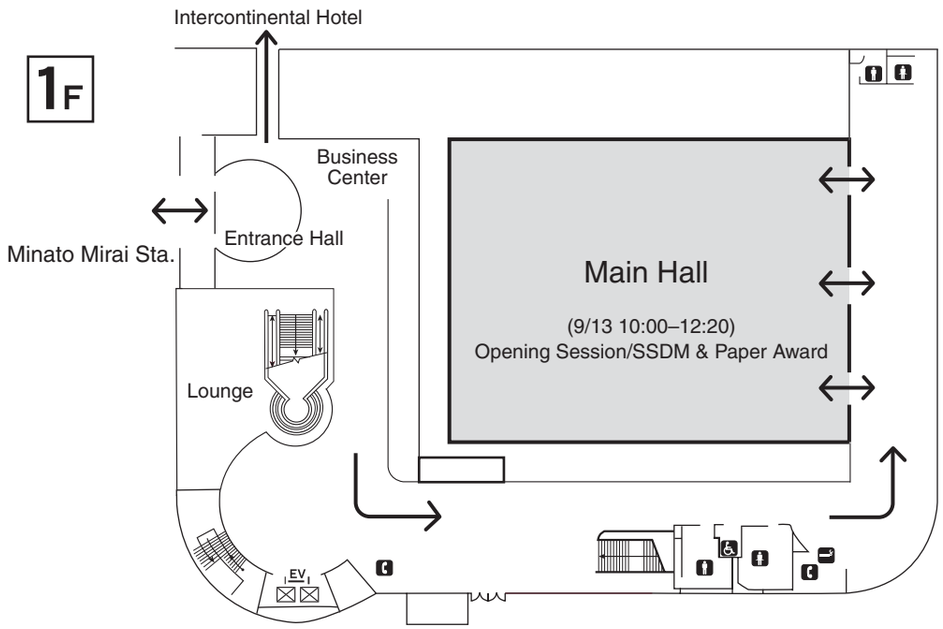

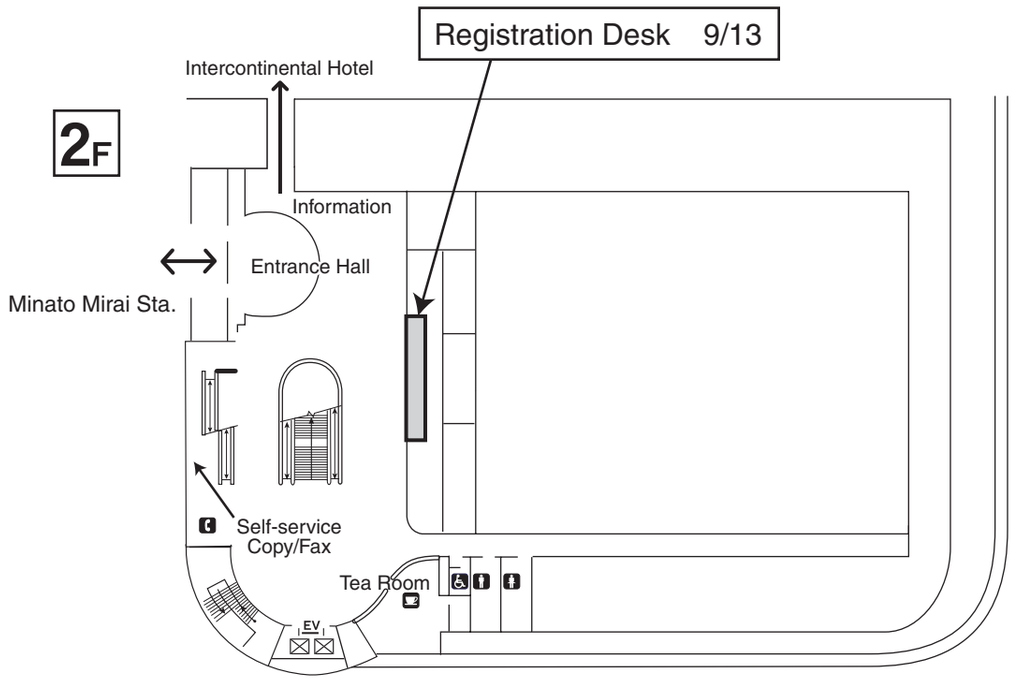

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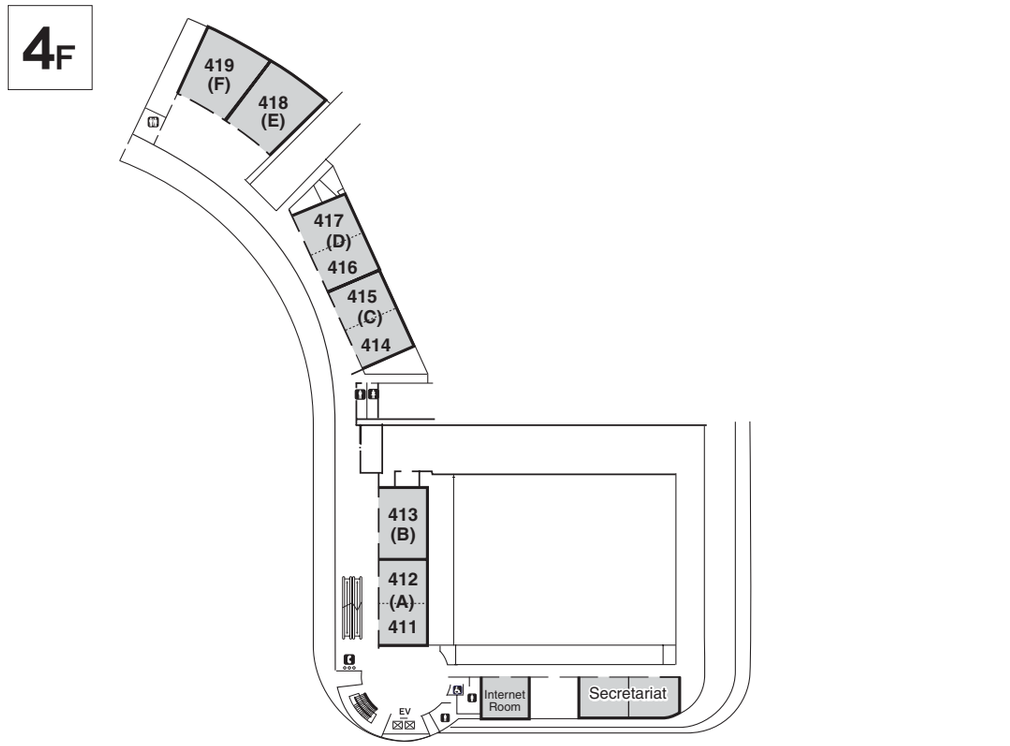

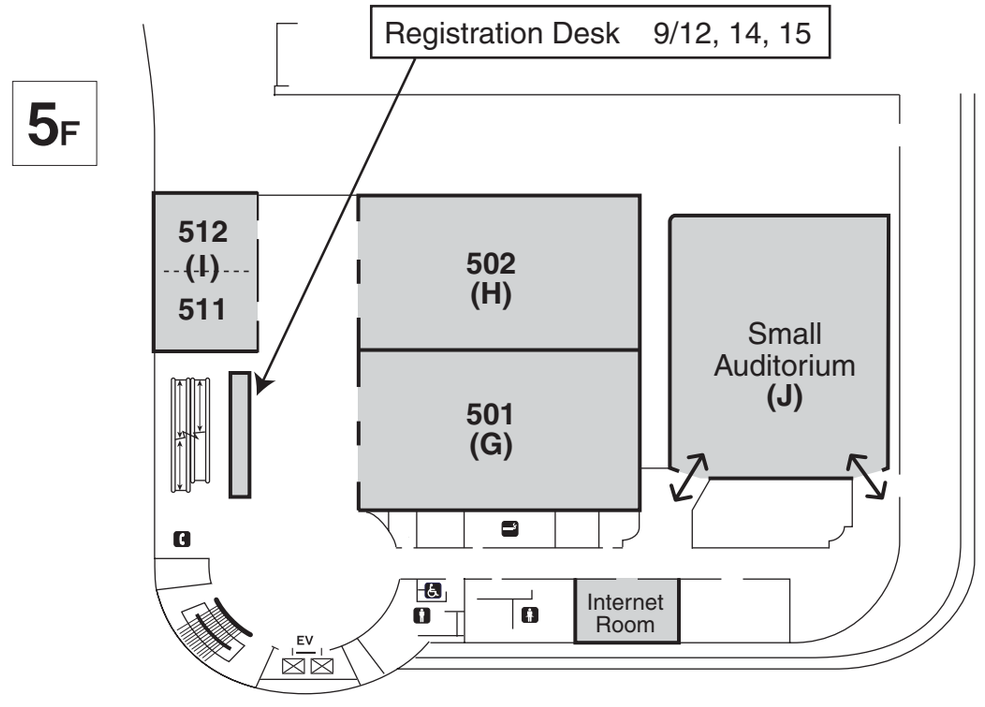

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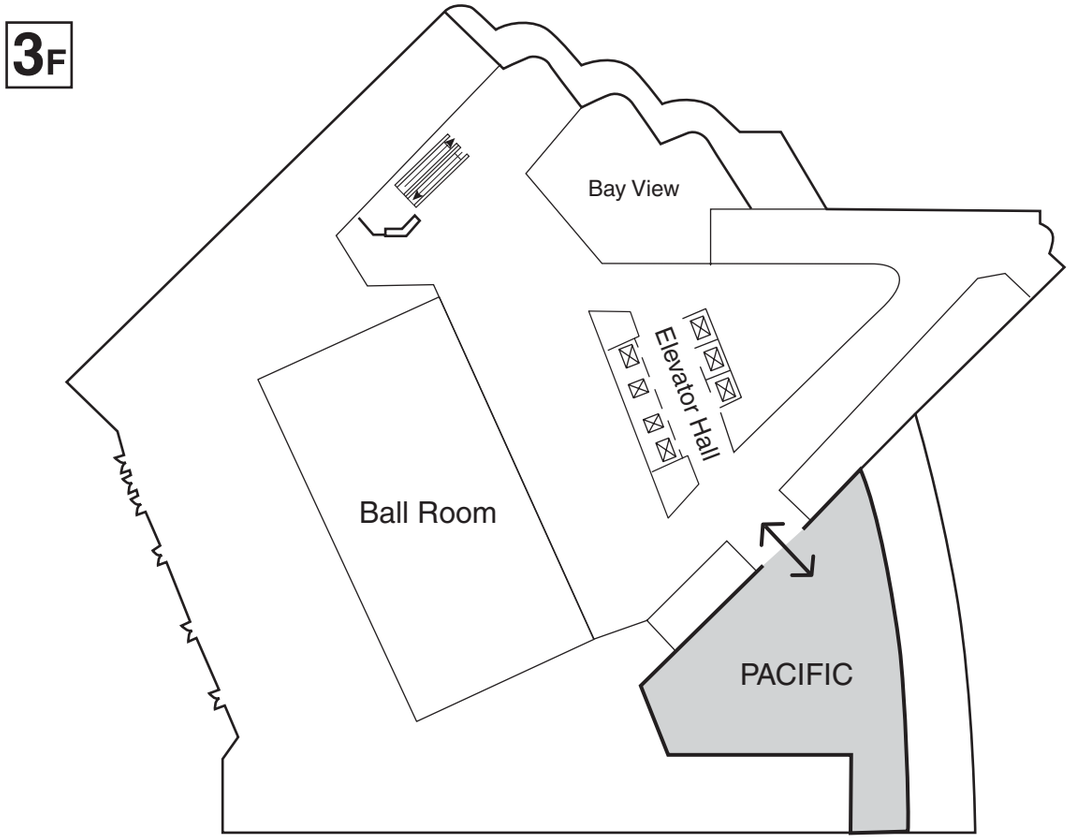

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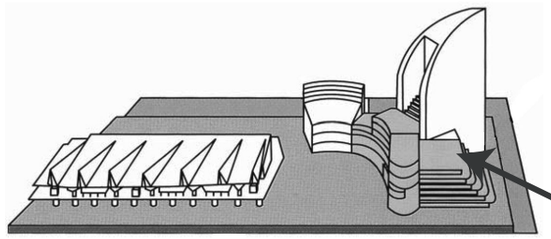

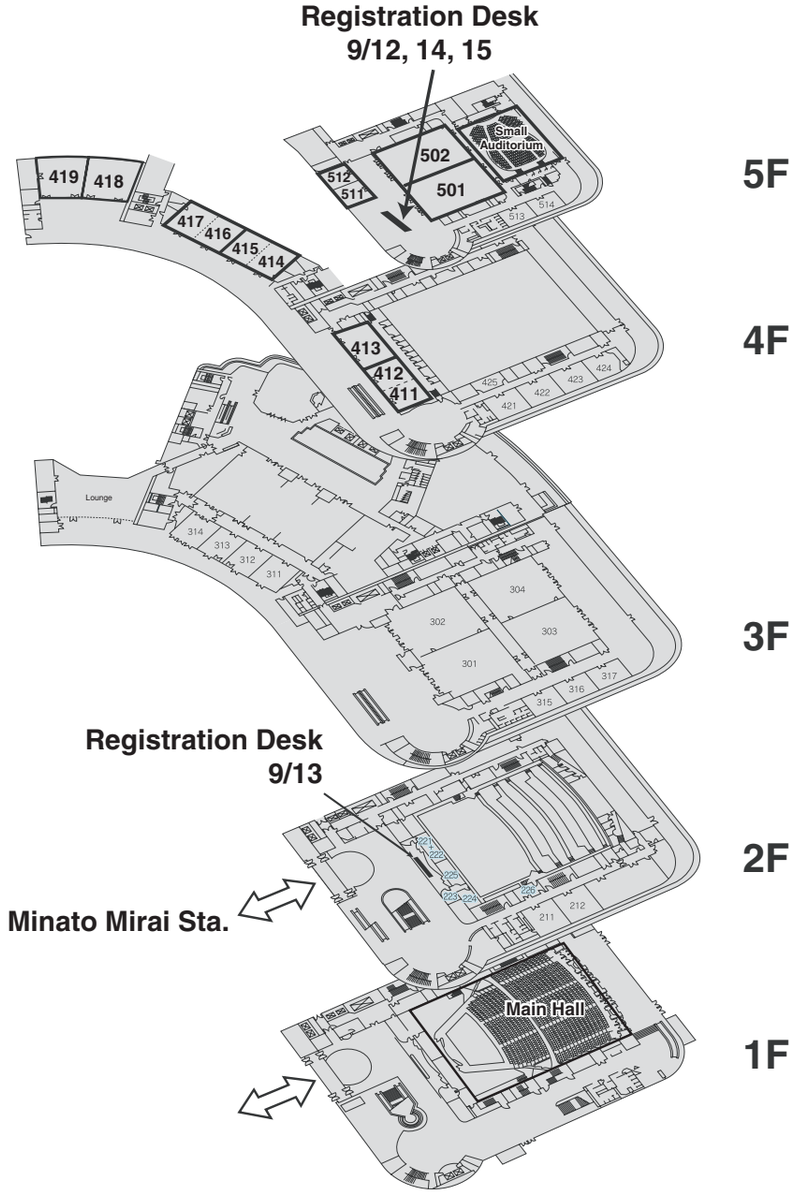

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