

ADVANCE PROGRAM

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INTERNATIONAL CONFERENCE ON

SOLID STATE

DEVICES AND MATERIALS



**2007 International Conference
on Solid State Devices and Materials (SSDM 2007)**

SECRETARIAT

c/o Inter Group Corp.
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1-7-2, Nishishimbashi, Minato-ku,
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Conference **September 19-21, 2007**

Short Course **September 18, 2007**

Place **Tsukuba International
Congress Center (Tsukuba, Ibaraki, Japan)**

Sponsored by
THE JAPAN SOCIETY OF APPLIED PHYSICS

Technical-Cosponsored by
IEEE Electron Devices Society

in cooperation with

The Electrochemical Society of Japan

IEEE EDS Japan Chapter

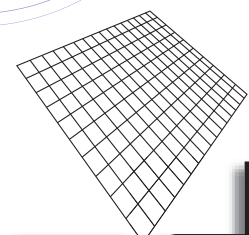
IEEE Japan Council

The Institute of Electrical Engineers of Japan

The Institute of Electronics, Information and Communication Engineers

The Institute of Image Information and Television Engineers

Japan Institute of Electronics Packaging



ssdm



ssdm
2007

Web Site : <http://www.ssdm.jp>

SSDM 2007 Time Table

Wednesday, September 19										
Main Convention Hall										
10:00-12:30 PL: Opening Session/SSDM Award										
Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
14:00-15:50 Area 1: Advanced Gate Stack /Si Processing Science A-1: Metal Gate-I	14:00-16:00 Area 3: CMOS Devices/Device Physics B-1: Ge, SiGe Channel Transistor Technology	14:00-15:50 Area 2: Characterization and Materials Engineering for Interconnect Integration C-1: Novel Interconnects	14:00-15:50 Area 5: Advanced Circuits and Systems D-1: Scaling and Circuit Design Concern	14:00-16:00 Area 7: Photonic Devices and Device Physics E-1: Quantum-Dot Devices	14:00-16:00 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-1: Compound Semiconductors	14:00-16:00 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-1: GaN FETs I	14:00-16:00 Area 10: Organic Materials Science, Device Physics, and Applications H-1: Organic Photo-Electronics	14:00-16:00 Area 9: Physics and Applications of Novel Functional Materials and Devices I-1: Novel Si Transistors	14:00-15:50 Area 4: Advanced Memory Technology J-1: DRAM I	
16:15-18:15 Area 1: Advanced Gate Stack /Si Processing Science A-2: Ge MIS	16:15-18:25 Area 3: CMOS Devices/Device Physics B-2: Transport in Nanoscale MOSFETs	16:15-17:30 Area 12: Spintronic Materials and Devices C-2: Spintronic Materials and Quantum Structures	16:15-18:15 Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) D-2: MEMS Technology	16:15-18:15 Area 7: Photonic Devices and Device Physics E-2: Special Session: Photonic Crystals and Si Photonics I	16:15-17:30 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-2: Oxides	16:15-18:00 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-2: GaN FETs II	16:15-18:00 Area 10: Organic Materials Science, Device Physics, and Applications H-2: Organic Light Emitting Devices	16:15-18:00 Area 9: Physics and Applications of Novel Functional Materials and Devices I-2: Transport Through Novel Materials and Structures	16:15-17:45 Area 4: Advanced Memory Technology J-2: Flash Memory I	
18:30-20:30 Banquet/Paper Award & Young Researcher Award (Multi-Purpose Hall 1F)										
Thursday, September 20										
Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
9:00-10:30 Area 1: Advanced Gate Stack /Si Processing Science A-3: Reliability-I	9:00-10:30 Area 3: CMOS Devices/Device Physics B-3: CMOS Integration	9:00-10:30 Area 2: Characterization and Materials Engineering for Interconnect Integration C-3: Plasma Induced Damage of Low-k Materials	9:00-10:20 Area 5: Advanced Circuits and Systems D-3: RF Components	9:00-10:30 Area 7: Photonic Devices and Device Physics E-3: Special Session: Photonic Crystals and Si Photonics II	9:00-10:15 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-3: Group-IV Semiconductors I	9:00-10:15 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-3: High-Speed Devices and ICs I	9:00-10:30 Area 13: Applications of Nanotubes and Nanowires H-3: Nanowire & Nanotube Sensors		9:00-10:20 Area 4: Advanced Memory Technology J-3: Flash Memory II	(Poster setting)
10:45-12:15 Short Presentation Area 1	10:45-12:15 Short Presentation Area 3	10:45-12:15 Short Presentation Area 2 and Area 12	10:45-12:15 Short Presentation Area 5 and Area 11	10:45-12:15 Short Presentation Area 7	10:45-12:15 Short Presentation Area 8	10:45-12:15 Short Presentation Area 6	10:45-12:15 Short Presentation Area 10 and Area 13	10:45-12:15 Short Presentation Area 9	10:45-12:15 Short Presentation Area 4	
13:00-15:00 Poster Session (Multi-Purpose Hall 1F)										
15:15-16:25 Area 1: Advanced Gate Stack /Si Processing Science A-5: Junction	15:15-16:35 Area 3: CMOS Devices/Device Physics B-5: Mobility Characterization	15:15-16:45 Area 12: Spintronic Materials and Devices C-5: Symposium on Magnetic Tunnel Junctions and Beyond	15:15-16:15 Area 5: Advanced Circuits and Systems D-5: RF CMOS Circuits and Systems	15:15-16:30 Area 7: Photonic Devices and Device Physics E-5: Special Session: Photonic Crystals and Si Photonics III	15:15-16:30 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-5: Group-IV Semiconductors II	15:15-16:15 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-5: High-Speed Devices and ICs II	15:15-16:30 Area 13: Applications of Nanotubes and Nanowires H-5: Nanowire Growth and Devices I		15:15-16:25 Area 4: Advanced Memory Technology J-5: PRAM	(Poster removed by 18:00)
16:45-18:05 Area 1: Advanced Gate Stack /Si Processing Science A-6: Reliability-II	16:45-18:05 Area 3: CMOS Devices/Device Physics B-6: Device Technology	17:00-18:00 Area 12: Spintronic Materials and Devices C-6: Symposium on Magnetic Tunnel Junctions and Beyond		16:45-18:00 Area 7: Photonic Devices and Device Physics E-6: Detectors and Sensors	16:45-17:45 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-6: Group-IV Semiconductors III	16:45-18:00 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-6: Process and Characterization	16:45-17:45 Area 13: Applications of Nanotubes and Nanowires H-6: Nanowire Growth and Devices II		16:45-17:55 Area 4: Advanced Memory Technology J-6: ReRAM	
18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-" Room 102(B) "New Materials meet Advanced Silicon Technology"										
Friday, September 21										
Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)	Multi-Purpose Hall (K)
9:00-10:30 Area 1: Advanced Gate Stack /Si Processing Science A-7: Metal Gate-II	9:00-10:20 Area 3: CMOS Devices/Device Physics B-7: Stress Enhancement Technologies	9:00-10:30 Area 2: Characterization and Materials Engineering for Interconnect Integration C-7: Interconnects for RF and Mixed Signal Application	9:00-10:30 Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) D-7: Nano-Bio Devices I	9:00-10:30 Area 7: Photonic Devices and Device Physics E-7: All-Optical Light Control	9:00-10:15 Area 8: Advanced Material Synthesis and Crystal Growth Technology F-7: Material Characterization	9:00-10:30 Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics G-7: Emerging Devices	9:00-10:30 Area 10: Organic Materials Science, Device Physics, and Applications H-7: Organic Transistor I		9:00-10:20 Area 4: Advanced Memory Technology J-7: DRAM II	
10:45-12:05 Area 1: Advanced Gate Stack /Si Processing Science A-8: High-k/Metal Gate Transistor	10:45-12:25 Area 3: CMOS Devices/Device Physics B-8: Modeling and Simulation	10:45-12:15 Area 2: Characterization and Materials Engineering for Interconnect Integration C-8: Interconnect Reliability	10:45-12:15 Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) D-8: Nano-Bio Devices II	10:45-12:15 Area 7: Photonic Devices and Device Physics E-8: Lasers and LEDs			10:45-12:15 Area 10: Organic Materials Science, Device Physics, and Applications H-8: Organic Transistor II	10:45-12:00 Area 9: Physics and Applications of Novel Functional Materials and Devices I-8: Novel Nanostructure Devices	10:45-12:05 Area 4: Advanced Memory Technology J-8: FeRAM/MRAM	
13:15-14:55 Area 1: Advanced Gate Stack /Si Processing Science A-9: FUSI	13:15-14:55 Area 3: CMOS Devices/Device Physics B-9: Post Planar CMOS	13:15-15:05 Area 2: Characterization and Materials Engineering for Interconnect Integration C-9: Low-k and Airgap	13:15-14:45 Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) D-9: Spectroscopy for Bio Sensing	13:15-15:00 Area 7: Photonic Devices and Device Physics E-9: LEDs	13:15-14:55 Area 1: Advanced Gate Stack/Si Processing Science F-9: Characterization	13:15-14:35 Area 5: Advanced Circuits and Systems G-9: Imaging Technology	13:15-14:45 Area 10: Organic Materials Science, Device Physics, and Applications H-9: Organic Transistor III	13:15-15:00 Area 9: Physics and Applications of Novel Functional Materials and Devices I-9: Quantum Dots and Qubits	13:15-15:00 Area 13: Applications of Nanotubes and Nanowires J-9: Carbon Nanotube Devices and Growth I	
	15:15-17:05 Area 3: CMOS Devices/Device Physics B-10: Noise and RF	15:25-16:25 Area 2: Characterization and Materials Engineering for Interconnect Integration C-10: Nanoscale Characterization	15:15-16:45 Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices) D-10: μ -TAS and Medical Applications		15:15-16:35 Area 1: Advanced Gate Stack/Si Processing Science F-10: Advanced Process	15:15-16:35 Area 5: Advanced Circuits and Systems G-10: Connectivity		15:15-16:45 Area 9: Physics and Applications of Novel Functional Materials and Devices I-10: Novel Devices	15:15-16:30 Area 13: Applications of Nanotubes and Nanowires J-10: Carbon Nanotube Devices and Growth II	

SSDM 2007 Advance Program General Information

DATE

Conference: **September 19-21, 2007 (Official language is English)**
Short Course: **September 18, 2007 (in Japanese)**

LOCATION

Tsukuba International Congress Center (EPOCHAL TSUKUBA)

2-20-3 Takezono, Tsukuba, Ibaraki, 305-0032, Japan
Phone: +81-29-861-0001 Fax: +81-29-861-1209

Tsukuba International Congress Center, located in Tsukuba Science City, is a core facility for research exchanges in Japan. People more than 2 million have visited the Center since its establishment in 1999, demonstrating the Center's great contribution to such exchanges. The Congress Center is located just 50 km from Tokyo and 40 km from Narita Airport. With the recent opening of the Tsukuba Express, Tsukuba can be accessed in 45 min from Akihabara, Tokyo.

<http://www.epocal.or.jp/index.html>

REGISTRATION

The registration desk will be open from September 18 to 21 in the entrance hall on the first floor. The registration hours are as follows:

September 18	9:00-17:00	Convention Hall (3F)
19	9:00-12:00	Main Convention Hall (1F)
19	12:00-17:00	Entrance Hall (1F)
20	9:00-17:00	Entrance Hall (1F)
21	9:00-15:30	Entrance Hall (1F)

Early registration will be accepted only through the conference website until August 17, 2007, 13:00

Japan time. (<http://www.ssdm.jp>)

Advanced registration through the conference website will be closed September 5, 2007, 17:00 Japan time. After the date, registration can be made at the conference site as on-site registration. Early registration is recommended.

	Registration Fee		Short Course (in Japanese)	Banquet
	Before 13:00, August 17 (Japan time)	After 13:00, August 17 (Japan time)		
Regular	JPY45,000	JPY50,000	JPY15,000	JPY7,000
Student	JPY7,000		JPY3,000	JPY4,000
Accompanied person				JPY4,000

* Fees include tax.

- 1) The registration fee includes one copy of the abstract book and a CD-ROM. However, it does not include the banquet, and an additional payment is required to attend the banquet (Regular: JPY7,000, Student/Accompanied person: JPY4,000).
- 2) Those who register as students are required to fax a copy of their current student ID to Kinki Nippon Tourist Co., Ltd. (KNT) (Fax: +81-3-5256-1588) at the time of registration and to present their student ID at the registration desk in order to be eligible for the student registration fee. When sending the fax, please write down your registration ID, which will be given at the completion of the online registration of individual information.
- 3) Registration is complete only after payment is made in full.

Payment Procedure

Payment can be made by:

- One of the following credit cards:
1. VISA 2. MasterCard 3. Diners Club 4. American Express 5. JCB
- A bank transfer to KNT Co., Ltd. (Message: SSDM)
Account at Sumitomo Mitsui Banking Corp., Suzuran Branch, 1-3-12 Nishishimbashi, Minato-ku, Tokyo 105-0003, Japan (SWIFT Code: SMBCJPJT, Ordinary Account: 6103515, Account Name: Kinki Nippon Tourist Co., Ltd.)

* Personal checks are not acceptable.

Confirmation of Pre-Registration

Upon receipt of your online registration, a written confirmation will be faxed or e-mailed to you after your payment is confirmed.

Please bring this confirmation slip with you and present it to the registration desk.

Registration Cancellation

Conference:

Cancellation fee of JPY3,000 will be deducted from the refund. Cancellation should be made in writing to KNT Co., Ltd. No cancellation will be accepted on or after August 21, 2007. Extended Abstracts will be sent to absent registrants after the conference.

Short Course:

Cancellation fee of JPY2,000 will be deducted from the refund. Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be accepted on or after August 21, 2007. Short-course textbooks will be sent to the absent registrants after the conference.

Banquet:

Cancellation fee of JPY1,000 will be deducted from the refund, Cancellations should be made in writing to KNT Co., Ltd. No cancellation will be accepted on or after August 21, 2007.

Inquiries for Registration

Kinki Nippon Tourist Co., Ltd. (KNT)
Global Business Management Branch
Tokyo Kintetsu Bldg. 6F
19-2 Kanda-Matsunaga-cho
Chiyoda-ku
Tokyo 101-8641, Japan
Phone: +81-3-5256-1581
Fax: +81-3-5256-1588
E-mail: ssdm2007-gb@or.knt.co.jp
Office hours: 9:30-17:30 (weekdays only)

On-site Registration

Registration fees should be paid in Japanese Yen or credit cards. VISA, MasterCard, Diners Club, American Express and JCB are acceptable. No personal checks are acceptable.

BANQUET

The conference banquet will be held on the evening of Wednesday, September 19. The banquet fee (Regular: JPY7,000, Student/Accompanied person: JPY4,000) is NOT included in the Registration fee. Participants who wish to attend the banquet are requested to order the banquet ticket through the on-line registration. Banquet tickets may also be purchased at the on-site registration desk.

LATE NEWS PAPERS

Submission of Late News Papers has been already closed on 24:00, July 30, 2007 (Japan time). The accepted papers will be on "Advance Program Part II" which will be distributed at the venue during the conference.

SPECIAL Issue of JJAP

Authors of papers presented at SSDM 2007 are encouraged to submit the original to the Special Issue of the Japanese Journal of Applied Physics, which will be published in April 2008.

RUMP SESSIONS - September 20 (Thursday) 18:30-20:30

Session A (Room 101, 1F)

“Oxide Electronics – Status and Outlook –”

Increasing interests on oxides are attracted by the rich possibilities and keen demands of metal-oxides as the key materials for future electronics. High-k oxides for alternative gate dielectrics and ferroelectric capacitors for non-volatile memories are well known examples for the SSDM community. Even more exciting applications are now being uncovered, from ultraviolet light emitting devices and high mobility thin film transistors through electric-control of magnetism in multiferroics to resistance change nonvolatile memories. Several keynotes will be delivered for the latter by panelists and near-future challenges in the emerging materials research will be discussed with the audience.

Organizer/Moderator: M. Kawasaki (Tohoku Univ., Japan)

Panelists: H. Akinaga (AIST, Japan)
T. Kamiya (Tokyo Tech., Japan)
H. Okamoto (Univ. of Tokyo, Japan)

A couple of panelists may be added.

Session B (Room 102, 1F)

“New Materials Meet Advanced Silicon Technology”

Scaling device dimensions has been the most powerful and effective strategy to boost device performance for last 40 years. In recent years, however, we face a number of obstacles to the effectiveness of this strategy. Unfortunately, some of the obstacles seem to be irremovable by evolving the traditional “silicon technology”. In fact, one might concern that some fundamental problems and limits reside in our traditional materials: Si, SiO₂, etc. Therefore, the introduction of materials which are/were new to researchers in silicon community is almost inevitable for enhancing device & LSI performance continuously (stepwise?) and for adding “new functionality” to LSIs in future, and will be a new vehicle, which takes us to a promised land (not a hell), where advanced LSIs improve our quality of life in many respects. In this rump session, we will discuss “new materials” for advanced silicon technology. Which materials will be used for which purposes, and when? What are criteria of introducing a certain material into LSIs? Can new or innovative materials (including nanoscale Si dots and wires) provide additional functionality to LSIs? By collaborating prominent panelists and audience, we will try to draw a private roadmap for new materials in LSIs. Particularly, we would like to encourage material specialists to join the discussion since the silicon technology really needs their help.

Organizer: H. Ishiuchi (Toshiba Corp., Japan)
Moderators: K. Uchida (Toshiba Corp., Japan)
F. Boeuf (ST Microelectronics, France)

Panelists: H. Watanabe (NEC Corp., Japan)
S. Takagi (Univ. of Tokyo, Japan)
T. Usui (Toshiba Corp., Japan)
A. S. Spinelli (Politecnico di Milano, Italy)
E. Y. Chang (National Chiao Tung Univ., Taiwan)
M. Mueller (NXP Semiconductors Research, Belgium)

One or two more panelists will be added.

SHORT COURSE

Short Course entitled “Emerging Silicon Technology” will be held on Tuesday, September 18 at Convention Hall (3F) . All lectures are given in Japanese.

AGREEMENT NOT TO PRE-PUBLISH ABSTRACTS

By submitting an abstract to the committee for review, the author(s) agrees that the work will not be published prior to presentation at the conference. Papers found to be in breach of this agreement will be withdrawn by the conference committee.

AWARDS

“SSDM Awards” will be given to outstanding papers presented at previous conferences.

SSDM Award

Given for an outstanding contribution to the field of solid state devices and materials, among papers presented prior to 2001.

SSDM Paper Award

Given for the best paper presented at the previous year’s conference.

SSDM Young Researcher Award

Given for outstanding papers authored by young researchers and presented at the previous year’s conference.

FINANCIAL SUPPORT

Limited financial support is available for presentations by full-time students. Student presenters who are interested in support should contact the secretariat directly (e-mail: ssdm@intergroup.co.jp) prior to the end of August after receiving their acceptance letter. A copy of their student ID should be submitted at application.

TRAVEL GRANT

A travel grant is available for young researchers under 35 years old from overseas universities or public research institutes. The grant is available only to those whose abstracts are accepted, and who have applied for the grant. Submitting an application form does not guarantee that the grant will be awarded. Each related area chair will choose one candidate from the applicants. Late news papers are not eligible for travel grant.

The grant is authorized by the Marubun Research Promotion Foundation (MRPF), which is one of the cooperation organizations. The grant covers part of the recipient’s travel costs, but does not necessarily cover all their expenses. Successful candidates must attend the ceremony which will be held during the conference (details of which will be given later) to receive the grant. Failure to attend will result in forfeiture of the grant.

VISA REQUIREMENT

All overseas participants must have a valid passport.

Overseas participants who require a visa should consult the nearest Japanese Embassy or Consulate as soon as possible. If your paper is accepted for presentation at SSDM 2007 and your visa application requires an invitation to attend the conference, please contact the SSDM Secretariat.

OFFICIAL TRAVEL AGENT

Kinki Nippon Tourist Co., Ltd. (KNT)

Global Business Management Branch

Tokyo Kintetsu Bldg. 6F, 19-2 Kanda-Matsunaga-cho, Chiyoda-ku

Tokyo 101-8641, JAPAN

Phone: +81-3-5256-1581 Fax: +81-3-5256-1588

E-mail: ssdm2007-gb@or.knt.co.jp

Hotel Accommodations

Rooms have been reserved at hotels around Conference venue (EPOCHAL TSUKUBA) by KNT. Hotel reservations are proceeded on first-come-first-served basis. If your selected hotel is fully booked, we will make a reservation at your second choice hotel. After application deadline, KNT will send a confirmation slip informing the confirmed hotel name, and the exact room charge. Reservations can be made through the conference website. (<http://www.ssdm.jp>)

Hotel Name	Okura Frontier Hotel Tsukuba
Room Rates	Single: JPY11,550 Twin: JPY10,500 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	1-1364-1, Azuma Tsukuba, Ibaraki 305-0031, Japan
Phone	+81-29-852-1112
Access to Hotel	2 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	6 min. walk

Hotel Name	Okura Frontier Hotel Tsukuba Epochal
Room Rates	Single: JPY11,550 Twin: JPY10,500 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:11:00
Address	2-20-1 Takezono, Tsukuba, Ibaraki 305-0032, Japan
Phone	+81-29-860-7700
Access to Hotel	8 min. walk from Tsukuba Sta. , A3 exit.
To Conference site	Next to the site

Hotel Name	Hotel Grand Shinonome
Room Rates	Single: JPY7,500
Hotel Deposit	JPY10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	488-1 Onozaki, Tsukuba, Ibaraki 305-0034, Japan
Phone	+81-29-856-2211
Access to Hotel	5 min. walk from Tsukuba Sta.
To Conference site	13 min. walk

Hotel Name	Hotel Route Tsukuba
Room Rates	Single: JPY6,825
Hotel Deposit	JPY10,000
Check-in/out	Check-in:15:00/Check-out:10:00
Address	1145-3 Hanamuro, Tsukuba, Ibaraki 305-0025, Japan
Phone	+81-29-860-2111
Access to Hotel	20 min. walk (or 5 min. by taxi) from Tsukuba Sta.
To Conference site	30 min. walk (or 10 min. by taxi)

Hotel Name	Tsukuba Daily Inn
Room Rates	Single: JPY6,930
Hotel Deposit	JPY10,000
Check-in/out	Check-in:16:00/Check-out:10:00
Address	1-12-4 Sengen, Tsukuba, Ibaraki 305-0047, Japan
Phone	+81-29-851-0003
Access to Hotel	30 min. walk (or 7 min. by taxi) from Tsukuba Sta.
To Conference site	15 min. walk (or 3 min. by taxi)

Hotel Name	Akihabara Washington Hotel
Room Rates	Single: JPY11,550 Twin: JPY8,925 (per person, per night)
Hotel Deposit	JPY20,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-8-3 Sakumacho, Kanda, Chiyoda-ku, Tokyo 101-0025, Japan
Phone	+81-3-3255-3311
Access to Hotel	1 min. walk from Tsukuba Express Akihabara Sta.
To Conference site	45 min. by Tsukuba Express and 8 min. walk

Hotel Name	Asakusa View Hotel
Room Rates	Single: JPY15,693
Hotel Deposit	JPY20,000
Check-in/out	Check-in:13:00/Check-out:11:00
Address	3-17-1 Nishi-Asakusa, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1111
Access to Hotel	1 min. walk from Tsukuba Express Asakusa Sta.
To Conference site	40 min. by Tsukuba Express and 8 min. walk

Hotel Name	Hotel Sunroute Asakusa
Room Rates	Single: JPY9,500
Hotel Deposit	JPY10,000
Check-in/out	Check-in:14:00/Check-out:10:00
Address	1-8-5 Kaminarimon, Taito-ku, Tokyo 111-8765, Japan
Phone	+81-3-3847-1511
Access to Hotel	5 min. walk from Tsukuba Express Asakusa Sta.
To Conference site	40 min. by Tsukuba Express and 8 min. walk

Hotel Name	Tsukuba Kenshu Center
Room Rates	Single: JPY4,900 Single with breakfast: JPY5,300
Hotel Deposit	The payment in full for your room charge
Check-in/out	Check-in:16:00(no later than 23:00)/Check-out:10:00
Address	1-13-5 Amakubo, Tsukuba, Ibaraki 305-0005, Japan
Phone	+81-29-851-5152
Access to Hotel	10 min. by bus and 10 min. walk from Tsukuba Sta.
To Conference site	10 min. walk and 15 min. by bus

- Notes: 1) All room rates are per person per night including breakfast and 10% service charge, but excluding consumption tax.
2) The above rates are valid only during the period of the SSDM 2007 meeting.
3) Communication fee of 500 JPY is required for per reservation and this is charged as handling charge for KNT.
4) The deposit will be deducted from your hotel bill. Please settle the balance with the hotel cashier.
5) The above rates and information are subject to change without notice.
6) It is excluding breakfast in room charge at Tsukuba Kenshu Center. More information, please contact to KNT.

Application and Payment

Participants wishing to reserve hotel accommodations should access the Registration and Accommodation pages of the conference website. The page will be opened in early June and hotel reservations should be made by no later than August 18, 2007 (Japan time). A confirmation sheet will be sent by KNT after the application deadline.

Application should be accompanied by the payment of room deposit and communication fee of 500 JPY.

No reservation will be confirmed in the absence of this payment. All payment must be paid only in Japanese yen by one of the following methods.

- 1) Credit Card:
(VISA, MasterCard, Diners Club, American Express or JCB only)
* Please fill in the necessary items with your signature in the credit card section of the application form.
- 2) Bank Transfer:
Sumitomo Mitsui Banking Corp.
Suzuran Branch
SWIFT Code: SMBCJPJT
Ordinary Account: 6103515
Account Name: Kinki Nippon Tourist Co., Ltd.

Cancellation Policy for Accommodations

In case of cancellation, a written notification should be sent to KNT by e-mail (ssdm2007-gb@or.knt.co.jp) or by FAX (+81-3-5256-1588) to avoid any trouble.

Hotels: Up to 14 days before the arrival date No Charge
13-7 days before 10 % of daily room charge
6-2 days before 40 % of daily room charge
Less than 2 days, or no notice given . 100 % of daily room charge

INSURANCE

The organizer cannot accept responsibility for accidents that may occur during a delegate's stay. Delegates are therefore encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home countries prior to departure.

CLIMATE

Tsukuba is warm and sometimes humid in September. The temperature range is 18-30°C .

ELECTRICAL APPLIANCES

Japan operates on 100 volts for electrical appliances. The frequency is 50 Hz in eastern Japan including Tsukuba (conference site) and Tokyo, and 60 Hz in western Japan including Kyoto and Osaka.

SSDM 2007 INSTRUCTION for SPEAKERS

Oral Presentation

Time Schedule

	Session Time	Presentation	Discussion
Plenary	40 min.	35 min.	5 min.
Invited	30 min.	25 min.	5 min.
Regular-1	20 min.	17 min.	3 min.
Regular-2	15 min.	12 min.	3 min.

Buzzer First: Warning, Second: End of speech , Third: End of discussion.

Audio-Visual Equipment

The meeting rooms will contain the following audiovisual equipment:

- LCD projector (**PC itself is not provided**)
- Microphone
- Projection laser pointer

Speakers wishing to present their papers using the LCD projector are requested to verify their PC's compatibility with the LCD projector that will be located in the Preview Room (402) on the fourth floor prior to their presentations.

Poster Presentation

Poster sessions are scheduled for Thursday, September 20, from 13:00 to 15:00 at Multi-Purpose Hall(1F). Poster boards will be available with identifying labels at Multi-Purpose Hall on the first floor. Authors are requested to prepare their posters between 9:00 and 12:00 on September 20 and remove them by 18:00 on September 20. Any posters remaining after 18:00 will be disposed of by the secretariat. Usable space on each poster board will be approximately 900 mm wide and 1,500 mm high. Pushpins will be available. Each presentation will be assigned a board, labeled with the paper number. Please display the paper title, author names and affiliations on the poster. Authors are requested to stay near their posters during the poster session for discussions.

Short Oral Presentation for Poster Presenters

All poster presenters are required to make 2 minutes short oral presentation of September 20. The presentation time should be kept strictly to 2 minutes per poster presentation, including the time needed to move on to the next speaker. To ensure the session progresses smoothly, it is essential that these short presentations be held in a quick, successive sequence. While one speaker is giving his/her presentation, the next several speakers should wait nearby in line for their turn in order to move on to the next presentation. Note that any absent speakers will be skipped and each presentation will be automatically stopped after 2 minutes have elapsed. Only a PC projector will be made available. You should send your presentation file to the secretariat (ssdm2007-abs@intergroup.co.jp) by e-mail by August 24. The file must be an exact "2-page" landscape PDF. Because the presentation time is limited, please describe your research objective and results clearly and do NOT show the author list or the title on your file, those of which will be prepared by the SSDM Secretariat.

Short oral presentations will be held, as follows.

Room 101	Area 1		
Room 102	Area 3	Room 303	Area 6
Room 201A	Area 2, 12	Room 304	Area 10, 13
Room 201B	Area 5, 11	Room 405	Area 9
Room 202A	Area 7	Room 406	Area 4
Room 202B	Area 8		

PL: Opening Session (10:00-12:30)

Chairpersons: Y. Awano, Fujitsu Labs. Ltd. and S. Zaima, Nagoya Univ.

10:00 PL-0

Welcome Address and Award Presentation

N. Yokoyama, Fujitsu Labs. Ltd.

10:30 PL-1

New Technology: Silicon Photonics: Opportunity, Challenges & Applications

M. Paniccia, Intel Corp., USA

11:10 PL-2

Organic Transistors: towards Ambient Electronics

T. Someya, Univ. of Tokyo, Japan

11:50 PL-3

Try Disruptive Technology!

H. Watanabe, Selete Inc., Japan

12:30-14:00 Lunch

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)	Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics	Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
A-1: Metal Gate-I (14:00-15:50) Chairs: Y. Nara (Selete) J. Yugami (Renesas Tech. Corp.)	B-1: Ge, SiGe Channel Transistor Technology (14:00-16:00) Chairs: J. C. S. Woo (Univ. of California, Los Angeles) Y. Momiyama (Fujitsu Labs. Ltd.)	C-1: Novel Interconnects (14:00-15:50) Chairs: T. Yoda (Toshiba Corp.) M. Nihei (Fujitsu Labs. Ltd.)	D-1: Scaling and Circuit Design Concern (14:00-15:50) Chairs: H. Kobayashi (Gunma Univ.) T. Komuro (Agilent Technologies International Japan, Ltd.)	E-1: Quantum-Dot Devices (14:00-16:00) Chairs: M. Sugawara (Fujitsu Labs. Ltd.) M. Tokushima (NEC Corp.)	F-1: Compound Semiconductors (14:00-16:00) Chairs: M. Takahashi (JAEA) T. Fukui (Hokkaido Univ.)	G-1: GaN FETs I (14:00-16:00) Chairs: S. Tanaka (NEC Corp.) M. Kuzuhara (Univ. of Fukui)	H-1: Organic Photo-Electronics (14:00-16:00) Chairs: H. Usui (Tokyo Univ. of Agri. and Tech.) H. Kajii (Osaka Univ.)	I-1: Novel Si Transistors (14:00-16:00) Chairs: Y. Takahashi (Hokkaido Univ.) Y. Suda (Tokyo Univ. of Agri. and Tech.)	J-1: DRAM I (14:00-15:50) Chairs: I. Asano (Elpida Memory, Inc.) H. Jeong (Samsung Electronics Co., Ltd.)

※ Country of first author's affiliation is shown in parentheses.

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
14:00 A-1-1 (Invited) Challenges for PMOS metal gate electrodes and solutions for low power applications J. Schaeffer, <i>Freescale Semiconductor Inc. (USA)</i>	14:00 B-1-1 High mobility Ge channel metal source/drain pMOSFETs with nickel fully silicided gate K. Ikeda ¹ , N. Taoka ² , Y. Yamashita ¹ , M. Harada ¹ , K. Suzuki ¹ , T. Yamamoto ¹ , N. Sugiyama ¹ and S. Takagi ^{2,3} , ¹ MIRAI-ASET, ² MIRAI-ASRC and ³ Univ. of Tokyo (Japan)	14:00 C-1-1 (Invited) Si-Based Infrared Light Emitters Using Semiconducting Iron Disilicide T. Suemasu, S. Murase, Y. Ugajin and M. Suzuno, <i>Univ. of Tsukuba (Japan)</i>	14:00 D-1-1 (Invited) Next generation compact model for digital and analog circuit design T. Ohguro, <i>Toshiba Corp. (Japan)</i>	14:00 E-1-1 (Invited) High-Speed Quantum Dot Lasers P. Bhattacharya and Z. Mi, <i>Univ. of Michigan (USA)</i>
14:30 A-1-2 PMOSFET Vth Modulation Technique using Fluorine Treatment through ALD-TiN Suitable for CMOS Devices K. Tai, S. Yamaguchi, K. Tanaka, T. Hirano, I. Oshiyama, S. Kazi, T. Ando, M. Nakata, M. Yamanaka, R. Yamamoto, S. Kanda, Y. Tateshita, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, N. Nagashima and S. Kadomura, <i>Sony Corp. (Japan)</i>	14:20 B-1-2 Integration of Dual Channels MOSFET on Defect-Free, Tensile-Strained Germanium on Silicon H. Zang ^{1,2} , W. Y. Loh ² , J. D. Ye ² , T. H. Loh ² , G. Q. Lo ² and B. J. Cho ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)	14:30 C-1-2 Electrical properties of carbon nanotubes grown at a low temperature by radical chemical vapor deposition for future LSI interconnects D. Yokoyama ¹ , K. Ishimaru ¹ , T. Iwasaki ¹ , S. Sato ² , T. Hyakushima ² , M. Nihei ² , Y. Awano ² and H. Kawarada ¹ , ¹ Waseda Univ. and ² MIRAI-Selete (Japan)	14:30 D-1-2 (Invited) Characterization and modeling of layout dependent parametric variability of nanometer devices C. Guardiani, <i>PDF Solutions (Italy)</i>	14:30 E-1-2 (Invited) MOCVD Growth of Quantum-Dot Optical Devices K. Kawaguchi ¹ , N. Yasuoka ¹ , M. Ekawa ¹ , H. Ebe ² , T. Akiyama ³ , M. Sugawara ^{1,3} and Y. Arakawa ² , ¹ Fujitsu Labs. Ltd., ² Univ. of Tokyo and ³ QD Laser Inc. (Japan)

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
14:00 F-1-1 (Invited) InAs/In(Ga,Al)AsSb Quantum Dot Heterostructures for Photonic Devices J. I. Chyi ^{1,2} , P. C. Chiu ¹ , M. J. Shiau ¹ , T. P. Hsieh ¹ and M. N. Chang ³ , ¹ National Central Univ., ² Academic Sinica and ³ National Nano Device Labs. (Taiwan)	14:00 G-1-1 (Invited) Next Generation High-Efficiency RF Transmitter Technology for Basestations P. Asbeck ¹ , D. Kimball ¹ , J. Jeong ² , P. Draxler ¹ , C. Hsia ¹ and L. Larson ¹ , ¹ Univ. of California, San Diego and ² Kwangwoon Univ. (USA)	14:00 H-1-1 (Invited) Plastic dye-sensitized solar cells and solidification with nano-carbon materials T. Miyasaka ^{1,2} , ¹ Toin Univ. of Yokohama and ² Peccell Tech., Inc. (Japan)	14:00 I-1-1 (Invited) 3D Stacked Nanowires CMOS Integration with a Damascene Finfet Process T. Ernst ¹ , C. Dupré ^{1,2} , E. Dornel ¹ , J. C. Barbé ¹ , S. Bécu ¹ , C. Vizioz ¹ , V. Delaye ¹ , F. Andrieu ¹ , J. M. Hartmann ¹ , S. Barnola ¹ , T. Poiroux ¹ , O. Faynot ¹ , G. Ghibaudo ² and S. Deleonibus ¹ , ¹ CEA-LETI and ² IMEP (France)	14:00 J-1-1 (Invited) Overview and Future Challenges of Floating Body RAM Technologies T. Shino, T. Ohsawa, T. Hamamoto and A. Nitayama, <i>Toshiba Corp. (Japan)</i>
14:30 F-1-2 (Invited) Present Status and Future Issues of III-V Semiconductor Nanowires K. Hiruma, M. Yazawa, K. Haraguchi, K. Ogawa and T. Katsuyama, <i>Hitachi, Ltd. (Japan)</i>	14:30 G-1-2 Normally-off AlGaIn/GaN MIS-HFETs Using Non-polar a-Plane M. Kuroda, T. Ueda and T. Tanaka, <i>Matsushita Electric Industrial Co., Ltd. (Japan)</i>	14:30 H-1-2 Efficiency Improvement of Organic Solar Cells by Annealing for Active Layer C. K. Chen, Y. S. Tsai, W. P. Chu, L. W. Ji and T. H. Meen, <i>National Formosa Univ. (Taiwan)</i>	14:30 I-1-2 3D Multi-gate NMOS Mobility Enhancement with High-tensile ILD-SiN _x Stressor W. S. Liao ¹ , S. Y. Huang ¹ , K. M. Chen ² , H. C. Tsen ¹ and L. Chung ¹ , ¹ UMC and ² National Nano Device Labs. (Taiwan)	14:30 J-1-2 URCAT (U-shaped-Recess-Channel-Array Transistor) Technology for 60nm DRAM and beyond C. Lee, J. C. Park, S. H. Park, S. S. Lee, S. D. Hong, I. G. Kim, Y. J. Choi, T. W. Lee, G. Y. Jin and K. Kim, <i>Samsung Electronics Co., Ltd. (Korea)</i>

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
14:50 A-1-3 Low Threshold Voltage Gate-First pMISFETs with Poly-Si/TiN/HfSiON Stacks Fabricated with PVD-based In-situ Solid Phase Interface Reaction (SPIR) Method N. Kitano ^{1,3} , H. Arimura ¹ , S. Horie ¹ , T. Hosoi ¹ , T. Shimura ¹ , H. Watanabe ¹ , T. Kawahara ² , S. Sakashita ² , Y. Nishida ² , J. Yugami ² , T. Minami ³ and M. Kosuda ³ , ¹ <i>Osaka Univ.</i> , ² <i>Renesas Tech. Corp.</i> and ³ <i>Canon ANELVA Corp. (Japan)</i>	14:40 B-1-3 Electrical Stress Effects on Mobility of Germanium-On-Insulator (GeOI) pMOSFETs with HfO ₂ Gate Dielectric J. H. Yi, S. Oh and H. S. P. Wong, <i>Stanford Univ. (USA)</i>	14:50 C-1-3 Carbon Nanotube Vias Fabricated by Remote Plasma-Enhanced Chemical Vapor Deposition M. Katagiri, N. Sakuma, M. Suzuki, T. Sakai, S. Sato, T. Hyakushima, M. Nihei and Y. Awano, <i>MIRAI-Selete (Japan)</i>	15:10 D-1-3 Investigation of Matching Performance for Uniaxial Strained PMOSFETs J. J. Y. Kuo, W. P. N. Chen and P. Su, <i>National Chiao Tung Univ. (Taiwan)</i>	15:00 E-1-3 First Demonstration of Electrically Driven 1.55 μm Single-Photon Generator T. Miyazawa ¹ , S. Hirose ² , S. Okumura ² , K. Takemoto ² , M. Takatsu ² , T. Usuki ¹ , N. Yokoyama ² and Y. Arakawa ¹ , ¹ <i>Univ. of Tokyo</i> and ² <i>Fujitsu Labs. Ltd. (Japan)</i>
15:10 A-1-4 Achieving Band Edge Effective Work Function of Gate First Metal Gate by Oxygen Anneal Processes: Low Temperature Oxygen Anneal (LTOA) and High Pressure Oxygen Anneal (HPOA) Processes C. S. Park ¹ , S. C. Song ¹ , C. Burham ² , H. B. Park ³ , H. Niimi ⁴ , B. S. Ju ¹ , J. Barnett ¹ , C. Y. Kang ¹ , P. Lysaght ¹ , G. Bersuker ¹ , R. Choi ¹ , H. K. Park ⁵ , H. Hwang ⁵ , B. H. Park ⁶ , S. Kim ⁶ , P. Kirsch ⁷ , B. H. Lee ⁷ and R. Jummy ⁷ , ¹ <i>SEMATECH</i> , ² <i>Univ. of Texas at Austin</i> , ³ <i>Samsung Assigner</i> , ⁴ <i>TI Assignee</i> , ⁵ <i>GIST</i> , ⁶ <i>Poongsan Microtec</i> and ⁷ <i>IBM (USA)</i>	15:00 B-1-4 Pt-germanide Formed by Laser Annealing and Its Application for Schottky Source/Drain MOSFET Integrated with TaN/CVD-HfO ₂ /Ge Gate Stack R. Li ¹ , S. J. Lee ¹ , D. Z. Chi ² , M. H. Hong ¹ and D. L. Kwong ³ , ¹ <i>National Univ. of Singapore</i> , ² <i>Inst. of Materials Research and Engineering</i> and ³ <i>Inst. of Microelectronics (Singapore)</i>	15:10 C-1-4 A Novel Contact-plug Process with Low Resistance Nucleation Layer Using B ₂ H ₆ -reduction W-ALD Method for 32 nm CMOS Devices and Beyond A. Yutani, K. Ichinose, K. Maekawa, K. Asai and M. Kojima, <i>Renesas Tech. Corp. (Japan)</i>	15:30 D-1-4 Novel Soft Error Hardened Latches and Flip-Flops T. Uemura, R. Tanabe, Y. Tosaka and S. Satoh, <i>Fujitsu Labs. Ltd. (Japan)</i>	15:15 E-1-4 Electroluminescence from Multiple-Stacked Structures of Impurity Doped Si Quantum Dots K. Okuyama, K. Makihara, M. Ikeda, S. Higashi and S. Miyazaki, <i>Hiroshima Univ. (Japan)</i>

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
15:00 F-1-3 In situ Metal Mask for Selective Area Growth of Thin Epitaxial Layers S. Ohkouchi ^{1,2} , N. Ozaki ³ , Y. Takata ³ , Y. Kitagawa ³ , Y. Nakamura ⁴ , N. Ikeda ⁵ , Y. Sugimoto ^{3,5} and K. Asakawa ³ , ¹ <i>AIST</i> , ² <i>NEC Corp.</i> , ³ <i>Univ. of Tsukuba</i> , ⁴ <i>Kumamoto Univ.</i> and ⁵ <i>NIMS (Japan)</i>	14:45 G-1-3 Gain Improvement of Enhancement-mode AlGaIn/GaN HEMTs Using Dual-Gate Architectures R. Wang, Y. Wu, W. C. W. Tang, K. M. Lau and K. J. Chen, <i>Hong Kong Univ. of Sci. and Tech. (China)</i>	14:45 H-1-3 Surface Plasmon Excitation and Emission Light properties for Prism/MgF ₂ /Ag/MEH-PPV Film Structure K. Shinbo, M. Hafuka, M. Minagawa, Y. Ohdaira, A. Baba, K. Kato and F. Kaneko, <i>Niigata Univ. (Japan)</i>	14:45 I-1-3 The Drivability Enhancement Mechanisms in Nano-grating MOSFETs X. Zhu ¹ , S. Kuroki ¹ , K. Kotani ¹ , M. Fukuda ² , H. Shido ² , Y. Mishima ² and T. Ito ¹ , ¹ <i>Tohoku Univ.</i> and ² <i>Fujitsu Labs. Ltd (Japan)</i>	14:50 J-1-3 RC-FinFET (Recessed Channel FinFET) Cell Transistor Technology for Future Generation DRAMs M. Yoshida, J. R. Kahng, J. S. Moon, K. H. Jung, K. Kim, H. Sung, C. Lee, C. K. Kim, W. Yang and D. Park, <i>Samsung Electronics Co., Ltd. (Korea)</i>
15:15 F-1-4 Optimization of Well Width and of N Composition on Optical Properties for GaNAs/GaAs MQW grown by RF-MBE K. Fujii ¹ , D. Nakase ¹ , T. Kumamoto ¹ , Y. Iwata ¹ , N. Tsurumachi ¹ , H. Miyagawa ¹ , H. Itoh ¹ , S. Nakanishi ¹ , H. Akiyama ² and S. Koshihara ¹ , ¹ <i>Kagawa Univ.</i> and ² <i>Univ. of Tokyo (Japan)</i>	15:00 G-1-4 p-type InGaN Cap Layer for Normally-off Operation in AlGaIn/GaN HFETs M. Shimizu ¹ , G. Piao ¹ , M. Inada ¹ , H. Okumura ¹ , Y. Yano ² and N. Akutsu ² , ¹ <i>AIST</i> and ² <i>Taiyo Nippon Sanso Corp. (Japan)</i>	15:00 H-1-4 Fabrication of Dual-disks Microlasers in Thiophene/Phenylene Co-oligomers F. Sasaki ¹ , S. Kobayashi ¹ , S. Haraichi ¹ , S. Fujiwara ² , Y. Ido ² , K. Bando ² , Y. Masumoto ² and S. Hotta ³ , ¹ <i>AIST</i> , ² <i>Univ. of Tsukuba</i> and ³ <i>Kyoto Inst. of Tech. (Japan)</i>	15:00 I-1-4 Low Contact Resistance with Low Schottky Barrier for N-type Silicon Using Yttrium Silicide T. Isogai, H. Tanaka, T. Goto, A. Teramoto, S. Sugawa and T. Ohmi, <i>Tohoku Univ. (Japan)</i>	15:10 J-1-4 Investigation on the Body Bias Dependency of Gate Induced Drain Leakage Current in the Body-Tied finFET C. Lee, M. Yoshida, K. H. Jung, C. K. Kim, H. J. Kim, H. Park, W. S. Lee, K. Kim, J. Kahng, W. Yang and D. Park, <i>Samsung Electronics Co., Ltd. (Korea)</i>

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration		Area 7: Photonic Devices and Device Physics
15:30 A-1-5 Gate First PFET Poly-Si/TiN/Al ₂ O ₃ Gate Stacks with Inversion Thicknesses Less than 15Å for High Performance or Low Power CMOS Applications B. P. Linder, V. Narayanan, V. K. Paruchuri, E. Cartier and S. Kanakasabapathy, <i>IBM (USA)</i>	15:20 B-1-5 Silicon Strain-Transfer-Layer (STL) and Graded Source/Drain Stressors for Enhancing the Performance of Silicon-Germanium Channel P-MOSFETs G. H. Wang ¹ , E. H. Toh ¹ , K. M. Hoe ¹ , S. Tripathy ¹ , S. Balakumar ¹ , G. Q. Lo ² , G. Samudra ¹ and Y. C. Yeol ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)	15:30 C-1-5 Plasma-Enhanced ALD Ru Thin Films on PVD-TaN Films with Smooth Morphology at Low Temperature Using DER Ru Precursor K. Namba ¹ , N. Hosoi ¹ , N. Tarumi ¹ , H. Shinriki ² and S. Ogawa ¹ , ¹ Selete and ² ASM Japan K.K. (Japan)		15:30 E-1-5 Electric-field control of coupled states in weakly coupled quantum dots I. Morohashi, K. Komori, K. Goshima, T. Sugaya, S. Yamauchi and A. Shikanai, ¹ AIST and ² CREST-JST (Japan)
	15:40 B-1-6 New Observations on the Narrow Width Effect of the Hot Carrier and NBTI Reliabilities in pMOSFETs with Various Types of Strains S. S. Chung ¹ , D. C. Huang ² , C. S. Lai ² , C. H. Tsai ³ , P. W. Liu ³ , Y. H. Lin ³ , C. T. Tsai ³ , G. H. Ma ³ , S. C. Chien ³ and S. W. Sun ³ , ¹ National Chiao Tung Univ., ² Chang Gung Univ. and ³ UMC (Taiwan)			15:45 E-1-6 Improvement in Characteristics of InGaAs/GaAs Quantum-Dot PIN Photodetectors with Antireflection Photonic Crystals J. J. Chen, Y. K. Su, R. W. Chuang, H. C. Yu, W. C. Chen, K. Y. Cheng and T. H. Shen, <i>National Cheng Kung Univ. (Taiwan)</i>

Wednesday, September 19

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
15:30 F-1-5 Formation of InGaAs-On-Insulator Structures by Epitaxial Lateral Over Growth from (111) Si T. Hoshii ¹ , M. Deura ¹ , M. Shichijo ¹ , M. Sugiyama ¹ , S. Sugahara ² , M. Takenaka ¹ , Y. Nakano ¹ and S. Takagi ¹ , ¹ Univ. of Tokyo and ² Tokyo Tech. (Japan)	15:15 G-1-5 Finger Length Optimization for AlGaIn/GaN HEMT and InGaP/GaAs HBT by Using FDTD Electromagnetic and Device Co-Simulation Technique A. Chokki, Y. Shinohara, R. Ishikawa and K. Honjo, <i>Univ. of Electro-Communications (Japan)</i>	15:15 H-1-5 Orientational Re-ordering of Polar Organic Monolayers by Cooperative Molecular Field Effect D. Taguchi, N. Kajimoto, T. Manaka and M. Iwamoto, <i>Tokyo Tech. (Japan)</i>	15:15 I-1-5 Double-Spacer Impact-ionization MOS Transistor: Characterization and Analysis E. H. Toh ¹ , G. H. Wang ¹ , G. Q. Lo ² , L. Chan ¹ , G. Samudra ¹ and Y. C. Yeol ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)	15:30 J-1-5 The Effect of Radical Oxidation on DRAM Cell Transistor with S-RCAT S. G. Park, S. H. Joe, J. H. Kim, H. S. Song, I. D. Choi, S. H. Han, Y. S. Ahn, S. B. Park, J. S. Lee, S. N. Kim, W. T. Choi, K. J. Kim and K. S. Oh, <i>SamSung Electronics Co., Ltd. (Korea)</i>
15:45 F-1-6 Growth of GaN on Si (111) using simultaneous AlN/ α -Si ₃ N ₄ buffer structure T. H. Yang, J. C. Chang, J. T. Ku, S. G. Shen, Y. C. Chen and C. Y. Chang, <i>National Chiao Tung Univ. (Taiwan)</i>	15:30 G-1-6 Layout Optimization of AlGaIn/GaN HEMTs for High-power Applications Y. S. Lin ¹ , T. C. Li ² , Y. C. Wang ³ and S. S. H. Hsu ¹ , ¹ National Tsing Hua Univ., ² Industrial Tech. Research Inst. and ³ National Chiao Tung Univ. (Taiwan)	15:30 H-1-6 Embedded Process and Characterization Analysis of Discrete Capacitor in Organic-Base Substrate S. M. Wu ¹ , E. Jahja ¹ , J. W. Wang ² , Z. Z. Lai ¹ and W. K. Yeh ¹ , ¹ National Univ. of Kaohsiung and ² ASE Electronics, Inc. (Taiwan)	15:30 I-1-6 Identification of Single and Coupled Acceptors in Silicon Nano Field-Effect Transistors M. A. H. Khalafalla, Y. Ono, K. Nishiguchi and A. Fujiwara, <i>NTT Corp. (Japan)</i>	

Room 101 (A) Room 102 (B) Room 201A (C) Room 201B (D) Room 202A (E)

Room 202B (F) Room 303 (G) Room 304 (H) Room 405 (I) Room 406 (J)

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

15:45 G-1-7
A New 20-element distributed Small-Signal Model and Integrated Intelligent Extraction Method applied to AlGaIn/GaN HEMTs up to 40GHz
J. Lu, B. Liu, Y. Wang, M. Li, L. Ma, Z. Wang and Z. P. Yu, *Tsinghua Univ. (China)*

Area 10: Organic Materials Science, Device Physics, and Applications

15:45 H-1-7
Influence of Organic Functional Groups on the Electrical Properties of Carbon Black - A Theoretical Study
A. Chutia, Z. Zhu, R. Sahnoun, H. Tsuboi, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*

Area 9: Physics and Applications of Novel Functional Materials and Devices

15:45 I-1-7
Photon-induced single-hole-tunneling current modulation in Si multiple-tunnel-junction field-effect transistor
Z. A. Burhanudin, R. Nuryadi and M. Tabe, *Shizuoka Univ. (Japan)*

Break

Area 1: Advanced Gate Stack/Si Processing Science

Area 3: CMOS Devices/Device Physics

Area 12: Spintronic Materials and Devices

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

Area 7: Photonic Devices and Device Physics

A-2: Ge MIS (16:15-18:15)
Chairs: S. Miyazaki (Hiroshima Univ.)
H. Hwang (Gwangju Inst. of Sci. & Engineering)

B-2: Transport in Nanoscale MOSFETs (16:15-18:25)
Chairs: F. Boeuf (STMicroelectronics)
Y. Kamakura (Osaka Univ.)

C-2: Spintronic Materials and Quantum Structures (16:15-17:30)
Chairs: Y. Ohno (Tohoku Univ.)
S. Sugahara (Tokyo Tech.)

D-2: MEMS Technology (16:15-18:15)
Chairs: M. Sasaki (Toyota Technological Inst.)
O. Nakagawara (Murata Manufacturing Co., Ltd.)

E-2: Special Session: Photonic Crystals and Si Photonics I (16:15-18:15)
Chairs: M. Sugawara (Fujitsu Labs. Ltd.)
M. Tokushima (NEC Corp.)

Break

Area 8: Advanced Material Synthesis and Crystal Growth Technology

Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics

Area 10: Organic Materials Science, Device Physics, and Applications

Area 9: Physics and Applications of Novel Functional Materials and Devices

Area 4: Advanced Memory Technology

F-2: Oxides (16:15-17:30)
Chairs: J. I. Chyi (National Central Univ.)
H. Yamaguchi (NTT Basic Research Labs.)

G-2: GaN FETs II (16:15-18:00)
Chairs: T. Tanaka (Matsushita Electric Industrial Co., Ltd.)
Y. Ohno (Univ. of Tokushima)

H-2: Organic Light Emitting Devices (16:15-18:00)
Chairs: S. Tokito (NHK)
M. Iwamoto (Tokyo Tech.)

I-2: Transport Through Novel Materials and Structures (16:15-18:00)
Chairs: T. Fujisawa (NTT)
K. Hirakawa (Univ. of Tokyo)

J-2: Flash Memory I (16:15-17:45)
Chairs: Y. Yamauchi (Sharp Corp.)
C. Hsu (eMemory Technology Inc.)

Wednesday, September 19

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 12: Spintronic Materials and Devices	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
16:15 A-2-1 Evaluation of SiO ₂ /GeO ₂ /Ge MIS Interface Properties by Low Temperature Conductance Method H. Matsubara ¹ , H. Kumagai ¹ , S. Sugahara ² , M. Takenaka ¹ , S. Takagi ¹ , ¹ Univ. of Tokyo and ² Tokyo Tech. (Japan)	16:15 B-2-1 (Invited) Technology Oriented Analytical Models of MOSFETs in the Quasi-Ballistic Regime R. Clerc ¹ , Q. Raffay ¹ , M. Ferrrier ¹ , P. Palestri ² , G. Ghibaudo ¹ and L. Selmi ² , ¹ IMEP and ² Univ. of Udine (France)	16:15 C-2-1 Atomically Controlled Hetero-Epitaxy of DO3-type Fe ₃ Si on Ge(111) Substrate K. Ueda ¹ , Y. Ando ¹ , M. Kumano ¹ , T. Sadoh ¹ , K. Narumi ² , Y. Maeda ³ and M. Miyao ¹ , ¹ Kyushu Univ., ² JAEA and ³ Kyoto Univ. (Japan)	16:15 D-2-1 (Invited) Fabrication of 3-dimensional structure by nanoimprint process Y. Hirai, <i>Osaka Prefecture Univ. (Japan)</i>	16:15 E-2-1 (Invited) Nanophotonic technologies for PC-SMZ-based all-optical flip-flop Switch: PC-FF Y. Sugimoto ^{1,2} and K. Asakawa ¹ , ¹ Univ. of Tsukuba, ² NIMS (Japan)
16:35 A-2-2 Direct Evidence of GeO Volatilization from GeO ₂ Films and Impact of Its Suppression on GeO ₂ /Ge MIS Characteristics S. Suzuki, K. Kita, H. Nomura, T. Nishimura and A. Toriumi, <i>Univ. of Tokyo (Japan)</i>	16:45 B-2-2 Influences of Elastic and Inelastic Scatterings on Ballistic Transport in MOSFETs H. Tsuchiya ¹ , S. Takagi ^{2,3} , ¹ Kobe Univ., ² MIRAI-ASRC and ³ Univ. of Tokyo (Japan)	16:30 C-2-2 MOVPE Condition Dependences of MnAs Nanoclusters Grown on GaInAs (111)A Surfaces H. Iguchi, S. Hara, J. Motohisa and T. Fukui, <i>Hokkaido Univ. (Japan)</i>	16:45 D-2-2 Large Displacement Micro XY-Stage with Paired Moving Plates M. Sasaki ¹ , F. Bono ² and K. Hane ² , ¹ Toyota Technological Inst. and ² Tohoku Univ. (Japan)	16:45 E-2-2 Optical-Nonlinearity-Induced Phase Shift via Selective Area Grown InAs-QDs in a Photonic Crystal Waveguide Y. Kitagawa ¹ , N. Ozaki ¹ , Y. Takata ¹ , N. Ikeda ² , S. Ohkouchi ^{1,3,4} , Y. Sugimoto ^{1,2} and K. Asakawa ^{1,2} , ¹ Univ. of Tsukuba, ² NIMS, ³ NEC Corp. and ⁴ AIST (Japan)
16:55 A-2-3 Experimental Evidence of Coexistence of Interface Traps Interacting with Majority and Minority Carriers in Ge MIS Structures N. Taoka ¹ , Y. Yamashita ² , M. Harada ² , K. Ikeda ² , T. Yamamoto ² , N. Sugiyama ² and S. Takagi ^{1,3} , ¹ MIRAI-ASRC, ² MIRAI-ASET and ³ Univ. of Tokyo (Japan)	17:05 B-2-3 Mobility and Backscattering in Germanium n-type Inversion Layers Q. Raffay ^{1,2} , P. Palestri ² , D. Esseni ² , R. Clerc ¹ and L. Selmi ² , ¹ IMEP and ² Univ. of Udine (France)	16:45 C-2-3 Structure and Magnetic Properties of Gd-doped Gallium Arsenide grown by MBE H. Miyagawa ¹ , H. Shiraoka ¹ , S. Higuchi ¹ , K. Fujii ¹ , N. Takahashi ¹ , Y. Watanabe ² , K. Oda ² , N. Tsurumachi ¹ , S. Nakanishi ¹ , H. Itoh ¹ and S. Koshiba ¹ , ¹ Kagawa Univ. and ² Univ. of Tokyo (Japan)	17:00 D-2-3 RF-MEMS Switch Structure for Low-Voltage Actuation and High-Density Integration K. Kuwabara ¹ , N. Sato ¹ , H. Morimura ¹ , J. Kodate ¹ , T. Kamei ² , K. Machida ² and H. Ishii ¹ , ¹ NTT Corp. and ² NTT Advanced Tech. Corp. (Japan)	17:00 E-2-3 Imprint Property of Optical Mach-Zehnder Interferometer Using Sputter Deposited (Ba,Sr)TiO ₃ at Low Temperature M. Suzuki, K. Nagata and S. Yokoyama, <i>Hiroshima Univ. (Japan)</i>

Wednesday, September 19

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
16:15 F-2-1 Characterization of Zinc Oxide Films Grown by a Newly Developed Plasma Enhanced MOCVD Employing Microwave Excited High Density Plasma H. Asahara ^{1,2} , A. Inokuchi ^{1,3} , K. Watanuki ^{1,4} , M. Hirayama ¹ , A. Teramoto ¹ and T. Ohmi ¹ , ¹ Tohoku Univ., ² ROHM Co., Ltd., ³ Tokyo Electron Ltd. and ⁴ Ube Industries Ltd. (Japan)	16:15 G-2-1 (Invited) Parasitic effects and reliability issues on GaN based HEMTs G. Meneghesso ¹ , C. Dua ² , M. Peroni ³ , M. Uren ⁴ and E. Zanoni ¹ , ¹ Univ. of Padova, ² Alcatel-Thales III-V Lab., ³ Selex-SI and ⁴ QinetiQ Ltd. (Italy)	16:15 H-2-1 (Invited) Charge Transport through Molecular Wires and Inorganic Nanowires T. Lee, W. K. Hong, G. Jo, T. W. Kim, J. Maeng, H. Song, G. Wang and A. Yoon, <i>GIST (Korea)</i>	16:15 I-2-1 (Invited) Nanopatterned epitaxial graphene for nano electronics C. Berger, <i>Georgia Inst. of Tech. (USA)</i>	16:15 J-2-1 (Invited) 3D Device Stacking Technology for Future Memory S. M. Jung, <i>Samsung Electronics Co., Ltd. (Korea)</i>
16:30 F-2-2 Dot-height dependence of Photoluminescence from ZnO quantum dots A. Nakamura ¹ , K. Okamatsu ¹ , T. Tawara ² , H. Gotoh ² , J. Temmyo ¹ and Y. Matsui ³ , ¹ Shizuoka Univ., ² NTT Corp. and ³ NIMS (Japan)	16:45 G-2-2 Reduced gate leakage for AlGaIn/GaN HEMTs grown on a-plane (1120) sapphire S. Lawrence Selvaraj and T. Egawa, <i>Nagoya Inst. of Tech. (Japan)</i>	16:45 H-2-2 Polymer Light-Emitting Diodes Using Poly(9,9-dioctylfluorene) Gel by Thermal Printing Method H. Kajii, D. Kasama and Y. Ohmori, <i>Osaka Univ. (Japan)</i>	16:45 I-2-2 Room Temperature Oscillation in Si/Si _{1-x} Ge _x Resonant Tunneling Diode Y. Suda ¹ , H. Maekawa ¹ , N. Asaoka ² and M. Suhara ² , ¹ Tokyo Univ. of Agri. and Tech. and ² Tokyo Metropolitan Univ. (Japan)	16:45 J-2-2 Improving the Cell Characteristics Using SiN Liner at Active Edge in 4 G NAND Flash D. Kang ^{1,2} , S. Jang ² , K. Lee ² , J. Kim ² , D. Chang ² , H. Kwon ² , W. Lee ² , I. H. Park ¹ , J. S. Kim ¹ , J. H. Lee ¹ , B. G. Park ¹ , J. D. Lee ¹ and H. Shin ¹ , ¹ Seoul National Univ. and ² Samsung Electronics Co., Ltd. (Korea)
16:45 F-2-3 Theoretical Study on Electronic and Electrical Properties of Nano Structural ZnO Z. Zhu, A. Chutia, R. Sahnoun, H. Tsuboi, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, <i>Tohoku Univ. (Japan)</i>	17:00 G-2-3 First Operation of AlGaIn Channel High Electron Mobility Transistors with Sufficiently Low Resistive Source/Drain Contact formed by Si Ion Implantation T. Nanjo ¹ , M. Takeuchi ^{2,3} , M. Suita ¹ , Y. Abe ¹ , T. Oishi ¹ , Y. Tokuda ¹ and Y. Aoyagi ^{2,3} , ¹ Mitsubishi Electric Corp., ² RIKEN and ³ Tokyo Tech. (Japan)	17:00 H-2-3 Co-doping in Spin-coated Hole Transport Layer for Flexible Organic Light Emitting Diodes S. L. Chen ¹ , S. H. Wang ¹ , F. S. Juang ¹ , Y. S. Tsai ¹ and P. H. Yeh ² , ¹ National Formosa Univ. and ² TPO Displays Corp. (Taiwan)	17:00 I-2-3 Direct Observation of Freeze-out Effect in Si by Kelvin Probe Force Microscope M. Ligowski ^{1,2} , R. Nuryadi ¹ , A. Ichiraku ¹ , M. Anwar ¹ , R. Jablonski ² and M. Tabe ¹ , ¹ Shizuoka Univ. and ² Warsaw Univ. of Tech. (Japan)	17:05 J-2-3 Nanocrystal floating gate memory devices using atomic layer deposited TiN/Al ₂ O ₃ nanolaminate layers S. Maikap ¹ , P. J. Tzeng ² , M. Anwar ¹ , H. Y. Lee ² , C. H. Lin ² , S. C. Lo ² , L. S. Lee ² , J. R. Yang ³ , M. J. Kao ³ and M. J. Tsai ² , ¹ Chang Gung Univ., ² Industrial Tech. Research Inst. and ³ National Taiwan Univ. (Taiwan)

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 12: Spintronic Materials and Devices	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
17:15 A-2-4 Fabrication of HfO _x N _y Dielectrics on Ge from HfN _x Deposition T. Maeda ¹ , Y. Morita ¹ and S. Takagi ^{1,2} , ¹ MIRAI, ASRC-AIST and ² Univ. of Tokyo (Japan)	17:25 B-2-4 Schottky Barrier MOSFETs as Resonant Tunneling Devices S. Toriyama ¹ and N. Sano ² , ¹ Toshiba Corp. and ² Univ. of Tsukuba (Japan)	17:00 C-2-4 Spin resolved spectroscopy of upper subbands in two-dimensional electron systems by direct transport measurements Y. Niida ^{1,2} , K. Takashina ¹ , A. Fujiwara ¹ , T. Fujisawa ¹ and Y. Hirayama ^{2,3} , ¹ NTT Corp., ² Tohoku Univ. and ³ SORST-JST (Japan)	17:15 D-2-4 Performance of Tense Thin Film Torsion Bar for Large-Rotation and Low-Voltage Driving of Micromirror M. Sasaki ¹ , S. Yuki ² and K. Hane ² , ¹ Toyota Technological Inst. and ² Tohoku Univ. (Japan)	17:15 E-2-4 (Invited) Quantum Confined Ultra-Thin Silicon Light-Emitting Transistor for On-Chip Optical Interconnection S. Saito, D. Hisamoto, H. Shimizu, H. Hamamura, R. Tsuchiya, Y. Matsui, T. Mine, T. Arai, N. Sugii, K. Torii, S. Kimura and T. Onai, Hitachi, Ltd. (Japan)
17:35 A-2-5 Thermally Robust Germanium MIS Gate Stacks with LaYO ₃ Dielectric Film T. Takahashi, Y. Zhao, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)	17:45 B-2-5 Coarse-Grain 3D Quantum Simulations of Nanoscale MOSFET G. Mil'nikov ¹ , N. Mori ¹ , Y. Kamakura ¹ and T. Ezaki ² , ¹ Osaka Univ. and ² Hiroshima Univ. (Japan)	17:15 C-2-5 The Reduction of g factor at Different Quantum States S. M. Huang ^{1,2} , H. Akimoto ¹ , K. Kono ¹ , J. J. Lin ² , S. Tarucha ^{3,4} and K. Ono ^{1,4} , ¹ RIKEN, ² National Chiao Tung Univ., ³ Univ. of Tokyo and ⁴ SORST-JST (Japan)	17:30 D-2-5 Ferrite and copper electroless plating to photopolymerized resin for micro molding of three-dimensional structures S. Kitayama, T. Yoshimura, S. Maruo and K. Mukai, Yokohama National Univ. (Japan)	17:45 E-2-5 Cavity Effect in Nanocrystalline Porous Silicon Ballistic Lighting Device B. Gelloz, M. Sato and N. Koshida, Tokyo Univ. of Agri. and Tech. (Japan)
17:55 A-2-6 Effects of Sulfur Passivation on Ge MOS Capacitors with High-k Gate Dielectric R. L. Xie, C. X. Zhu, National Univ. of Singapore (Singapore)	18:05 B-2-6 Multiband Simulation of Uniaxially Stressed Silicon MOSFETs Based on Non-Equilibrium Green's Function Method H. Fitriawan, S. Souma and M. Ogawa, Kobe Univ. (Japan)		17:45 D-2-6 Durability of Quartz Mold and Failure Mode Analysis in Imprint Lithography H. Ooe, T. Kanagawa, T. Hagi and Y. Yoshino, Murata Manufacturing Co., Ltd. (Japan)	18:00 E-2-6 Visible Light Emission from Controlled α -Si/SiN Multi-layer Structures Q. Chen ¹ , W. K. Tan ¹ , M. B. Yu ¹ , L. Ding ² , T. P. Chen ² , G. Q. Lo ¹ and D. L. Kwong ¹ , ¹ Inst. of Microelectronics and ² Nanyang Technological Univ. (Singapore)

Wednesday, September 19

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
17:00 F-2-4 Defect Passivation by Hydrogen in Zinc Oxide Films Grown by MOCVD J. Jo ¹ , O. Seo ² , H. Choi ¹ and B. Lee ³ , ¹ Ajou Univ., ² Samsung Advanced Inst. of Tech. and ³ CDA Co., Ltd. (Korea)	17:15 G-2-4 Hot-Carrier Stress Effects on AlGaIn/GaN HEMTs Employing 500 °C Oxidized Ni/Au Gate Y. H. Choi, J. Lim, I. H. Ji, K. H. Cho and M. K. Han, Seoul National Univ. (Korea)	17:15 H-2-4 Interface Control by Surface-Initiated Deposition Polymerization and its Application to Organic Light Emitting Devices A. Kawakami ¹ , K. Katsuki ¹ , R. C. Advincula ² , K. Tanaka ¹ and H. Usui ¹ , ¹ Tokyo Univ. of Agri. And Tech. and ² Univ. of Houston (Japan)	17:15 I-2-4 Effect of Size Reduction on Operation Temperature and Switching Power in GaAs-Based Schottky-Wrap-Gate Quantum Wire Transistors Y. Shiratori and S. Kasai, Hokkaido Univ. (Japan)	17:25 J-2-4 Memory Window Enhancement of MOS Memory Devices with High Density Self-Assembled Tungsten Nano-dot Y. Pei, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku Univ. (Japan)
17:15 F-2-5 Development of the multi-scale simulator for the dye-sensitized TiO ₂ nanoporous electrode based on quantum chemical calculation K. Ogiya, C. Lv, R. Sahnoun, M. Koyama, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, Tohoku Univ. (Japan)	17:30 G-2-5 Increase of Breakdown Voltage in AlGaIn/GaN HEMTs by Employing As+ Ion Implantation on SiO ₂ Passivation Layer J. Lim ¹ , Y. H. Choi ¹ , I. H. Ji ¹ , K. H. Cho ¹ , J. Lee ² , W. Jo ² and M. K. Han ¹ , ¹ Seoul National Univ. and ² Ewha Womans Univ. (Korea)	17:30 H-2-5 Multi-Color Panel Based on a White Organic Light Emitting Diode with Color Filter S. H. Su ¹ , C. C. Hou ¹ , H. Tu ¹ , C. M. Wu ¹ , G. Y. Lian ¹ , J. F. Li ² , M. Yokoyama ¹ and K. S. Hwang ² , ¹ I-Shou Univ. and ² National Chung Cheng Univ. (Taiwan)	17:30 I-2-5 Structure, Conductance and Strength of Atomic-Sized Iridium Wires T. Kizuka and M. Ryu, Univ. of Tsukuba (Japan)	
	17:45 G-2-6 Enhanced DC Characteristics of Si delta-doped AlGaIn/GaN HFETs with p-GaN Backbarrier H. C. Lee ¹ , S. Y. Hyun ¹ , S. W. Yun ¹ , C. Ostermaier ¹ , W. Y. Lee ¹ , J. B. Ha ¹ , H. I. Cho ¹ , S. H. Hahn ¹ , C. K. Hahn ² , H. C. Choi ¹ and J. H. Lee ¹ , ¹ Kyungpook National Univ. and ² Korea Electronics Tech. Inst. (Korea)	17:45 H-2-6 Utilizing Transparent ZnO Thin Film as Permeation-Barrier to Assist Top Emission Polymer Light-Emitting Devices Light Outcoupling and Longevity Y. H. Lu, Y. H. Liao, C. Y. Shih, Y. C. Huang and K. C. Liu, Chang Gung Univ. (Taiwan)	17:45 I-2-6 Pulse-controlled electromigration T. Hayashi and T. Fujisawa, NTT Corp. (Japan)	

Wednesday, September 19

Room 101 (A)

Room 102 (B)

Room 201A (C)

Room 201B (D)

Room 202A (E)

Area 11: Micro/Nano
Electromechanical
and Bio-Systems
(Devices)

18:00 D-2-7
Dual-FFPI
Temperature Sensor
with a Low-Cost LED
Light Source
M. C. Wang¹,
Y. T. Tseng²,
F. G. Tseng²,
J. E. Wang³ and
H. F. Taylor³, ¹*Ming-
Hsin Univ. of Sci. and
Tech.*, ²*National Tsing
Hua Univ.* and ³*Texas
A&M Univ. (Taiwan)*

18:30-20:30 Banquet/Paper Award & Young Reseacher Award (Multi-Purpose Hall 1F)

Wednesday, September 19

Room 202B (F)

Room 303 (G)

Room 304 (H)

Room 405 (I)

Room 406 (J)

18:30-20:30 Banquet/Paper Award & Young Reseacher Award (Multi-Purpose Hall 1F)

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
A-3: Reliability-I (9:00-10:30) Chairs: J. Yugami (Renesas Tech. Corp.) Y. Tsunashima (Toshiba Corp.)	B-3: CMOS Integration (9:00-10:30) Chairs: K. Shibahara (Hiroshima Univ.) H. Wakabayashi (Sony Corp.)	C-3: Plasma Induced Damage of Low-k Materials (9:00-10:30) Chairs: S. Ogawa (Selete) T. Tatsumi (Sony Corp.)	D-3: RF Components (9:00-10:20) Chairs: R. Fujimoto (Toshiba Corp.) T. Hamasaki (Texas Instruments Japan Ltd.)	E-3: Special Session: Photonic Crystals and Si Photonics II (9:00-10:30) Chairs: O. Wada (Kobe Univ.) R. Akimoto (AIST)
9:00 A-3-1(Invited) A Study of NBTI and PBTI (Charge Trapping) in High k Stacks with NiSi, TiN, Re Gates S. Zafar, Y. H. Kim, V. Paruchuri, V. Narayanan, B. Doris, A. Callegari, J. Stathis and T. Ning, <i>IBM (USA)</i>	9:00 B-3-1(Invited) Low Standby Power CMOS Process Integration Scheme for 45-32 nm node K. Imai, <i>NEC Electronics Corp. (Japan)</i>	9:00 C-3-1(Invited) Generation Mechanism of Etching Damages on Low-k SiOCH Films and Development of Novel Damage Evaluation Technique M. Hori, <i>Nagoya Univ. (Japan)</i>	9:00 D-3-1 A 0.49-6.50 GHz Wideband LC-VCO with High-IRR in a 180 nm CMOS Technology Y. Kobayashi, K. Ohashi, Y. Ito, H. Ito, K. Okada and K. Masu, <i>Tokyo Tech. (Japan)</i>	9:00 E-3-1(Invited) LSI on-chip optical interconnection with Si nano-photonics J. Fujikata ¹ , K. Nishi ¹ , A. Gomyo ¹ , J. Ushida ¹ , T. Ishi ¹ , H. Yukawa ¹ , D. Okamoto ¹ , M. Nakada ¹ , T. Shimizu ¹ , M. Kinoshita ¹ , K. Nose ¹ , M. Mizuno ¹ , T. Tsuchizawa ² , T. Watanabe ² , K. Yamada ² , S. Itabashi ² and K. Ohashi ¹ , <i>¹MIRAI-Selete and ²NTT Microsystem Integration Labs. (Japan)</i>

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
F-3: Group-IV Semiconductors I (9:00-10:15) Chairs: K. Hiruma (Hokkaido Univ.) K. Nishi (NEC Corp.)	G-3: High-Speed Devices and ICs I (9:00-10:15) Chairs: S. Yamahata (NTT) Y. J. Chan (National Central Univ. Taiwan)	H-3: Nanowire & Nanotube Sensors (9:00-10:30) Chairs: K. Matsumoto (Osaka Univ.) Y. Cui (Stanford Univ.)		J-3: Flash Memory II (9:00-10:20) Chairs: Y. Shimamoto (Hitachi, Ltd.) C. Hsu (eMemory Tech. Inc.)
9:00 F-3-1 Fabrication of 3-D Silicon Micro Probes for Neural Recording Using Multi-Step VLS Growth A. Ikedo ¹ , N. Funagayama ¹ , T. Kawashima ¹ , H. Takao ^{1,2} , K. Sawada ^{1,2} and M. Ishida ^{1,2} , <i>¹Toyohashi Univ. of Tech. and ²CREST-JST (Japan)</i>	9:00 G-3-1(Invited) Class-F Microwave Amplifier Design Using GaAs-HBT and GaN-HEMT K. Honjo, R. Ishikawa, T. Yoshida and C. Zheng, <i>Univ. of Electro-Communications (Japan)</i>	9:00 H-3-1(Invited) Nanowires for Nanoscale Electronics, Biosensors and Energy Applications S. Meister, C. K. Chan, H. Peng and Y. Cui, <i>Stanford Univ. (USA)</i>		9:00 J-3-1 2-bit/cell Characteristics of High-Density and High-Performance SONOS Flash Memory Cell with Recessed Channel Structure K. R. Han, Y. M. Kim, K. H. Park, S. G. Jung, B. K. Choi and J. H. Lee, <i>Kyungpook National Univ. (Korea)</i>

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
9:30 A-3-2 Comprehensive Understanding of PBTI and NBTI reliability of High-k / Metal Gate Stacks with EOT Scaling to sub-1nm M. Sato ¹ , K. Yamabe ² , K. Shiraishi ² , S. Miyazaki ³ , K. Yamada ⁴ , C. Tamura ² , R. Hasunuma ² , S. Inumiya ¹ , T. Aoyama ¹ , Y. Nara ¹ and Y. Ohji ¹ , ¹ Selete, ² Univ. of Tsukuba, ³ Hiroshima Univ. and ⁴ Waseda Univ. (Japan)	9:30 B-3-2 High Performance and Low Leakage CMOS for 45nm Low Power Technology and Beyond J. P. Han ¹ , Y. M. Lee ² , H. Utomo ³ , R. Lindsay ¹ , M. Eller ¹ , J. C. Kim ⁴ , V. Sardesai ³ , V. Chan ³ , S. Fang ³ , J. Holt ³ , T. N. Adam ³ , H. Zhuang ¹ , W. Wille ³ , Z. Lun ² , H. Wang ³ , T. Dyer ³ , J. Yan ¹ , O. J. Kwon ³ , O. S. Kwon ¹ , C. W. Lai ² , T. J. Tang ² , S. S. Tan ² , J. Yuan ³ , J. Li ³ , H. Ng ³ , H. Shang ³ , J. Sudijono ² , D. Schepis ³ , M. Jeong ³ , Y. Li ³ , J. H. Ku ⁴ , A. Gutmann ¹ and M. Hierlemann ¹ , ¹ Infineon Technologies AG, ² Chartered Semiconductor Manufacturing Ltd., ³ IBM and ⁴ Samsung Electronics Co., Ltd. (USA)	9:30 C-3-2 Impact of Barrier Metal Sputtering on Low-k SiOCH Films with Various Chemical Structures N. Inoue, N. Furutake, F. Ito, H. Yamamoto, T. Takeuchi and Y. Hayashi, <i>NEC Corp. (Japan)</i>	9:20 D-3-2 Evaluation of Digital Crosstalk Noise on a Differential Input VCO A. Toya ¹ , Y. Murasaka ² , T. Ohmoto ² and A. Iwata ^{1,2} , ¹ Hiroshima Univ. and ² A-R-Tec Corp. (Japan)	9:30 E-3-2 A Study on the Design and Properties of an SiON/SiO ₂ Waveguide: The Effect of the Substrate on Propagation Loss J. Ushida ¹ , A. Gomyo ¹ , J. Fujikata ¹ , D. Okamoto ¹ , K. Nishi ¹ , K. Ohashi ¹ , T. Watanabe ² , T. Tsuchizawa ² , K. Yamada ² and S. Itabashi ² , ¹ MIRAI-Selete and ² NTT Microsystem Integration Labs. (Japan)
9:50 A-3-3 Performance and Reliability Improvement by Optimized Nitrogen Content of TaSiN _x Metal Gate in Metal/HfSiON nFETs T. Onizawa, M. Sato, T. Aoyama, T. Eimori, Y. Nara and Y. Ohji, <i>Selete (Japan)</i>	9:50 B-3-3 In-Depth Study of Two-Dimensional Layout Dependences in Multiple-Stressor CMOS for 45 nm Technology Node High-Performance Applications T. Miyashita ¹ , J. Ogura ² , T. Owada ² , T. Sakuma ¹ , H. Nomura ² , H. Miyaoka ² , A. Hasegawa ² , S. Yamaguchi ² and S. Satoh ¹ , ¹ Fujitsu Labs. Ltd. and ² Fujitsu Ltd. (Japan)	9:50 C-3-3 Process Induced Damage Analysis of Low-k SiOCH Films Focusing on Siloxane Network and Methyl End Group S. Nakao, K. Kinoshita and S. Ogawa, <i>Selete (Japan)</i>	9:50 D-3-3 A New Symmetric Inductor Model for RF Circuits under Single-end and Differential Operations J. C. Guo and T. Y. Tan, <i>National Chiao Tung Univ. (Taiwan)</i>	9:45 E-3-3 Proposal of a Silicon Optical Modulator Based on Inversion-Carrier Absorption T. Hirata, K. Kajikawa, T. Tabei and H. Sunami, <i>Hiroshima Univ. (Japan)</i>

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
9:15 F-3-2 Demonstration of holes in strained Ge quantum wells with much higher drift mobility and density than that of electrons in strained Si channels M. Myronov ¹ , K. Sawano ¹ , K. M. Itoh ² and Y. Shiraki ¹ , ¹ Musashi Inst. of Tech. and ² Keio Univ. (Japan)	9:30 G-3-2 High-Performance InGaAs/InP Composite-Channel High Electron Mobility Transistors Grown by Metal Organic Vapor-Phase Epitaxy H. Sugiyama ¹ , T. Kosugi ¹ , H. Yokoyama ¹ , K. Murata ¹ , Y. Yamane ² , M. Tokumitsu ¹ and T. Enoki ¹ , ¹ NTT Corp. and ² NTT Electronics Corp. (Japan)	9:30 H-3-2 Electrical Sensing of Calcium Ions using Silicon Nanowire Array A. Agarwal ¹ , W. L. Wong ^{1,2} , K. L. Yang ² , S. Balakumar ¹ , N. Balasubramanian ¹ and D. L. Kwong ¹ , ¹ Inst. of Microelectronics and ² National Univ. of Singapore (Singapore)		9:20 J-3-2 ESR and PL Study of Charge Trapping Centers in Silicon Nitride Films and Its Verification with Novel ONO-Sidewall 2-bit/cell Nonvolatile Memory A. Toki ¹ , N. Shinohara ¹ , M. Nakano ² , H. Kotaki ² and Y. Kamigaki ¹ , ¹ Kagawa Univ. and ² Sharp Corp. (Japan)
9:30 F-3-3 Pulsed Laser Irradiation of Silicon-Germanium-on-Insulator (Si _{0.17} Ge _{0.83} OI) Substrates for Strain Relaxation and Defect Reduction G. H. Wang ¹ , E. H. Toh ¹ , X. Wang ² , K. M. Hoe ³ , S. Tripathy ¹ , G. Q. Lo ³ , G. Samudra ¹ and Y. C. Yeo ¹ , ¹ National Univ. of Singapore, ² Singapore Inst. of Manufacturing Tech. and ³ Inst. of Microelectronics (Singapore)	9:45 G-3-3 Low Power Consumption and Low Noise InGaP/GaAs HBT MMIC Amplifier for Full-Band UWB Receiver R. Ishikawa ¹ , T. Abe ¹ , M. Shimada ² and K. Honjo ¹ , ¹ Univ. of Electro-Communications and ² NANOTECH Corp. (Japan)	9:45 H-3-3 Fabrication of vertically-aligned CNT electrodes using plasma-enhanced CVD for chemical sensors Y. Kojima, S. Kishimoto, M. Okochi, H. Honda and T. Mizutani, <i>Nagoya Univ. (Japan)</i>		9:40 J-3-3 ONO Thickness Dependency of Complementary Bit Disturb in SONOS-type Nonvolatile Memory K. Kikuchi, <i>Spansion Japan Ltd. (Japan)</i>

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
10:10 A-3-4 nMOSFET Reliability Improvement attributed to the Interfacial Dipole formed by La Incorporation in HfO ₂ C. Y. Kang ¹ , P. Kirsch ² , D. Heh ¹ , C. Young ¹ , P. Sivasubramani ¹ , G. Bersuker ¹ , S. C. Song ¹ , R. Choi ¹ , B. H. Lee ² , J. Lichtenwalner ³ , J. S. Jur ³ , A. I. Kingon ³ and R. Jammy ² , ¹ SEMATECH, ² IBM Assignee and ³ North Carolina State Univ. (USA)	10:10 B-3-4 Is a "Power Optimized" Roadmap Realistic for High Performance Applications? F. Boeuf and T. Skotnicki, <i>STMicroelectronics (France)</i>	10:10 C-3-4 Plasma Cure Process for Porous SiOCH Films using CF ₄ Gas K. Tomioka, J. Nakahira, S. Kondo, S. Ogawa and S. Saito, <i>Selete (Japan)</i>	10:10 D-3-4 Thick Au High-Q Inductor and Its Chip-on-Chip Bonding on an RF IC for Various Frequencies J. Kodate ¹ , K. Kuwabara ¹ , N. Sato ¹ , H. Morimura ¹ , K. Kudou ² , K. Machida ² and H. Ishii ¹ , ¹ NTT Corp. and ² NTT AT (Japan)	10:00 E-3-4 Photoelastic Effect in Silicon Ring Resonator Y. Amemiya, Y. Tanushi, T. Tokunaga and S. Yokoyama, <i>Hiroshima Univ. (Japan)</i>
				10:15 E-3-5 Magneto-optic Effect in Amorphous Bi ₃ Fe ₅ O ₁₂ Waveguide Sputtered at Room Temperature H. Taura, Y. Shishido, Y. Tanushi, T. Tokunaga and S. Yokoyama, <i>Hiroshima Univ. (Japan)</i>

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
9:45 F-3-4 Strain-Relaxed Si _{1-x} Ge _x and Strained Si Grown by Sputter Epitaxy H. Hanafusa ¹ , Y. Suda ¹ , A. Kasamatsu ² , N. Hirose ² , T. Mimura ² and T. Matsui ² , ¹ Tokyo Univ. of Agri. and Tech. and ² NICT. (Japan)	10:00 G-3-4 Ku-band Compact Multi-layer Monolithic Microwave Digital Attenuator using InP/InGaAs PIN Diodes H. Eom, J. G. Yang, S. Choi and K. Yang, <i>KAIST (Korea)</i>	10:00 H-3-4 Comparison of Top gate Structures for Carbon Nanotube Field Effect Transistor Biosensor M. Abe ^{1,2,3} , K. Murata ^{1,2,3} , T. Ataka ^{1,2} and K. Matsumoto ^{2,3,4,5} , ¹ Olympus Corp., ² NEDO, ³ CREST-JST, ⁴ AIST and ⁵ Osaka Univ. (Japan)		10:00 J-3-4 Ramping Amplitude Multi-Frequency Charge Pumping Technique for Silicon-Oxide-Nitride-Oxide-Silicon Flash EEPROM Cell Transistors W. H. Choi ¹ , H. S. Joo ¹ , I. S. Han ¹ , S. S. Park ¹ , H. M. Kwon ¹ , T. G. Goo ¹ , O. S. Yoo ¹ , M. K. Na ¹ , J. C. Om ² , S. S. Lee ² , G. H. Bae ² , H. D. Lee ¹ and G. W. Lee ¹ , ¹ Chungnam National Univ. and ² Hynix Semiconductor Inc. (Korea)
		10:15 H-3-5 Development of gas sensors based on tungsten oxide nanowires in a metal/SiO ₂ /metal structure and their sensing responses to NO ₂ R. M. Ko ¹ , Z. F. Wen ¹ , S. J. Wang ¹ , J. K. Lin ¹ , G. H. Fan ¹ , W. I. Shu ¹ and B. W. Liou ² , ¹ National Cheng Kung Univ. and ² WuFeng Inst. of Tech. (Taiwan)		

Break

Short Presentation P-1 (10:45-12:15) Chair: H. Fukutome (Fujitsu Labs. Ltd.)	Short Presentation P-3 (10:45-12:15) Chair: S. Hayashi (Matsushita Electric Industrial Co., Ltd.)	Short Presentation P-2 and P-12 (10:45-12:15) Chair: S. Ogawa (Selete)	Short Presentation P-5 and P-11 (10:45-12:15) Chairs: R. Fujimoto (Toshiba Corp.) H. Tabata (Univ. of Tokyo)	Short Presentation P-7 (10:45-12:15) Chair: M. Sugawara (Fujitsu Labs. Ltd.)
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Break

Short Presentation P-8 (10:45-12:15) Chair: H. Yamaguchi (NTT Corp.)	Short Presentation P-6 (10:45-12:15) Chair: M. Kuzuhara (Univ. of Fukui)	Short Presentation P-10 and P-13 (10:45-12:15) Chairs: T. Kamata (AIST) K. Matsumoto (Osaka Univ.)	Short Presentation P-9 (10:45-12:15) Chair: Y. Takahashi (Hokkaido Univ.)	Short Presentation P-4 (10:45-12:15) Chair: I. Asano (Elpida Memory, Inc.)
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POSTER SESSION (13:00-15:00, Multi Purpose Hall)

P1
Advanced Gate Stack / Si
Processing Science
 (24 Papers)
P-1-1

Real-time monitoring of initial oxidation of Si(110)-16×2 Surface by Si 2p Photoemission spectroscopy
 Y. Yamamoto¹, H. Togashi¹, A. Kato¹, S. Hasegawa¹, S. Goto¹, T. Nakano¹, M. Suemitsu¹, Y. Narita², A. Yoshigoe³ and Y. Teraoka, ¹Tohoku Univ., ²Kyushu Inst. of Tech. and ³JAEA (Japan)

P-1-2

Si Oxidation Mechanism in Ar/O₂ Surface Wave Plasma
 K. Takeda, S. Takashima and M. Hori, Nagoya Univ. (Japan)

P-1-3

A lithographical method by oxidization through a conductive template in contact with a silicon substrate mediated by a thin water layer
 C. H. Hsieh, J. D. Liao, C. S. Kuo, C. Y. Huang and B. H. Wu, National Cheng Kung Univ. (Taiwan)

P-1-4

Pr-Oxide-Based Dielectric Films on Ge Substrates
 M. Sakashita, N. Kito, A. Sakai, H. Kondo, O. Nakatsuka, M. Ogawa and S. Zaima, Nagoya Univ. (Japan)

P-1-5

Physical and Electrical Properties of Addition Ti into Er₂O₃ Gate Dielectrics
 T. M. Pan, W. H. Hsu, C. C. Huang, W. S. Huang, K. C. Huang and J. L. Hong, Chang Gung Univ. (Taiwan)

P-1-6

In-Situ Fluorinated Low-Temperature Polycrystalline Silicon (LTPS) Thin-Film Transistors (TFT) with Low Trapping and Off Current by CF₄ Plasma
 W. H. Sung¹, C. H. Kao¹, H. K. Peng¹, S. F. Huang², W. F. Tsai², C. F. Ai², C. R. Chen³ and C. S. Lai, ¹Univ. of Chang Gung, ²Inst. of Nuclear Energy Research and ³Corp. of Material Sci. Service (Taiwan)

P-1-7

Improvement of Electrical Characteristics for Novel Fluorine-Incorporated Poly-Si TFTs with TiN Gate Electrode and Pr₂O₃ Gate Dielectric
 C. W. Chang¹, J. J. Huang¹, H. R. Chang¹, J. W. Lee² and T. F. Lei¹, ¹National Chiao Tung Univ. and ²Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)

P-1-8

Nanoscale-order Homogeneous Structure of SiO₂ Film on Poly-silicon Grown at Room Temperature using UV Light Excited Ozone
 N. Kameda^{1,2}, T. Nishiguchi^{1,2}, Y. Morikawa¹, M. Kekura¹, H. Nonaka² and S. Ichimura², ¹Meidensha Corp. and ²AIST (Japan)

P-1-9

Robust High-κ HfO_xN_y n-MOSFETs Using Low Work Function TbN Gate
 N. C. Su, C. H. Wu, S. J. Wang, C. K. Chiang, and C. C. Cheng, National Cheng Kung Univ. (Taiwan)

P-1-10

Crystalline and electrical properties of mictamict TiSiN gate MOS capacitors
 K. Furumai, H. Kondo, M. Sakashita, A. Sakai, M. Ogawa and S. Zaima, Nagoya Univ. (Japan)

P-1-11

Tuning of Work Function of Er-germanide Metal Gates on High-K Dielectric
 S. L. Liew, D. H. L. Seng and D. Z. Chi, *Inst. of Materials Research and Engineering (Singapore)*

P-1-12

Galvanic Corrosion Suppression of High-k/Metal Gates using Organic Solvent based HF
 D. Watanabe, H. Aoki, S. Hotta, C. Kimura and T. Sugino, Osaka Univ. (Japan)

P-1-13

Dual Metal Gate MOSFETs with Symmetrical Threshold Voltages Using Work Function Tuned Ta/Mo Bi-layer Metal Gates
 T. Matsukawa, Y. X. Liu, K. Endo, M. Masahara, Y. Ishikawa, H. Yamauchi, J. Tsukada, K. Ishii and E. Suzuki, AIST (Japan)

P-1-14

TiN Gate Work Function Control Using Nitrogen Gas Flow Ratio and RTA-Temperature
 Y. X. Liu¹, T. Hayashida², T. Matsukawa¹, K. Endo¹, M. Masahara¹, S. O'uchi¹, K. Sakamoto¹, K. Ishii¹, J. Tsukada¹, Y. Ishikawa¹, H. Yamauchi¹, A. Ogura² and E. Suzuki¹, ¹AIST and ²Meiji Univ. (Japan)

P-1-15

Reduced Interfacial Layer Thickness and Gate Leakage Current of ALD Grown HfAlO with TaN Gates using Chemical Oxides and Spike-Annealing
 Y. J. Lee¹, B. A. Tsai², H. Y. Peng¹, C. P. J. Tzeng³ and K. S. Chang-liao², ¹National Nano Device Labs., ²National Tsing Hua Univ. and ³Industrial Tech. Research Inst. (Taiwan)

P-1-16

Full Range Work Function Modulation by Nitrogen Incorporation in Hf-Mo Binary Alloys Gate Electrode
 C. S. Lai¹, C. W. Huang¹, H. K. Peng¹, C. H. Chen¹, Y. C. Fang², L. Hsu², H. C. Wang², C. Y. Lee³ and S. J. Lin³, ¹Chang Gung Univ., ²Chung-Shan Inst. and ³Nanya Tech. Corp. (Taiwan)

P-1-17

Quantitative Characterization of Plasma-Induced Defect Generation Process in Exposed Thin Si Surface Layers
 K. Eriguchi, A. Ohno, D. Hamada, M. Kamei, H. Fukumoto and K. Ono, Kyoto Univ. (Japan)

P-1-18

Pulsed Focused-Laser Beam Annealing of Ultra-Shallow Implanted Silicon and In Situ Dopant Activation Monitoring
 W. S. Yoo and K. Kang, WaferMasters, Inc. (USA)

P-1-19

UV-VIS Raman Characterization of High Dose Ultra Shallow Implanted Silicon before and after Excessive Annealing
 T. Sasaki¹, H. Minami¹, K. Kisoda², W. S. Yoo³, M. Yoshimoto¹ and H. Harima¹, ¹Kyoto Inst. of Tech., ²Wakayama Univ. and ³WaferMasters, Inc. (Japan)

P-1-20

Activation of Implanted Phosphorus Atoms in Silicon Wafers by Infrared Semiconductor Laser Annealing Using Carbon Films as Optical Absorption Layers
 N. Sano¹, T. Sameshima², Y. Matsuda³ and Y. Andoh³, ¹Hightec Systems Corp., ²Tokyo Univ. of Agri. and Tech. and ³Nissin Ion Equipment Co., Ltd. (Japan)

P-1-21

Effect of Ion Implantation on Dislocation Motion in SiGe/Si Heterostructures
 A. Hara, Tohoku-Gakuin Univ. (Japan)

P-1-22

Schottky Barrier Height Modulation for Nickel Silicide on n-Si (100) using Antimony Segregation
 H. S. Wong, L. Chan, G. Samudra and Y. C. Yeo, National Univ. of Singapore (Singapore)

P-1-23

In-situ Doped Si Selective Epitaxial Growth for Raised Source/Drain Extension CMOSFET
 T. Ikuta^{1,2}, Y. Miyamoto¹, S. Fujita¹, H. Iwamoto¹, S. Kadomura¹, T. Shimura², H. Watanabe² and K. Yasutake², ¹Sony Corp. and ²Osaka Univ. (Japan)

P-1-24

Top-view imaging of 65 nm gate length metal-oxide-semiconductor field effect transistors by scanning capacitance microscopy
 Y. Naitou¹, A. Ando¹, H. Ogiso¹, S. Kamohara², F. Yano² and A. Nishida², ¹AIST and ²MIRAI-Selete (Japan)

P2
Characterization and
Materials Engineering for
Interconnect Integration
 (14 Papers)
P-2-1

Low Dielectric Constant Non-Porous Fluorocarbon Films for Inter-Layer Dielectric
 A. Itoh^{1,2}, A. Inokuchi^{1,3}, S. Yasuda¹, A. Teramoto¹, T. Goto¹, M. Hirayama¹ and T. Ohmi¹, ¹Tohoku Univ., ²ZEON Corp. and ³Tokyo Electron Inc. (Japan)

P-2-2

The Evaluation of New Amorphous Hydrocarbon Film aCHx, for Copper Barrier Dielectric Film in Low-k Copper Metallization
 H. Ishikawa^{1,2}, T. Nozawa¹, T. Matsuoka¹, A. Teramoto², M. Hirayama², T. Ito² and T. Ohmi², ¹Tokyo Electron Ltd. and ²Tohoku Univ. (Japan)

P-2-3

Effects of vapor phase transport synthesis on the properties of porous silica films
 Y. Cho¹, T. Seo¹, K. Kohmura² and T. Kikkawa¹, ¹Hiroshima Univ. and ²Mitsui Chemicals, Inc. (Japan)

P-2-4

Integration of MIM Capacitors on BCB with Thin-Film MCM-D Technology
 J. Maeng¹, S. Song¹, C. S. Yoo¹, H. Lee² and K. Seo¹, ¹Seoul National Univ. and ²Samsung Electronics Co., Ltd. (Korea)

P-2-5

Novel Ta-Precursors for the CVD and ALD of TaN_x diffusion barrier layers
 M. Pokoj, I. Nemeth, K. Volz, D. Gaess, A. Merkoulou, J. Sundermeyer and W. Stolz, Philipps Univ. (Germany)

P-2-6

Enhanced Thermal Stability of Nickel Germanide with Ultrathin Ti Layer
 S. Zhu, M. B. Yu, G. Q. Lo and D. L. Kwong, *Inst. of Microelectronics (Singapore)*

P-2-7

Characterization of Strain in Si for High Performance MOSFETs
 D. Kosemura¹, Y. Kakemura¹, T. Yoshida¹, A. Ogura¹, M. Kohno², T. Nishita² and T. Nakanisi², ¹Meiji Univ. and ²Tokyo Electron AT Ltd. (Japan)

P-2-8

Raman Spectroscopic Study for Determining Stress Component in Single Crystal Silicon Microstructure using Multivariate Analysis
 N. Naka¹, S. Kashiwagi¹, Y. Nagai², T. Namazu², S. Inoue² and K. Ohtsuki¹, ¹HORIBA, Ltd. and ²Univ. of Hyogo (Japan)

P-2-9

Characterization of Patterned Oxide Buried in Bonded Silicon-on-Insulator Wafers by Near-Infrared Scattering Topography and Microscopy
 X. Wu^{1,2}, J. Uchikoshi¹, T. Hirokane¹, R. Yamada¹, K. Arima¹ and M. Morita¹, ¹Osaka Univ. and ²Xi'an Jiaotong Univ. (Japan)

P-2-10

Simulation and fabrication of embedded capacitors in the multilayer printed circuit board
 H. W. You and J. H. Koh, Kwangwoon Univ. (Korea)

P-2-11

Non-destructive extraction of width bias variations for deep sub-micron interconnect lines
 M. C. Tang, M. F. Wang, T. Cheng, D. Chen, C. S. Yeh and S. C. Chien, UMC (Taiwan)

P-2-12

Transmission property of flip chip package with adhesive interconnection for high frequency applications
 J. W. Kim, J. H. Ko, W. Nah and S. B. Jung, Sungkyunkwan Univ. (Korea)

P-2-13

SAW Bumpless Bonding at Low Temperature in Ambient Air
 Y. H. Wang¹, T. Sato², T. Sugiura² and T. Suga¹, ¹Univ. of Tokyo and ²Samsung Yokohama Research Inst. (Japan)

P-2-14

Void Free Room Temperature Silicon Direct Bonding by Sequential Plasma Activated Process
 C. Wang, E. Higurashi and T. Suga, Univ. of Tokyo (Japan)

**P3
CMOS Devices /Device
Physics**

(26 Papers)

P-3-1Impact of Zr/Hf Ratio on Reliability of HfZrO_x Gate DielectricJ. C. Liao¹, Y. K. Fang¹, Y. T. Hou², W. H. Tseng², J. Y. Yang², P. F. Hsu², Y. S. Chao², K. C. Lin², K. T. Huang², T. L. Lee² and M. S. Liang², ¹National Cheng Kung Univ. and ²Taiwan Semiconductor Manufacturing Company Ltd., (Taiwan)**P-3-2**Current Transportation Mechanism of HfO₂Gate Dielectrics with Silicon Surface Fluorine Implantation (SSFI) in CMOS Application
W. C. Wu¹, C. S. Lai², T. M. Wang², J. C. Wang³, M. W. Ma¹ and T. S. Chao¹, ¹National Chiao Tung Univ., ²Chang Gung Univ. and ³Nanya Tech. Corp. (Taiwan)**P-3-3**

Extra Bonus on Transistor Optimization with Stress Enhanced Notch-gate Technology for sub-90nm CMOSFET

W. K. Yeh¹, C. M. Lai², Y. K. Fang², C. W. Hsu¹, C. T. Lin³, C. H. Hsu³, L. W. Chen³, Y. T. Huang³ and C. T. Tsai³, ¹National Univ. of Kaohsiung, ²National Cheng Kung Univ. and ³UMC (Taiwan)**P-3-4**

Performance Comparison of Ultra-thin FD-SOI Inversion-, Intrinsic- and Accumulation-Mode MOSFETs

R. Kuroda^{1,2}, A. Teramoto¹, S. Sugawa¹ and T. Ohmi¹, ¹Tohoku Univ. and ²JSPS Research Fellow(DCI) (Japan)**P-3-5**In-situ Comparison of Si/High-K and Si/SiO₂ interface properties in FD SOIMOSFETs operated at low temperature
L. Pham-Nguyen^{1,2}, C. Fenouillet-Beranger³, S. Cristoloveanu¹, A. Vandooren², M. Orłowski² and G. Ghibaudo¹, ¹IMEP, ²Freescale Semiconductors and ³STMicroelectronics (France)**P-3-6**

Impact of Gate Overlap on the Performance of Schottky Barrier MOSFETs including GIBL Effect

L. Zeng, Z. L. Xia, G. Du, J. F. Kang, R. Q. Han and X. Y. Liu, Peking Univ. (China)

P-3-7

SiGe Recessed Source-Drain (RSD) Stressors for PMOS:

Effect of Device Integration Flow and Increased Ge Content on Electrical Performance

V. Machkaoutsan¹, P. Verheyen², P. Tomasini³, G. Eneman^{2,4,5}, R. Loo², P. Absil², S. G. Thomas³, J. P. Lu⁶, J. W. Weijtmans⁷ and R. Wise⁷, ¹ASM Belgium N.V., ²IMEC, ³ASM America Inc., ⁴Catholic Univ. of Leuven, ⁵Fund for scientific research Flanders, ⁶Texas Instruments assignee to IMEC and ⁷Texas Instruments (Belgium)**P-3-8**

Combined Effects of an Epitaxial Ge Channel and Si Substrate on Ge-on-Si MOS Capacitors and Field Effect Transistors

J. Oh¹, P. Majhi¹, H. Lee^{2,4}, S. H. Lee², S. Banerjee², P. Kalra³, R. Harris¹, H. H. Tseng¹ and R. Jammy¹, ¹SEMATECH, ²Univ. of Texas at Austin, ³Univ. of California Berkeley and ⁴Chungnam National Univ. (USA)**P-3-9**

Investigation of Impact Ionization in Strained-Si nMOSFETs

T. K. Kang¹, Y. H. Sa¹, P. C. Huang², S. L. Wu¹ and S. J. Chang², ¹Cheng Shiu Univ. and ²National Cheng Kung Univ. (Taiwan)**P-3-10**

Impact of Strain on Ballistic Current in Si n-i-n Structures

H. Minari and N. Mori, Osaka Univ. (Japan)

P-3-11Effect of STI Stress Enhanced Boron Diffusion on Leakage and V_{cc_min} of Sub-65nm node Low-Power SRAMT. H. Lee¹, Y. K. Fang¹, T. Lin¹, E. Hsu², T. Sheng², C. L. Kuo², O. Cheng² and S. C. Chien², ¹National Cheng Kung Univ. and ²UMC (Taiwan)**P-3-12**

Impacts of SiN Deposition Conditions on NMOSFETs

C. S. Lu¹, K. H. Chan¹, H. C. Lin^{1,2} and T. Y. Huang¹, ¹National Chiao Tung Univ. and ²National Nano Device Labs. (Taiwan)**P-3-13**

The Effect of Etch Stop Layer Stress on Negative Bias Temperature Instability of Deep Submicron p-MOSFETs

M. S. Chen¹, Y. K. Fang¹, T. H. Lee¹, C. T. Lin¹, J. Ko², Y. K. Sheu², T. L. Shen² and W. L. Liao², ¹National Cheng Kung Univ. and ²UMC (Taiwan)**P-3-14**

New Observation of NBTI Degradation and Recovery Effect of Plasma Nitrided Oxide in Nano Scale PMOSFETs

I. S. Han¹, H. H. Ji², T. G. Goo¹, O. S. You¹, W. H. Choi¹, M. K. Na¹, Y. G. Kim², S. H. Park², H. S. Lee², Y. S. Kang², D. B. Kim² and H. D. Lee¹, ¹Chungnam National Univ. and ²MagnaChip Semiconductor Inc. (Korea)**P-3-15**

Enhanced NBTI Degradation by SMT in Short-Channel pMOSFET

C. S. Huang¹, P. T. Liu¹, P. S. Lim², C. C. Chen², H. J. Tao² and Y. J. Mii², ¹National Chiao Tung Univ. and ²Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)**P-3-16**

Effects of hot carriers on DC and RF performances of deep submicron PMOSFET for low-power and high frequency applications

M. C. Tang¹, Y. K. Fang¹, D. Chen², C. S. Yeh² and S. C. Chien², ¹National Cheng Kung Univ. and ²UMC (Taiwan)**P-3-17**

NBTI-Stress Induced Grain-Boundary Degradation in Low-Temperature Poly-Si Thin-Film Transistors

C. Y. Chen¹, M. W. Ma¹, W. C. Chen², H. Y. Lin², K. L. Yeh², S. D. Wang¹ and T. F. Lei¹, ¹National Chiao Tung Univ. and ²Toppoly Optoelectronics Corp. (Taiwan)**P-3-18**

Investigation of Random Dopant Fluctuation for Multi-Gate MOSFETs Using Analytical Solution of 3-D Poisson's Equation

Y. S. Wu and P. Su, National Chiao Tung Univ. (Taiwan)

P-3-19

Accurate Extraction of Mobility, Effective Channel Length and Source/Drain Resistance in 60 nm MOSFETs

J. Kim, J. Lee, Y. Yun, B. G. Park, J. D. Lee and H. Shin, Seoul National Univ. (Korea)

P-3-20

Determining the Gate-Finger Width for the Minimum Gate Resistance in RF MOSFETs

Y. Jeong, I. M. Kang, J. Lee and H. Shin, Seoul National Univ. (Korea)

P-3-21

Non-Quasi-Static Small-Signal Model of RF MOSFETs Valid up to 110 GHz

I. M. Kang, Y. Yoon, J. D. Lee and H. Shin, Seoul National Univ. (Korea)

P-3-22

Spatial Distribution of Channel Thermal Noise in Short-Channel MOSFETs

J. Jeon, Y. Yun, B. G. Park, J. D. Lee and H. Shin, Seoul National Univ. (Korea)

P-3-23

Impacts of Body Contact Structures on SOI NMOSFET DC, RF and 1/f Noise Characteristics

R. Yang^{1,2}, Y. Z. Xiong¹, J. L. Shi¹, H. Qian², J. F. Li², J. Fu¹, W. Y. Loh¹, M. B. Yu¹, G. Q. Lo¹, N. Balasubramanian¹ and D. L. Kwong¹, ¹Inst. of Microelectronics and ²IMECAS (Singapore)**P-3-24**

Mechanism and Reliability Index of Hot-Carrier Degradation in LDMOS Transistors

K. S. Tian¹, J. F. Chen¹, W. C. Wang¹, S. Y. Chen¹, K. M. Wu², J. R. Lee¹, C. M. Liu² and S. L. Hsu², ¹National Cheng Kung Univ. and ²Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)**P-3-25**

Anomalous Hot-Carrier-Induced On-Resistance Degradation in High-Voltage LDMOS Transistors

S. Y. Chen¹, J. F. Chen¹, K. M. Wu², J. R. Lee¹, C. M. Liu² and S. L. Hsu², ¹National Cheng Kung Univ. and ²Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)**P-3-26**

Analysis of Temperature Effects on the High-Frequency Characteristics of RF LDMOS Transistors

H. H. Hu¹, K. M. Chen², G. W. Huang², C. Y. Chang¹, Y. C. Lu³, Y. C. Yang³ and E. Cheng³, ¹National Chiao Tung Univ., ²National Nano Device Labs. and ³UMC (Taiwan)**P4****Advanced Memory
Technology**

(7 Papers)

P-4-1

Effect of nano-grain on the memory characteristics of high-κ HfAlO charge trapping layers for nano-scale non-volatile memory device applications

T. Y. Wang¹, S. Maikap², P. J. Tzeng³, D. Panda², L. S. Lee³, M. J. Tsai³ and J. R. Yang¹, ¹National Taiwan Univ., ²Chang Gung Univ. and ³Industrial Tech. Research Inst. (Taiwan)**P-4-2**

An Improved Low Voltage Programming Scheme Using Forward Bias Assisted Drain Avalanche Induced Hot Electron Injection on P-Channel EEPROMs

Y. H. Huang and S. S. Chung, National Chiao Tung Univ. (Taiwan)

P-4-3Electronic characteristics of charge trapping memory using Al₂O₃ dielectricY. J. Seo¹, K. C. Kim¹, H. D. Kim¹, M. S. Joo², Y. T. Kim², S. H. Pyi², H. Y. Cho³ and T. G. Kim¹, ¹Korea Univ., ²Hynix Semiconductor Inc. and ³Dongguk Univ. (Korea)**P-4-4**Low temperature Poly-Si TFT nonvolatile memory devices with In₂O₃ nanoparticles embedded in polyimideH. M. Koo¹, D. U. Lee², S. P. Kim², E. K. Kim², J. Jung³ and W. J. Cho¹, ¹Kwangwoon Univ., ²Hanyang Univ. and ³Sejong Univ. (Korea)**P-4-5**

Si Quantum Dot TFT Nonvolatile Memory for System-On-Panel Applications

W. Yong¹, M. B. Yu², R. Yang², W. Y. Loh², J. Fu^{1,2}, C. Zhu¹, G. Q. Lo², N. Balasubramanian² and D. L. Kwong², ¹National Univ. of Singapore and ²Inst. of Microelectronics (Singapore)**P-4-6**Effect of Ni_{1-x}Pt_x Alloy Electrode on the Improved Resistive Switching Characteristics of NiO Thin Films

C. B. Lee, B. S. Kang, M. J. Lee, S. E. Ahn, G. Stefanovich, W. Xianyu, K. H. Kim, H. Yin, Y. Park and I. K. Yoo, Samsung Advanced Inst. of Tech. (Korea)

P-4-7Resistance Switching of HfO₂ Film and Its Application to Non-Volatile Memory

J. Lee, I. S. Park, J. Park, K. J. Jung, S. Lee and J. Ahn, Hanyang Univ. (Korea)

**P5
Advanced Circuits and
Systems**

(11 Papers)

P-5-1

Delay-Compensation Flip-Flops for Timing-Error Tolerant Circuit Design
K. Hirose, Y. Manzawa, M. Goshima and S. Sakai, *Univ. of Tokyo (Japan)*

P-5-2

Tungsten Through-Si Via (TSV) Technology for Three-Dimensional LSIs
H. Kikuchi¹, Y. Yamada¹, A. M. Ali^{1,2}, J. Liang¹, T. Fukushima¹, T. Tanaka¹ and M. Koyanagi¹, ¹Tohoku Univ. and ²Assiut Univ. (Japan)

P-5-3

A Novel Wide Dynamic Range CMOS Imager with Adaptive Logarithmic Response employing an In-pixel One-transistor Comparator
H. Y. Cheng and S. Collins, *Univ. of Oxford (UK)*

P-5-4

CMOS Voltage Reference Based on the Threshold Voltage of a MOSFET
K. Ueno, T. Hirose, T. Asai and Y. Amemiya, *Hokkaido Univ. (Japan)*

P-5-5

High-Q Resonator on Thin-Film Substrate for mm-wave System-on-Package (SOP)
S. Song and K. Seo, *Seoul National Univ. (Korea)*

P-5-6

Through-Only De-embedding for On-Chip Symmetric Devices
Y. Goto and M. Fujishima, *Univ. of Tokyo (Japan)*

P-5-7

Wideband CMOS Transimpedance Amplifier Design Using Transformer-Peaking Technique
J. D. Jin and S. S. H. Hsu, *National Tsing Hua Univ. (Taiwan)*

P-5-8

A Compact and Power-Efficient Implementation of Rank Order Filters Using Time-Domain Digital Computation Technique
L. T. Nguyen, K. Ito and T. Shibata, *Univ. of Tokyo (Japan)*

P-5-9

A Compact Bell-Shaped Analog Matching Cell Module for Digital-Memory-Based Associative Processors
T. T. Bui and T. Shibata, *Univ. of Tokyo (Japan)*

P-5-10

UWB Transmission Characteristics of Bow-tie Antennas on Si
S. Kubota, X. Xiao, K. Kimoto and T. Kikkawa, *Hiroshima Univ. (Japan)*

P-5-11

A Compact Balanced Filter on Thin Film Substrate for mmWave application
C. S. Yoo^{1,2}, J. M. Maeng¹, S. S. Song¹, H. S. Lee³, W. S. Lee², N. K. Kang² and K. S. Seo¹, ¹Seoul National Univ., ²Korea Electronics Tech. Inst. and ³Samsung Electronics Co., Ltd. (Korea)

P6**Compound Semiconductor
Circuits, Electron Devices
and Device Physics**

(10 Papers)

P-6-1

Dependence of Carrier Lifetime in InAlAs/InGaAs HEMTs on Gate-to-Source Voltage
H. Taguchi, T. Sato, M. Oura, T. Iida and Y. Takanashi, *Tokyo Univ. of Sci. (Japan)*

P-6-2

Feasibility Study of ZnO-Based FBAR Devices for Mobile WiMAX Applications
L. Mai, J. Lee, V. Pham and G. Yoon, *Information and Communications Univ. (Korea)*

P-6-3

Optimum Rapid Thermal Activation for Mg-doped p-type GaN
M. Nagamori¹, S. Ito¹, H. Saito¹, K. Shiojima¹, S. Yamada², N. Shibata² and M. Kuzuhara¹, ¹Univ. of Fukui and ²Toyoda gosei Corp. (Japan)

P-6-4

Effects of High-*k* Passivation Films on AlGaIn/GaN HEMT
S. Yagi¹, M. Shimizu¹, H. Okumura¹, H. Ohashi¹, K. Arai¹, Y. Yano² and N. Akutsu², ¹AIST and ²Taiyo Nippon Sanso Corp. (Japan)

P-6-5

High performance 50 nm In_{0.65}Al_{0.35}As/In_{0.75}Ga_{0.25}As Metamorphic HEMTs with Si₃N₄ passivation on thin InGaAs/InP layer
S. J. Yeon, J. Seong, M. Park and K. Seo, *Seoul National Univ. (Korea)*

P-6-6

High-speed and Low-Power SCFL-Type NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology
H. Kim, S. Yeon and K. Seo, *Seoul National Univ. (Korea)*

P-6-7

60 GHz LNA Module Using Low Temperature Co-fired Ceramic Technology
W. Chang, D. Y. Kim, H. Kim and H. K. Yu, *ETRI (Korea)*

P-6-8

High performance 70 nm In_{0.8}GaP/In_{0.4}AlAs/In_{0.35}GaAs Metamorphic HEMT With Pd Schottky Contacts
S. Kim, Y. Koh and K. Seo, *Seoul National Univ. (Korea)*

P-6-9

The Impact of Mixed-mode Electrical Stress on High-Frequency and RF Power Characteristics of SiGe HBTs
S. Y. Huang¹, C. C. Hung¹, W. S. Liao¹, C. Y. Lin¹, C. W. Fan¹, C. Y. Tzeng¹, V. Liang¹, K. M. Chen² and C. Y. Chang³, ¹UMC, ²National Nano Device Labs. and ³National Chiao Tung Univ. (Taiwan)

P-6-10

Hydrogen-Sensing Behaviors of an InAlAs-Based Schottky Diode with a Pt Catalytic Thin Film
C. W. Hung, H. I. Chen, T. P. Chen, T. H. Tsai and W. C. Liu, *National Cheng Kung Univ. (Taiwan)*

P7**Photonic Devices and
Device Physics**

(16 Papers)

P-7-1

InGaAs/InP p-i-n Photodiode with Extrinsic Pad Isolation Structure
M. Kim, *Kongju National Univ. (Korea)*

P-7-2

Anomalous Electroluminescence Phenomena in InGaIn/GaN Multiple Quantum Well Light-emitting Diodes with Electron Tunneling Layer
H. Y. Chen¹, Y. F. Chen¹, W. T. Su¹, K. Y. Cheng¹, J. C. Wang¹, H. T. Shen¹, T. E. Nee¹ and Y. F. Wu², ¹Chang Gung Univ. and ²Tech. and Sci. Inst. of Northern Taiwan (Taiwan)

P-7-3

Quaternary AlInGaIn Solar Blind UV Detectors with Photo-CVD SiO₂ Cap Layers
C. H. Chen, *Cheng Shiu Univ. (Taiwan)*

P-7-4

Steep On-Off Ratio of Photocurrent through Metal-Oxide-Semiconductor Tunneling Structures
R. Yamada, H. Hashimoto, K. Arima, J. Uchikoshi and M. Morita, *Osaka Univ. (Japan)*

P-7-5

Observation of Ultraviolet-Light Emission from Si/SiO₂ Multilayer Films Prepared by Using RF Magnetron Sputtering
K. Miura, Y. Kato, H. Hoshino and O. Hanaizumi, *Gunma Univ. (Japan)*

P-7-6

GaN Metal-Semiconductor-Metal Photodetectors with an un-activated Mg-doped GaN Cap Layer
P. C. Chang¹, Y. C. Wang², K. H. Lee², C. L. Yu² and S. J. Chang², ¹Nan Jeon Inst. of Tech. and ²National Cheng Kung Univ. (Taiwan)

P-7-7

Ion Beam Deposition of Quantum Dots from Colloidal Solution
Y. Tani, S. Kobayashi and H. Kawazoe, *HOYA Corp. (Japan)*

P-7-8

A High Performance Photodetector Suitable for Visible Light and Near IR Applications
K. S. Lai, J. C. Huang and K. Y. J. Hsu, *National Tsing Hua Univ. (Taiwan)*

P-7-9

Experimental and Theoretical Examination of Field Emission in Surface Conduction Electron-Emitter Displays
H. Y. Lo¹, Y. Li¹, C. H. Tsai¹, H. Y. Chao¹, F. M. Pan¹, M. C. Chiang² and C. N. Mo², ¹National Chiao Tung Univ. and ²Chunghwa Picture Tubes, Ltd. (Taiwan)

P-7-10

AlGaIn MSM Photodetectors with SiN/GaN double buffer layers
Y. D. Zhou, S. J. Chang, Y. K. Su, C. H. Liu, M. L. Lee and M. R. Wu, *National Cheng Kung Univ. (Taiwan)*

P-7-11

Coupling of surface plasmons between two silver films in a plasmonic thermal emitter
C. Y. Chen, M. W. Tsai, Y. H. Ye, J. W. Jiang, Y. T. Chang and S. C. Lee, *National Taiwan Univ. (Taiwan)*

P-7-12

Dispersion relations of localized surface plasmon polaritons in a plasmonic thermal emitter
Y. H. Ye, M. W. Tsai, C. Y. Chen, J. W. Jiang, Y. T. Chang and S. C. Lee, *National Taiwan Univ. (Taiwan)*

P-7-13

A study of deposition single crystal SiCN thin film on porous silicon for ultraviolet light detecting applications
T. H. Chou¹, Y. K. Fang¹, T. W. Kuo¹, D. H. Jaw², F. S. Lai², J. F. Huang² and J. S. Shie², ¹National Cheng Kung Univ. and ²Wufeng Inst. of Tech. (Taiwan)

P-7-14

Mechanism investigation of (NH₄)₂S_x-treated III—V compounds multi-junction solar cell
L. W. Lai, J. T. Chen and C. T. Lee, *National Cheng Kung Univ. (Taiwan)*

P-7-15

GaN Ultraviolet MSM Photodetectors by capping a Low-Temperature AlN Layer
K. H. Lee¹, P. C. Chang², Y. C. Wang¹, C. L. Yu¹ and S. J. Chang¹, ¹National Cheng Kung Univ. and ²Nan Jeon Inst. of Tech. (Taiwan)

P-7-16

AlGaIn MSM Photodetectors with SiN/GaN double buffer layers
Y. D. Zhou, S. J. Chang, Y. K. Su, C. H. Liu, M. L. Lee and M. R. Wu, *National Cheng Kung Univ. (Taiwan)*

P8**Advanced Material
Synthesis and Crystal
Growth Technology**

(17 Papers)

P-8-1

Self organized Micro Cones on Si substrate by Microwave Plasma Chemical Vapor Deposition
M. Moriya, Y. Matsumoto, Y. Mizugaki, T. Kobayashi and K. Usami, *Univ. of Electro-Communications (Japan)*

P-8-2

Facile Fabrication of Gold Nanoparticle -Titanium Oxide Multilayer Assemblies by Surface Sol-Gel Processes
T. Kawahara, T. Arakawa, T. Akiyama and S. Yamada, *Kyushu Univ. (Japan)*

P-8-3

Vanadium Dioxide Films Deposited on SiO₂- and Al₂O₃-coated Si Substrates Using Reactive RF-Magnetron Sputter Deposition Technique
S. J. Yun, J. W. Lim, B. G. Chae and H. T. Kim, *Electronics and Telecommunications Research Inst. (Korea)*

P-8-4

Lateral Recrystallized Si Thin Films with Large Tensile Strain for High Performance Thin Film Transistors
S. Fujii, S. Kuroki, Z. Xiaoli, M. Numata, K. Kotani and T. Ito, *Tohoku Univ. (Japan)*

P-8-5

High-Performance LTPS-TFTs Fabricated by Continuous Wave Laser Annealing
C. C. Tsai¹, K. F. Wei¹, Y. J. Lee², J. L. Wang¹, I. C. Lee¹ and H. C. Cheng¹, ¹National Chiao Tung Univ. and ²National Nano Device Labs. (Taiwan)

P-8-6

Growth of GaNAs films with As₂ source in atomic hydrogen-assisted molecular beam epitaxy
A. Takata, R. Oshima and Y. Okada, *Univ. of Tsukuba (Japan)*

P-8-7

High Quality Crack-Free GaN-Based Epitaxy on Patterned Si(111) Substrate
S. J. Lee, G. H. Bak, S. R. Jeon, S. H. Lee, S. Kim, S. H. Jeong and J. H. Baek, *KOPTI (Korea)*

P-8-8

MOVPE Growth of M-Plane GaN Using LiAlO₂ Substrates
Y. K. Su, A. T. Cheng, W. C. Lai and Y. Z. Chen, *National Cheng Kung Univ. (Taiwan)*

P-8-9

The Elimination of Inversion Domains in MBE-GaN Grown Using Low Temperature Nitridation
J. C. Chang, T. H. Yang, S. G. Shen, Y. C. Chen, J. T. Ku and C. Y. Chang, *Nation Chiao Tung Univ. (Taiwan)*

P-8-10

Growth and Characterization of GaN Nano-column Grown on Gallium Coated Si by Molecular Beam Epitaxy
K. Santhakumar¹, D. W. Kim¹, D. H. Kang¹, D. W. Kim² and C. R. Lee¹, ¹Chonbuk National Univ. and ²Chungnam National Univ. (Korea)

P-8-11

Electron transport at InGaN/ electrolyte interface and its application to water photolysis using visible light
S. Usui¹, T. Narumi¹, J. Tokue¹, N. Kobayashi¹, J. Yamamoto², Y. Ban² and K. Wakao², ¹Univ. of Electro-Communications and ²Nippon EMC. Ltd. (Japan)

P-8-12

Fabrication and Characterization of In_xGa_{1-x}N Quantum Dots using NNAD Growth Technique
D. H. Kang¹, D. W. Kim¹, S. H. Lee¹, S. J. Lee², J. S. Kim¹, K. Santhakumar¹ and C. R. Lee¹, ¹Chonbuk National Univ. and ²Korea Photonics Tech. Inst. (Korea)

P-8-13

Growth of InN on patterned sapphire substrates and its characterization
H. Song, D. H. Kang, J. C. Song, E. S. Jang, I. H. Lee, K. Santhakumar, D. W. Kim and C. R. Lee, *Chonbuk National Univ. (Korea)*

P-8-14

Fabrication and characteristics of the low resistivity p-type ZnO thin films by nitrogen ion implantation
S. Y. Tsai¹, Y. M. Lu² and M. H. Hon¹, ¹National Cheng Kung Univ. and ²National Univ. of Tainan (Taiwan)

P-8-15

Stability of Phosphorus-doped p-ZnO thin films
J. K. Kim^{1,2}, J. W. Lim², H. T. Kim², S. H. Kim² and S. J. Yun^{1,2}, ¹Univ. of Sci. and Tech. and ²Electronics and Telecommunications Research Inst. (Korea)

P-8-16

Properties of Zinc Oxide Films Cosputtered with Various Aluminum Contents at Room Temperature
D. S. Liu¹, C. W. Sheu¹, F. C. Tsai¹ and C. T. Lee², ¹National Formosa Univ. and ²National Cheng Kung Univ. (Taiwan)

P-8-17

Activation of Nitrogen-acceptors in Al-N Codoped Zinc Oxide Films Prepared by Radio Frequency Magnetron Cosputtering Technology
D. S. Liu¹, C. Y. Wu¹, C. S. Shei¹ and C. T. Lee², ¹National Formosa Univ. and ²National Cheng Kung Univ. (Taiwan)

P9**Physics and Applications of Novel Functional Materials and Devices**

(14 Papers)

P-9-1

Control of electrostatic coupling observed for Si double quantum dot structures
G. Yamahata¹, Y. Tsuchiya^{1,3}, S. Oda^{1,3} and H. Mizuta^{1,2,3}, ¹Tokyo Tech., ²Univ. of Southampton and ³SORST-JST (Japan)

P-9-2

Electrically detected exciton photo-absorption in semiconductor double quantum dot
K. Takahashi¹, K. Kono¹, S. Tarucha², H. Kosaka^{2,3} and K. Ono^{1,4}, ¹RIKEN, ²Univ. of Tokyo, ³Tohoku Univ. and ⁴CREST-JST (Japan)

P-9-3

Transient Behavior of Germanium Quantum-dot Resonant Tunneling Diode
W. T. Lai and P. W. Li, *National Central Univ. (Taiwan)*

P-9-4

Magneto-capacitance measurement of a selectively doped n-AlGaAs/GaAs heterojunction with InGaAs quantum dots
T. Kawazu¹ and H. Sakaki^{1,2}, ¹NIMS and ²Toyota Technological Inst. (Japan)

P-9-5

Fabrication of InGaN/GaN Multiple Quantum Wells Nanopillars by Focused Ion Beam Milling
S. E. Wu, T. H. Hsueh, C. P. Liu, J. K. Sheu, W. C. Lai and S. J. Chang, *National Cheng Kung Univ. (Taiwan)*

P-9-6

A Physics-based Compact Model for I-MOS Transistors
C. Shen¹, E. H. Toh¹, J. Lin¹, C. H. Heng¹, D. Sylvester², G. Samudra¹ and Y. C. Yeol¹, ¹National Univ. of Singapore and ²Univ. of Michigan (Singapore)

P-9-7

Development of a Seebeck Coefficient Prediction Simulator Using Tight-Binding Quantum Chemical Molecular Dynamics
H. Tsuboi, K. Ogiya, A. Chutia, Z. Zhu, C. Lv, R. Sahnoun, M. Koyama, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, *Tohoku Univ. (Japan)*

P-9-8

Programmable VO₂ temperature sensor controlled by a constant voltage
B. J. Kim, Y. W. Lee, S. Choi, B. G. Chae, S. J. Yun and H. T. Kim, *Electronics and Telecommunications Research Inst. (Korea)*

P-9-9

Chemical Bonding Self-Organizations in Non-crystalline Hf Si Oxynitride Dielectrics: Low Direct Tunneling and Defect Levels Comparable to SiO₂
S. Lee¹, H. Seo¹, G. Lucovsky¹ and J. C. Phillips², ¹North Carolina State Univ. and ²Rutgers Univ. (USA)

P-9-10

Novel Vacuum Encapsulation Applied for Improving Short-Channel Immunity on Poly-Si Thin Film Transistors
T. C. Liao¹, C. Y. Wu¹, S. W. Tu¹, F. T. Chien², W. K. Lin¹, J. C. Liu¹, H. W. Chen¹, C. C. Lin¹ and H. C. Cheng¹, ¹National Chiao Tung Univ. and ²Feng Chia Univ. (Taiwan)

P-9-11

A Quasi-planar Thin Film Field Emission Diode
K. C. Lin, H. W. Chen, R. L. Lai, C. P. Juan, Y. Y. Hsu and H. C. Cheng, *National Chiao Tung Univ. (Taiwan)*

P-9-12

Dopant Dependency of Nickel Silicide and Its Improvement Utilizing Ni-Pd(5%) on SOI Substrate for Nano-scale CMOSFET
S. Y. Jung¹, Y. Y. Zhang¹, Z. Zhong¹, S. G. Li¹, K. Y. Park¹, Y. C. Kim², G. W. Lee¹, J. S. Wang¹ and H. D. Lee¹, ¹Chungnam National Univ. and ²Korea Univ. of Tech. and Education (Korea)

P-9-13

Abrupt metal insulator transition of TiO₂ and Al_xTi_{1-x}O_y thin films
J. W. Lim, S. J. Yun, Y. W. Lee, B. J. Kim and H. T. Kim, *ETRI (Korea)*

P-9-14

Current and Speed Enhancements at 90nm Node through Package Strain
W. S. Liao¹, S. Y. Huang¹, T. Shih¹ and C. W. Liu², ¹UMC and ²National Taiwan Univ. (Taiwan)

P10**Organic Materials Science, Device Physics, and Applications**

(10 Papers)

P-10-1

Applications of PVA/PAA proton exchange membrane in fuel cell
P. C. Kuo, D. S. Wu, L. L. Wang, M. Y. Shia and H. H. Yu, *National Formosa Univ. (Taiwan)*

P-10-2

Novel Sub-10nm Polymer Thin Film Resistance Switching Device
D. Lee, S. Choi, M. Ree and O. Kim, *Pohang Univ. of Sci. and Tech. (Korea)*

P-10-3

Electrical Conducting Properties of Amorphous Carbon Nanowhiskers Studied by In Situ High-Resolution Transmission Electron Microscopy
R. Kato¹, K. Miyazawa² and T. Kizuka¹, ¹Univ. of Tsukuba and ²NIMS (Japan)

P-10-4

Lateral Carrier Transport in Pentacene Polycrystalline Films-Hole Transport Barrier and Effective Mass in Crystals –
R. Matsubara, N. Ohashi, M. Sakai, K. Kudo and M. Nakamura, *Chiba Univ. (Japan)*

P-10-5

Low-Voltage Operation of Organic Thin Film Transistors by using Dual Gate Dielectrics
S. B. Kong and C. K. Song, *Dong-A Univ. (Korea)*

P-10-6

Fabrication and characterization of poly(3-hexylthiophene)-based field-effect transistors with silsesquioxane gate insulators
K. Tomatsu¹, T. Hamada^{1,4}, T. Nagase^{1,4}, T. Kobayashi^{1,4}, S. Murakami^{2,4}, K. Matsukawa^{3,4} and H. Naito^{1,4}, ¹Osaka Prefecture Univ., ²TRI-Osaka, ³Osaka Municipal Technical Research Inst. and ⁴JST (Japan)

P-10-7

Organic Thin Film Transistors fabricated by All Solution Processes
S. K. Ahn and C. K. Song, *Dong-A Univ. (Korea)*

P-10-8

Fully Self-Aligned Organic Field-Effect Transistors
K. Nomura, S. Naka and H. Okada, *Univ. of Toyama (Japan)*

P-10-9

Observation of Carrier Behavior in Organic Field Effect Transistor with Electroluminescence under AC Electric Field
Y. Ohshima, H. Kohn, E. Lim, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

P-10-10

The Study of Organic Light Emitting Diode with a Doped Electron Transport Layer
C. C. Hou, R. S. Shieh, S. H. Su, C. M. Wu and M. Yokoyama, *I-Shou Univ. (Taiwan)*

P11**Micro/Nano Electromechanical and Bio-Systems (Devices)**

(11 Papers)

P-11-1

Development of Power Supply System for Three-Dimensionally Staked Retinal Prosthesis Chip
K. Komiya, R. Kobayashi, T. Kobayashi, K. Sato, T. Fukushima, H. Tomita, H. Kurino, T. Tanaka, M. Tamai and M. Koyanagi, *Tohoku Univ. (Japan)*

P-11-2

Immobilization of Protein Molecules on Step-Controlled Sapphire Surfaces and Characterization of the Adhesion Forces
R. Aoki¹, T. Arakawa¹, T. Oya¹ and T. Ogino^{1,2}, ¹Yokohama National Univ. and ²CREST-JST (Japan)

P-11-3

Tracking of Cell Adhesion Process to Self-Assembled Monolayer of Alkanethiols with Various Functional Groups
Y. Arima and H. Iwata, *Kyoto Univ. (Japan)*

P-11-4

Self-spreading Behavior of Supported Lipid Bilayer through Single Sub-100-nm Gap
Y. Kashimura, J. Duraio, K. Furukawa and K. Torimitsu, *NTT Corp. (Japan)*

P-11-5

A Novel High-k Y₂O₃ Sensing Membrane for pH-ISFET
T. M. Pan, K. M. Liao, J. C. Lin, C. H. Cheng, Z. W. Lin and C. J. Chang, *Chang Gung Univ. (Taiwan)*

P-11-6

The Development of Oligonucleotide Micro Array Detecting System
J. Z. Tsai, C. J. Chen, K. H. Shiue, Z. C. Liu, W. Y. Chen and Y. M. Hsin, *National Central Univ. (Taiwan)*

P-11-7

Vibration Evaluation and Gas Transfer of Distilled Water and Bovine Blood in Intravascular Lung Assist Device using PZT Actuator
G. B. Kim¹, C. U. Hong¹, M. H. Kim¹, S. J. Kim² and H. S. Kang¹, ¹*Chonbuk National Univ. and* ²*Iksan National Collage (Korea)*

P-11-8

A Controller of Microfluidic Fraction Mixing Induced by DC and AC Electric Fields
W. J. Luo¹, K. C. Chang², K. F. Yam² and M. H. Shih³, ¹*National Chin-Yi Univ. of Tech.*, ²*Far East Univ. and* ³*Military Academy (Taiwan)*

P-11-9

Effect of Rise Time on Atmospheric Plasma generated using Micro-triode
J. Kim, K. Kim, S. Jin and Y. Kim, *Hong-ik Univ. (Korea)*

P-11-10

Pulsating Tension Fatigue Testing of Single and Poly-Crystalline Silicon Microstructures for Silicon MEMS
T. Namazu, Y. Nagai and S. Inoue, *Univ. of Hyogo (Japan)*

P-11-11

Novel inorganic pH-insensitive membrane prepared by post N₂O plasma treatment on conventional Si₃N₄/SiO₂ stack layer for REFET application
T. C. Wang¹, T. F. Lu¹, C. H. Chin¹, C. E. Lue¹, C. M. Yang¹, Y. C. Fang², L. Hsu², H. C. Wang² and C. S. Lai¹, ¹*Chang Gung Univ. and* ²*Chung-Shan Inst. (Taiwan)*

P12

Spintronic Materials and Devices

(3 papers)

P-12-1

Hydrogenation Induced Room-Temperature Ferromagnetism in Co-doped ZnO Nanocrystals
Y. Wang, L. Sun, Y. Li, Y. Zhang, D. Han, L. Liu, J. Kang, X. Zhang and R. Han, *Peking Univ. (China)*

P-12-2

Design of Reconfigurable Logic Circuits based on Single-Layer Magnetic-Tunnel-Junction Elements
S. Lee, G. Lee, H. Lee, S. Lee and H. Shin, *Ewha W. Univ. (Korea)*

P-12-3

Appearance of Variable-Range-Hopping Conduction and Enhanced Spin Dependent Transport by Low Temperature Heat Treatment for Magnetite Nanoparticle Sinter
H. Kobori¹, K. Ohnishi¹, A. Sugimura¹ and T. Taniguchi², ¹*Konan Univ. and* ²*Osaka Univ. (Japan)*

P13

Applications of Nanotubes and Nanowires

(11 paper)

P-13-1

ZnO Nanowire-Based CO Sensors Prepared at Various Temperatures
T. J. Hsueh¹, S. J. Chang¹, C. L. Hsu² and I. C. Chen³, ¹*National Cheng Kung Univ.*, ²*National Univ. of Tainan and* ³*Industrial Tech. Research Inst. (Taiwan)*

P-13-2

Effects of Cu Catalyst and Water Vapor on the Growth of Ge-GeO_x Core-Shell Nanowires via the Carbothermal Reduction of GeO₂ Powders
W. L. Lo, T. J. Hsu and W. T. Lin, *National Cheng Kung Univ. (Taiwan)*

P-13-3

Band-Gap Tuning of an Individual Single-Walled Carbon Nanotube with Uniaxial Strain
H. Maki¹, T. Sato¹ and K. Ishibashi², ¹*Keio Univ. and* ²*RIKEN (Japan)*

P-13-4

Synthesis of VO₂ Nanowire and Observation of the Metal-Insulator Transition
S. Choi, B. J. Kim, Y. W. Lee, S. J. Yun and H. T. Kim, *ETRI (Korea)*

P-13-5

Band Structure of Surface Terminated Silicon Nanowire
S. You, M. Gao and Y. Wang, *Tsinghua Univ. (China)*

P-13-6

CNT-FETs with High Modulated Drain Current utilizing Size-classified Fe Particles as a Catalyst
I. Soga^{1,2}, M. Norimatsu^{1,2}, D. Kondo^{1,2}, Y. Yamaguchi^{1,2,3}, S. Sato^{1,2}, T. Iwai^{1,2,3} and Y. Awano^{1,2,3}, ¹*Fujitsu Labs. Ltd.*, ²*Fujitsu Ltd. and* ³*CREST-JST (Japan)*

P-13-7

Design of Vertical Nanowire FETs
L. E. Wernersson, *Lund Univ. (Sweden)*

P-13-8

In Situ Transmission Electron Microscopy of Deformation of Crystalline C₆₀ Nanotubes
K. Saito¹, R. Kato¹, K. Miyazawa² and T. Kizuka¹, ¹*Univ. of Tsukuba and* ²*NIMS (Japan)*

P-13-9

Growth of vertical GaN Nano-Column on Au Droplet/Si (111) Substrate using Pulsed Flow MOCVD Method
J. C. Song¹, S. H. Lee¹, H. Song¹, S. J. Lee², J. S. Kim¹, K. Santhakumar¹ and C. R. Lee¹, ¹*Chonbuk National Univ. and* ²*Korea Photonics Tech. Inst. (Korea)*

P-13-10

Internal Structure of Vertically Aligned Single-Walled Carbon Nanotube Arrays
E. Einarsson, T. Yamamoto, Y. Ikuhara and S. Maruyama, *Univ. of Tokyo (Japan)*

P-13-11

Control of Electric Conduction of Carbon Nanowalls
W. Takeuchi¹, M. Ura¹, Y. Tokuda², M. Hiramatsu³, H. Kano⁴ and M. Hori¹, ¹*Nagoya Univ.*, ²*Aichi Inst. of Tech.*, ³*Meijo Univ. and* ⁴*NU Eco-Engineering Co., Ltd. (Japan)*

Thursday, September 20

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 12: Spintronic Materials and Devices	Area 5: Advanced Circuits and Systems	Area 7: Photonic Devices and Device Physics
A-5: Junction (15:15-16:25) Chairs: B. Mizuno (Ultimate Junction Technologies Inc.) H. Fukutome (Fujitsu Labs. Ltd.)	B-5: Mobility Characterization (15:15-16:35) Chairs: Y. Kamakura (Osaka Univ.) K. Takeuchi (NEC Corp.)	C-5: Symposium on Magnetic Tunnel Junctions and Beyond (15:15-16:45) Chairs: M. Tanaka (The Univ. of Tokyo) K. Ando (AIST)	D-5: RF CMOS Circuits and Systems (15:15-16:15) Chairs: K. Masu (Tokyo Tech.) T. Matsuoka (Osaka Univ.)	E-5: Special Session: Photonic Crystals and Si Photonics III (15:15-16:30) Chairs: M. Tokushima (NEC Corp.) O. Wada (Kobe Univ.)
15:15 A-5-1(Invited) Study of Dopant Diffusion and Defect Evolution for Advanced Ultra Shallow Junctions based on Atomistic Modeling T. Noda ¹ , W. Vandervorst ² , S. Felch ³ , V. Parihar ³ , C. Vrancken ² , S. Severi ² , T. Y. Hoffmann ² , A. Falpin ² , B. van Daele ² , T. Jannsens ² , H. Bender ² , P. Eyben ² , M. Niwa ¹ , R. Schreutelkamp ³ , F. Nouri ³ , P. P. Absil ² , M. Jurczak ² , K. De Meyer ² and S. Biesemans ² , ¹ Matsushita Electric Industrial Co., Ltd., ² IMEC and ³ AMAT (Japan)	15:15 B-5-1 Experimental Study of Uniaxial Stress Effects on Coulomb-limited Electron and Hole Mobility in Si-MOSFETs S. Kobayashi, M. Saitoh, Y. Nakabayashi and K. Uchida, <i>Toshiba Corp. (Japan)</i>	15:15 C-5-1(Invited) Spin Transfer Torque RAM (STT-RAM) Technology Y. Huai, Z. Diao, Y. Ding, A. Panchula, S. Wang, Z. Li, D. Apalkov, X. Luo, H. Nagai, A. Driskill-Smith and E. Chen, <i>Grandis, Inc. (USA)</i>	15:15 D-5-1(Invited) RF CMOS Circuits- Overview and Perspective T. Tsukahara, <i>Univ. of Aizu (Japan)</i>	15:15 E-5-1 Thermal Modulation of Group Delay of Pillar-Photonic-Crystal Waveguide M. Tokushima, <i>NEC Corp. (Japan)</i>
15:45 A-5-2 Electron Holography Characterization of Ultra-Shallow Junctions in 30-nm Gate-length MOS-FETs N. Ikarashi ¹ , M. Oshida ¹ , M. Miyamura ¹ , M. Saitoh ¹ , A. Mineji ² and S. Shishiguchi ² , ¹ NEC Corp. and ² NEC Electronics Corp. (Japan)	15:35 B-5-2 Physical Mechanism for Hole Mobility Enhancement in (110)-Surface Strained-Si/Strained-SiGe Structures with Anisotropic/Biaxial Strain T. Mizuno ^{1,3} , T. Irisawa ² , N. Hirashita ² , Y. Moriyama ² , T. Tezuka ² , N. Sugiyama ² and S. Takagi ^{1,4} , ¹ MIRAI-AIST, ² MIRAI-ASET, ³ Kanagawa Univ. and ⁴ Univ. of Tokyo (Japan)	15:45 C-5-2(Invited) Structural Study on CoFeB/MgO/CoFeB Magnetic Tunnel Junctions K. Tsunekawa ^{1,2} , Y. Choi ¹ , Y. Nagamine ¹ , H. Maehara ¹ , D. D. Djayaprawira ¹ , T. Takeuchi ² and Y. Kitamoto ² , ¹ Canon ANELVA Corp. and ² Tokyo Tech. (Japan)	15:45 D-5-2(Invited) Compensation techniques for integrated analog device issues A. Matsuzawa, <i>Tokyo Tech. (Japan)</i>	15:30 E-5-2(Invited) Plasmonic Crystals and Nanophotonic Sensing Devices T. A. Kelf ¹ , Y. Sugawara ² , R. M. Cole ³ , N. M. B. Perney ³ , J. J. Baumberg ³ , M. E. Abdelsalam ³ and P. N. Bartlett ³ , ¹ Hokkaido Univ., ² FUJIFILM Corp. and ³ Univ. of Southampton (Japan)

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
F-5: Group-IV Semiconductors II (15:15-16:30) Chairs: K. Nishi (NEC Corp.) H. Yamaguchi (NTT Basic Research Labs.)	G-5: High-Speed Devices and ICs II (15:15-16:15) Chairs: S. Kuroda (Eudyna Devices Inc.) K. Maezawa (Univ. of Toyama)	H-5: Nanowire Growth and Devices I (15:15-16:30) Chairs: J. Motohisa (Hokkaido Univ.) T. Fukui (Hokkaido Univ.)		J-5: PRAM (15:15-16:25) Chairs: M. Moniwa (Renesas Technology Corp.) I. Asano (Elpida Memory, Inc.)
15:15 F-5-1(Invited) Bottom-up approach for the nanopatterning of Si(001) R. Koch, <i>Johannes Kepler Univ. (Austria)</i>	15:15 G-5-1 A 7.6-ps Pulse Generator Using 0.13- μ m InP-based HEMTs for Ultra Wide-Band Impulse Radio Systems Y. Nakasha ¹ , Y. Kawano ¹ , T. Suzuki ¹ , T. Ohki ² , T. Takahashi ¹ , K. Makiyama ¹ , T. Hirose ² and N. Hara ¹ , ¹ Fujitsu Ltd. and ² Fujitsu Labs. Ltd. (Japan)	15:15 H-5-1(Invited) III-V semiconductor hetero-structure nanowires by selective area MOVPE T. Fukui, S. Hara and J. Motohisa, <i>Hokkaido Univ. (Japan)</i>		15:15 J-5-1(Invited) Current Status and Future View of Phase Change Memory Y. Matsui, <i>Hitachi, Ltd. (Japan)</i>
15:45 F-5-2 Plasma Deposition of HfO ₂ and TiO ₂ onto Plasma-Nitrided Ge Surfaces S. Lee ¹ , G. Lucovsky ¹ , J. P. Long ¹ and J. Lüning ² , ¹ North Carolina State Univ. and ² Stanford Synchrotron Research Lab. (USA)	15:30 G-5-2 Novel MOBILE Circuits Using 3 RTDs Operating up to 12.5 Gb/s H. Kim, N. Jeon and K. Seo, <i>Seoul National Univ. (Korea)</i>	15:45 H-5-2 InP Nodes in GaP-based Free-standing Nanowires on Si(111) K. Tateno, G. Zhang, T. Sogawa and H. Nakano, <i>NTT Corp. (Japan)</i>		15:45 J-5-2 Three-Dimensional Electro-Thermal Compact Model for Reset Operation of Phase Change Memories A. Sakai, K. Sonoda, M. Moniwa, K. Ishikawa, O. Tsuchiya and Y. Inoue, <i>Renesas Tech. Corp. (Japan)</i>

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 12: Spintronic Materials and Devices		Area 7: Photonic Devices and Device Physics
16:05 A-5-3 Si _{1-x} Ge _x /Si Selective Etch with HCl for Thin Si-Channel Transistors Integration N. Loubet ¹ , S. Denorme ¹ , A. Pouydebasque ² , F. Leverd ¹ , P. Gouraud ¹ , C. Tallaron ¹ , T. Skotnicki ¹ and D. Dutartre ¹ , ¹ STMicroelectronics and ² NXP Semiconductors (France)	15:55 B-5-3 Behavior of Low-Temperature Phonon-Limited Electron Mobility of Double-Gate Field-Effect Transistor with (111) Si Surface Channel T. Yamamura, S. Sato and Y. Omura, <i>Kansai Univ. (Japan)</i>	16:15 C-5-3(Invited) Giant TMR in CoFeB/MgO/CoFeB Magnetic Tunnel Junctions S. Ikeda ¹ , J. Hayakawa ^{2,1} , Y. M. Lee ^{1,3} , K. Miura ^{2,1} , R. Sasaki ¹ , F. Matsukura ¹ , T. Meguro ¹ and H. Ohno ¹ , ¹ Tohoku Univ., ² Hitachi, Ltd. and ³ Fujitsu Labs. Ltd. (Japan)		16:00 E-5-3 Application of Surface-Plasmon Antenna to Near-Infrared Photodetectors for Optical Communication D. Okamoto, J. Fujikata, K. Nishi and K. Ohashi, <i>NEC Corp. (Japan)</i>
	16:15 B-5-4 Mobility Degradation in (110)-Oriented Ultra-thin Body Double-Gate pMOSFETs with SOI Thickness of less than 5nm K. Shimizu and T. Hiramoto, <i>Univ. of Tokyo (Japan)</i>			16:15 E-5-4 Cavity mode in trilayer Ag/SiO ₂ /Au plasmonic thermal emitter M. W. Tsai, Y. W. Jiang, C. Y. Chen, Y. H. Ye and S. C. Lee, <i>National Taiwan Univ. (Taiwan)</i>
Break				

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
16:00 F-5-3 A Novel Process-Compatible Floating Channel Crystallization Technique to Fabricate High-Performance Poly-Si TFTs C. W. Chang ¹ , J. W. Lee ² , C. L. Chang ¹ and T. F. Lei ¹ , ¹ National Chiao Tung Univ. and ² TSMC (Taiwan)	15:45 G-5-3 Ultra-Short Pulse Generators Using Resonant Tunneling Diodes and Their Integration with Antennas on Ceramic Substrates N. Kamegai ¹ , S. Kishimoto ¹ , K. Maezawa ² , T. Mizutani ¹ , H. Andoh ³ , K. Akamatsu ⁴ and H. Nakata ⁴ , ¹ Nagoya Univ., ² Univ. of Toyama, ³ Toyota National College of Tech. and ⁴ Nippon Mining & Metals Co., Ltd. (Japan)	16:00 H-5-3 CMOS Compatible Si-Nanowire Inverter Logic Gate for Low Power Applications N. Singh, K. D. Buddharaju, S. C. Rustagi, S. H. G. Teo, A. Agarwal, L. Y. Wong, L. J. Tang, C. H. Tung, J. Yu, G. Q. Lo, N. Balasubramanian and D. L. Kwong, <i>Inst. of Microelectronics (Singapore)</i>		16:05 J-5-3 Comprehensive HSPICE Model of Phase Change Memory Cell for Static and Transient Programming D. S. Chao ^{1,2} , Y. K. Chen ³ , Y. B. Liao ³ , M. H. Chiang ³ , C. Lien ² , M. J. Kao ¹ and M. J. Tsai ¹ , ¹ EOL/ITRI, ² National Tsing Hua Univ. and ³ National Ilan Univ. (Taiwan)
16:15 F-5-4 Low Temperature Ultra-thin Hafnium Oxide Dielectrics by Sputtering of Hf Metal on Tilted Substrate Followed by Nitric Acid Oxidation then Anodization Compensation in D. I. Water C. H. Chang and J. G. Hwu, <i>National Taiwan Univ. (Taiwan)</i>	16:00 G-5-4 High Tuning-Range VCO Using a Gated Tunnel Diode M. Årlelid, M. Nilsson, G. Astromskas, E. Lind and L. E. Wernersson, <i>Lund Univ. (Sweden)</i>	16:15 H-5-4 Silicon Nanowire Schottky Barrier NMOS Transistors E. J. Tan ^{1,2,3} , K. L. Pey ¹ , N. Singh ² , G. Q. Lo ² , D. Z. Chi ³ , K. M. Hoe ² , P. S. Lee ¹ and G. D. Cui ¹ , ¹ Nanyang Technological Univ., ² Inst. of Microelectronics and ³ Inst. of Materials Research and Engineering (Singapore)		
Break				

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Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 12: Spintronic Materials and Devices		Area 7: Photonic Devices and Device Physics
A-6: Reliability-II (16:45-18:05) Chairs: K. Shiraishi (Univ. of Tsukuba), Y. Nara (Selete)	B-6: Device Technology (16:45-18:05) Chairs: K. Shibahara (Hiroshima Univ.), H. C. Lin (National Chiao Tung Univ.)	C-6: Symposium on Magnetic Tunnel Junctions and Beyond (17:00-18:00) Chairs: K. Ando (AIST), M. Tanaka (Univ. of Tokyo)		E-6: Detectors and Sensors (16:45-18:00) Chairs: M. Gotoda (Mitsubishi Electric Corp.), M. Sugawara (Fujitsu Labs. Ltd.)
16:45 A-6-1 Effects of O ₂ Plasma Treatment on the Reliabilities of Metal Gate/High-k Dielectric MOSFETs K. T. Lee ^{1,5} , C. Y. Kang ² , R. Choi ² , S. C. Song ² , B. H. Lee ^{2,3} , H. D. Lee ^{4,5} and Y. H. Jeong ¹ , ¹ Pohang Univ. of Sci. and Tech., ² SEMATECH, ³ IBM, ⁴ Chungnam National Univ. and ⁵ Univ. of Texas at Austin (Korea)	16:45 B-6-1 Modeling of Floating-Body Effect in SOI-MOSFET with Complete Surface-Potential Description T. Murakami, M. Ando, N. Sadachika and M. Miura-Mattausch, <i>Hiroshima Univ. (Japan)</i>	17:00 C-6-1(Invited) Giant TMR and future nonvolatile memory S. S. P. Parkin, <i>IBM (USA)</i>		16:45 E-6-1 In(Ga)As Quantum Rings for Terahertz Detectors J. H. Dai, J. H. Lee, Y. L. Lin and S. C. Lee, <i>National Taiwan Univ. (Taiwan)</i>
17:05 A-6-2 The origin of slow and fast trapping under Bias Temperature Instability in HfSiO ₂ MOSFET M. Jo ¹ , H. Park ¹ , M. Chang ¹ , H. S. Jung ² , J. H. Lee ² and H. Hwang ¹ , ¹ GIST and ² Samsung Electronics Co., Ltd. (Korea)	17:05 B-6-2 Device Performance and Reliability Considerations of Biaxially Strained Si by Wafer-Bonding-Technology W. Y. Loh ¹ , D. S. H. Chan ² , D. Y. J. Choo ^{1,2} , S. M. Koh ^{1,2} , R. Yang ¹ , X. W. Zhang ¹ , C. Cai ³ , G. Q. Lo ¹ and D. L. Kwong ¹ , ¹ Inst. of Microelectronics, ² National Univ. of Singapore and ³ IHPC (Singapore)	17:30 C-6-2(Invited) Spin Injection and Transport in Ferromagnet/semiconductor Structures C. J. Palmstrom, <i>Univ. of Minnesota (USA)</i>		17:00 E-6-2 Design of a spin-coherent photo detector for high-fidelity and high-yield photon-spin quantum state transfer Y. Rikitake ^{1,2} , H. Imamura ^{1,2} and H. Kosaka ^{1,3} , ¹ CREST-JST, ² AIST and ³ Tohoku Univ. (Japan)

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
F-6: Group-IV Semiconductors III (16:45-17:45) Chairs: R. Koch (Johannes Kepler Univ.), S. Shimomura (Ehime Univ.)	G-6: Process and Characterization (16:45-18:00) Chairs: A. Nakagawa (New Japan Radio Co., Ltd.), K. J. Chen (Hong Kong Univ. of Sci. and Tech.)	H-6: Nanowire Growth and Devices II (16:45-17:45) Chairs: K. Tateno (NTT), K. Ishibashi (RIKEN)		J-6: ReRAM (16:45-17:55) Chairs: K. Ito (NEC Corp.), Y. Shimamoto (Hitachi Ltd.)
16:45 F-6-1 MBE-grown Ge _{1-x} C _x nanocrystals by using a novel bio-nanoprocess due to protein "ferritin" Y. Nakama, J. Ohta and M. Nunoshita, <i>NAIST (Japan)</i>	16:45 G-6-1 Dynamic response of interface state charges in GaN MIS structures K. Ooyama ^{1,2} , H. Kato ¹ , M. Miczek ¹ and T. Hashizume ¹ , ¹ Hokkaido Univ. and ² Sumitomo Metal Mining (Japan)	16:45 H-6-1 Poly-Si Nanowire Thin-Film Transistors with Inverse-T Gate H. H. Hsu ¹ , H. C. Lin ^{1,2} , J. F. Huang ¹ and C. J. Su ¹ , ¹ National Chiao Tung Univ. and ² National Nano Device Labs. (Taiwan)		16:45 J-6-1(Invited) Current Development Status and Future Challenge of Metal Oxide RRAM Technologies N. Awaya, <i>Sharp Corp. (Japan)</i>
17:00 F-6-2 Enhancement of crystal growth rate of Bio-Nano Crystallization by Pulsed Rapid Thermal Annealing M. Ochi ¹ , Y. Nanjo ¹ , Y. Sugawara ¹ , Y. Uraoka ¹ , T. Fuyuki ¹ , M. Okuda ² and I. Yamashita ^{1,2} , ¹ NAIST and ² Matsushita Electric Industrial Co., Ltd. (Japan)	17:00 G-6-2 Temperature dependence of current-voltage characteristics for AlGaIn-based vertical conducting diodes A. Nishikawa, K. Kumakura and T. Makimoto, <i>NTT Corp. (Japan)</i>	17:00 H-6-2 Strained Ge-rich SiGe Nanowire pFETs with High-k/Metal Gate Fabricated using Germanium Condensation Technique Y. Jiang ^{1,2} , N. Singh ¹ , D. S. H. Chan ² , T. Y. Liow ^{1,2} , W. Y. Loh ¹ , S. Balakumar ¹ , Y. Sun ¹ , G. Q. Lo ¹ and D. L. Kwong ^{1,2} , ¹ Inst. of Microelectronics and ² National Univ. of Singapore (Singapore)		17:15 J-6-2 Elucidation of ReRAM Mechanism and Improvement of Memory Characteristics by HPHA D. Seong, D. Lee, S. Oh, M. Pyun and H. Hwang, <i>GIST (Korea)</i>

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics			Area 7: Photonic Devices and Device Physics
17:25 A-6-3 A Comparative Study of Plasma Source-Dependent Charging Polarity in MOSFETs with High-k and SiO ₂ Gate Dielectrics K. Eriguchi ¹ , M. Kamei ¹ , D. Hamada ¹ , K. Okada ¹ and K. Ono ¹ , ¹ Kyoto Univ. and ² MIRAI-AIST (Japan)	17:25 B-6-3 LDMOS Model for Device and Circuit Optimization M. Yokomichi, M. Miyake, T. Kajiwara, N. Sadachika, A. Yumisaki, H. J. Mattausch and M. Miura-Mattausch, <i>Hiroshima Univ. (Japan)</i>			17:15 E-6-3 Functional Enhancement of Metal-Semiconductor-Metal (MSM) Infrared Photodetectors on Heteroepitaxial SiGe-on-Si Using the Anodic Oxidation/Passivation Method R. W. Chuang ¹ , Z. L. Liao ¹ , H. T. Chiang ¹ and N. Usami ² , ¹ National Cheng Kung Univ. and ² Tohoku Univ. (Taiwan)
17:45 A-6-4 Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs N. Mise, T. Matsuki, T. Watanabe, T. Robata, T. Morooka, T. Eimori and Y. Nara, <i>Selete (Japan)</i>	17:45 B-6-4 A New Insulated Gate Bipolar Transistor Structure employing an Embedded Over-current Protection Device I. H. Ji ¹ , K. H. Cho ¹ , Y. H. Choi ¹ , S. S. Kim ² , K. H. Oh ² , C. M. Yun ² and M. K. Han ¹ , ¹ Seoul National Univ. and ² Fairchild Semiconductor (Korea)			17:30 E-6-4 A MSM Photodetector on p-type GaN for UV Image system H. B. Lee, H. I. Cho, J. H. Lee and S. H. Hahm, <i>Kyungpook National Univ. (Korea)</i>
				17:45 E-6-5 MOVPE Prepared ZnO/Si Heterojunction Diodes with Dual Functions: Light-Emission and UV Photo-Detection J. D. Ye ¹ , S. L. Gu ² , X. W. Sun ^{1,3} , G. Q. Lo ¹ , D. L. Kwong ¹ and Y. D. Zheng ² , ¹ Inst. of Microelectronics, ² Nanjing Univ. and ³ Nanyang Technological Univ. (Singapore)

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"

Thursday, September 20

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 13: Applications of Nanotubes and Nanowires		Area 4: Advanced Memory Technology
17:15 F-6-3 Compositionally Bi-layered Formation of Interfacial Voids in a Porous Anodic Alumina Template Directly Formed on Si H. S. Seo ¹ , Y. G. Jung ¹ , S. W. Jee ¹ , J. M. Yang ² and J. H. Lee ¹ , ¹ Hanyang Univ. and ² National Nanofab Center (Korea)	17:15 G-6-3 Investigations of Metal/Insulator/AlGaIn/GaN Structures by Capacitance-Voltage Measurements and Auger Chemical Profiling B. Adamowicz ¹ , M. Miczek ^{1,2} , T. Hashizume ² , A. Klimasek ¹ , P. Bobek ¹ and J. Żywicki ³ , ¹ Silesian Univ. of Tech., ² Hokkaido Univ. and ³ High-Tech International Services Inc. (Poland)	17:15 H-6-3 High quality Si _{1-x} Gex nanowire and its application to MOSFET integrated with HfO ₂ /TaN/Ta gate stack W. F. Yang ¹ , S. J. Lee ¹ , S. J. Whang ¹ , S. Y. Lim ¹ , B. J. Cho ¹ and D. L. Kwong ² , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)		17:35 J-6-3 Gd doping improved resistive switching characteristics of TiO ₂ -based resistive memory devices L. F. Liu, J. F. Kang, H. Tang, N. Xu, Y. Wang, X.. Y. Liu, X. Zhang and R. Q. Han, <i>Peking Univ. (China)</i>
17:30 F-6-4 Computational Chemistry Study of Diamond-like Carbon: Functions and Structure Control by Frictional Force Y. Morita, T. Shibata, T. Onodera, R. Sahnoun, M. Koyama, H. Tsuboi, N. Hatakeyama, A. Endou, H. Takaba, M. Kubo, C. A. Del Carpio and A. Miyamoto, <i>Tohoku Univ. (Japan)</i>	17:30 G-6-4 Shuttle Activation Annealing of Implanted Al in 4H-SiC T. Watanabe, R. Hattori, M. Imaizumi and T. Oomori, <i>Mitsubishi Electric Corp. (Japan)</i>	17:30 H-6-4 Epitaxial insertion of Au ₅ Si nanodiscs during the growth of silicon nanowires H. D. Um, Y. G. Jung, H. S. Seo, K. T. Park and J. H. Lee, <i>Hanyang Univ. (Korea)</i>		
	17:45 G-6-5 Silicon oxide Gate Dielectric on N-Type 4H-SiC Prepared by Low Thermal Budget Anodization Method K. C. Chuang and J. G. Hwu, <i>National Taiwan Univ. (Taiwan)</i>			

18:30-20:30 Rump Session Room 101(A) "Oxide Electronics -Status and Outlook-"
Room 102(B) "New Materials meet Advanced Silicon Technology"

Friday, September 21

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
A-7 : Metal Gate-II (9:00-10:30) Chairs: T. Nabatame (ASET) K. Shiraishi (Univ. of Tsukuba)	B-7 : Stress Enhancement Technologies (9:00-10:20) Chairs: F. Boeuf (STMicroelectronics) H. Wakabayashi (Sony Corp.)	C-7 : Interconnects for RF and Mixed Signal Application (9:00-10:30) Chairs: Y. Hayashi (NEC Corp.) M. Matsuura (Renesas Technology Corp.)	D-7 : Nano-Bio Devices I (9:00-10:30) Chairs: T. Nishimoto (Shimadzu Corp.) H. Tabata (Univ. of Tokyo)	E-7 : All-Optical Light Control (9:00-10:30) Chairs: R. Akimoto (AIST) Y. Lee (Hitachi, Ltd.)
9:00 A-7-1 (Invited) Schottky Barrier and Stability of Metal/High-k Interfaces; Theoretical View T. Nakayama, <i>Chiba Univ. (Japan)</i>	9:00 B-7-1 NMOS Current Enhancement and Layout Dependency Improvement by Using Atomic Layer Deposition SIN Spacer H. Nagai, K. Ookoshi, H. Morioka, T. Mori, M. Kojima, Y. Takao, M. Kase and K. Hashimoto, <i>Fujitsu Ltd. (Japan)</i>	9:00 C-7-1 Impacts of Cu/TaN Electrode on the Electrical Properties of Metal-insulator-metal (Ba,Sr)TiO ₃ Thin-film Capacitors W. F. Wu ¹ , K. C. Tsai ^{1,2} , C. G. Chao ² , J. T. Lee ² , W. C. Chang ³ , T. K. Kang ³ , G. S. Jheng ¹ and J. Y. Lin ⁴ , ¹ National Nano Device Labs., ² National Chiao Tung Univ., ³ Feng Chia Univ. and ⁴ National Yunlin Univ. of Sci. and Tec. (Taiwan)	9:00 D-7-1 (Invited) Si based Planer Type Ion-channel Biosensor and Its Applications T. Urisu ^{1,2} , H. Uno ² , T. Asano ² , M. Y. Li ¹ , R. Tero ^{1,2} and K. Ishii ³ , ¹ Inst. for Molecular Sci., ² Graduate Univ. for Advanced Studies and ³ Chubu Univ. (Japan)	9:00 E-7-1 (Invited) GaN-Based High-Speed Intersubband Optical Switches N. Iizuka ¹ , K. Kaneko ¹ , N. Suzuki ¹ , C. Kumtornkittikul ² , T. Shimizu ² , M. Sugiyama ² and Y. Nakano ² , ¹ Toshiba Corp. and ² Univ. of Tokyo (Japan)
9:30 A-7-2 Anomalous positive V _{th} shift in HfAlO _x MOS gate stacks W. Wang ¹ , K. Akiyama ² , W. Mizubayashi ¹ , M. Ikeda ² , H. Ota ¹ , T. Nabatame ² and A. Toriumi ^{1,3} , ¹ MIRAI-ASRC, AIST, ² MIRAI-ASET, AIST and ³ Univ. of Tokyo (Japan)	9:20 B-7-2 In-situ Doped Embedded-SiGe Source/Drain Technique for 32 nm-node pMOSFET H. Okamoto, A. Hokazono, K. Adachi, N. Yasutake, H. Itokawa, S. Okamoto, M. Kondo, H. Tsujii, T. Ishida, N. Aoki, M. Fujiwara, S. Kawanaka, A. Azuma and Y. Toyoshima, <i>Toshiba Corp. (Japan)</i>	9:20 C-7-2 Fully Analytical Modeling of Cu Interconnects Up to 110 GHz J. D. Jin ¹ , S. S. H. Hsu ¹ , T. J. Yeh ² , M. T. Yang ² and S. Liu ² , ¹ National Tsing Hua Univ. and ² Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)	9:30 D-7-2 An immunosensor based on N-doped multiwalled carbon nanotubes S. A. Contera, H. J. Burch, M. de Planque, K. Voitchovsky and J. F. Ryan, <i>Univ. of Oxford (UK)</i>	9:30 E-7-2 Characterization of Narrow Mesa Width Waveguide for All Optical Switching Device Based on Intersubband Transition in II-VI Based Quantum Wells K. Akita, R. Akimoto, C. Guangwei, T. Hasama and H. Ishikawa, <i>AIST (Japan)</i>

Friday, September 21

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications		Area 4: Advanced Memory Technology
F-7 : Material Characterization (9:00-10:15) Chairs: K. Kobayashi (Waseda Univ.) T. Iwai (Fujitsu Labs. Ltd.)	G-7 : Emerging Devices (9:00-10:30) Chairs: T. Hashizume (Hokkaido Univ.) R. Hattori (Mitsubishi Electric Corp.)	H-7 : Organic Transistor I (9:00-10:30) Chairs: T. Minakata (Asahi-KASEI Corp.) K. Fujita (Kyushu Univ.)		J-7 : DRAM II (9:00-10:20) Chairs: I. Asano (Elpida Memory, Inc.) M. Moniwa (Renesas Technology Corp.)
9:00 F-7-1 (Invited) In-Situ X-Ray Diffraction during Semiconductor Nanostructure Growth M. Takahashi, <i>JAEA (Japan)</i>	9:00 G-7-1 (Invited) Growth of InAs Channel HEMT Structure on Si substrate and It's Possible Application for Low Power Logic E. Y. Chang, H. Yamaguchi, Y. C. Lin, M. Ueki, Y. Hirayama and C. Y. Chang, <i>National Chiao Tung Univ. (Taiwan)</i>	9:00 H-7-1 (Invited) Jet-pinted Polymer Transistor Display Backplanes R. A. Street, A. C. Arias and J. H. Daniel, <i>Palo Alto Research Center (USA)</i>		9:00 J-7-1 Ru/TiO ₂ /ZrO ₂ /TiN (RIT-TiO ₂ /ZrO ₂) Capacitor Structure for the 50nm DRAM Device and beyond J. S. Lim, K. C. Kim, K. H. Lee, J. H. Choi, Y. S. Tak, W. D. Kim, J. Y. Kim, K. Cho, Y. Kim, J. H. Chung, Y. S. Kim, S. T. Kim and W. Han, <i>Samsung Electronics Co.,Ltd. (Korea)</i>
9:30 F-7-2 <i>In situ</i> Analysis for Initial Formation Process of Gold Nanoparticles in Discharge in Aqueous Solution C. Miron ¹ , M. A. Bratescu ² , T. Ishizaki ¹ , N. Saito ¹ and O. Takai ² , ¹ Nagoya Univ. and ² EcoTopia Sci. Inst. (Japan)	9:30 G-7-2 N-channel MOSFETs with <i>In-situ</i> Silane-Passivated Gallium Arsenide Channel and CMOS-Compatible Palladium-Germanium Contacts H. C. Chin ¹ , M. Zhu ¹ , K. M. Hoe ² , G. S. Samudra ¹ and Y. C. Ye ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)	9:30 H-7-2 Frequency Dependence of Displacement Current and Channel Current in Pentacene Thin-Film Transistors S. Suzuki, Y. Yasutake and Y. Majima, <i>Tokyo Tech. (Japan)</i>		9:20 J-7-2 Electrical Properties of TiO/LaTiO/TiO Stacked Thin Films H. Hara ¹ , M. Tanioku ² , M. Yamato ¹ and T. Kikkawa ¹ , ¹ Hiroshima Univ. and ² Elpida Memory, Inc. (Japan)

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
9:50 A-7-3 Effect of Ultra-thin Al ₂ O ₃ Insertion on Fermi-level Pinning at Metal/Ge Interface T. Nishimura, K. Kita and A. Toriumi, <i>Univ. of Tokyo (Japan)</i>	9:40 B-7-3 Principal Guideline of Stress Design for Ion Enhancement in Advanced MOSFET Structure with Dual Stress Liner Technique M. Nishikawa ¹ , H. Nomura ¹ , T. Miyashita ² , M. Kojima ¹ , Y. Takao ¹ and K. Hashimoto ¹ , ¹ Fujitsu Ltd. and ² Fujitsu Labs. Ltd. (Japan)	9:40 C-7-3 A Small Area, 3-Dimensional On-chip Inductors for High-speed Signal Processing under Low Power Supply Voltages K. Hijioka, A. Tanabe, Y. Amamiya and Y. Hayashi, <i>NEC Corp. (Japan)</i>	9:45 D-7-3 Reverse Electroporation with Carbon Nanotubes-loaded Electrode for Highly Efficient Gene Transfer Y. Inoue ¹ , H. Fujimoto ¹ , T. Ogino ² and H. Iwata ¹ , ¹ Kyoto Univ. and ² Yokohama National Univ. (Japan)	9:45 E-7-3 Saturation characteristics simulation of Intersubband absorption for [(CdS/ZnSe/BeTe)/(ZnSe/BeTe)] coupled quantum wells G. W. Cong, R. Akimoto, K. Akita, T. Hasama and H. Ishikawa, <i>AIST (Japan)</i>
10:10 A-7-4 Systematic studies on Fermi level pinning of Hf-based high-k gate stacks K. Shiraiishi ^{1,2} , Y. Akasaka ^{3,1,7} , G. Nakamura ^{3,7} , M. Kadoshima ³ , H. Watanabe ⁴ , K. Ohmori ⁵ , T. Chikyow ⁶ , K. Yamabe ¹ , Y. Nara ³ , Y. Ohji ³ and K. Yamada ⁵ , ¹ Univ. of Tsukuba, ² CREST-JST, ³ SELETE, ⁴ Osaka Univ., ⁵ Waseda Univ., ⁶ NIMS and ⁷ Tokyo Electron Inc. (Japan)	10:00 B-7-4 Study of Stress from Discontinuous SiN Liner for Fully-Silicided Gate Process T. Yamashita ^{1,2} , Y. Nishida ¹ , T. Okagaki ¹ , Y. Miyagawa ¹ , J. Yugami ¹ , H. Oda ¹ , Y. Inoue ¹ and K. Shibahara ² , ¹ Renesas Tech. Corp. and ² Hiroshima Univ. (Japan)	10:00 C-7-4 (Invited) Wiring technology for analog and mixed signal LSIs A. Matsuzawa, <i>Tokyo Tech. (Japan)</i>	10:00 D-7-4 Rapid and High Sensitive Detection of Bacteria Sensor using a Porous Ion Exchange Film K. Miyano ¹ , H. Aoki ¹ , S. Hotta ¹ , N. Fujiwara ² , D. Yano ³ , K. Sano ³ , K. Yamanaka ³ , C. Kimura ¹ and T. Sugino ¹ , ¹ Osaka Univ., ² TRI-Osaka and ³ Organo Corp. (Japan)	10:00 E-7-4 Magneto-Optical (Cd,Mn)Te/(Cd,Zn)Te Quantum Well Waveguide with Broadband Operation Optical Isolator M. C. Debnath, V. Zayets and K. Ando, <i>AIST (Japan)</i>
	10:20 B-7-5 Strained N-channel FinFETs with High-stress Nickel Silicide-Carbon Contacts and Integration with FUSI Metal Gate Technology T. Y. Liow ^{1,2} , R. T. P. Lee ¹ , K. M. Tan ¹ , M. Zhu ¹ , K. M. M. Hoe ² , G. S. Samudra ¹ , N. Balasubramanian ² and Y. C. Ye ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)		10:15 D-7-5 Ion-Sensitive Field Effect Transistor Based on Silicon and Zinc Oxide for DNA Sensor M. Seki, T. Uno, M. Noguchi and H. Tabata, <i>Univ. of Tokyo (Japan)</i>	10:15 E-7-5 Passive Optical Alignment with High Accuracy for Low-Loss Optical Interposer M. Fujiwara ^{1,2} , S. Terada ¹ , Y. Shirato ¹ , H. Owari ¹ , K. Watanabe ¹ , M. Matsuyama ¹ , K. Takahama ¹ , T. Mori ¹ , K. Miyao ¹ , K. Choki ¹ , T. Fukushima ² , T. Tanaka ² and M. Koyanagi ² , ¹ Sumitomo Bakelite Co., Ltd and ² Tohoku Univ. (Japan)

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 8: Advanced Material Synthesis and Crystal Growth Technology	Area 6: Compound Semiconductor Circuits, Electron Devices and Device Physics	Area 10: Organic Materials Science, Device Physics, and Applications		Area 4: Advanced Memory Technology
9:45 F-7-3 Scanning Surface Hall Potentiometry on Semiconductor Wafers Y. Hidaka, D. Maruyama, J. Uchikoshi, M. Morita and K. Arima, <i>Osaka Univ. (Japan)</i>	9:45 G-7-3 Improved electrical characteristics of Pt/Gd ₂ O ₃ /GaAs MOS capacitors with surface preparation procedures C. C. Cheng ¹ , C. H. Chien ^{1,2} , G. L. Luo ² , C. K. Tseng ¹ , H. C. Chiang ¹ , C. H. Yang ² and C. Y. Chang ¹ , ¹ National Chiao Tung Univ. and ² National Nano Device Labs. (Taiwan)	9:45 H-7-3 Analysis of charge accumulation in pentacene field effect transistor with ferroelectric gate insulator on the basis of Maxwell-Wagner model R. Tamura, S. Yoshita, E. Lim, T. Manaka and M. Iwamoto, <i>Tokyo Tech. (Japan)</i>		9:40 J-7-3 Nitrogen Profile Study for SiON Gate Dielectrics of Advanced DRAM S. Murakawa ^{1,2} , M. Takeuchi ³ , M. Honda ³ , S. Ishizuka ³ , T. Nakanishi ³ , Y. Hirota ³ , T. Sugawara ¹ , Y. Tanaka ¹ , Y. Akasaka ¹ , A. Teramoto ² , S. Sugawa ² and T. Ohmi ² , ¹ Tokyo Electron Ltd., ² Tohoku Univ. and ³ Tokyo Electron AT Ltd. (Japan)
10:00 F-7-4 Investigation of FePt Nano-Dots Fabricated by Self-Assembled Nano-Dot Deposition Method Using X-ray Photoelectron Spectroscopy M. Murugesan ¹ , J. C. Bea ¹ , C. K. Yin ² , H. Nohira ³ , E. Ikenaga ⁴ , T. Hattori ³ , M. Nishijima ² , T. Fukushima ² , T. Tanaka ² , M. Miyao ⁵ and M. Koyanagi ² , ¹ JST, ² Tohoku Univ., ³ Musashi Inst. of Tech., ⁴ JASRI and ⁵ Kyushu Univ. (Japan)	10:00 G-7-4 Performance and Stability of ZnO/ZnMgO Hetero-MIS FETs S. Sasa, T. Hayafuji, M. Kawasaki, K. Koike, M. Yano and M. Inoue, <i>Osaka Inst. of Tech. (Japan)</i>	10:00 H-7-4 An Analytic Current-Voltage Equation for Top-contact OTFTs Including the Effects of Variable Series Resistance K. D. Jung, B. J. Kim, Y. C. Kim, B. G. Park, H. Shin and J. D. Lee, <i>Seoul National Univ. (Korea)</i>		10:00 J-7-4 Effect of Boron-Nitride Formation at the Interface of Diffusion Barrier in Tungsten Polymetal Gate Stacks on Gate Interfacial Resistance M. G. Sung, K. Y. Lim, Y. S. Kim, H. J. Cho, S. R. Lee, S. A. Jang, M. S. Joo, J. H. Lee, T. Y. Kim, T. O. Youn, J. H. Kim, G. O. Kim, Y. T. Hwang, H. S. Yang, J. C. Ku and J. W. Kim, <i>Hynix Semiconductor Inc. (Korea)</i>
	10:15 G-7-5 The Effect of Rapid Thermal Annealing on the Electrical Characteristics of ZnO TFTs K. Remashan, D. K. Hwang, S. J. Park and J. H. Jang, <i>GIST (Korea)</i>	10:15 H-7-5 Potential Fluctuation within a Crystalline Domain in Pentacene Thin Film Transistors and its Origin N. Ohashi, H. Tomii, R. Matsubara, M. Sakai, K. Kudo and M. Nakamura, <i>Chiba Univ. (Japan)</i>		

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Break

Area 1: Advanced Gate Stack/Si Processing Science

A-8 : High-k/Metal Gate Transistor (10:45-12:05)
Chairs: H. Fukutome (Fujitsu Labs. Ltd.)
Y. Tsunashima (Toshiba Corp.)

10:45 A-8-1

Production-Worthy HfSiON Gate Dielectric Fabrication Enabling EOT Scalability Down to 0.86 nm and Excellent Reliability by Polyatomic Layer Chemical Vapor Deposition Technique
D. Ishikawa¹, S. Kamiyama¹, A. Sano², S. Horii², T. Aoyama¹ and Y. Nara¹, ¹Selete and ²Hitachi Kokusai Electric Inc. (Japan)

11:05 A-8-2

Tinv Scaling and Jg Reducing for nMOSFET with HfSi₂/HfO₂ Gate Stack by Interfacial Layer Formation Using Ozone Water Treatment Process
I. Oshiyama¹, K. Tai¹, T. Hirano¹, S. Yamaguchi¹, K. Tanaka¹, Y. Hagimoto¹, T. Uemura¹, T. Ando¹, K. Watanabe¹, R. Yamamoto¹, S. Kanda¹, J. Wang¹, Y. Tateshita¹, H. Wakabayashi¹, Y. Tagawa¹, M. Tsukamoto¹, H. Iwamoto¹, M. Saito¹, M. Oshima², S. Toyoda², N. Nagashima¹ and S. Kadomura¹, ¹Sony Corp. and ²Univ. of Tokyo (Japan)

Area 3: CMOS Devices/Device Physics

B-8 : Modeling and Simulation (10:45-12:25)
Chairs: A. Hokazono (Toshiba Corp.)
Y. Momiyama (Fujitsu Labs. Ltd.)

10:45 B-8-1

Capacitive Parameter Extraction for Nanometer-Size Field-Effect Transistors
H. Inokawa¹, A. Fujiwara², K. Nishiguchi² and Y. Ono², ¹Shizuoka Univ. and ²NTT Corp. (Japan)

11:05 B-8-2

Study of Parasitic Resistance Behavior and Its Extraction Method on Deeply Scaled MOSFETs
H. Tsujii, A. Hokazono, M. Fujiwara, S. Kawanaka, A. Azuma, N. Aoki and Y. Toyoshima, *Toshiba Corp. (Japan)*

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-8 : Interconnect Reliability (10:45-12:15)
Chairs: K. Ueno (Shibaura Inst. of Technology)
M. Kodera (Toshiba Corp.)

10:45 C-8-1 (Invited)

Stress Migration Phenomenon in Narrow Copper Interconnects
T. Nakamura and T. Suzuki, *Fujitsu Labs. Ltd. (Japan)*

11:15 C-8-2

Improvement of Adhesion at the Interface between Low-k Spin-on Dielectric and underlying SiCO Barrier by Plasma Treatments
Y. Takigawa, S. Nakao, M. Shiohara, N. Oda and S. Ogawa, *Selete (Japan)*

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

D-8 : Nano-Bio Devices II (10:45-12:15)
Chairs: I. Yamashita (Nara Inst. of Sci. and Tech.)
S. Antoranz Contera (Univ. of Oxford)

10:45 D-8-1 (Invited)

Bio-Nano Approaches to Fabrication of Quantum Dot Floating Gate Flash Memories
S. K. Banerjee¹, S. Tang¹, C. Mao², J. Sarkar¹, H. Liu¹, D. Shahrjerdi¹, C. H. Lee¹ and J. D. Trent³, ¹Univ. of Texas at Austin, ²Univ. of Oklahoma and ³NASA Ames Research Center (USA)

11:15 D-8-2

Floating Gate MOS Capacitor with High-Density Nanodots Array Produced by Protein Supramolecule
K. Yamada^{1,2}, S. Yoshii¹, S. Kumagai¹, A. Miura², Y. Uraoka², T. Fuyuki² and I. Yamashita^{1,2,3}, ¹Matsushita Electric Industrial Co., Ltd., ²NAIST and ³CREST-JST (Japan)

Area 7: Photonic Devices and Device Physics

E-8 : Lasers and LEDs (10:45-12:15)
Chairs: M. Ezaki (Toshiba Corp.)
M. Gotoda (Mitsubishi Electric Corp.)

10:45 E-8-1 (Invited)

Widely Tunable Integrated DBR Laser Array with Fast Wavelength Switching
S. Tsuji^{1,2}, H. Arimoto^{1,2}, T. Tsuchiya^{1,2}, T. Kitatani^{1,2}, K. Shinoda^{1,2}, T. Otoshi¹ and M. Aoki^{1,2}, ¹Hitachi, Ltd. and ²OITDA (Japan)

11:15 E-8-2

High Density Two Dimensional LED Arrays Using Single Crystal Semiconductor Thin Films
T. Suzuki, H. Fujiwara, T. Sagimori, T. Igari, H. Furuta, Y. Nakai, I. Abiko, M. Sakuta and M. Ogihara, *Okii Digital Imaging Corp. (Japan)*

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Break

Area 10: Organic Materials Science, Device Physics, and Applications

H-8 : Organic Transistor II (10:45-12:15)
Chairs: K. Nomoto (Sony Corp.)
K. Kudo (Chiba Univ.)

10:45 H-8-1

Hall effect measurements of polycrystalline pentacene TFTs with double gate structures
Y. Takamatsu, T. Sekitani and T. Someya, *Univ. of Tokyo (Japan)*

11:00 H-8-2

Probing of channel formation in organic field effect transistors by optical second harmonic generation measurement
E. Lim, H. S. Lee, T. Manaka and M. Iwamoto, *Tokyo Tech. (Japan)*

Area 9: Physics and Applications of Novel Functional Materials and Devices

I-8 : Novel Nanostructure Devices (10:45-12:00)
Chairs: M. Watanabe (Tokyo Tech.)
H. Mizuta (Tokyo Tech.)

10:45 I-8-1

Self-Assembling Formation of Ni Nanodots on SiO₂ Induced by Remote H₂ -plasma Treatment and Their Electrical Charging Characteristics
K. Makihara, K. Shimanoe, M. Ikeda, S. Higashi and S. Miyazaki, *Hiroshima Univ. (Japan)*

11:00 I-8-2

Reduction of a Ferritin Core Embedded in Silicon Oxide Film for An Application to Floating Gate Memory
T. Matsumura¹, A. Miura¹, Y. Uraoka¹, T. Fuyuki¹, S. Yoshii^{2,3} and I. Yamashita^{1,2,3}, ¹NAIST, ²Matsushita Electric Industrial Co., Ltd. and ³CREST-JST (Japan)

Area 4: Advanced Memory Technology

J-8 : FeRAM/MRAM (10:45-12:05)
Chairs: T. Eshita (Fujitsu Ltd.)
H. Jeong (Samsung Electronics Co. Ltd.)

10:45 J-8-1

Improvement of Thermal Stability of MRAM Device with SiN Protective Film Deposited by HDP CVD
K. Suemitsu¹, Y. Kawano², H. Utsumi¹, H. Honjo¹, R. Nebashi¹, S. Saito¹, N. Ohshima¹, T. Sugibayashi¹, H. Hada¹, T. Nohisa², T. Shimazu², M. Inoue² and N. Kasai¹, ¹NEC Corp. and ²Mitsubishi Heavy Industries, Ltd. (Japan)

11:05 J-8-2

Two-Dimensional Electron Gas Switching in an Ultra Thin Epitaxial ZnO Layer on a Ferroelectric Gate Structure
Y. Kaneko, H. Tanaka, Y. Kato and Y. Shimada, *Matsushita Electric Industrial Co., Ltd. (Japan)*

Friday, September 21

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
11:25 A-8-3 Highly manufacturable CMOSFETs with Single High-k (HfLaO) and Dual Metal Gate Integration Process X. P. Wang ^{1,2,3} , M. F. Li ^{1,2,4} , H. Y. Yu ³ , J. J. Yang ¹ , C. X. Zhu ¹ , W. S. Hwang ¹ , W. Y. Loh ² , A. Y. Du ² , J. D. Chen ^{1,2} , A. Chin ⁵ , S. Biesemans ³ , G. Q. Lo ² and D. L. Kwong ² , ¹ National Univ. of Singapore, ² Inst. of Microelectronics, ³ IMEC, ⁴ Fudan Univ. and ⁵ National Chiao Tung Univ. (Singapore)	11:25 B-8-3 Two-step Inverse Modeling for Estimation of Channel Impurity Pile-up T. Nagumo ¹ , K. Takeuchi ¹ , Y. Akiyama ² and M. Hane ¹ , ¹ NEC Corp. and ² NEC Electronics Corp. (Japan)	11:35 C-8-3 Effect of temperature and film thickness on resistivity of CoWP J. Gambino ¹ , F. Chen ¹ , S. Mongeon ¹ , D. Meatyrd ¹ , E. Adams ¹ , P. Dehaven ¹ , C. Cabral ² and I. Ivanov ³ , ¹ IBM, ² IBM T. J. Watson Research Center and ³ Blue29, LLC (USA)	11:30 D-8-3 Label Free Electrical Detection of Single Nucleotide Polymorphisms using Nanowire Biosensors E. S. Selamat ^{1,2} , A. Agarwal ¹ , N. Balasubramanian ¹ and W. T. Liu ^{1,2} , ¹ Inst. of Microelectronics and ² National Univ. of Singapore (Singapore)	11:30 E-8-3 Improvement of Kink-Free Light Output for Fiber Pump Semiconductor Lasers N. Shomura and T. Numai, <i>Ritsumeikan Univ. (Japan)</i>
11:45 A-8-4 Highly Manufacturable and Cost-effective Single Ta _x C / Hf _z Zr _(1-x) O ₂ Gate CMOS Bulk Platform for LP Applications at the 45nm Node and Beyond M. Müller ^{1,4} , C. Hobbs ² , A. Zauner ¹ , S. Barnola ² , T. Salveta ⁵ , S. Lhostis ³ , S. Couderc ³ , P. Perreau ⁵ , D.H. Triyoso ² , M. Raymond ² , E. Luckowski ² , M. Rafik ³ , A. Cathignol ³ , G. Ribes ³ , D. Fleury ³ , K. Romanjek ¹ , S. Pokrant ¹ , S. Jullian ¹ , P. Morin ³ , M. Aminpur ² , P. Gouraud ³ , C. Laviro ⁵ , S. Zoll ³ , P. Garnier ¹ and F. Salvetti ¹ , ¹ NXP Semiconductors, ² Freescale, ³ STMicroelectronics, ⁴ NXP Semiconductors Research and ⁵ CEA-LETI (France)	11:45 B-8-4 Discrete-Dopant-Fluctuated Threshold Voltage Roll-Off in Sub-16nm Bulk FinFETs Y. Li, C. H. Hwang, H. M. Huang and T. C. Yeh, <i>National Chiao Tung Univ. (Taiwan)</i>	11:55 C-8-4 Highly Reliable Cu Interconnect using Low Hydrogen Silicon Nitride Film Deposited at Low Temperature for Cu-Diffusion Barrier T. Murata, K. Kono, Y. Tsunemine, M. Fujisawa, M. Matsuura, K. Asai and M. Kojima, <i>Renesas Tech. Corp. (Japan)</i>	11:45 D-8-4 Microfluidic Amperometric Biochips Based on Carbon Nanotube Arrayed Electrodes Y. Tsujita ¹ , K. Maehashi ¹ , K. Matsumoto ¹ , H. Kwon ² , Y. Takamura ² and E. Tamiya ¹ , ¹ Osaka Univ. and ² JAIST (Japan)	11:45 E-8-4 Multiwavelength emitting InGaN/GaN quantum well grown on V-shaped GaN (1101) microfacet J. W. Ju ¹ , L. W. Jang ¹ , S. J. Lee ² , J. H. Baek ² and I. H. Lee ¹ , ¹ Chonbuk National Univ. and ² Korea Photonics Tech. Inst. (Korea)

Friday, September 21

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
		Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
		11:15 H-8-3 Study of Pentacene-Based Organic Thin Film Transistor with PMMA as Insulator T. S. Huang, Y. K. Su and B. C. Wang, <i>National Cheng Kung Univ. (Taiwan)</i>	11:15 I-8-3 Characterization of Multistep Electron Charging and Discharging of Silicon-Quantum-Dots Floating Gate by Applying Pulsed Gate Biases R. Matsumoto, M. Ikeda, S. Higashi and S. Miyazaki, <i>Hiroshima Univ. (Japan)</i>	11:25 J-8-3 Manufacturable High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process K. R. Udayakumar ¹ , T. S. Moise ¹ , S. R. Summerfelt ¹ , K. Boku ¹ , J. Rodriguez ¹ , K. Remack ¹ , J. Gertas ¹ , M. Arendt ¹ , G. Shinn ¹ , J. Eliason ² , R. Bailey ² and P. Staubs ² , ¹ Texas Instruments Inc. and ² Ramtron International Corp. (USA)
		11:30 H-8-4 Transient Current Characteristics of Organic Field Effect Transistors with Polymer and Inorganic Gate Insulators K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, T. Kodzasa and T. Kamata, <i>AIST (Japan)</i>	11:30 I-8-4 Photon Position Detector Consisting of Single-Electron Devices A. K. Kikombo ¹ , M. Tabe ² and Y. Amemiya ¹ , ¹ Hokkaido Univ. and ² Shizuoka Univ. (Japan)	11:45 J-8-4 Endurance Characterization of Ferroelectric Cell in 64Mb FRAM Device By Analyzing the Space Charge Concentration E. S. Lee, Y. M. Kang, D. J. Jung, H. H. Kim, Y. K. Hong, J. H. Park, S. K. Kang, J. H. Kim, H. S. Kim, W. W. Jung, W. S. Ahn, J. Y. Jung, J. Y. Kang, D. Y. Choi, H. K. Goh, S. Y. Kim, S. Y. Lee and H. S. Jeong, <i>Samsung Electronics Co., Ltd. (Korea)</i>

Friday, September 21

Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
			12:00 D-8-5 Fabrication of single electron transistor using cage-shaped protein supramolecule S. Kumagai ¹ , S. Yoshii ¹ , N. Matsukawa ¹ , R. Tsukamoto ³ , K. Nishio ¹ and I. Yamashita ^{1,2,3} ¹ Matsushita Electric Industrial Co., Ltd, ² NAIST and ³ Core Research for Evolutional Sci. and Tech. (Japan)	12:00 E-8-5 Realization of 340nm-band high-power (>7mW) InAlGaN quantum well UV-LED with p-type InAlGaN S. Fujikawa ¹ , T. Takano ^{1,2} , Y. Kondo ^{1,2} and H. Hirayama ¹ , ¹ RIKEN and ² Matsushita Electric Works, Ltd. (Japan)

Friday, September 21

Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
		Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 4: Advanced Memory Technology
		11:45 H-8-5 Mobility Improvement of Pentacene Thin Film Transistors by Introduction of H ₂ during Evaporation T. Yokoyama, C. B. Park, Y. Kikuchi, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)	11:45 I-8-5 Improved Photoconduction Effects of Nanometer-Sized Si Dot Multilayers Y. Hirano ¹ , S. Yamazaki ² and N. Koshida ² , ¹ NHK Sci. and Technical Research Labs. and ² Tokyo Univ. of Agriculture and Tech. (Japan)	
		12:00 H-8-6 Evidence of Electron Trapping Center at Pentacene/SiO ₂ Interface C. B. Park, T. Yokoyama, T. Nishimura, K. Kita and A. Toriumi, Univ. of Tokyo (Japan)		

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Lunch

Area 1: Advanced Gate Stack/Si Processing Science

A-9 : FUSI (13:15-14:55)
Chairs: T. Tatsumi (NEC Corp.)
T. Nabatame (ASET)

13:15 A-9-1
Practical Solutions to Enhance EWF Tunability of Ni FUSI Gates on HfO₂
X. P. Wang^{1,2,3}, J. J. Yang¹, H. Y. Yu³, M. F. Li^{1,2,4}, J. D. Chen¹, R. L. Xie¹, C. X. Zhu¹, A. Y. Du², P. C. Lim⁵, A. Lim^{1,2}, Y. Y. Mi⁵, D. M. Y. Lai⁵, W. Y. Loh², S. Biesemans³, G. Q. Lo² and D. L. Kwong²,
¹National Univ. of Singapore, ²Inst. of Microelectronics, ³IMEC, ⁴Fudan Univ. and ⁵Inst. of Materials Research and Engineering (Singapore)

13:35 A-9-2
Effectiveness of Aluminum Incorporation in Nickel Silicide and Nickel Germanide Metal Gates for Work Function Reduction
A. E. J. Lim¹, R. T. P. Lee¹, A. T. Y. Koh¹, G. S. Samudra¹, D. L. Kwong² and Y. C. Ye¹,
¹National Univ. of Singapore and ²Inst. of Microelectronics (Singapore)

Area 3: CMOS Devices/Device Physics

B-9 : Post Planar CMOS (13:15-14:55)
Chairs: A. Hokazono (Toshiba Corp.)
H. Sayama (Renesas Technology Corp.)

13:15 B-9-1
Wide-Range V_{th} Controllable SOTB (Silicon on Thin BOX) Integrated with Bulk CMOS Featuring Fully Silicided NiSi Gate Electrode
T. Ishigaki¹, R. Tsuchiya¹, Y. Morita¹, N. Sugii¹, S. Kimura¹, T. Iwamatsu², T. Ipposhi², Y. Inoue² and T. Hiramoto³,
¹Hitachi, Ltd., ²Renesas Tech. Corp. and ³Univ. of Tokyo (Japan)

13:35 B-9-2
Additivity between SSOI- and CESL-induced nMOSFETs Performance Boosts
F. Andrieu¹, F. Allain¹, C. Buj-Dufournet¹, O. Faynot¹, F. Rochette¹, M. Cassé¹, V. Delaye¹, F. Aussenac¹, L. Tosti¹, P. Maury¹, L. Vandroux¹, N. Daval², I. Cayrefourcq³ and S. Deleonibus¹,
¹CEA-LETI MINATEC and ²SOITEC (France)

Area 2: Characterization and Materials Engineering for Interconnect Integration

C-9 : Low-k and Airgap (13:15-15:05)
Chairs: J. Koike (Tohoku Univ.)
J. Gambino (IBM)

13:15 C-9-1 (Invited)
Low-k/Cu Integration Consistent from 90 nm thru 32 nm
T. Nogami, *IBM (USA)*

13:45 C-9-2
Influences of Skeletal Structure and Porosity on Dielectric and Mechanical Properties of Porous Organosilica Low-k Films
S. Takada, N. Hata, Y. Seino and T. Yoshino, *AIST (Japan)*

Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)

D-9 : Spectroscopy for Bio Sensing (13:15-14:45)
Chairs: K. Ajito (NTT)
M. Niwano (Tohoku Univ.)

13:15 D-9-1 (Invited)
THz and microwave biochip
C. K. Sun, *National Taiwan Univ. (Taiwan)*

13:45 D-9-2
In-Situ Detection and Classification of DNA by Porous Alumina Filter in Conjugation with Infrared Absorption Spectroscopy
R. Yamaguchi, A. Hirano, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, *Tohoku Univ. (Japan)*

Area 7: Photonic Devices and Device Physics

E-9 : LEDs (13:15-15:00)
Chairs: Y. Lee (Hitachi Ltd.)
M. Ezaki (Toshiba Corp.)

13:15 E-9-1
High-Brightness Ultraviolet LEDs on Si Using Quaternary InAlGa_{0.5}N Multi-Quantum-Wells with High Indium Contents
Y. Fukushima, Y. Takase, M. Usuda, K. Orita, T. Ueda and T. Tanaka, *Matsushita Electric Industrial Co., Ltd. (Japan)*

13:30 E-9-2
Effect of Multiquantum Barriers on Carrier Transport Mechanism of InGa_{0.5}N/GaN Multiple Quantum Well Light-emitting Diodes
W. T. Su¹, Y. F. Chen¹, H. Y. Chen¹, J. C. Wang¹, H. T. Shen¹, T. E. Nee¹ and Y. F. Wu²,
¹Chang Gung Univ. and ²Tech. and Sci. Inst. of Northern Taiwan (Taiwan)

Friday, September 21

Room 202B (F) Room 303 (G) Room 304 (H) Room 405 (I) Room 406 (J)

Lunch

Area 1: Advanced Gate Stack/Si Processing Science

F-9 : Characterization (13:15-14:55)
Chairs: S. Miyazaki (Hiroshima Univ.)
H. Hwang (Gwangju Inst. of Science & Engineering)

13:15 F-9-1
Advanced Characterization of High-k Gate Stack by Internal Photo Emission (IPE): Interfacial Dipole and Band Diagram in Al/Hf(Si)O₂/Si MOS Structure
J. Widiez, K. Kita, T. Nishimura and A. Toriumi, *Univ. of Tokyo (Japan)*

13:35 F-9-2
Characterization of the Sc₂O₃/La₂O₃ High-k Gate Stack by STM
Y. C. Ong¹, D. S. Ang¹, S. J. O' Shea², K. L. Pey¹, T. Kawanago³, K. Kakushima³ and H. Iwai³,
¹Nanyang Technological Univ., ²Inst. of Material Research and Engineering and ³Tokyo Tech. (Singapore)

Area 5: Advanced Circuits and Systems

G-9 : Imaging Technology (13:15-14:35)
Chairs: H. Yamauchi (Samsung Electronics Co., Ltd.)
T. Matsuoka (Osaka Univ.)

13:15 G-9-1
Real-Time Variable-Resolution and Dynamic Range Boosting CMOS Image Sensor
J. J. Wang, C. J. Lin and Y. C. King, *National Tsing Hua Univ. (Taiwan)*

13:35 G-9-2
High Sensitivity Dynamic Range Enhanced CMOS Imager with Noise Suppression
S. Adachi¹, W. Lee², N. Akahane², H. Oshikubo¹, K. Mizobuchi¹ and S. Sugawa²,
¹Texas Instruments Japan and ²Tohoku Univ. (Japan)

Area 10: Organic Materials Science, Device Physics, and Applications

H-9 : Organic Transistor III (13:15-14:45)
Chairs: T. Kamata (AIST)
T. Someya (Univ. of Tokyo)

13:15 H-9-1 (Invited)
Vertical Type Organic Transistors for Flexible Opto-electric Devices
K. Kudo, *Chiba Univ. (Japan)*

13:45 H-9-2
Highly Reliable Bottom-Contact Pentacene TFTs with a Poly(p-chloroxylylene) Layer Selectively Grown on a Gate-Insulator
R. Yasuda¹, N. Hirai¹, I. Yagi¹, K. Nomoto¹, J. Kasahara¹, T. Minari², K. Tsukagoshi² and Y. Aoyagi²,
¹Sony Corp. and ²RIKEN (Japan)

Area 9: Physics and Applications of Novel Functional Materials and Devices

I-9 : Quantum Dots and Qubits (13:15-15:00)
Chairs: T. Usuki (Univ. of Tokyo)
K. Ono (RIKEN)

13:15 I-9-1 (Invited)
Scanning Probe Measurements on Semiconductor Nanostructures
T. Ihn, A. Gildemeister, A. Pioda, S. Kicin and K. Ensslin, *ETH Zurich (Switzerland)*

13:45 I-9-2
Spin-conserved Single-electron Transport between Zeeman Sublevels in a Few-electron Quantum Dot
T. Fujisawa^{1,2}, G. Shinkai^{1,2} and T. Hayashi¹,
¹NTT Corp. and ²Tokyo Tech (Japan)

Area 13: Applications of Nanotubes and Nanowires

J-9 : Carbon Nanotube Devices and Growth I (13:15-15:00)
Chairs: Y. Ochiai (JST)
Y. Ohno (Nagoya Univ.)

13:15 J-9-1 (Invited)
Digital Circuits with Carbon Nanotube Transistors
A. Raychowdhury^{1,2}, J. Kurtin¹, K. Roy², V. De¹ and A. Keshavarzi¹,
¹Intel Corp. and ²Purdue Univ. (USA)

13:45 J-9-2 (Invited)
Advances in Carbon Nanotube Devices and Circuits
Y. M. Lin, Z. Chen, J. Appenzeller, P. M. Solomon and P. Avouris, *IBM (USA)*

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Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
13:55 A-9-3 Impacts of Fluorine and Nitrogen Incorporation on NiSi Induced Junction Leakage on Si(110) Substrate M. Tsuchiaki and A. Nishiyama, <i>Toshiba Corp. (Japan)</i>	13:55 B-9-3 Novel Extended-Pi Shaped Silicon-Germanium (eII-SiGe) Source/Drain Stressors for Strain and Performance Enhancement in P-Channel FinFETs K. M. Tan ¹ , T. Y. Liow ^{1,2} , R. T. P. Lee ¹ , M. Zhu ¹ , K. M. Hoe ² , C. H. Tung ² , N. Balasubramanian ² , G. S. Samudra ¹ and Y. C. Yeo ¹ , ¹ National Univ. of Singapore and ² Inst. of Microelectronics (Singapore)	14:05 C-9-3 Properties of Methyl Boron Nitride Film for Next Generation Low-K Interconnection S. Tokuyama, M. K. Mazumder, D. Watanabe, C. Kimura, H. Aoki and T. Sugino, <i>Osaka Univ. (Japan)</i>	14:00 D-9-3 CMOS Optical Polarization Analyzer Chip for μ TAS T. Tokuda, S. Sato, M. Nunoshita and J. Ohta, <i>NAIST (Japan)</i>	13:45 E-9-3 MOCVD Growth of GaN-Based LEDs with Naturally Formed Nano-pyramids C. E. Lee, C. H. Chiu, M. H. Lo, H. W. Huang, T. C. Lu, H. C. Kuo and S. C. Wang, <i>National Chia Tung Univ. (Taiwan)</i>
14:15 A-9-4 Phase and Composition Control of Ni-FUSI gates by N ₂ I/I with Double Ni-silicidation K. Yamamoto ¹ , S. Sakashita ² , Y. Sato ¹ , M. Inoue ² , M. Anma ² , T. Oosuka ¹ and J. Yugami ² , ¹ Matsushita Electric Industrial Co., Ltd. and ² Renesas Tech. Corp. (Japan)	14:15 B-9-4 Impact of Gradual Source/Drain Impurity Profiles on Performance of Germanium Channel Double-Gated pMISFETs T. Yamamoto ¹ , M. Harada ¹ , N. Taoka ² , Y. Yamashita ¹ , N. Sugiyama ¹ and S. Takagi ^{2,3} , ¹ MIRAI-ASET, ² MIRAI-AIST and ³ Univ. of Tokyo (Japan)	14:25 C-9-4 Effects of Silylation on Electrical and Mechanical Characteristics of Mesoporous Pure Silica Zeolite Films T. Seo ¹ , T. Yoshino ² , N. Ohnuki ² , Y. Seino ² , N. Hata ² and T. Kikkawa ^{1,2} , ¹ Hiroshima Univ. and ² AIST (Japan)	14:15 D-9-4 Label-Free Immunosensing for α -Fetoprotein in Human Plasma using Surface Plasmon Resonance K. Kawano ¹ , Y. Teramura ² , M. Oda ³ , T. Suzuki ² , H. Kotera ² and H. Iwata ² , ¹ CREATE-JST, ² Kyoto Univ. and ³ TERAMECS CO., LTD (Japan)	14:00 E-9-4 A Novel Sn-based Metal Substrate Technology for the Fabrication of Vertical-Structure GaN-Based High Power Light-Emitting Diodes H. Y. Kuo ¹ , S. J. Wang ¹ , K. M. Uang ² , S. L. Chen ¹ , T. M. Chen ^{1,2} , P. R. Wang ¹ , C. C. Tsai ¹ and H. Kuan ³ , ¹ National Cheng Kung Univ., ² WuFeng Inst. of Tech. and ³ Far East Univ. (Taiwan)

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Area 1: Advanced Gate Stack/Si Processing Science	Area 5: Advanced Circuits and Systems	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 13: Applications of Nanotubes and Nanowires
13:55 F-9-3 Origin of Structural Phase Transformation of SiO ₂ -doped HfO ₂ K. Tomida, K. Kita and A. Toriumi, <i>Univ. of Tokyo (Japan)</i>	13:55 G-9-3 A Moving-Object-Localization Hardware Algorithm Employing OR-Amplification of Pixel Activities Y. Niki, Y. Manzawa, S. Kametani and T. Shibata, <i>Univ. of Tokyo (Japan)</i>	14:00 H-9-3 Fabrication of Soluble Semiconductor Thin Film Transistor with Printed Electrodes using h-PDMS Stamp J. Jo ¹ , T. M. Lee ¹ , D. S. Kim ¹ , K. Y. Kim ¹ , E. S. Lee ¹ , K. Y. Park ² and M. Esashi ³ , ¹ KIMM, ² IITEP and ³ Tohoku Univ. (Korea)	14:00 I-9-3 Fano-Kondo effect in three quantum dots aiming at charge qubit measurement T. Tanamoto, Y. Nishi and S. Fujita, <i>Toshiba Corp. (Japan)</i>	14:15 J-9-3 A Triple Quantum Dot in a Single Wall Carbon Nanotube K. Grove-Rasmussen ^{1,2} , H. I. Jørgensen ² , T. Hayashi ¹ , P. E. Lindelof ² and T. Fujisawa ¹ , ¹ NTT Corp. and ² Univ. of Copenhagen (Japan)
14:15 F-9-4 Characteristics of Pure Ge ₃ N ₄ Dielectric Layers Formed by High-Density Plasma Nitridation K. Kutsuki, G. Okamoto, T. Hosoi, T. Shimura, K. Yasutake and H. Watanabe, <i>Osaka Univ. (Japan)</i>	14:15 G-9-4 New Reconfigurable Memory Architecture for Parallel Image Processing LSI with Three-Dimensional Structure S. Kodama, D. Amano, T. Sugimura, T. Fukushima, T. Tanaka and M. Koyanagi, <i>Tohoku Univ. (Japan)</i>	14:15 H-9-4 Double-Shot Inkjet Printing of Organic Charge-Transfer Compounds M. Hiraoka ¹ , T. Hasegawa ¹ , T. Yamada ¹ , Y. Takahashi ¹ , S. Horiuchi ¹ and Y. Tokura ^{1,2} , ¹ AIST and ² Univ. of Tokyo (Japan)	14:15 I-9-4 Study of Single-Charge Polarization on two Charge Qubits Integrated onto a Double Single-Electron Transistor Readout Y. Kawata ^{1,3} , S. Nishimoto ¹ , Y. Tsuchiya ^{1,3} , S. Oda ^{1,3} and H. Mizuta ^{1,2,3} , ¹ Tokyo Tech., ² Univ. of Southampton and ³ SORST-JST (Japan)	14:30 J-9-4 Electric Property Control of Carbon Nanotubes by Defects S. Suzuki ¹ , J. Hashimoto ^{1,2} , T. Ogino ² and Y. Kobayashi ¹ , ¹ NTT Corp. and ² Yokohama National Univ. (Japan)

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Area 1: Advanced Gate Stack/Si Processing Science	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	Area 7: Photonic Devices and Device Physics
14:35 A-9-5 CMP-less Co-Integration of Tunable Ni-TOSI CMOS for Low Power Digital and Analog Applications G. Bidal ^{1,5} , M. Müller ¹ , S. Denorme ² , D. Aimé ³ , M. Rafik ² , A. Cathignol ² , G. Ribes ² , S. Pokrant ¹ , P. Gouraud ² , T. Kormann ¹ , G. Chabanne ³ , C. Blanc ³ , S. Bonnetier ³ , D. Barge ¹ , C. Laviron ⁴ , A. Tarnowka ¹ , G. Ghibaubo ⁵ , F. Boeuf ² and T. Skotnicki ² , ¹ <i>NXP Semiconductors</i> , ² <i>STMicroelectronics</i> , ³ <i>Freescale</i> , ⁴ <i>CEA-LETI</i> and ⁵ <i>IMEP (France)</i>	14:35 B-9-5 A Double-Gate Tunneling Field-Effect Transistor with Silicon-Germanium Source for High-Performance, Low Standby Power, and Low Power Technology Applications E. H. Toh, G. H. Wang, L. Chan, D. Sylvester, C. H. Heng, G. Samudra and Y. C. Yeo, <i>National Univ. of Singapore (Singapore)</i>	14:45 C-9-5 Determination of mechanical properties of porous silica low-k films on Si substrates using orientation dependence of surface acoustic wave T. Takimura, N. Hata, S. Takada and T. Yoshino, <i>AIST (Japan)</i>	14:30 D-9-5 In-Situ Surface Infrared Study of DNA Attachment and Hybridization at Si Surfaces A. Hirano, K. Tanaka, K. Ishibashi, K. Miyamoto, Y. Kimura and M. Niwano, <i>Tohoku Univ. (Japan)</i>	14:15 E-9-5 The Aluminum Packaging for LED using Selectively Anodizing Method K. M. Kim ¹ , S. H. Shin ² , Y. K. Lee ² , S. M. Choi ² and Y. S. Kwon ¹ , ¹ <i>KAIST</i> and ² <i>Samsung Electro-Mechanics (Korea)</i>
				14:30 E-9-6 The Fabrication of the Circular Ring Laser Resonators by Excimer Laser Assisted Etching at Cryogenic Temperature M. C. Shih and S. C. Wang, <i>National Univ. of Kaohsiung (Taiwan)</i>
				14:45 E-9-7 Red emission from ZnO-based double heterojunction diode T. Ohashi, K. Yamamoto, A. Nakamura and J. Temmyo, <i>Shizuoka Univ. (Japan)</i>

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	Area 5: Advanced Circuits and Systems	Area 10: Organic Materials Science, Device Physics, and Applications	Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 13: Applications of Nanotubes and Nanowires
14:35 F-9-5 Surface Treatment of Ge(001) Surface by Radical Nitridation H. Kondo, M. Fujita, A. Sakai, M. Ogawa and S. Zaima, <i>Nagoya Univ. (Japan)</i>		14:30 H-9-5 Fabrication of Flexible OTFT-backplanes for Active Matrix Electrophoretic Display M. W. Lee and C. K. Song, <i>Dong-A Univ. (Korea)</i>	14:30 I-9-5 Formation and control of 2-qubits exciton state in a coupled quantum dots K. Goshima ^{1,2} , K. Komori ^{1,2} and T. Sugaya ^{1,2} , ¹ <i>AIST</i> and ² <i>CREST-JST (Japan)</i>	14:45 J-9-5 Single charge sensitivity of single-walled carbon nanotube single-hole transistor T. Kamimura ^{1,2} , Y. Ohno ^{1,2} and K. Matsumoto ^{1,2,3} , ¹ <i>Osaka Univ.</i> , ² <i>CREST-JST</i> and ³ <i>AIST (Japan)</i>
			14:45 I-9-6 Decoherence of nuclear spins in a GaAs quantum well probed by a submicron scale all-electrical NMR device T. Ota ^{1,2} , N. Kumada ¹ , G. Yusa, ^{1,3,4} , S. Miyashita ⁵ , T. Fujisawa ¹ and Y. Hirayama ^{1,2,4} , ¹ <i>NTT Corp.</i> , ² <i>SORST-JST</i> , ³ <i>PRESTO-JST</i> , ⁴ <i>Tohoku Univ.</i> and ⁵ <i>NTT-AT (Japan)</i>	

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)		
B-10 : Noise and RF (15:15-17:05) Chairs: D. Hisamoto (Hitachi Ltd.) K. Takeuchi (NEC Corp.)	C-10 : Nanoscale Characterization (15:25-16:25) Chairs: N. Hata (NEDO) S. Ogawa (Selete)	D-10 : μ -TAS and Medical Applications (15:15-16:45) Chairs: K. Sawada (Toyohashi Univ. of Technology) H. Tabata (The Univ. of Tokyo)		
15:15 B-10-1 (Invited) RTN Effects in Scaled Flash Memory Arrays A. S. Spinelli, C. M. Compagnoni, R. Gusmeroli, M. Ghidotti and A. L. Lacaita, <i>Politecnico di Milano (Italy)</i>	15:25 C-10-1 Characterization of Line-edge Roughness in Cu/low-k Interconnect Pattern A. Yamaguchi ¹ , D. Ryuzaki ¹ , K. Takeda ¹ , J. Yamamoto ¹ , H. Kawada ² and T. Iizumi ² , ¹ Hitachi, Ltd. and ² Hitachi High-Technologies Corp. (Japan)	15:15 D-10-1 One-Chip Integration of the Rapid Diagnosis Infectious Disease Chip Based on New Phenomena of DNA Trap and Denature in Nano-Gaps S. Hashioka ^{1,2} , K. Masu ¹ and Y. Horiike ² , ¹ Tokyo Tech. and ² NIMS (Japan)		
15:45 B-10-2 Analysis of Random Telegraph Signal Noise in Dual and Single Oxide Device And Its Application to CMOS Image Sensor Readout Circuit H. Lee, Y. Yoon, J. Jeon and H. Shin, <i>Seoul National Univ. (Korea)</i>	15:45 C-10-2 Nano-Scale Stress Field Evaluation with Shallow Trench Isolation Structure Assessed by Cathodoluminescence, Raman Spectroscopy, and Finite Element Method Analyses M. Kodera ¹ , T. Iguchi ¹ , N. Tsuchiya ¹ , M. Tamura ² , S. Kakinuma ³ , N. Naka ³ and S. Kashiwagi ³ , ¹ Toshiba Corp., ² Toshiba I. S. Corp. and ³ Horiba, Ltd. (Japan)	15:30 D-10-2 Droplet device for immunoassay detection C. H. Chang, S. Hashioka, T. Chikyo and Y. Horiike, <i>NIMS (Japan)</i>		

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
Area 1: Advanced Gate Stack/Si Processing Science	Area 5: Advanced Circuits and Systems		Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 13: Applications of Nanotubes and Nanowires
F-10 : Advanced Process (15:15-16:35) Chairs: O. Faynot (CEA-LETI) T. Tatsumi (NEC Corp.)	G-10 : Connectivity (15:15-16:35) Chairs: M. Horiguchi (Renesas Technology Corp.) T. Komuro (Agilent Technologies International Japan, Ltd.)		I-10 : Novel Devices (15:15-16:45) Chairs: Y. Uraoka (Nara Inst. of Science and Technology) B. G. Park (Seoul National Univ.)	J-10 : Carbon Nanotube Devices and Growth II (15:15-16:30) Chairs: S. Akita (Osaka Prefecture Univ.) Y. Homma (Tokyo Univ. of Science)
15:15 F-10-1 Dependence of Electrical Characteristics on Interfacial Structures of Epitaxial NiSi ₂ /Si Schottky Contacts Formed from Ni/Ti/Si System O. Nakatsuka, A. Suzuki, S. Akimoto, A. Sakai, M. Ogawa and S. Zaima, <i>Nagoya Univ. (Japan)</i>	15:15 G-10-1 PCA-based Object Detection/Recognition Chip for Wireless Interconnected 3-D Integration H. Ando, S. Kameda, D. Arizono, N. Fuchigami, K. Kaya, M. Sasaki and A. Iwata, <i>Hiroshima Univ. (Japan)</i>		15:15 I-10-1 High Performance Germanium Quantum-dot Single-hole Transistors with Self-aligned Electrodes S. H. Hsu, W. T. Lai and P. W. Li, <i>National Central Univ. (Taiwan)</i>	15:15 J-10-1 New Measurement Method of Carbon Nanotube Energy Band Gap M. Maeda ^{1,4} , T. Kamimura ^{2,4} , S. Iwasaki ^{2,4} and K. Matsumoto ^{2,3,4} , ¹ Univ. of Tsukuba, ² Osaka Univ., ³ AIST and ⁴ CREST-JST (Japan)
15:35 F-10-2 A Breakthrough Electronic Lithography Process Through Si Layer for Self Aligning Gates in Planar Double-Gate Transistors for 32nm Node And Below R. Wacquez ^{1,2,4} , P. Coronel ¹ , M. P. Samson ^{1,2} , D. Delille ³ , L. R. Clement ³ , V. Delaye ² , L. Baud ² , N. Loubet ¹ , J. Bustos ¹ , A. Pouydebasque ³ , B. Guillaumot ^{1,2} , T. Ernst ² , P. Masson ⁴ , J. P. Gouy ² and T. Skotnicki ¹ , ¹ STMicroelectronics, ² CEA-LETI, MINATEC, ³ NXP and ⁴ L2MP (France)	15:35 G-10-2 Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link A. Kumar, N. Miura and T. Kuroda, <i>Keio Univ. (Japan)</i>		15:30 I-10-2 Single Electron-based Flexible Multi-valued Exclusive-OR Logic Gate S. J. Kim, C. K. Lee, R. S. Chung, M. S. Kim, E. S. Park, S. J. Shin and J. B. Choi, <i>Chungbuk National Univ. (Korea)</i>	15:30 J-10-2 Self-aligned Fabrication Process for Pd-Contacted and PMMA-Passivated Carbon Nanotube Field-Effect Transistors L. Rispal, H. Yang, R. Heller, G. Hess, G. Tzschöckel and U. Schwalke, <i>Darmstadt Univ. of Tech. (Germany)</i>

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	Area 3: CMOS Devices/Device Physics	Area 2: Characterization and Materials Engineering for Interconnect Integration	Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)	
	16:05 B-10-3 Simultaneous Extraction of Locations and Energies of Two Independent Traps in Gate Oxide From Four-level RTS noise S. Yang, H. Lee and H. Shin, <i>Seoul National Univ. (Korea)</i>	16:05 C-10-3 Channel Strain in Advanced CMOSFETs Measured Using Nano-Beam Electron Diffraction A. Toda ¹ , H. Nakamura ² , T. Fukai ² and N. Ikarashi ¹ , ¹ NEC Corp. and ² NEC Electronics Corp. (Japan)	15:45 D-10-3 High-Throughput Fluorometric Assay of Enzymatic Reactions on a Microreactor Array Chip T. Ichiki ^{1,2} , Y. Hosoi ¹ , J. Liu ¹ , T. Osawa ¹ , T. Akagi ¹ , M. Biyani ² and N. Nemoto ^{2,3} , ¹ Univ. of Tokyo, ² CREATE-JST and ³ Janusys Corp. (Japan)	
	16:25 B-10-4 Analog Performance of Asymmetric Schottky Tunneling Source nFET for RF and Mixed-Mode Application R. Jhaveri and J. C. S. Woo, <i>Univ. of California (USA)</i>		16:00 D-10-4 Development of a multi-chip retinal stimulator for in vivo experiments toward retinal prosthesis T. Tokuda ¹ , R. Asano ¹ , Y. Terasawa ² , M. Nunoshita ¹ , K. Nakauchi ³ , T. Fujikado ³ , Y. Tano ³ and J. Ohta ¹ , ¹ NAIST, ² NIDEK Co., Ltd. and ³ Osaka Univ. (Japan)	

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Area 1: Advanced Gate Stack/Si Processing Science	Area 5: Advanced Circuits and Systems		Area 9: Physics and Applications of Novel Functional Materials and Devices	Area 13: Applications of Nanotubes and Nanowires
15:55 F-10-3 Contact Technology employing Nickel-Platinum Germanosilicide Alloys for P-Channel FinFETs with Silicon-Germanium Source and Drain Stressors R. T. P. Lee ¹ , K. M. Tan ¹ , A. E. J. Lim ¹ , T. Y. Liow ¹ , X. C. Chen ¹ , M. Zhu ¹ , A. T. Y. Koh ¹ , K. M. Hoe ³ , S. Y. Chow ² , G. Q. Lo ³ , G. S. Samudra ¹ , D. Z. Chi ² and Y. C. Yeo ¹ , ¹ National Univ. of Singapore, ² Inst. of Materials Research and Engineering and ³ Inst. of Microelectronics (Singapore)	15:55 G-10-3 Scaling Characteristics of Si On-chip Integrated Antennas K. Kimoto, N. Sasaki and T. Kikkawa, <i>Hiroshima Univ. (Japan)</i>		15:45 I-10-3 Self-Aligned Dual-Gate Single-Electron Transistors (DG-SETs) S. Kang ¹ , D. H. Kim ² , I. H. Park ¹ , J. H. Kim ¹ , J. E. Lee ¹ , J. D. Lee ¹ and B. G. Park ¹ , ¹ Seoul National Univ. and ² Kookmin Univ. (Korea)	15:45 J-10-3 Individual Carbon Nanotubes as Nano-incandescent S. Akita ^{1,3} and Y. Nakayama ^{2,3} , ¹ Osaka Prefecture Univ., ² Osaka Univ. and ³ CREST-JST (Japan)
16:15 F-10-4 An Optimized Silicidation Technique for Source and Drain of FINFET K. Okuyama, A. Sugimura and H. Sunami, <i>Hiroshima Univ. (Japan)</i>	16:15 G-10-4 A Fully Integrated SiGe Optical Receiver Using Differential Active Miller Capacitor for 4.25 Gb/s Fiber Channel Application J. C. Huang, K. S. Lai and K. Y. J. Hsu, <i>National Tsing Hua Univ. (Taiwan)</i>		16:00 I-10-4 Design Control of Random Dopant-induced Multiple-Tunnel-Junction Arrays for Turnstile Operation D. Moraru, K. Yokoi, H. Ikeda and M. Tabe, <i>Shizuoka Univ. (Japan)</i>	16:00 J-10-4 A Field-Emission Device with Novel Self-Focus Gate Structure H. W. Chen, K. C. Lin, C. P. Juan, Y. S. Leou, Y. Y. Hsu and H. C. Cheng, <i>National Chiao Tung Univ. (Taiwan)</i>

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Room 101 (A)	Room 102 (B)	Room 201A (C)	Room 201B (D)	Room 202A (E)
	<p>Area 3: CMOS Devices/Device Physics</p> <p>16:45 B-10-5 Frequency Dependence of Measured MOSFET Distortion Characteristic T. Minami¹, Y. Takeda¹, M. Miyake¹, M. Miura-Mattausch¹, H. J. Mattausch¹, T. Ohguro², T. Iizuka², M. Taguchi² and S. Miyamoto², ¹Hiroshima Univ. and ²STARC (Japan)</p>	<p>Area 2: Characterization and Materials Engineering for Interconnect Integration</p>	<p>Area 11: Micro/Nano Electromechanical and Bio-Systems (Devices)</p> <p>16:15 D-10-5 UWB Imaging for Early Breast Cancer Detection by Confocal Algorithm X. Xiao^{1,2} and T. Kikkawa¹, ¹Hiroshima Univ. and ²Tianjin Univ. (Japan)</p> <p>16:30 D-10-6 Development of a CMOS-based Neural Imaging and Interface Device D. C. Ng, T. Mizuno, T. Tokuda, K. Kagawa, M. Nunoshita, H. Tamura, S. Shiosaka and J. Ohta, <i>NAIST (Japan)</i></p>	

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Room 202B (F)	Room 303 (G)	Room 304 (H)	Room 405 (I)	Room 406 (J)
<p>Area 1: Advanced Gate Stack/Si Processing Science</p>	<p>Area 5: Advanced Circuits and Systems</p>		<p>Area 9: Physics and Applications of Novel Functional Materials and Devices</p> <p>16:15 I-10-5 Acoustic Wave Manipulation by Phased Operation of Two-Dimensionally Arrayed Nanocrystalline Silicon Ultrasonic Emitters B. Gelloz, M. Sugawara and N. Koshida, <i>Tokyo Univ. of Agri. and Tech. (Japan)</i></p> <p>16:30 I-10-6 New Type Oxygen Sensor Using Micro-fabricated Layered Semiconductor Compound T. Nugroho, A. Ikeda, Y. Kakahara, H. Kuriyaki and Y. Kuroki, <i>Kyushu Univ. (Japan)</i></p>	<p>Area 13: Applications of Nanotubes and Nanowires</p> <p>16:15 J-10-5 Combinatorial Control of Catalyst Nanoparticles for Customized Production of Single- and Multi-Walled Carbon Nanotubes S. Noda, K. Hasegawa, H. Sugime, K. Kakehi, S. Maruyama and Y. Yamaguchi, <i>Univ. of Tokyo (Japan)</i></p>

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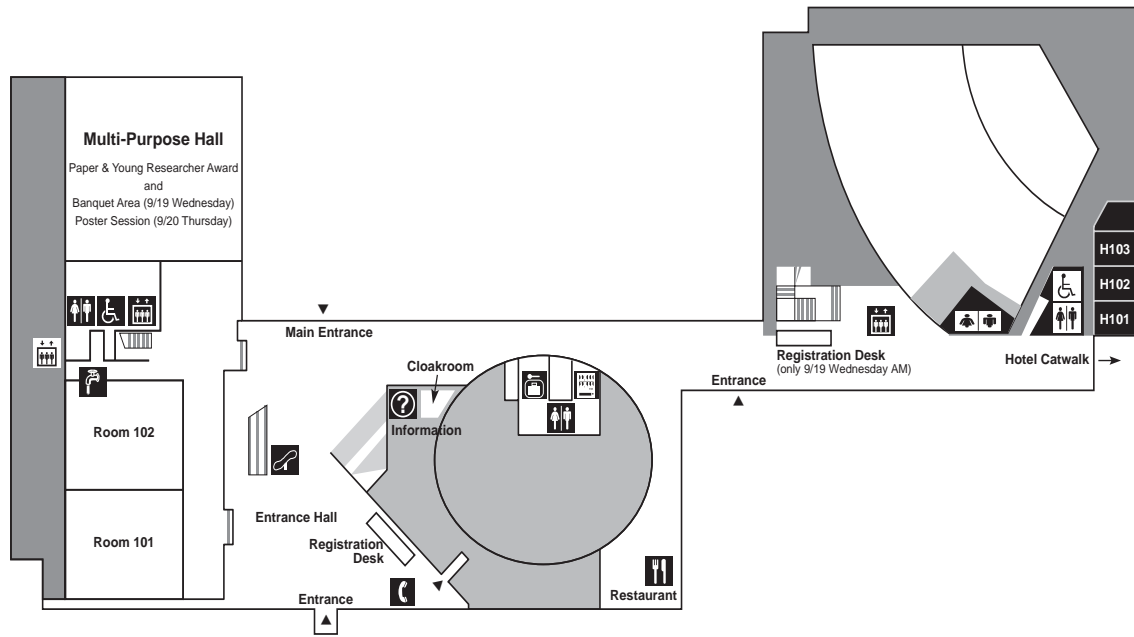
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E-mail: ssdm@intergroup.co.jp

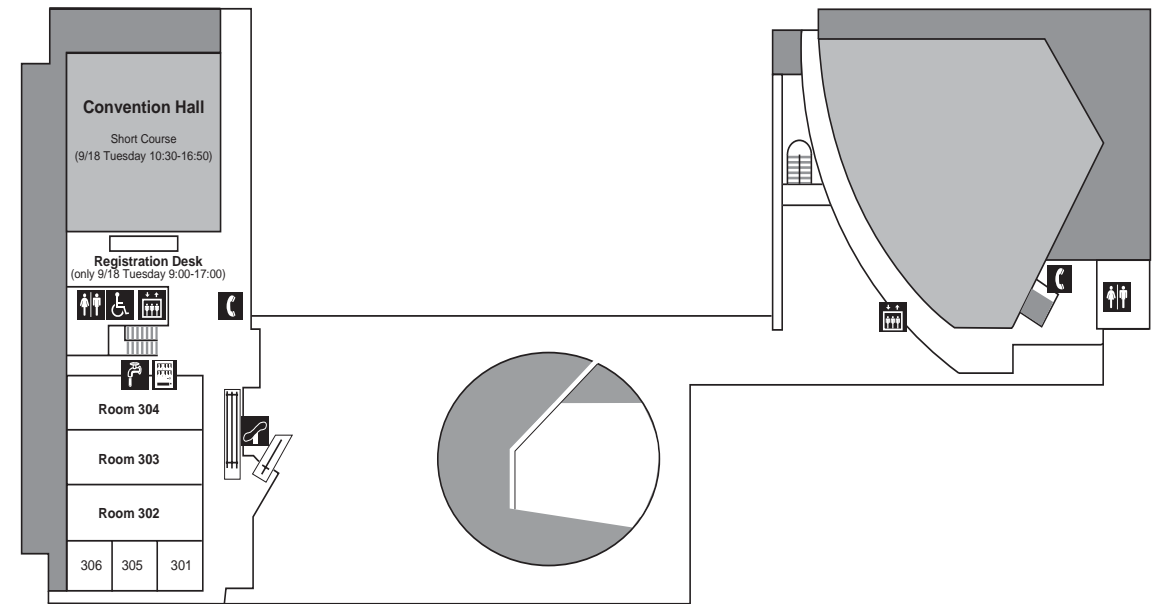
SSDM 2007 is subsidized by the following organization:

* The Ministry of Education, Culture, Sports, Science and Technology

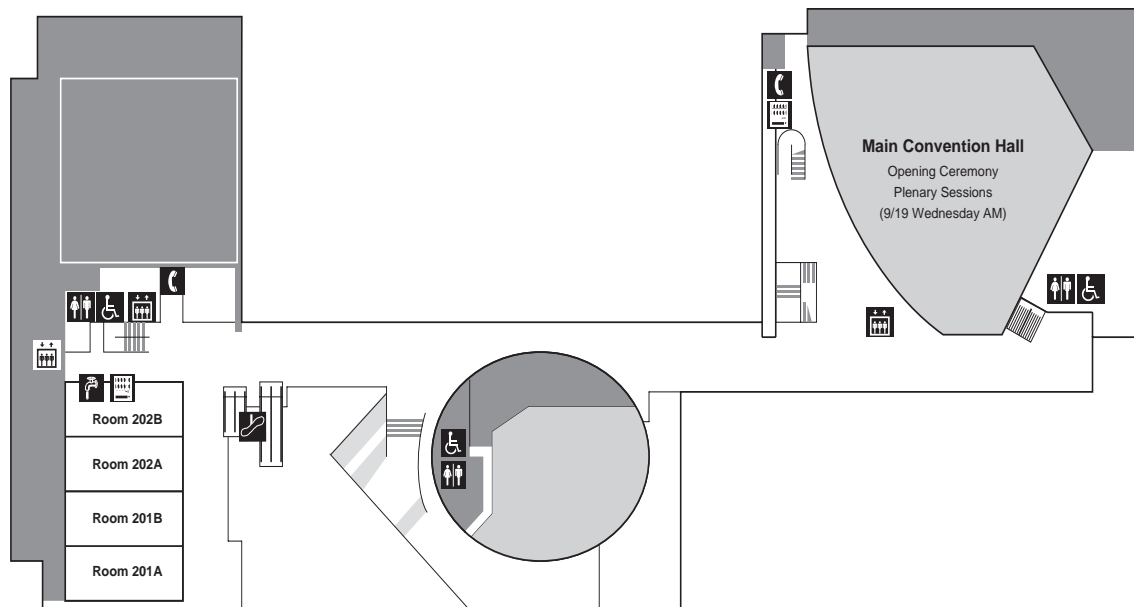
1F



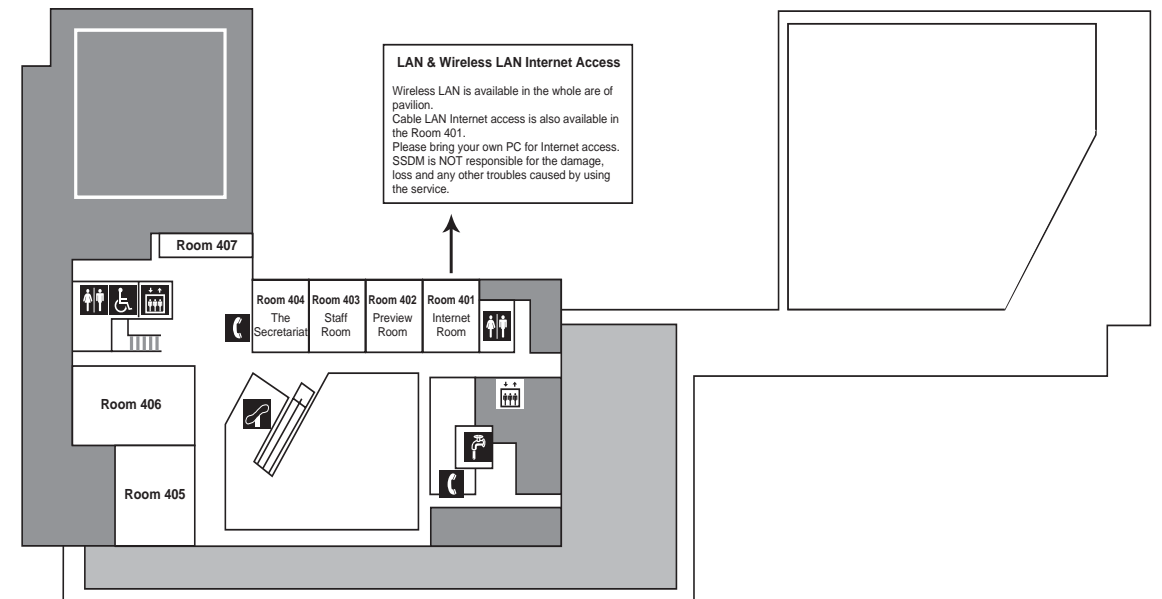
3F



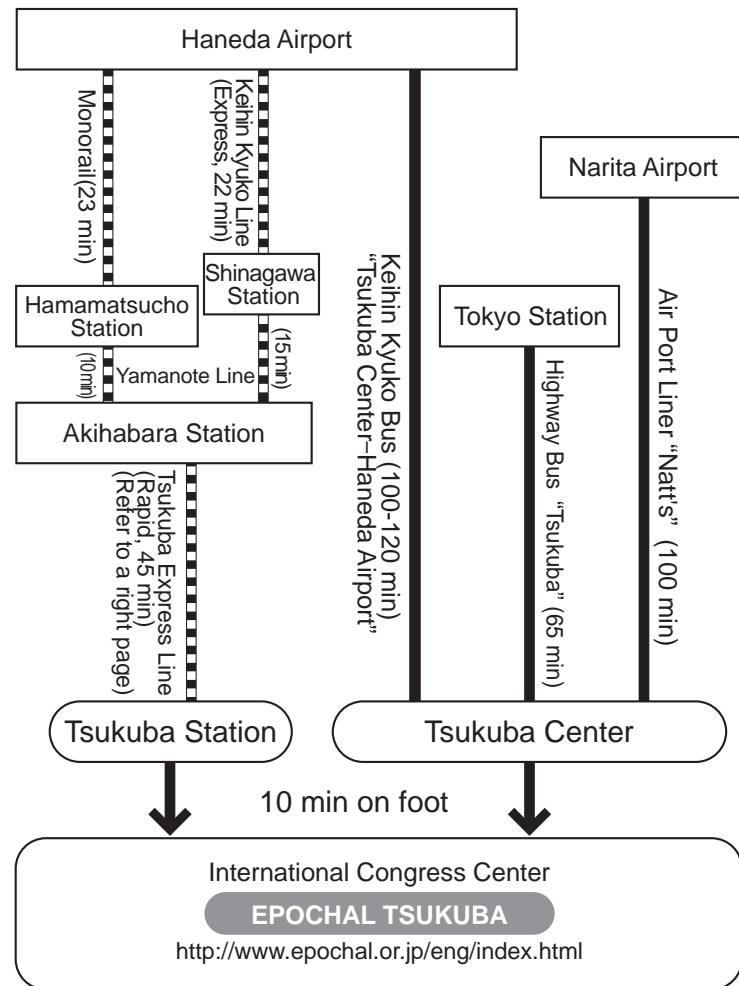
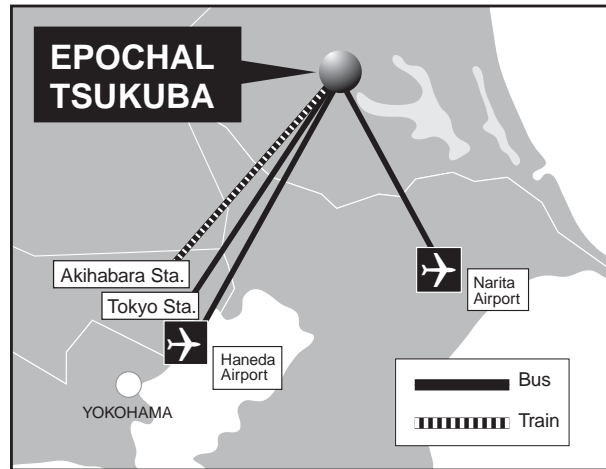
2F



4F



ACCESS TO EPOCHAL TSUKUBA



Tsukuba Express Time Table (Weekdays)

To Tsukuba (@Akihabara Sta.)

5	30	45			
6	05	20	43		
7	00	12	24	37	45
8	02	10	25	31	46
9	01	15	30	45	
10	00	15	30	45	
11	00	15	30	45	
12	00	15	30	45	
13	00	15	30	45	
14	00	15	30	45	
15	00	15	30	45	
16	00	15	30	45	52
17	00	17	30	40	
18	00	10	20	30	40
19	00	10	20	30	40
20	00	12	36		
21	00	12	36		
22	00	15	45		
23	00	15	30		

To Akihabara (@Tsukuba Sta.)

5	07	28	42		
6	12	34	56	57	
7	12	26	27	42	56
8	12	26	32	47	
9	07	18	31	41	48
10	11	18	41	48	
11	11	18	41	48	
12	11	18	41	48	
13	11	18	41	48	
14	11	18	41	48	
15	11	18	30	41	48
16	11	18	39	52	
17	09	12	32	49	52
18	02	19	22	42	
19	02	20	25	38	57
20	01	18	24	49	
21	08	16	45		
22	08	15	40		
23	05	14			

Red: Rapid (45 min)

Blue: Section Rapid (52 min)

Black: Local