SESSION 10 – TAPA I
Advanced SRAM Circuits

Thursday, June 17, 10:25 a.m.
Chairperson: G. Lehmann, Infineon Technologies AG
T. Sekiguchi, Hitachi, Ltd.

10.1 - 10:25 a.m.
A 28-nm Dual-Port SRAM Macro with Active Bitline Equalizing Circuitry Against Write Disturb Issue, Y. Ishii, H. Fujiwara, K. Nii, H. Chigasaki, O. Kuromiya,T. Saiki, A. Miyanishi, Y. Kihara, Renesas Technology Corp, Japan

We propose circuit techniques for an 8T dual-port SRAM to improve its minimum operating voltage. Active bitline equalizing technique improves the write margin whenever a write-disturb occurs. It is applicable for both synchronous and asynchronous clock frequencies between ports. We designed and fabricated a 256kb SRAM macro using 28-nm low-power technology and achieved low-voltage operation at 0.66V and 1.4ns write access time at 25°C, which are 120mV lower and 40% faster than the conventional performance.

10.2 - 10:50 a.m.
Multi-Step Word-Line Control Technology in Hierarchical Cell Architecture for Scaled-Down High-Density SRAMs, K. Takeda, T. Saito, S. Asayama, Y. Aimoto, H. Kobatake, S. Ito, T. Takahashi, K. Takeuchi, M. Nomura, Y. Hayashi, NEC Electronics Corporation, Japan

For scaled-down SRAMs, a new hierarchical cell architecture and a multi-step word-line control technology were developed to overcome rapid increase in random variability with no area-penalty in SRAM. We have successfully fabricated a 40nm-node 0.248 mm^2-cell SRAM using a single power supply, pushing up bit-density to 2.98Mb/mm^2.

10.3 - 11:15 a.m.
A Large σV_{TH}/VDD Tolerant Zigzag 8T SRAM with Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme, J.-J. Wu, Y.H. Chen, M.-F. Chang, P.-W. Chou, C.-Y. Chen, H.-J. Liao, M.-B. Chen*, Y.-H. Chu*, W.-C. Wu*, H. Yamauchi**, National Tsing Hua University, Taiwan, *ITRI,Taiwan, **Fukuoka Institute of Technology, Japan

This paper demonstrates for the first time quantitative performance advantages of a zigzag 8T-SRAM (Z8T) cell over the decoupled single-end sensing 8T-SRAM (DS8T) with write-back schemes For the same VDDmin/speed, Z8T can save the cell area by 15%. A fabricated 256-row 32Kb Z8T SRAM, using a 65nm low-power process, is 14% smaller area and 53% faster than DS8T SRAM, and is 430mV lower VDDmin than 6T-SRAM.

10.4 - 11:40 a.m.
A 32nm 8.3GHz 64-entry x 32b Variation Tolerant Near-Threshold Voltage Register File, A. Agarwal, S. Hsu, S. Mathew, M. Anders, H. Kaul, F. Sheikh, R. Krishnamurthy, Intel Corp, USA

This paper describes a 64-entry x 32b 1-read, 1-write ported register file with measured 8.3GHz operation consuming 83mW, fabricated in 1.0V 32nm CMOS. Contention-free shared keeper circuits combined with variation tolerant dual-ended transmission gate write memory cells enable 300mV Vcc-min reduction and measured scalable near-threshold voltage operation to 340mV with energy efficiency of 550GOPS/W.