SESSION 12 – TAPA I
Digital Circuits Resilent

Thursday, June 17, 1:30 p.m.
Chairperson: V. De, Intel Corp.
M. Nomura, NEC Electronics Corp.

12.1 - 1:30 p.m.
Resonant Supply Noise Canceller utilizing Parasitic Capacitance of Sleep Blocks, J. Kim, T. Nakura, H. Takata*,K. Ishibashi*, M. Ikeda, K. Asada, University of Tokyo, Japan, *Renesas Technology Corporation, Japan

This paper proposes a resonant supply noise canceller utilizing parasitic capacitance of sleep blocks. It has small area penalty because we use sleep blocks for noise cancelling. Measurement results show that the test chip fabricated in 0.18um CMOS process achieved 43.3% and 12.5% supply noise reduction on the abrupt supply voltage switching and the abrupt wake-up of a sleep block, respectively. These results make fast switching of power mode possible for DVS and power gating.

12.2 - 1:55 p.m.
On-Chip Waveform Capture and Diagnosis of Power Delivery in SoC Integration, T. Hashida, M. Nagata, Kobe University, Japan

On-chip waveform capture exhibits the resolution of 10 ps and 200 uV with 1024 steps, and SFDR of 63.2dB in 700- MHz signal bandwidth of interest. On-chip signal probing as well as digital waveform processing are merged in systems-on- chip (SoC) integration. An exciter is combined for on-chip derivation of LCR parasitics from oscillatory waveforms of a power delivery network that are effectively seen by SoC circuits.

12.3 - 2:20 p.m.
65nm Bistable Cross-coupled Dual Modular Redundancy Flip-Flop Capable of Protecting Soft Errors on the C-element, J. Furuta, C. Hamanaka*, K. Kobayashi*, H. Onodera, Kyoto University, Japan, Kyoto Institute of Technology, Japan

We propose a Bistable Cross-coupled Dual Modular Redundancy (BCDMR) Flip-Flop to enhance soft-error immunity. It is based on a BISER FF but its cross-coupled structure enhances soft-error immunity without any area/delay overhead. We fabricated a 65nm LSI including 60,480bit shift registers with the BCDMR and BISER structures. Experimental results using alpha-particles reveals that the soft-error immunity of the BCDMR is enhanced by 150x at 160MHz clock frequency compared with the BISER FFs.

12.4 - 2:45 p.m.
Low-Cost Gate-Oxide Early-Life Failure Detection in Robust Systems, Y.M. Kim, Y. Kameda*, H. Kim, M. Mizuno*, S. Mitra, Stanford University, USA, *NEC Corporation, Japan

We present a new low-cost technique for detecting gate-oxide early-life failures (ELF) to overcome reliability challenges in robust systems without requiring expensive concurrent error detection. Using 90nm test chips, we demonstrate the following key results: 1. A gate-oxide ELF transistor inside a combinational logic circuit results in delay shifts over time before functional failures appear. 2. The delay shifts can be successfully detected during on-line self-test and diagnostics using our on-chip clock control technique.