SESSION 17 – TAPA II
Interference Robust RF Receivers

Friday, June 18, 8:30 a.m.
Chairperson: L. Breems, NXP Semiconductors
H. Ishikuro, Keio University

17.1 - 8:30 a.m.
Quadrature Sampling Mixer Topology for SAW-Less GPS Receivers in 0.18µm CMOS, O. Ikeuchi, N. Saito, B. Nauta*, Asahi Kasei Microdevices Corporation, Japan, *University of Twente, The Netherlands

This paper describes a new switching topology of a sampling mixer for SAW-less GPS (L1 band) receivers. The GPS receivers with the new mixer achieved NF 2.5dB and good blocking performance. In an alternative implementation, the mixer is stacked under a Quadrature VCO to reuse supply current. As a result, the current consumption of GPS receiver is 11mA from 1.8V supply while maintaining blocking performance and NF 3.5dB.

17.2 - 8:55 a.m.
A 65nm CMOS Quad-Band SAW-Less Receiver for GSM/GPRS/EDGE, A. Mirzaei, A. Yazdi, Z. Zhou, E. Chang, P. Suri, H. Darabi, Broadcom Corporation, USA

A quad-band 2.5G receiver integrates the front-end SAW filters, the LNA matching, as well as the RF baluns, achieving a typical sensitivity of close to -111dBm. Utilizing an arrangement of only four baseband capacitors and MOS switches driven by 4-phase 25% duty-cycle clocks, high-Q BPF's are realized to attenuate the 0dBm out-of-band blocker. The SAW-less receiver draws 55mA from the battery, and measures an out-of-band 1dB-compression of > +2dBm.

17.3 - 9:20 a.m.
A 6-phase Harmonic Rejection Down-Converter with Digital Assist, T. Yamaji, J. Matsuno, H. Aoyama, M. Furuta, T. Takida, I. Akita, A. Kuroda, T. Itakura, N. Itoh, Toshiba Corp, Japan

A down-converter insensitive to 2nd and 3rd harmonics and a digital assisting circuit that cancels residual sensitivity due to device mismatches are proposed. Measured 2nd and 3rd harmonic rejection ratios of over 60 dB are achieved. This performance allows a simple RF filter, and it is effective to reduce the die size.

17.4 - 9:45 a.m.
0.6V, 5dB NF, -9.8dBm IIP_3, 900MHz Receiver with Interference Cancellation, A. Balankutty, P. Kinget, Columbia University, USA

We present an integrated 900MHz receiver with 56.4dB conversion gain, 5dB NF, and -9.8dBm IIP3 using on-chip in-band feed-forward interference cancellation. The interference cancellation at baseband gives more than 13dB IIP3 improvement and makes operation from an ultra-low 0.6V supply possible. The direct-conversion receiver including baseband filters and polyphase LO filters and buffers consumes 26.4mW from a 0.6V supply and occupies 2.56mm^2 in a low power 65nm CMOS process.