SESSION 18 – TAPA I
DRAM

Friday, June 18, 10:25 a.m.
Chairperson: J. Barth, IBM Microelectronics
K. Kajigaya, Elpida Memory, Inc.

18.1 - 10:25 a.m.
1-Tbyte/s 1-Gbit DRAM Architecture with Micro-pipelined 16-DRAM Cores, 8-ns Cycle Array and 16-Gbit/s 3D Interconnect for High Throughput Computing, K. Ono, A. Kotabe, Y. Yanagawa, T. Sekiguchi, Hitachi, Ltd, Japan

A novel DRAM architecture with an ultra-high bandwidth is proposed for high throughput computing. The proposed architecture employs three techniques: 1) five-stage pipelined 16-DRAM cores, 2) an early bar write scheme for an 8-ns cycle array operation, and 3) a 16-Gbit/s I/O circuit on each of 32 through-silicon-via pairs/DRAM core. We conducted a circuit simulation assuming a 45-nm 1-Gbit chip and confirmed that the proposed architecture achieved a 1-Tbyte/s bandwidth with 19.5-W power consumption.

18.2 - 10:50 a.m.
In-situ Measurement of Variability in 45-nm SOI Embedded DRAM Arrays, K. Agarwal, J. Hayes, J. Barth, M. Jacunski, K. Nowka, T. Kirihata, S. Iyer, IBM Corp, USA

A technique for in-situ measurement of process variation in deep trench capacitance, bitline capacitance, and device threshold voltage in embedded DRAM (eDRAM) arrays is presented. The technique is used to directly measure the parameter statistics in two product representative 45-nm SOI eDRAM arrays.

18.3 - 11:15 a.m.
A 1.1V, 667MHz Random Cycle, Asymmetric 2T Gain Cell Embedded DRAM with a 99.9 Percentile Retention Time of 110µsec, K.C. Chun, P. Jain, T.-H. Kim, C. Kim, University of Minnesota, USA

A logic compatible embedded DRAM test macro fabricated in a 65nm LP CMOS process has a 512 cells-per-BL array architecture and achieves a random access frequency and latency of 667MHz and 1.65nsec, respectively at 1.1V, 85°C. The refresh period for a 99.9% bit yield was 110µsec. Key features include an asymmetric 2T gain cell, a pseudo-PMOS diode based current sensing scheme, a half swing write BL driver, and a stepped write WL technique.

18.4 - 11:40 a.m.
A 40nm 7Gb/s/pin Single-ended Transceiver with Jitter and HSI Reduction Techniques for High-Speed DRAM Interface, S.-J. Bae, Y.-S. Sohn, T.-Y. Oh, S.-H. Kwak, D.-M. Kim, D.-H. Kim, Y.-S. Kim, Y.-S. Yang, S.-Y. Doo, J.-I. Lee, S.-Y. Bang, S.-Y. Park, K.-W. Yeom, J.-Y. Lee, H. Park, W.-S. Kim, H.-J. Yang, K.-I. Park, J.S. Choi, Y.-H. Jun, Samsung Electronics, Korea

A 7Gb/s single ended transceiver with low jitter and ISI is implemented in 40nm DRAM process. DRAM optimized LC PLL achieves inductor Q of 3.86 and results in random jitter of 670fs rms. A clock tree regulator with closed loop replica path reduces low as well as high frequency noise. RX 2-tap hybrid DFE combining sampling and integration methods reduces power and area by 37% and 24%, compared to the integrating DFE. Moreover, on-chip de-emphasis circuit in TX multiplexer reduces ISI of both on and off chip.