SESSION 2 – TAPA I
Medical and Vision Processors

Wednesday, June 16, 10:25 a.m.
Chairperson: C. Sechen, University of Texas at Dallas
K. Kobayashi, Kyoto Institute of Technology

2.1 - 10:25 a.m.
Microwatt Embedded Processor Platform for Medical System-on-Chip Applications, S. Sridhara, M. DiRenzo, S. Lingam, S.-J. Lee, R. Blazquez, J. Maxey, S. Ghanem*, Y.-H. Lee*, R. Abdallah*, P. Singh**, M. Goel*, Texas Instruments, *University of Illinois at Urbana-Champaign, **University of Michigan at Ann Arbor, USA

A medical system-on-chip (SoC) that integrates an ARM Cortex-M3 processor is presented. Ultra-low power operation is achieved via 0.5-1.0 V operation, a 28 fW/bit fully differential subthreshold 6T SRAM, a 90%-efficient DC-DC converter, and a 100-nJ fast Fourier transform (FFT) accelerator to reduce processor workload. Using a combination of novel circuit design, system architecture, and SoC implementation, the first sub-microwatt per channel electroencephalograph (EEG) seizure detection is demonstrated.

2.2 - 10:50 a.m.
A 1.2mW On-Line Learning Mixed Mode Intelligent Inference Engine for Robust Object Recognition, J. Oh, S. Lee, M. Kim, J. Kwon, J. Park, J.-Y. Kim, H.-J. Yoo, KAIST, Korea

An intelligent inference engine (IIE) is proposed as a controller for low power high speed robust object recognition processor. It contains an analog digital mixed mode neuro-fuzzy circuit for the on-line learning to increase attention efficiency. It achieves 1.2mW power consumption with 94% classification accuracy within 1us operation. The 0.765mm2 IIE achieves 76% attention efficiency, and power and processing delay of the 50mm2 recognition processor are reduced by up to 37% and 28%,respectively,with 96 % recognition accuracy.

2.3 - 11:15 a.m.
A Low Power ECG Signal Processor for Ambulatory Arrhythmia Monitoring System, H. Kim, R.F. Yazicioglu, T. Torfs, P. Merken, H.-J. Yoo*, C. Van Hoof, IMEC, Belgium, *KAIST, Korea

An ECG signal processor (ESP) is proposed for ambulatory arrhythmia monitoring systems. The ESP consists of three heterogeneous processors and performs filtering, data compression, ECG classification, and encryption. A data reduction scheme, consisting of skeleton and Huffman coding, are employed to reduce the on-chip memory capacity and memory access power. Clock gating and voltage scaling are also applied to reduce the power consumption. The ESP consumes 1.26-μW at 0.7V, while providing real time signal processing.

2.4 - 11:40 a.m.
1.4μW/Channel 16-Channel EEG/ECoG Processor for Smart Brain Sensor SoC, T.-C. Chen, T.-H. Lee, Y.-H. Chen, T.-C. Ma, T.-D. Chuang, C.-J. Chou, C.-H. Yang, T.-H. Lin, L.-G. Chen, National Taiwan University, Taiwan

A 16-channel smart brain sensor SoC is proposed with the integrated digital EEG/ECoG processor (DEEP) to perform multi-dimension feature space analysis algorithms. The DEEP has three processing pipelines to filter out the artifacts, extract the multi-domain features, and interpret the inherent meanings according to the applications. Dedicated accelera-tors as well as a RISC are embedded to provide efficient computation and flexibility. Processing folding among chan-nels saves the dominating leakage power. 1.4μW/channel power is achieved after the implementation in 90nm process.