SESSION 20 – TAPA I
Signal Processing for Wireless

Friday, June 18, 1:45 p.m.
Chairperson: B. Nikolic, University of California, Berkeley
M. Hariyama, Tohoku University

20.1 - 1:45 p.m.
A 1-190MSample/s 8-64 Tap Energy-Efficient Reconfigurable FIR Filter for Multi-Mode Wireless Communication, F. Sheikh, M. Miller, B. Richards, D. Markovic, B. Nikolic, University of California, Berkeley, USA

An energy-efficient reconfigurable distributed-arithmetic FIR filter for multi-mode wireless communication is fabricated in 7M1P 90nm CMOS and occupies 1.5mm2. A 6-way parallel, 2-way time-multiplexed architecture with circuits for memory offset binary coding and memory partitioning enable input wordlength and tap configurability with 1–190MSample/s throughput and 10–130mW total power measured at 1.1V, 25C.

20.2 - 2:10 p.m.
A 5.8mW 3GPP-LTE Compliant 8x8 MIMO Sphere Decoder Chip with Soft-Outputs, C.-H. Yang, T.-H. Yu, D. Markovic, University of California, Los Angeles, USA

A MIMO chip for 3GPP-LTE standard and beyond is described. The chip implements sphere decoding algorithm with 16-core architecture. The chip is flexible to support multiple configurations: antenna arrays from 2x2 to 8x8, modulations from BPSK to 64QAM, FFT sizes from 128 to 2048 and hard/soft outputs. The chip dissipates 5.8mW for the 3GPP-LTE standard in 3.35mm2 area in 65nm CMOS.

20.3 - 2:35 p.m.
A 4.84 mm^2 847-955 Mb/s 397 mW Dual-Path Fully-Overlapped QC-LDPC Decoder for the WiMAX System in 0.13 µm CMOS, B. Xiang, X. Zeng, Fudan University, China

This paper presents a dual-path fully-overlapped QC-LDPC decoder for the WiMAX system. Each phase scans nonzero sub-matrices two by two in block row-wise order, and two phases are fully overlapped. It reduces memory accesses by 24.3-48.8%, and takes only 48-54 clock cycles per iteration. It is fabricated in SMIC 0.13 µm 1P8M CMOS process, which occupies 4.84 mm2, attains 847-955 Mb/s, and consumes 397 mW with power efficiency of 42 pJ per bit per iteration.

20.4 - 3:00 p.m.
A 10.37 mm2 675 mW reconfigurable LDPC and Turbo encoder and decoder for 802.11n, 802.16e and 3GPP-LTE, F. Naessens, V. Derudder, H. Cappelle, L. Hollevoet, P. Raghavan, M. Desmet, A. AbdelHamid, I. Vos, L. Folens, S. O'Loughlin, S. Singirikonda, S. Dupont, J.-W. Weijers, A. Dejonghe, L. Van der Perre, IMEC, Belgium

This paper describes the implementation of a flexible Turbo and LDPC outer modem engine which is capable of supporting the WiFi(802.11n), WiMax(802.16e) and 3GPP-LTE standard on the same hardware resources. The chip is implemented in a 65nm CMOS technology and occupies 10.37mm2. The maximum clock speed can be set to 320MHz allowing a decoder output rate in excess of 140Mbps for Turbo and 640Mbps for LDPC with a maximum power consumption of 675mW.