SESSION 22 – TAPA I
Nonvolatile Memories

Friday, June 18, 3:40 p.m.
Chairperson: O. Jungroth, Intel Corporation
N. Lu, Etron Technology, Inc.

22.1 - 3:40 p.m.
A 100MHz Ladder FeRAM Design with Capacitance-Coupled-Bitline (CCB) Cell, D. Takashima, Y. Nagadomi, T. Ozaki, Toshiba Corp, Japan

This paper proposes a new ladder FeRAM architecture with CCB cell for high-end embedded application. This configuration realizes small 0.35μm^2 cell using highly reliable large ferroelectric capacitor of 0.145μm^2 and highly compatible process with logic-LSI. The proposed ladder FeRAM with a new early plateline pull-down read scheme also achieves fast random read/write of 10ns cycle and 8ns access at 150C. A 64Kb test chip using 128Mb chain FeRAM process is designed to verify these performances.

22.2 - 4:05 p.m.
A Low Store Energy, Low VDDmin, Nonvolatile 8T2R SRAM with 3D Stacked RRAM Devices for Low Power Mobile Applications, P.-F.Chiu, M.-F. Chang, S.-S. Sheu*, *K.-F. Lin, P.-C. Chiang*, C.-W. Wu, W.-P. Lin*, C.-H. Lin*, C.-C. Hsu, F.T. Chen*, K.-L. Su*, M.-J. Kao*, M.-J. Tsai*, National Tsing Hua University, Taiwan, *EOL, ITRI, Taiwan

This work demonstrates the first fabricated macro-level RRAM-based nonvolatile SRAM that use a new 8T2R (Rnv8T) cell to achieve fast NVM storage and low VDDmin read/write operations. The Rnv8T cell uses two RRAM devices, 3D stacked over the 8T, to achieve low store energy with a compact cell area. A 2T RRAM-switch provides write-assist functions. The fabricated 16Kb Rnv8T macro achieves the lowest store energy and R/W VDDmin (0.45V) than other nvSRAM and “SRAM+NVM” solutions.

22.3 - 4:30 p.m.
OxID: On-Chip One-Time Random ID Generation using Oxide Breakdown, N. Liu, S. Hanson, D. Sylvester, D. Blaauw, University of Michigan, USA

A new chip ID generation method is presented that leverages the random and permanent characteristics of oxide breakdown. A 128b ID array is implemented in 65nm CMOS and two algorithms for stressing the oxides are presented, showing a near-ideal Hamming distance of 63.92 in silicon measurements and consistent IDs across voltage and temperature.

22.4 - 4:55 p.m.
A 60% Higher Write Speed, 4.2Gbps, 24-Channel 3D-Solid State Drive (SSD) with NAND Flash Channel Number Detector and Intelligent Program-Voltage Booster, T. Hatanaka, K. Ishida, T. Yasufuku, S. Miyamoto*, H. Nakai*, M. Takamiya, T. Sakurai, K. Takeuchi, University of Tokyo, *Toshiba Corporation, Japan

The fastest ever 4.2Gbps 3D-SSD with the NAND flash channel number detector and the intelligent boosting scheme is proposed. By dynamically optimizing the switching clock of the booster, the proposed 3D-SSD achieves both the fastest write and the lowest energy consumption. In the sequential write with a large data size, the SSD write speed increases by 60%. In the random write with a small data size, the energy consumption of the booster decreases by 32%.