SESSION 5 – HONOLULU SUITE
Clocking Building Blocks

Wednesday, June 16, 1:30 p.m.
Chairperson: K. Chang, Rambus, Inc.
M. Takamiya, University of Tokyo

5.1 - 1:30 p.m.
A Programmable Phase Rotator Based on Time-Modulated Injection-Locking, F. O'Mahony, B. Casper, M. Mansuri, M. Hossain*, Intel Corp, USA *University of Toronto, Canada

A 7-bit 360-degree phase rotator in 45nm CMOS interpolates between coarse phases by modulating the injection point of an oscillator. This architecture decouples phase resolution from device sizing. INL and DNL are improved by independently adapting the delay of each oscillator stage. A digital phase- locked loop using a time-to-digital converter based on a tracking ADC keeps the oscillator tuned to the injection frequency. The measured DNL and INL at 4.05GHz with phase calibration are 0.4 and 1.2 LSBs, respectively, while consuming 14.3mW.

5.2 - 1:55 p.m.
A 5-20GHz Tunable LC-VCO using Variable Bridge Inductor, A. Tanabe, K. Jijioka, H. Nagase, Y. Hayashi, NEC Electronics Corp, Japan

A wide frequency range tunable LC-VCO is developed using a novel multi-stage variable inductor which has a bridge architecture and a miniature 3D solenoid structure. Because of this inductor, over 15GHz continuous tuning range up to 20GHz is achieved with 10.6mW total power consumption. Phase noise at 1MHz offset is -103dBc/Hz (@10GHz) and -87dBc/Hz (@20GHz). This miniature variable inductor also realizes chip area smaller than 1/10 of reported wide range LC-VCOs.

5.3 - 2:20 p.m.
A 198.9GHz-to-201.0GHz Injection-Locked Frequency Divider in 65nm CMOS, B.-Y. Lin, I.-T. Lee, C.-H. Wang, S.-I. Liu, National Taiwan University, Taiwan

An injection-locked frequency divider (ILFD) is realized in 65nm CMOS technology for G-band (140 to 220GHz) applications. Its core area is $0.2\times0.16mm^2$. This ILFD consumes 8.8mW from a 1.1V supply excluding the buffers. Due to the limited output power of the source module (i.e., frequency multiplier), the measured locking range of this ILFD is from 198.9GHz to 201.0GHz.

5.4 - 2:45 p.m.
A 10MHz to 7GHz Quadrature Signal Generation Using a Divide-by-4/3, -3/2, -5/3, -2, -5/2, -3, -4, and -5 Injection-Locked Frequency Divider, S. Hara, K. Okada, A. Matsuzawa, Tokyo Institute of Technology, Japan

This paper presents a wideband LC-based VCO using a divide-by-fractional-N injection-locked frequency divider (ILFD), and the fractional-N division is realized by the proposed modulated injection technique. A 2-stage differential-type IFLD achieves the multi-decade frequency tuning with quadrature outputs. The proposed circuit is implemented by using a 90nm CMOS process, and the measured results achieves 10MHz-to-7GHz of continuous frequency tuning range with 9.6-15.6mW of power consumption. The chip area is 250 x $200\mu m^2$.