

SESSION 7 – HONOLULU SUITE
Advanced Transceivers Techniques

Wednesday, June 16, 3:25 p.m.

Chairperson: J. Lloyd, Analog Devices
M. Igarashi, Sony Corporation

7.1 - 3:25 p.m.

An Ultra-Wide Range Bi-Directional Transceiver with Adaptive Power Control Using Background Replica VCO Gain Calibration, T. Ebuchi, Y. Komatsu, M. Miura, T. Chiba, T. Iwata, S. Dosho, T. Yoshikawa, Panasonic Corporation, Japan

A novel transceiver with adaptive power control (APC) using a process and frequency monitor (PFM) based on a new power optimization concept is proposed. The PFM employs gain calibration with a replica VCO and operates in the background. A test chip, employing adaptive amplitude scaling, adaptive bias scaling, and adaptive supply-voltage scaling, achieved adaptive power over a wide frequency-range (0.05-3.4Gbps). At 100Mbps the measured power with APC was reduced by 75% compared to conventional architecture without APC.

7.2 - 3:50 p.m.

A 5Gb/s Speculative DFE for 2x Blind ADC-Based Receivers in 65-nm CMOS, S. Sarvari, T. Tahmoureszadeh, A. Sheikholeslami, H. Tamura*, M. Kibune*, University of Toronto, Canada, *Fujitsu Laboratories Limited, Japan

This paper presents the design of a DFE for a 2x blind ADC-based RX. The DFE is implemented in 65-nm CMOS along with a 2x blind CDR and ADC. Our measured results confirm 5Gb/s data recovery with BER less than 1E-12 with a channel introducing 13.3dB of attenuation at the Nyquist frequency of 2.5GHz. Without the DFE, the BER exceeds 1E-8.

7.3 - 4:15 p.m.

A 5Gb/s Automatic Sub-Bit Between-Pair Skew Compensator for Parallel Data Communications in 0.13 μ m CMOS, Y. Zheng, J. Liu*, R. Payne, M. Morgan, H. Lee*, Texas Instruments, Inc., *University of Texas at Dallas, USA

A between-pair skew compensator for parallel data communications is presented. It can detect time skew between two independent data sequences using continuous-time correlations and then automatically align the two using a voltage controlled wide-bandwidth data delay line. A 5Gb/s sub-bit between-pair skew compensator in 0.13 μ m CMOS occupies 0.03mm² active die area and dissipates 22.5mW.

7.4 - 4:40 p.m.

FDM-based Wireless Source Synchronous 15-Mbps TRx with PLL-less Receiver and 1-mm On-chip Integrated Antenna for 1.25-cm Touch-and-Proceed Communication, H. Ishizaki, T. Araki*, S. Takahashi, J. Ryu*, S. Uchida**, N. Yoshida, M. Takamiya*, M. Mizuno, NEC Corporation, Japan, *The University of Tokyo, Japan, **NEC Electronics Corporation, Japan

A 15-Mbps, single-channel wireless source synchronous (SWSS) transceiver with a 1-mm on-chip integrated loop antenna has been developed in 90-nm CMOS for 1.25-cm 'touch-and-proceed communication' between electronic devices. A newly developed FDM-based SWSS architecture makes simultaneous CLOCK and DATA transmission possible with only a single antenna as well as the elimination of PLL and clock recovery blocks in Rx. We have successfully demonstrated a 1.0-cm robust alignment of antenna position for 1.0-cm communication distance with a 1-mm on-chip antenna at BER<10⁻⁵.

7.5 - 5:05 p.m.

A 5Gb/s Link with Clock Edge Matching and Embedded Common Mode Clock for Low Power Interfaces, J. Zerbe, B. Daly, L. Luo, B. Stonecypher, W. Dettloff, J. Eble, T. Stone, J. Ren, B. Leibowitz, M. Bucher, P. Satarzadeh, Q. Lin, Rambus Inc, USA

A 5Gb/s signaling system was designed and fabricated in TSMC's 40nm LP CMOS process. A new clock/data skew minimization technique with a source-synchronous transmit clock delay line and integrating receiver tolerates high frequency transmit clock jitter and supports rapid turn-on without the clock buffer latency of conventional source-synchronous systems. A second method to minimize clock distribution via embedded clocking with superposition of clock in the common-mode was also explored.