

2010 VLSI Circuits Short Course Program
Honolulu I

Circuit Design for Technology Challenges

Tuesday, June 15, 8:30 a.m.

Organizers/Chairs: Azeez Bhavnagarwala, IBM TJ Watson Research
Koichi Nose, Renesas Corp.

- 8:30 a.m. Introduction**
Azeez Bhavnagarwala, IBM TJ Watson Research
- 8:45 a.m. CMOS Technology Trends**
Ghavam Shahidi, IBM TJ Watson Research
- 9:45 a.m. CMOS Logic and Embedded Memory Design**
Kevin Zhang, Intel
- 10:45 a.m. Break**
- 11:00 a.m. Design Methodology and Tools in an Evolving CMOS Technology**
Clive Bittlestone, Texas Instruments
- 12:00 p.m. Lunch**
- 1:00 p.m. Analog/Mixed Signal Design in Digital CMOS**
David Fishette, AMD
- 2:00 p.m. Chip-Package-Co-Design**
Atsushi Nakamura, Renesas
- 3:00 p.m. Break**
- 3:15 p.m. Memory Design**
- a. **Low Power DRAM Circuits and Interface Design**,
Yasuhiro Takia, Elpida
 - b. **Disturbance and interference Issues in NAND Flash Design**
Yeong T. Lee, Samsung
- 5:00 p.m. Conclusion**
Koichi Nose, Renesas Corp.