A-SSCC 2005

The 1st

IEEE Asian Solid-State Circuits Conference

1 - 3 November 2005 - Hsinchu, Taiwan

Advance Program

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A-SSCC 2005 Conference Program: November 1st, 2005

Nov. 1	9:00-9:05	**Opening**			
	9:05-9:50	**Plenary Talk I**(*Ballroom A*)			
		Design and TechnologyCollaboration Shang-yi Chiang(TSMC)			
	9:50-10:35	**Plenary Talk II**(*Ballroom A*)			
		T-Engine: The Open Platform for the Ubiquitous Computing Age Ken Sakamura(University of Tokyo)			
		Break			
	Industry Session 10:50-12:30	**Industry Session I**(*Ballroom A*) Session Chair: Raymond Chiu(ASTRI)	**Industry Session II**(*Ballroom B*) Session Chair: J.L. Yeh(iCreate Technologies)		Design Contest/Poster Session I
		Lunch			
	Session 1-3 13:30-15:10	**Session 1(***Ballroom A***): High-speed interconnects for system integration** Session Co-Chairs: Stefan Rusu(Intel), Vojin Oklobdzija(UCD)	**Session 2(***Ballroom B***): Analog Signal Processing Circuits** Session Co-Chairs: Michael Flynn(University of Michigan), Takahiro Miki(Renesas)	**Session 3(***Ballroom D***): Emerging Sensor and Control Systems** Session Co-Chairs: C. Patrick Yue(Carnegie Mellon), Cheng-Wen Wu(NTHU)	Design Contest/Poster Session I
		Break/Poster discussion(*Ballroom C*)			
	15:40-17:10	**Panel Discussion I**(*Ballroom A*) Moderator: Tohru Furuyama(Toshiba)	**Panel Discussion II**(*Ballroom D*) Moderator: Masao Taguchi(Spansion)		Design Contest/Poster Session I
		Wonder Drug for NRE Explosion: FPGA, Reconfigurable Processor, Structured ASIC, SiP, or Conventional Approach?	What is the Best NV Memory for Portable Digital Consumer Applications?		
	17:15-17:50	Author Interview/Poster discussion(*Ballroom C*)			
	18:00-20:00	Banquet(*Ballroom B*)			

A-SSCC 2005 Conference Program: November 2nd, 2005

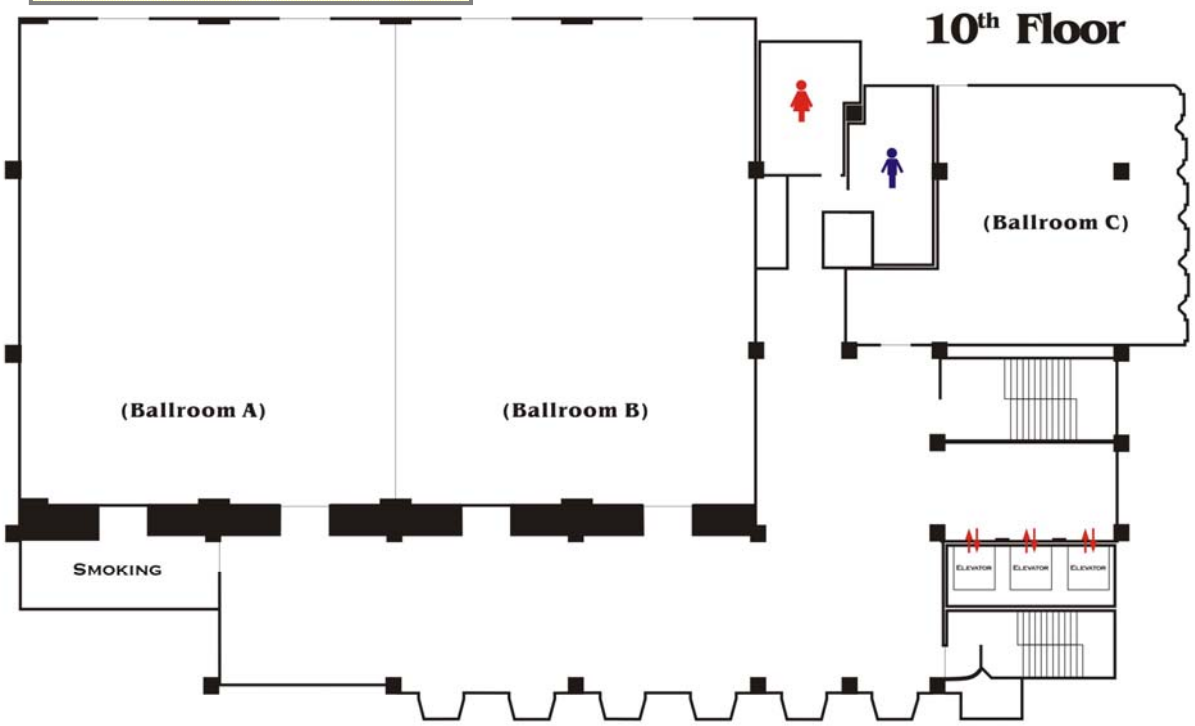
Nov. 2	9:00-9:45	**Plenary Talk III**(*Ballroom A*)			
		Memory Technologies for Mobile Era Kinam Kim(Samsung)			
		Break			
	Session 7-9 10:00-11:40	**Session 4(***Ballroom A***): Memory** Session Co-Chairs: Changhyun Kim(Samsung), Hideto Hidaka(Renesas)	**Session 5(***Ballroom B***): Amplifiers** Session Co-Chairs: Jri Lee(NTU), Hyun-Kyu Yu(ETRI)	**Session 6(***Ballroom D***): Emerging Integration and Voltage Conversion Techniques** Session Co-Chairs: Masahiro Nomura(NEC), David Chang(ITRI)	Poster Session II(Ballroom C)
		Lunch			
	Session 7-9 12:40-14:20	**Session 7(***Ballroom A***): Wireline communication Circuits** Session Co-Chairs: Deog-Kyoon Jeong(SNU), Tai-Cheng Lee(NTU)	**Session 8(***Ballroom B***): Frequency Synthesizers** Session Co-Chairs: Ting-ping Liu(Winbond Electronics), Huei Wang(NTU)	**Session 9(***Ballroom D***): Digital Circuits for Communication Systems** Session Co-Chairs: Chen-yi Lee(NCTU), Myung H. Sunwoo(Ajou University)	Poster Session II
		Break/Poster discussion			
	Session 10-12 14:55-17:00	**Session 10(***Ballroom A***): Wireless Communication Circuits** Session Co-Chairs: Dennis C.W. Lo(Ralink Technology), Mototsugu Hamada(Toshiba)	**Session 11(***Ballroom B***): VCOs and PLLs** Session Co-Chairs: Shen-Iuan Liu(NTU), Seung-Jun Lee(EWHA Womans University)	**Session 12(***Ballroom D***): High-performance Digital Circuits Design** Session Co-Chairs: Hideyuki Kabuo(Matushita), Gin-Kou Ma(ITRI)	Poster Session II
	17:05-17:30	Author Interview/Poster discussion			

A-SSCC 2005 Conference Program: November 3rd, 2005

Nov. 3	9:00-10:15	**Tutorial I**(*Ballroom B*)	**Tutorial II**(*Ballroom D*)
		PLL/DLL C.K. Ken Yang(UCLA)	**Analog Circuit Design Towards Nanometer Technologies** Michiel Steyaert(Katholic University)
		Break	
	10:45-12:00	**Tutorial III**(*Ballroom B*)	**Tutorial IV**(*Ballroom D*)
		Crypto Chip Design Cetin Kaya Koc(Oregon State University)	**High Performance DRAM Design** Young-Hyun Jun(Samsung)
		Lunch	
	13:00-14:15	**Tutorial I**(*Ballroom B*)	**Tutorial II**(*Ballroom D*)
		PLL/DLL C.K. Ken Yang(UCLA)	**Analog Circuit Design Towards Nanometer Technologies** Michiel Steyaert(Katholic University)
		Break	
	14:45-16:00	**Tutorial III**(*Ballroom B*)	**Tutorial IV**(*Ballroom D*)
		Crypto Chip Design Cetin Kaya Koc(Oregon State University)	**High Performance DRAM Design** Young-Hyun Jun(Samsung)

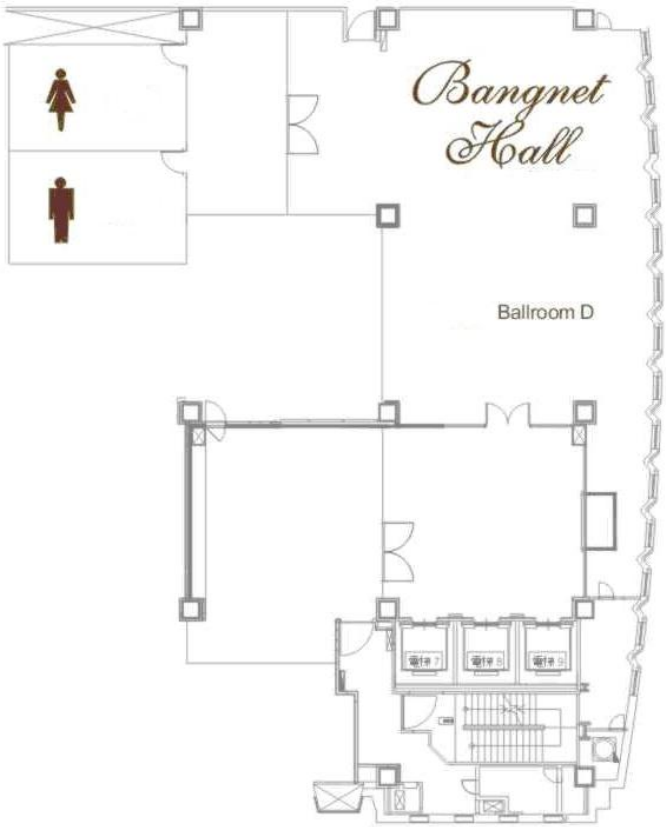
10th F

Ballroom A, B, C



11th F

Ballroom D



Session P-I Plenary Talk I

Nov. 1 9:05-9:50

P-I 9:05-9:50

Design and Technology Collaboration

Shang-Yi Chiang(TSMC)

Keywords:

Abstract: With the advancement of technology into nanometer regime, the complexity of design at advanced technology has escalated exponentially. Notable areas of difficulty are timing closure, signal integrity, power optimization etc. Many of the issues facing designers, however, can be lessened or resolved by close collaboration with technology partners. Advanced foundries, with estimated close to 40% of worldwide 90nm tapeouts, are taking several initiatives to help designers make best use of the technologies. The goal of the collaboration is to produce designs that are competitive in both performance and cost structure. In this presentation, I will discuss key initiatives in TSMC's design collaboration and share collaboration results.

Session P-II Plenary Talk II

Nov. 1 9:50-10:35

P-II 9:50-10:35

T-Engine: The Open Platform for the Ubiquitous Computing Age

Ken Sakamura(University of Tokyo)

Keywords:

Abstract: T-Engine is an open platform for embedded systems in the ubiquitous computing age. It consists of standard real-time kernel, T- Kernel, running on the standard hardware with networking facilities. It provides infrastructure for the embedded system development of highly networked and highly value-added products in a short period of time. Providing a standard platform for the ubiquitous computing network, the T Engine creates broad application opportunities based on the collaboration of nanoelectronics, software and embedded system technologies. This plenary talk provides introduction of the T-Engine project and its current status, and vision of the future of the ubiquitous computing opened up by the T-Engine.

Session P-III Plenary Talk III

Nov. 2 9:00-9:45

P-III 9:00-9:45

Memory Technologies for Mobile Era

Kinam Kim(Samsung Electronics)

Keywords:

Abstract: For last three decades, semiconductor memory business has been greatly grown due to the tremendous progress of electronic data processing (EDP) mainly led by outstanding evolution of PC technology. Recently, various mobile appliances such as hand-held phone, DCS, and MP3 drive new

growth of semiconductor memory, which results in unprecedented demand of non-volatile memories, especially mass storage NAND Flash. The mobile appliances which aim for smaller and lighter products while improving the performance under ever-increased demand of longer battery lifetime impose different requirements on the semiconductor memories. The newly defined requirements along with short life cycle and customer orientation of mobile products transform the memory semiconductor from standard data storage memory to diverse solution memory. It is predicted that this trend will be magnified in the future memory market. In this paper, it will be discussed about the technology trend of memory semiconductor in the mobile era and also the memory technology required to satisfy the mobile appliances.

Session I-I Industry Session I

Nov. 1 10:50-12:30

Session Chair: *Raymond Chiu(ASTRI)*

I-I-1 10:50-11:15

A Comparison between 63nm 8Gb and 90nm 4Gb Multi-Level Cell NAND Flash Memory for Mass Storage Application

Dae-Seok Byeon(Samsung Electronics), Sung-Soo Lee(Samsung Electronics), Young-Ho Lim(Samsung Electronics), Dongku Kang(Samsung Electronics), Wook-Kee Han(Samsung Electronics), Dong-Hwan Kim(Samsung Electronics), Kang-Deog Suh(Samsung Electronics)

Keywords:

Abstract: This paper compares design concepts of 63nm-8Gb and 90nm-4Gb multi-level cell (MLC) NAND flash memory. For 8Gb MLC NAND flash memory, locations of peripheral circuits and charge pumps are determined to optimize area and signal speed. Page buffer is simplified by reducing the number of transistor with minimal connection thereby resulting in the smaller size. The performance is mainly improved by using fast read/write cycle with reduced signal paths. Furthermore, two-MAT-cell-array architecture is used for 2x read/write operations. Various techniques are used to suppress noisy effects such as common source line (CSL) noise and coupling noise.

I-I-2 11:15-11:40

A 16M SRAM with Improved Characteristics Using DRAM Technology

Yuji Kihara(Renesas Technology Corp.), Yasushi Nakashima(Renesas Technology Corp.), Takashi Izutsu(Renesas Technology Corp.), Masayuki Nakamoto(Renesas Technology Corp.), Yasuhiro Konishi(Renesas Technology Corp.), Tsutomu Yoshihara(Waseda University)

Keywords:

Abstract: A 16Mbit Low Power SRAM with a 0.98um^2 cell using 0.15um DRAM and TFT technology has been developed. A new type memory cell technology achieves enough low power, low cost and high soft error immunity without large investment

I-I-3 11:40-12:05

The Power Conscious Synergistic Processor Element of a CELL Processor

Scott Cottier(IBM Systems and Technology Group, Austin, TX), Osamu Takahashi(IBM Systems and Technology Group, Austin, TX), Sang Dhong(IBM Systems and Technology Group, Austin, TX), Brian

Flachs(IBM Systems and Technology Group, Austin, TX), Koji Hirairi(Sony Computer Entertainment of America, Austin, TX), H. Peter Hofstee(IBM Systems and Technology Group, Austin, TX), Brad Michael(IBM Systems and Technology Group, Austin, TX), Hiromi Noro(Toshiba America Electronic Components), Dieter Wendel(IBM Systems and Technology Group, Austin, TX), Michael White(IBM Systems and Technology Group, Austin, TX)

Keywords: CELL, Synergistic Processor, Low Power, Architecture
Abstract: A 4-way SIMD Streaming Processor of a CELL Processor is developed in a 90nm SOI technology. CMOS static gates implement the majority of the logic. Dynamic circuits are used in critical areas, occupying 19% of the non-SRAM area. ISA, micro-architecture, and physical implementation are co-optimized to achieve a compact and power efficient design.

I-I-4 12:05-12:30

A Wireless LAN Baseband LSI for High-Definition A/V Content Transmission

Hideaki Nakakita(Toshiba Corp.), N. Kato(Toshiba Corp.), T. Wakutsu(Toshiba Corp.), Y. Miyamoto(Toshiba Corp.), A. Yamaga(Toshiba Corp.), S. Kaburaki(Toshiba Corp.), M. Sekiya(Toshiba Corp.), T. Kamimura(Toshiba Corp.), K. Matsue(Toshiba Corp.), K. Tsuchie(Toshiba Corp.)

Keywords:
Abstract: This paper presents the first wireless LAN baseband LSI capable of transmitting the high-definition audio with video (HD-A/V) contents with secure content protection. The LSI fully complies with the IEEE 802.11a, e, h, and i. The Hybrid Coordination function controlled Channel Access (HCCA) of the 802.11e is employed to guarantee the period transmitting the HD A/V contents. In addition, the block acknowledgement of the 802.11e with a forward error correction mechanism is introduced to increase the throughput. Moreover, the digital transmission content protection over the Internet protocol (DTCP-IP) is implemented to prohibit casual copying. High availability of this LSI is provided by two kinds of host interfaces (PCI-bus and IIC-bus), a MPEG2 Transport Stream interface, and a digital beam forming LSI interface.

Session I-II Industry Session II

Nov. 1 10:50-12:30

Session Chair: *J.L. Yeh(iCreate Technologies)*

I-II-1 10:50-11:15

A Vernier Over Sampling and Alignment Technique for Gb/s Serial Communication

Kazuyuki Omote(THine Electronics), Katsunori Shimizu(THine Electronics), Jun-Ichi Okamura(THine Electronics)

Keywords: Hi-speed Serial Communication, Over Sampling, PLL, DLL
Abstract: A new circuit technique of de-serializing for Gb/s serial communication is proposed. Vernier Over Sampling and Alignment technique can achieve both low power and low bit error rate at high frequency operation in serial communication receiver application. VOSA circuit is simple and mostly digitally controlled, therefore it is robust and portable. Demonstrating VOSA performance, the circuit is implemented to the digital flat panel communication link receiver as Hard-IP core with the industry standard 0.25um CMOS process.

I-II-2 11:15-11:40

A Wide Band CDR for Digital Video Data Transmission

Seiichi Ozawa(THine Electronics), Satoshi Miura(THine Electronics), Seiichi Kousokabe(THine Electronics), Yohei Ishizone(THine Electronics), Shinichiro Tomosugi(THine Electronics), Jun-Ichi Okamura(THine Electronics)

Keywords: CDR, Serial Interface

Abstract: This paper describes a wide band CDR with a new encoding scheme for a digital video data transmission. The CDR works from 105Mbps to 1365Mbps without any external frequency references. The proposed encoding scheme uses both PECT (Periodic Embedded Clock Transition) and PECT (Periodic Embedded Clock Period) scheme, and it helps the CDR's capture process. The CDR is using both digital and analog techniques. Digital block adjusts VCO frequency utilizing PECT and PECP scheme, and analog block maintains lock with small jitter.

I-II-3 11:40-12:05

A Sub-1V CMOS 2.5Gb/s Serial Link Transceiver Using 2X Oversampling

Chih-Chien Hung(RealTek Corp.), Ming-Cheng Chiang(RealTek), An-Ming Lee(RealTek), Sheng-Chou Lee(RealTek)

Keywords:

Abstract: This paper presents the design of a 2.5Gb/s serial link transceiver with a power consumption of 70mW. With 1V supply voltage, the transceiver achieves the bit error rate of 10^{-14}. A supply regulated PLL is shared by the transmitter and the receiver to facilitate the low-power and low-voltage design. The output jitter of the transmitter is 53.9ps peak-to-peak and the chip area is approximately 0.54 mm^2.

I-II-4 12:05-12:30

3.3/5V Multi-rate Laser Diode Driver and Limiting Amplifier for Optical Transceivers

Mark Chen(iCreate Technologies Corporation), Chihyang Wang(iCreate Technologies Corporation)

Keywords:

Abstract: A laser diode driver and a limiting amplifier for multi-rate and multi-standard optical transceiver modules from 155Mb/s to 2.1Gb/s had been developed using a 0.5μm SiGe BiCMOS technology. With new driving circuit, the laser can be DC-coupled to the laser diode driver for reduced component count and ease of multi-rate operation. Automatic power control (APC), modulation compensation and built-in temperature-compensation are also achieved. Careful circuit design enables the limiting amplifier to realize better input sensitivity of 2mVp-p and provides approximately 50dB of gain. A novel Received Signal Strength Indicator (RSSI) circuit is proposed to accomplish the input signal-detect function, and the circuit complexity and current consumption can be reduced. A low-frequency feedback loop is integrated in the limiting amplifier to reduce input offset, making it below 100uV typically.

Session 1　High-speed interconnects for system integration

Nov. 1　13:30-15:10

Session Co-Chairs: *Stefan Rusu(Intel) and Vojin Oklobdzija(University of California, Davis)*

1-1　13:30-13:55

A 3-mW, 270-Mbps, Clock-Edge Modulated Serial Link for Mobile Displays

Won-Jun Choe(Seoul National University), Bong-Joon Lee(Seoul National University), Jaeha Kim(Seoul National University), Deog-Kyoon Jeong(Seoul National University), Gyudong Kim(Silicon Image Inc.)

Keywords:

Abstract: In this paper, a single channel clock-edge modulated serial link for mobile display interface is presented. Clock edge modulation (CEM) enables all necessary signals between a graphics processor and a LCD timing controller to be transferred over a single, DC-balanced differential channel, thus greatly saving the power and costs of the existing parallel lines. A simple DLL-based CEM decoder is described that recovers the data with low power consumption and high jitter tolerance. The use of a voltage-mode driver and a single-side termination further reduces the power. A prototype CEM transceiver was implemented in a 0.18um CMOS process and dissipates 3.12mW when operating at 270-Mb/s and 1.2V.

1-2　13:55-14:20

A 667MT/s 10.7GB/s Multiprocessor Bus Interface

Harry Muljono(Enterprise Microprocessor Group), Stefan Rusu(Intel Corp.), Kathy Tian(Intel Corp.), Mubeen Atha(Intel Corp.)

Keywords: I/O, analog, processor

Abstract: A 130nm 1.2V GTL bus interface with compensated slew rate and termination achieves 667MT/s 10.7MB/s data rate in a 3-load MP environment. The design utilizes preboost and postboost methods, current steering circuit to minimize simultaneous switching noise and negative hysteresis to speed up the common-clock delay. The design also incorporates system-level I/O loopback for system timing marginality test.

1-3　14:20-14:45

A 6-Gbps/pin Half-Duplex LVDS I/O　for High-Speed Mobile DRAM

Sua Kim(Sungkyunkwan University), Jin-Hyun Kim(Samsung Electronics), Woo-Seop Kim(Samsung Electronics), Bae-Sun Kong(Sungkyunkwan University), Chil-gi Lee(Sungkyunkwan University), Young-Hyun Jun(Samsung Electronics), Changhyun Kim(Samsung Electronics)

Keywords: LVDS, I/O, DRAM

Abstract: This paper presents a high-speed LVDS I/O interface for mobile DRAMs. The data rate of 6Gbps/pin and transmit-jitter of 57.31ps pk-pk was demonstrated using an 800MHz clock and 200mV swing. The power consumed by the only I/O circuit was measured to be 6.2mW/pin, when connected to a 10pF load, at a 1.2V output supply voltage. The proposed mobile DRAM has 6-data pin and 4-address/commad pin for multi-chip package (MCP). The transmitter uses a feed-back LVDS output driver and a common-mode feed-back controller, achieving the reduction of driver currents and the

constant common-mode as half voltage level. To achieve the low-transmit jitter, the driver uses the double step pre-emphasis. The receiver employs a shared pre-amplifier scheme. This scheme ensures transmit power reduction. The proposed DRAM with LVDS I/O is fabricated using an 80-nm, DRAM process. It exhibits 161.1mVx150ps rms eye-windows on the given channel

1-4 14:45-15:10

A Self-Calibrate All-Digital 3Gbps SATA Driver Design

Hsin-Wen Wang(National Chiao Tung University), Hung-Wen Lu(National Central University), Chau-Chin Su(National Chiao Tung University)

Keywords: high-speed serial link

Abstract: This paper presents an all digital Low Voltage Differential Signal (LVDS) driver for Serial-ATA (SATA-II) with simultaneous switching noise (SSN) reduction capability. An auto calibration mechanism is included to deal with the process and environmental variation. The chip is implemented using TSMC 0.18μm 1P6M CMOS technology. The core area is 350x350μm^2. The transmitter operates at 3 Gbps under a 1.8V power supply and consumes 11mW of power.

Session 2 Analog Signal Processing Circuits

Nov. 1 13:30-15:10

Session Co-Chairs: *Michael Flynn(University of Michigan) and Takahiro Miki(Renesas)*

2-1 13:30-13:55

A 14-bit 20-MS/s Pipelined ADC with Digital Distortion Calibration

Mutsuo Daito(Sharp Corporation), Hirofumi Matsui(Sharp Corporation), Masaya Ueda(Sharp Corporation), Kunihiko Iizuka(Sharp Corporation)

Keywords: Pipelined ADC, Digital Calibration, Distortion Calibration

Abstract: We present a 14-bit 20-MS/s pipelined analog-to-digital converter (ADC) using a new digital distortion calibration technique. The calibration parameters are obtained using the same system as the conventional digital gain calibration. The ADC has been fabricated in a 0.18μm CMOS process and consumes 33.7 mW at 2.8 V. With the calibration it achieves 15-dB improvement of the third-order nonlinearity. The measured SNDR and SFDR are 71.6 dB and 82.3 dB respectively.

2-2 13:55-14:07

Reconstructive Oscillator Based Sinusoidal Signal Generator for ADC BIST

Hsin-Wen Ting(National Cheng Kung University), Cheng-Wu Lin(National Cheng Kung University), Bin-Da Liu(National Cheng Kung University), Soon-Jyh Chang(National Cheng Kung University)

Keywords: reconstructive oscillator, sigma-delta modulator, built-in self-test, transmission parameters, static parameters

Abstract: This paper presents a reconstructive oscillator based sinusoidal signal generator which can produce both high and low frequency signals by switching the oscillator into different mode. In addition, analog and digital signals can be produced concurrently in both modes. Also, signal amplitude and oscillation frequency can be precisely controlled compared with pure analog signal generator. Except for

a 1-bit D/A converter and analog filter, the circuits are entirely constructed by digital circuits. One can trade the digital hardware complexity to moderate the difficulties in designing the analog reconstructive filter. The generated high and low frequency signals are suitable to serve as the test stimuli in built-in self test methodology for A/D converters to extract the transmission and static parameters, respectively.

2-3 14:08-14:20

Practical Synthesis of 13-bit 40-MSample/s Pipelined ADC

Yu-Tsun Chien(SoC Technology Center, Industrial Technology Research Institute), Gin-Kou Ma(Industrial Technology Research Institute), Tamal Mukherjee(Carnegie Mellon University)

Keywords: ADC, Pipelined, Analog Synthesis

Abstract: A 13-bit pipelined ADC achieving 67 dB SNDR without digital calibration while consuming 313mW @ 3.3V 40 MSPS is esigned using analog synthesis tools. The MDACs in the pipeline have identical topology and can be synthesized to optimize pipeline performance in less than 1 day. Figure of merit of the three test keys comparing a manually designed, partially synthesized, and fully synthesized ADC is reported showing the efficacy and efficiency of the proposed approach.

2-4 14:20-14:45

An Outside-Rail Opamp Design Targeting for Future Scaled Transistors

Koichi Ishida(University of Tokyo), Atit Tamtrakarn(University of Tokyo), Hiroki Ishikuro(Toshiba Corp.), Takayasu Sakurai(University of Tokyo)

Keywords: technology scaling, analog circuit design, opamp

Abstract: An outside-rail output opamp targeting for future scaled MOSFETs is designed and the 3-V-output operation is successfully verified using 1.8-V standard CMOS process. This is the first experimental verification of an outside-rail opamp design which shows area advantage over un-scaled and inside-rail design while keeping signal-to-noise ratio and gain bandwidth constant. The proposed opamp realizes 3-V output swing without gate-oxide stress although implemented in a 1.8-V 0.18-um standard CMOS process. The chip area is estimated to be 47% of the conventional opamp using a 0.35-um CMOS and about an order of magnitude smaller compared with the conventional inside-rail 0.18-um CMOS design due to reduced capacitor area.

2-5 14:45-14:57

Sampled-and-Hold Based Automatic Calibration Modulator for WLAN Transmitter

Chao-Shiun Wang(National Taiwan University), Chorng-Kuang Wang(National Taiwan University)

Keywords:

Abstract: This paper presents an automatic calibration circuit to correct the I/Q imbalance and DC offset in the modulator of a WLAN transmitter. The impairments are estimated and compensated by a sampled-and-hold negative feedback circuits. The circuit architecture is controlled by an on chip 12 steps state machine. After the calibration, the LO leakage at the modulator output can be suppressed more than 50dB. The side band unwanted signal also can be eliminated 45dB at least. The proposed self-calibrated modulator with quadrature LO generator is implemented in 0.25μm 1P5M mixed-mode CMOS process. The chip area is 1.2mm x 1.7mm. The total power dissipates 17 mW at 1.1~1.3 GHz from a single 2.5V supply voltage.

2-6 14:58-15:10

Low Power 0.18um CMOS Dual-Band Front-End

Kittichai Phansathitwong(Lund University), Henrik Sjoland(Lund University)

Keywords: CMOS receiver frontend dual-band

Abstract: A dual-band CMOS front-end was designed and fabricated in a 0.18um CMOS process. The front-end employs a common-gate low noise amplifier (LNA) with capacitive cross coupling (CCC) technique and a passive mixer. The band selection is performed by switching a capacitor in and out of the LNA load, changing the resonance frequency between 2.2GHz and 4.0GHz. The measured noise figure is below 3.5dB for both frequency bands for supply voltages from 1.8V down to 1V. The conversion gain is more than 10dB, and the third order intercept point (IIP3) is above -6dBm. The circuit draws 2.4mA from a 1V supply.

Session 3 Emerging Sensor and Control Systems

Nov. 1 13:30-15:10

Session Co-Chairs: *C. Patrick Yue(Carnegie Mellon) and Cheng-Wen Wu(National TsingHua University)*

3-1 13:30-13:55

A 142dB Dynamic Range CMOS Image Sensor with Multiple Exposure Time Signals

Jong-Ho Park(Shizuoka University), Mitsuhito Mase(Shizuoka University), Shoji Kawahito(Shizuoka University), Masaaki Sasaki(Sendai National College of Technology), Yasuo Wakamori(Yamaha Corp.), Yukihiro Ohta(Hamamatsu Industrial Research Institute of Shizuoka Prefecture)

Keywords:

Abstract: A ultra wide dynamic range image sensor with a linear response is presented. The proposed extremely short accumulation (ESA) signal readout technique enables the dynamic range of image sensor to be expanded up to 142dB. Including the ESA signals, total of 4 different accumulation time signals are read out in one frame based on burst readout mode. To achieve the high-speed readout required for the multiple exposure signals, column parallel A/D converters are integrated at the upper and lower sides of pixel array. The improved column parallel cyclic 12-b ADC with a built-in CDS circuit has the differential non-linearity of +0.3LSB/-0.3LSB.

3-2 13:55-14:20

A Large-Displacement CMOS-Micromachined Thermal Actuator with Capacitive Position Sensing

Li-Sheng Zheng(National Tsing Hua University), Michael Lu(National Tsing Hua University)

Keywords: CMOS MEMS, Capacitive sensing, Input-referred noise

Abstract: We present the design and characterization of a large-displacement thermal actuator fabricated in a conventional CMOS process. The thermally-driven microstructure is fabricated by two dry etching steps after the completion of CMOS. To avoid drift caused by change of ambient temperature, we adopt a capacitive sensing scheme that uses vertically sensed comb electrodes with a nominal sensing capacitance of 40 fF. The microactuator is characterized by static and dynamic measurements, with a measured out-of-plane motion up to 24 um at 17 mW, and a thermal time constant of 0.24 ms. The

measured minimum input-referred noise voltage of the sensing pre-amplifier is 5.9 uV/rtHz, equivalent to a noise displacement of 0.16 nm/rtHz.

3-3 14:20-14:32

A Monolithic Control Circuit for a 1cm^3 Microrobot for Biological Experiments

Raimon Casanova(University of Barcelona), Angel Dieguez(University of Barcelona), Junajo Lacort(University of Barcelona), Marc Nierlich(Fraunhofer-Institute for Biomedical Engineering), Oliver Steinmetz(Fraunhofer-Institute for Biomedical Engineering), Anna Arbat(University of Barcelona), Manel Puig-Vidal(University of Barcelona), Josep Samitier(University of Barcelona)

Keywords: Microrobotics, piezoactuators control, digital controller, low power

Abstract: A digital controller for a 1 cm^3 microrobot fabricated in a 0.35μm CMOS process is presented. The robot is provided with two piezoatuators based on stick-slip and non-sliding movement: a carrier platform and a rotor to position an arm provided with a nanomanipulation tool as an AFM tip. The control signals are generated by the controller chip using the Bresenham algorithm. It has been adapted to the robot movements improving the power consumption. Power reduction is of at least 30%.

3-4 14:33-14:45

Realization of Trans-impedance Amplifier for Particle Counting Chip

Jung-Tang Huang(National Taipei University of Technology), Hsin-Nan Chen(National Taipei University of Technology)

Keywords: transimpedance amplifier, particle count

Abstract: MEMS (Micro Electro Mechanical Systems) technology could be applied on bio-chips to measure and detect micro objects. Generally, the detected signal is so small that we need to amplify it for next processing (such as A/D converter). In this study, we develop a trans-impedance amplifier (TIA) circuit to detect the blocking conductance when particles across an ion-pore. Consider the simple circuits, simple manufacture process, and the capability of integrating with MEMS process, The TIA circuit and the MEMS ion-pore is designed based on 0.35um CMOS process. The measured results of this amplifier are 94dBΩ high gain, low noise as the M.D.S. of 25nA, and the bandwidth larger than 15MHz.

3-5 14:45-14:57

On-Chip Voice-Coil Motor Driver for Mobile Auto-Focus Camera Applications

Sung-Hyun Yang(LG Electronics), Sung-Min Sohn(LG Electronics), Kuk-Tae Hong(LG Electronics), Hyeong-Soo Lee(LG Electronics), Bo-Ik Sohn(LG Electronics)

Keywords: Voice-Coil Motor (VCM), VCM Driver, Digital camera

Abstract: On-chip voice-coil motor (VCM) driver for mobile auto-focus (AF) camera applications is proposed and integrated with image signal processor (ISP) satisfying small size and low-power consumption. In order to control the location of AF lens, a charge pump (CP) or digital-to-analog converter (DAC) can be selected. Since a large current is required to drive the VCM, the buffer amplifier was inserted after charge pump or DAC. On-chip VCM driver is fabricated using a commercial 0.18um CMOS technology. As the result, the chip shows the fast speed enough to operate with 30-fps image signal processor and the quiescent current consumption of 0.32-mA. The total IP size of the on-chip VCM driver is 480umx436um.

3-6 14:58-15:10

Initial-On ESD Protection Design with PMOS-Triggered SCR Device

Ming-Dou Ker(National Chiao-Tung University), Shih-Hung Chen(SoC Technology Center, Industrial Technology Research Institute)

Keywords: ESD Protection Circuit, Initial-On SCR Design

Abstract: A novel SCR design with *initial-on* function is proposed to achieve the lowest trigger voltage and the fastest turn-on speed of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on design is implemented by PMOS-triggered SCR device, which can be realized in general CMOS processes. This initial-on SCR design also presents a high enough holding voltage to avoid latchup issue. The new proposed initial-on ESD protection design with PMOS-triggered SCR device has been successfully verified in a 0.25μm CMOS process.

Session 4 Memory

Nov. 2 10:00-11:40

Session Co-Chairs: *Changhyun Kim(Samsung) and Hideto Hidaka(Renesas)*

4-1 10:00-10:25

SRAM Circuit with Expanded Operating Margin and Reduced Stand-by Leakage Current Using Thin-BOX FD-SOI Transistors

Masanao Yamaoka(Hitachi, Ltd., Central Research Laboratory), Ryuta Tsuchiya(Hitachi, Ltd., Central Research Laboratory), Takayuki Kawahara(Hitachi, Ltd., Central Research Laboratory)

Keywords: low-power SRAM, thin-BOX FD-SOI, operating margin, leakage current

Abstract: We propose a low-power SRAM circuit using thin-BOX FD-SOI transistors. The SRAM circuit uses back-gate bias effectively, and acquires high operating margin and high speed operation under low supply voltage. The leakage current in stand-by state is reduced. This SRAM achieves 30% faster writing time under low-voltage operation, and 90% less stand-by power.

4-2 10:25-10:50

A Low Power 128Mb Pseudo SRAM Using Hyper Destructive Read Architecture

Jin-Hong Ahn(Hynix Semiconductor Inc.), Sang Hoon Hong(Hynix Semiconductor Inc.), Jae-Bum Ko(Hynix Semiconductor Inc.), Se Jun Kim(Hynix Semiconductor Inc.), Sung-Won Shin(Hynix Semiconductor Inc.), Hee-Bok Kang(Hynix Semiconductor Inc.), Jae-Jin Lee(Hynix Semiconductor Inc.), Joong-Sik Kih(Hynix Semiconductor Inc.)

Keywords: peudo SRAM

Abstract: A 128Mb Pseudo SRAM is developed using a special type of architecture with the purpose of effectively reducing the standby current. Standby current, especially the off leakage current is becoming more difficult problem to handle in modern devices because shorter channel length in high density and high speed devices are at a point where off leakage is the major source. In order to solve this issue, Hyper Destructive Read Architecture (HyDRA) is developed. HyDRA is a special DRAM architecture enabling destructive reading of DRAM cells using global bitline and extra tag memory. The paper demonstrates

HyDRA utilizing its fast row cycle capability to instead minimize standby power to 150uA @ 2.1V and 90°C while maintaining the speed and chip area of the conventional scheme using the same process technology.

4-3 10:50-11:15

A 75MHz MRAM with Pipe-Lined Self-Reference Read Scheme for Mobile Robotics Memory System

Taeyun Kim(Waseda University), Tsutomu Yoshihara(Waseda University), Tsukasa Ooishi(Renesas Technology Corp.), Fuminori Kimura(Waseda University), Yusuke Matsui(Waseda University), Yuji Kihara(Renesas Technology Corp.), Masahiro Hatanaka(Renesas Technology Corp.)

Keywords: MRAM, Memory, Reference Amp.

Abstract: In this paper, we propose a pipe-lined self-reference read scheme of MRAM with read modify write which can make an operation period short. It also brings continuous read out accompanied with a mixed mat architecture. A self-reference sense amplifier supported by a voltage trans-ferred circuit has a wide margin. It is able to tolerate 50% MTJ resistance variation for sensing operation, and makes 75MHz operation at 1.2V Vcc possible. It brings a robust memory module for embedded memory system and suits mobile/robotics memory system.

4-4 11:15-11:27

An Internal Voltage Generation System of Flash Memory Module Embedded in a Microcontroller

Hiroyuki Tanikawa(Renesas Technology Corp.), Toshihiro Tanaka(Renesas Technology Corp.), Akira Kato(Renesas Technology Corp.), Takashi Yamaki(Renesas Technology Corp.), Yukiko Umemoto(Renesas Technology Corp.), Jiro Ishikawa(Renesas Technology Corp.), Takeshi Shimozato(Renesas Technology Corp.), Isao Nakamura(Renesas Technology Corp.), Yutaka Shinagawa(Renesas Technology Corp.)

Keywords: flash, voltage generator, verify, trimming, temperature dependency generator

Abstract: We present a new internal voltage generation system of flash memory module embedded in a microcontroller. One of the features is wide range voltage generator for the evaluation of the memory cell, which is effective mainly at the development early stage. The second feature is new temperature dependency voltage generator matched to memory cell property for the improvement of reliability. The third is an auto-trimming system that arranges output of internal voltage generators with target values. It suppresses voltage variations for many chips simultaneously, so we can reduce test cost and improve reliability in the stage of mass production.

4-5 11:28-11:40

An Experimental 1Mb 0.11um 4.5F2 1.8Volt Multilevel Vertical Split Gate Source Side Injection Test Vehicle for Giga-Bit Density NOR Flash Memory

Hieu V Tran(Silicon Storage Technology, Inc), Anh Ly(Silicon Storage Technology, Inc), Vishal Sarin(Silicon Storage Technology, Inc), Sang Nguyen(Silicon Storage Technology, Inc), Hung Nguyen(Silicon Storage Technology, Inc), Loc Hoang(Silicon Storage Technology, Inc), Huyn-Bai Kim(Silicon Storage Technology, Inc), Isao Nojima(Silicon Storage Technology, Inc), Dana Lee(Silicon Storage Technology, Inc)

Keywords: Flash, MLC, Vertical Split Gate, Coupled Senseline Incremental Program, SF sense

Abstract: An experimental 0.11um 4.5F2 1.8V multilevel 1Mb vertical floating gate split gate source side injection (SSI) test vehicle for Giga-bit NOR flash memory is shown for the first time. Novel coupled sense line programming for 25mV precise charge placement and novel low cell current ~10ua mode source follower sense amplifier is shown to enable high speed high density G-bit MLC NOR flash memory system.

Session 5 Amplifiers

Nov. 2 10:00-11:40

Session Co-Chairs: *Jri Lee(National Taiwan University) and Hyun-Kyu Yu(ETRI)*

5-1 10:00-10:25

A 0.1-25.5-GHz Differential Cascaded-Distributed Amplifier in 0.18-um CMOS Technology

Chihun Lee(National Taiwan University), Lan-Chou Cho(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords:

Abstract: A differential distributed amplifier employs a loss-compensation L section to increase the bandwidth of the interstage by a factor of 3.5. To demonstrate the proposed circuit, a cascaded distributed amplifier with five stages is presented. It has been fabricated in a 0.18μm CMOS process and achieves a gain of better than 15 dB and a pass bandwidth of 100 MHz to 25.5 GHz while consuming 171 mW from a 1.9-V supply.

5-2 10:25-10:50

Low Power 60 dB Gain Range with 0.25 dB Resolution CMOS RF Programmable Gain Amplifier for Dual-band DAB/T-DMB Tuner IC

Tae Wook Kim(Integrant technologies, Inc.), Bonkee Kim(Integrant technologies, Inc.), Youngho Cho(Integrant technologies, Inc.), Seyeob Kim(Integrant Technologies, Inc.), Boeun Kim(Integrant technologies, Inc.), Kwyro Lee(KAIST)

Keywords: CMOS, DAB, IIP3, PGA, Linearity.

Abstract: Low power CMOS RF digitally programmable gain amplifiers for dual-band (Band-III and L-Band) DAB/T-DMB receiver IC are implemented using 0.18 mm CMOS process. For a stable operation among large interference situation, it is required to have wide gain range and fine resolution in RF domain. In order to meet such requirements, various programmable gain amplifier architectures are proposed. Also employing a Differential Multiple Gated TRansistor (DMGTR) technique which is a differential circuit gm cancellation method, maximum 22 dB IIP3 improvement is obtained. The IC exhibits 60 dB gain range with 0.25 dB resolution, 2.7 dB NF, -14 dBm IIP3 and 42 dB voltage gain at 22 mW power consumption for L-Band case, 50 dB gain range with 0.25 dB resolution, 3 dB NF, -5 dBm IIP3 and 28 dB voltage gain for Band-III case at 16mW power consumption.

5-3 10:50-11:15

A Fully Integrated CMOS RF Power Amplifier with Parallel Power Combining and Power Control

Patrick Reynaert(KULeuven ESAT-MICAS), Michiel Steyaert(KULeuven ESAT-MICAS)

Keywords: CMOS, RF Power Amplifier, power combining

Abstract: This paper presents a fully integrated RF power amplifier (PA) operating at 2.45 GHz and integrated in a 0.13um CMOS technology. To achieve an output power of 23dBm, the architecture consists of four amplifiers whose outputs are combined by an on-chip power combining and matching network. The power added efficiency is 28% at 2.45 GHz and -6dBm input power. At lower power levels, the efficiency is increased by using only one power amplifier. This technique reduces the power consumption of the driver stages. The presented fully integrated solution reduces the required board area and increases the overall transmitter efficiency.

5-4 11:15-11:40

A 1.0-V 15.6-dBm 39.5%-PAE CMOS Class-E Power Amplifier with On-Chip Transformer for Q Enhancement

Ping Song(Hong Kong University of Science & Technology), Howard Cam Luong(Hong Kong University of Science & Technology)

Keywords: Power amplifier, on-chip Q enhancement, CMOS 0.18-um

Abstract: A 1-V fully-differential two-stage CMOS Class-E power amplifier operating at 2.4 GHz is presented. An on-chip transformer-feedback topology is applied in the pre-amplifier in order to provide a high swing to drive the second stage. Injection-mode-locking topology is employed in the second stage to achieve high output power and high efficiency. Implemented in a 0.18μm CMOS process, the amplifier delivers an output power of 15.6dBm with 39.5% PAE at a 1-V supply and an output power of 20.3dBm with 43% PAE at a 1.8-V supply, respectively.

Session 6 Emerging Integration and Voltage Conversion Techniques

Nov. 2 10:00-11:40

Session Co-Chairs: *Masahiro Nomura(NEC) and David Chang(ITRI)*

6-1 10:00-10:25

VDD-Hopping Accelerator for On-Chip Power Supplies Achieving Nano-Second Order Transient Time

Kohei Onizuka(University of Tokyo), Takayasu Sakurai(University of Tokyo)

Keywords: Power supply, VDD-hopping

Abstract: A VDD-hopping accelerator for on-chip power supply circuits is proposed and the effectiveness of the accelerator circuit is experimentally verified. The circuit enables nano-second order transient time in on-chip distributed power supply systems. The measured transition time is less than 5ns with load circuit equivalent to 25k logic gates in 0.18-um CMOS. This is to be compared with the case without the accelerator of the order of us and thus the acceleration by two orders of magnitude is achieved. Automatic generation of the timings in a self-aligned manner is also discussed.

6-2 10:25-10:37

95% Leakage-Reduced FPGA using Zigzag Power-gating, Dual-VTH/VDD and Micro-VDD-Hopping

Canh Quang Tran(University of Tokyo), Hiroshi Kawaguchi(University of Tokyo), Takayasu Sakurai(University of Tokyo)

Keywords: FPGA, low power, VDD hopping, Zigzag super cutoff CMOS

Abstract: Low-power FPGA architecture is proposed based on fine-grained VDD control scheme called

micro-VDD-hopping. Four Configurable Logic Blocks (CLB) are grouped into one block where VDD is shared. In the micro-VDD-hopping scheme, VDD of each block is varied between the higher VDD (VDDH) and the lower VDD (VDDL) spatially and temporally to achieve lower power, while keeping performance undegraded. A level shifter that has less contention is proposed. The FPGA also incorporates Zigzag power-gating scheme, special care has been taken to cope with sneak leakage path problem. The proposed FPGA is fabricated using 0.35μm CMOS technology together with the conventional fixed-VDD FPGA. Measurement shows that the dynamic power can be reduced by 86% when the required speed is half of the highest speed. Simulation using 90nm CMOS technology shows that a leakage power reduction of 95% can be achieved, when the proposed method is used. Area overhead of the proposed FPGA is 2%.

6-3 10:38-10:50

A Fast Settling Low Dropout Linear Regulator with Single Miller Compensation Capacitor

Sao-Hung Lu(National Taiwan University), Wei-Jen Hung(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords:

Abstract: A 1.8-V, 150-mA fast settling low dropout linear regulator (LDO) with single Miller compensation capacitor is presented. By utilizing the digital-controlled dynamic bias circuit to track the output current, the proposed LDO provides fast settling time, 4us with 0.5% error, for the output capacitors with low and high equivalent series resistance (ESR). The proposed LDO has been fabricated in a 0.35-um 2P4M CMOS technology, and the active chip area is 480um x 675 um. Furthermore, the line and load regulations are 0.127%/V and 40ppm/mA, respectively. The measured quiescent current is 45uA in 5V supply voltage.

6-4 10:50-11:02

On-Chip High-Voltage Charge Pump Circuit in Standard CMOS Processes with Polysilicon Diodes

Ming-Dou Ker(National Chiao-Tung University), Shih-Lun Chen(National Chiao-Tung University)

Keywords: on-chip, high-voltage, charge pump circuit

Abstract: An on-chip high-voltage charge pump circuit realized with the polysilicon diodes in standard (bulk) CMOS process is presented in this paper. Because the polysilicon diodes are fully isolated from the substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of MOSFETs. The polysilicon diodes can be implemented in the standard CMOS processes without extra process steps. The proposed charge pump circuit has been fabricated in a 0.25-um 2.5-V standard CMOS process. The output voltage of the 12-stage charge pump circuit can be pumped up to 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage (18.9 V) in a 0.25-um 2.5-V standard CMOS process.

6-5 11:03-11:15

A Dual-Phase Digital PWM Controller for DC-DC Switching Converters with Current Balancing

Tysh-Bin Liu(National Taiwan University), Wei-Jen Huang(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: DC-DC converters, PWM, current balancing

Abstract: A dual-phase digital PWM controller is presented for DC-DC switching converters. This controller not only regulates the output voltage of a DC-DC converter, but also provides current balancing for the dual-phase power converter. By using voltage-current reaction current balancing, the system complexity is reduced. The chip has been fabricated in 0.35um CMOS process and the active area is 1.996mm2. It consumed 40mW from a 3.3V supply.

6-6 11:15-11:40

Measurements of Digital Signal Delay Variation Due to Dynamic Power Supply Noise

Mitsuya Fukazawa(Kobe University), Makoto Nagata(Kobe University)

Keywords: Delay, Power supply noise, IR drop

Abstract: On-chip 100-ps/100-uV waveform accurate measurements on signal transition in a large-scale digital circuits clearly demonstrate the correlation of dynamic delay variation with power supply noise waveforms. An approximately linear dependence of delay increase with drop height holds under the existence of static IR drop, however, the coefficient of delay increase is strongly influenced by a dynamic power supply noise waveform. Another cause of delay variation is found as a distortion of signal waveforms during logic transition by dynamic power supply noise, where the process is sensitive not only to a noise waveform but also to a relative time difference among victim and aggressor pairs, which can be generally found in a design with multiple clock domains.

Session 7 Wireline communication Circuits

Nov. 2 12:40-14:20

Session Co-Chairs: *Deog-Kyoon Jeong(Seoul National University) and Tai-Cheng Lee(National Taiwan University)*

7-1 12:40-13:05

A 5Gbps CMOS Automatic Gain Control Amplifier for 10GBase-LX

I-Hsin Wang(National Taiwan University), Wei-Sheng Chen(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: CMOS AGC 10GBase-LX VGA Optical communication

Abstract: A 5Gbps automatic gain control amplifier is presented with 27.8dB input dynamic range for 10GBase-LX4 Ethernet in 0.18um CMOS technology. Five push-pull inverters use self-bias resistors and inductive-series peaking technique to realize a variable gain amplifier (VGA). This VGA achieves 4GHz bandwidth and 20dB linear-in-dB gain tuning range. The proposed 5Gbps AGC amplifier yields constant output amplitude 100mV for an input 27.8dB dynamic range.

7-2 13:05-13:30

A CMOS Gm-C Analog Pre-Equalizer for 1000BASE-T Analog Receive Filters

Jingyu Huang(Marvell semiconductor inc.), Richard Spencer(University of California, Davis)

Keywords: CMOS transconductor, Gm-C filter, analog equalizer, analog receive filter, analog front end, low distortion, 1000BASE-T, Gigabit Ethernet

Abstract: An analog pre-equalizer, which is used in 1000BASE-T analog front ends, is implemented by a Gm-C filter in a 2.5V 0.25um digital CMOS process. A new linearization circuit is used in the

transconductance cells. Measured filter response can be programmed for 10m- to 150m-long cable, the total harmonic distortion is -47.5dB with a 1Vpp input at 13.4MHz, and the input dynamic range is 51dB. The power dissipation is 25mW, and the active area is 0.5mm^2.

7-3 13:30-13:42

A 90 dBΩ, 10 Gbps Optical Receiver in a 0.18 μm CMOS Technology

Wei-Zen Chen(National Chiao-Tung University), Da-Shin Lin(National Chiao-Tung University), Yueh-Hsun Tsai(National Chiao-Tung University)

Keywords:

Abstract: A 90 dBΩ optical receiver analog front-end (AFE), including a transimpedance amplifier, an automatic gain control circuit, and a post amplifier, is fabricated using a 0.18μm CMOS technology. The receiver front-end provides a -3 dB bandwidth of 7.86 GHz and a GBW of 248.5 THzΩ that exceeds the state of the arts. The photo current received by the receiver AFE is amplified to a differential voltage swing of 900 mVpp when driving 50Ω output loads. The sensitivity of the optical receiver is -13 dBm at a bit error rate of 10-12 with a 231-1 PRBS test pattern.

7-4 13:43-13:55

A Wideband CMOS Variable-Gain Low-Noise Amplifier for Cable TV Tuners

Shuzuo Lou(Hong Kong University of Science & Technology), Howard Cam Luong(Hong Kong University of Science & Technology)

Keywords: Cable tuner, low-noise amplifier, noise figure, wideband, shunt feedback

Abstract: A 54 MHz - 880 MHz low-noise variable-gain amplifier (LNA) for use in cable TV tuners is designed in a 0.18μm CMOS process. An active shunt feedback is used to achieve wideband input matching without degrading the noise figure. Inductive shunt-peaking is employed at the output to extend bandwidth. The LNA gain can be tuned from 10 dB to 22 dB. The amplifier measures a NF of 2.8dB in the high-gain setting, IIP3 of 5.0dBm at low-gain setting and draws a current of 23mA from a 1.8-V supply.

7-5 13:55-14:07

Noise Reduction in LNAs Using a Conductive Path to Ground Technique in SiGe Technology

Javier Alvarado Jr(Cornell University), Jon Duster(Cornell University), Kevin Kornegay(Cornell University)

Keywords:

Abstract: A passive noise suppression technique was implemented on a family of monolithic low-noise amplifiers. This method provides the entire circuit with a conductive ground path to the P- substrate. Near active device regions, noise injection and crosstalk paths are shunted to ground. This technique decreased the LNAs noise figures by 1.88dB, 0.34dB, and 0.82dB at 5.25GHz, 2.45GHz, and 2.14GHz respectively. While power consumption decreased, gain improved by 5.3dB and 2.5dB at 5.25GHz and 2.14GHz respectively.

7-6 14:08-14:20

4/2 PAM Pre-emphasis Transmitter with Combined Driver and Mux

Chih-Hsien Lin(National Central University), Shyh-Jye Jou(National Chiao Tung University)

Keywords: Transmitter, pre-emphasis, Mux

Abstract: A new multi-Gbps pre-emphasis design methodology and circuits for a 4/2 PAM transmitter over cable are proposed. Theoretical analysis of the total frequency response of pre-emphasis, package, cable and termination are carried out. Then, we propose a pre-emphasis design method so that the over all frequency response in the receiver side is uniform within the desired frequency range. A test chip of transmitter with pre-emphasis, PLL circuit and on-chip termination resistors are implemented to verify the design methodology. The measurement results of 10/5 Gbps (4/2 PAM) are carried out over 5 meter (m) long cable and is in agreement with our analysis and simulation results.

Session 8 Frequency Synthesizers

Nov. 2 12:40-14:20

Session Co-Chairs: *Ting-ping Liu(Winbond Electronics) and Huei Wang(National Taiwan University)*

8-1 12:40-13:05

A Wideband 0.18-um CMOS Delta Sigma Fractional-N Frequency Synthesizer with a single VCO for DVB-T

Eun-Yung Sung(Samsung Electronics), Kun-Seok Lee(Samsung Electronics), Dong-Hyun Baek(Samsung Electronics), Young-Jin Kim(Samsung Electronics), Byeong-Ha Park(Samsung Electronics)

Keywords: frequency synthesizer, PLL, AFC, VCO, DVB-T, wideband, charge pump

Abstract: This paper describes the design of the ÄÓ fractional-N frequency synthesizer for digital video broadcasting – terrestrial (DVB-T) receiver, which is fabricated in a 0.18-um CMOS technology. A 3-bit 4th order sigma-delta (ΔΣ) modulator is employed for the fractional value implementation. A single on-chip voltage-controlled oscillator (VCO) covers a wideband frequency range– 900MHz to 1730MHz (63.1%) and provides the local oscillator (LO) signal - 470MHz to 862MHz via divider-2. The frequency synthesizer supports the whole channels and keeps the loop stable in operating and the performance variation is minimized over the wide frequency band. The variation of channel-to-channel switching time is also reduced. The measurement results show in-band phase noise is less than -80 dBc/Hz and out-of-band phase noise at 1.25 MHz offset is less than –128 dBc/Hz over all frequency range. The total lock time is less than 300 us. The implemented frequency synthesizer consumes 10mA from 2.8-V power-supply.

8-2 13:05-13:30

A Fast-Switching Frequency Synthesizer for UWB Applications

Che-Fu Liang(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: synthesizer, ultra-wide band, fast-switching

Abstract: A fast-switching frequency synthesizer is presented for ultra-wideband MB-OFDM applications. This synthesizer generates three frequency tones with 528MHz spacing. By using single-sideband mixers with Q-enhancement bandpass filters and switched-cascode multiplexers, the sideband rejection is less than -30dB at least and the frequency switching time is less than 7ns. The chip

has been fabricated in 0.18um CMOS process and the area is 1.32mm^2. It consumed 70mW from a 1.8V supply.

8-3 13:30-13:42

A Multimode GSM/DCS/WCDMA Double Loop Frequency Synthesizer

Franck Badets(STMicroelectronics), Sebastien Rieubon(STMicroelectronics), Laurent Camino(STMicroelectronics), Thierry Divel(STMicroelectronics), Sebastien Dedieu(STMicroelectronics), Patrick Cerisier(STMicroelectronics), Didier Belot(STMicroelectronics)

Keywords:

Abstract: In this paper a multimode frequency synthesizer designed in a STMicroelectronics RF 0.25 um BiCMOS technology for a multimode WCDMA/GSM/DCS/PCS monochip transceiver is described. It consists in a double integer loop with a programmable direct divider in order to provide fractional steps. Measured phase noise complies with all mode specifications. Measured phase noise at 400 kHz of the 3.8 Ghz carrier is -118 dBc/Hz. Power consumption is about 21 mA from a 2.5 V battery.

8-4 13:43-13:55

A 40-GHz Distributed-Load Static Frequency Divider

Tai-Cheng Lee(National Taiwan University), Hua-Chin Lee(National Taiwan University), Keng-Jan Hsiao(National Taiwan University), Yen-Chuan Huang(National Taiwan University), Guan-Jun Chen(National Taiwan University)

Keywords:

Abstract: A distributed-load static frequency divider is designed in a 0.13μm CMOS technology for wideband operation. The technique of a distributed load utilized in a current-mode logic (CML) circuit improves operating frequency by about 30% based on simulation results. Driven by a differential signal, the divider operates from 16 to 40 GHz while consuming 10 mW from a 2-V power supply.

8-5 13:55-14:07

Ultra-Low-Voltage CMOS Static Frequency Divider

Jun-Chau Chien(National Taiwan University), Liang-Hung Lu(National Taiwan University)

Keywords: ultra-low-voltage, frequency divider

Abstract: This paper presents an ultra-low-voltage static frequency divider fabricated in a standard 0.18 μm CMOS technology. Employing forward body-biasing (FBB) technique and parallel current switching topology, the 2:1 frequency divider operates up to 4.5 GHz while consuming 2.7 mW from a supply voltage of 0.6 V. When operating at a supply voltage of 0.7 V, a maximum operating frequency of 6.6 GHz is achieved at the cost of higher power dissipation.

8-6 14:08-14:20

A 10-GHz CMOS PLL with an Agile VCO Calibration

Yu-Jen Lai(National Taiwan University), Tsung-Hsien Lin(National Taiwan University)

Keywords:

Abstract: This paper reports a fully-integrated 10-GHz CMOS PLL with an agile VCO frequency

calibration circuit. The proposed method automatically searches for the optimum VCO tuning curve out of a band of curves using much less time than other existing approaches. The agility is due to the novel searching technique which is based on the comparison of signal periods, rather than counting signal cycles or reading the VCO control voltage after the PLL settled. The proposed PLL is implemented in a 0.18-um CMOS process. The measured PLL output phase noise at 10 GHz is -102 dBc/Hz at 1-MHz offset frequency and the reference spurs are below -48 dBc. The PLL consumes 44 mW in the low-current mode. The calibration time is less than 4 usec.

Session 9 Digital Circuits for Communication Systems

Nov. 2 12:40-14:20

Session Co-Chairs: *Chen-yi Lee(National Chiao Tung University) and Myung H. Sunwoo(Ajou University)*

9-1 12:40-13:05

A Low Power Digital IC Design Inside the Wireless Endoscopy Capsule

Xiang Xie(Tsinghua University), Guolin Li(Tsinghua University), XinKai Chen(Tsinghua University), Lu Liu(Tsinghua University), Chun Zhang(Tsinghua University), ZhiHua Wang(Tsinghua University)

Keywords: digital IC design, wireless endoscopy, quincunx pattern, image compression, low power, power management.

Abstract: This paper proposes an analog-digital mix-mode low power IC architecture inside the wireless endoscopic capsule, which assures that the capsule can implement the diagnoses of whole human digestive tract and provides real time endoscopic image monitoring. A new low complexity and low power digital IC design inside the wireless endoscopic capsule is discussed in detail. To decrease the power consumption, a novel architecture of three-stage clock management is applied for such a system. A new image compression algorithm based on Bayer image format and its corresponding hardware architecture are both presented for low power and low communication data rate application. The digital circuits were verified on FPGAs and have been implemented in 0.18um CMOS process.

9-2 13:05-13:30

A Triple-Mode MAP/VA IP Design for Advanced Wireless Communication Systems

Chen-Hung Lin(National Taiwan University), Fan-Min Li(National Taiwan University), Xin-Yu Shi(National Taiwan University), An-Yeu Wu(National Taiwan University)

Keywords:

Abstract: In this paper, A Triple-Mode MAP/VA kernel for advanced wireless communication Systems is implemented in a 0.18μm CMOS process. We employ triple-mode MAP/VA timing charts that can run two different algorithms at the same time by complementing each other. In order to conform to the advance communication standard, our kernel can also perform as a reconfigurable trellis decoder. For 3GPP standards, the throughput rate of the proposed kernel achieves 4.17Mbps@6 iterations for turbo decoding and 1.56Mbps for convolutional decoding in concurrent MAP/VA mode, when maximum clock frequency of this kernel is measured at 100 MHz.

9-3 13:30-13:42

A MRMDF FFT Processor for MIMO OFDM Applicatons

Yu-Wei Lin(National Chiao Tung University), Wan-Chun Liao(National Chiao Tung University), Chen-Yi Lee(National Chiao Tung University)

Keywords: FFT, MIMO OFDM

Abstract: In this paper, the proposed pipelined FFT processor, which is based on MRMDF structure, can deal with the simultaneous multiple input sequences more efficiently for MIMO OFDM applications. Furthermore, the hardware costs of memory and complex multipliers in our method can be saved by means of delay feedback and data scheduling approaches. The higher-radix FFT algorithm is also realized in our processor to reduce the number of complex multiplications. A test chip for 802.11n system has been designed using 0.13 um 1P8M CMOS process with core area of 2142x660 um2. Power dissipation is 5.2mW when 128 points FFT with four data streams are calculated.

9-4 13:43-13:55

A Universal Architecture for RS Error and Erasure Decoder

Fuke Chang(National Chiao Tung University), Chienching Lin(National Chiao Tung University), Hsie-Chia Chang(National Chiao Tung University), Chen-Yi Lee(National Chiao Tung University)

Keywords: Universal, Reed Solomon, Erasure, Berlekamp Massey algorithm

Abstract: This paper presents a universal architecture for Reed Solomon (RS) error-and-erasure decoder that can accommodate any codeword with different code parameters and finite field definitions. In comparison with other reconfigurable RS decoders, the proposed design, based on the Montgomery multiplication algorithm, can support various finite field degrees, different primitive polynomials, and erasure decoding functions. In addition, the decoder features an on-the-fly finite field inversion table for high speed error evaluation. The area efficient design approach is also presented.

9-5 13:55-14:07

Energy-Efficient Optimization of the Viterbi ACS Unit Architecture

Hoang Dao(University of California, Davis), Bart Zeydel(University of California, Davis), Vojin Oklobdzija(University of California, Davis)

Keywords: energy efficiency, architecture, pipelining, parallelism, ASC, Viterbi

Abstract: Different architectural approaches for saving energy are considered for the ACS unit of a Viterbi decoder. It was found that although providing less throughput improvement than parallelism, pipelining is more energy efficient. The optimal mix of these two architectures favors more pipelining at lower throughput requirements.

9-6 14:08-14:20

A 1.1Gb/s 4092-bit Low-Density Parity-Check Decoder

Engling Yeo(STMicroelectronics), Borivoje Nikolic(University of California, Berkeley)

Keywords: DSP, Forward-error correction, Decoders

Abstract: A 4092-bit low-density parity-check decoder, based on staggered decoding schedule, is implemented in a 0.13µm 6M CMOS technology. The rate 0.75 code is constructed based on finite-field geometries. Serial, shift-register based architecture enables a compact decoder implementation. The

8.6mm2 chip operates at 1.1 GHz at 1.2V resulting in a throughput of 1.1Gb/s per iteration.

Session 10 Wireless Communication Circuits

Nov. 2 14:55-17:00

Session Co-Chairs: *Dennis C.W. Lo(Ralink Technology) and Mototsugu Hamada(Toshiba)*

10-1 14:55-15:20

A Wireless-Interface SoC Powered by Energy Harvesting for Short-range Data Communication

Shinji Mikami(Kanazawa University), Tetsuro Matsuno(Kanazawa University), Masayuki Miyama(Kanazawa University), Masahiko Yoshimoto(Kobe University), Hiroaki Ono(Linear Circuit Corp.)

Keywords: RF, Wireless, Enregy Harvesting, Battery-less, SoC, Low Power, Low Voltage

Abstract: This paper describes the design and estimation of a wireless-interface SoC for wireless battery-less mouse with short-range data communication capability. It comprises an RF transmitter and microcontroller. An SoC, which is powered by an electric generator that exploits gyration energy by dragging the mouse, was fabricated using the TSMC 0.18-um CMOS process. Features of the SoC are the adoption of a simple FSK modulation scheme, a single-end configuration on the RF transmitter, and the specific microcontroller design for mouse operation. We verified that the total power consumption in the SoC is 2.2 mW. This is sufficiently low for energy harvesting.

10-2 15:20-15:45

A 4.0-mW 2-Mbps Programmable BFSK Transmitter For Capsule Endoscope Applications

Meng-Wei Shen(National Tsing Hua University), Chi-Ying Lee(National Tsing Hua University), Jenn-Chyou Bor(National Tsing Hua University)

Keywords: BFSK, Transmitter,

Abstract: A low power BFSK transmitter has been proposed. The transmitter IC includes a LDO regulator, a crystal oscillator, a class-E power amplifier and a dual-loop frequency synthesizer. The parameters of the transmitter, including carrier frequency, and etc., can be set by a serial 3-wire interface. This IC is implemented in 0.35μm CMOS process, occupies 3.47 mm2 and can be fabricated in a fully digital process. For supply voltage 1.85 V, and the transmitter center frequency set to 416 MHz, a maximum data rate of 2 Mbps can be achieved with -24 dBm output power and only 4.0mW power consumption.

10-3 15:45-16:10

A Fully-Integrated Direct Conversion Receiver for CDMA and GPS applications

Kyoohyun Lim(Future Communication IC, Inc.), Sanghoon Lee(Future Communication IC, Inc.), Sunki Min(Future Communication IC, Inc.), Sungmin Ock(Future Communication IC, Inc.), Myung-Woon Hwang(Future Communication IC, Inc.), Changhee Lee(Future Communication IC, Inc.), Kyung-Lok Kim(Future Communication IC, Inc.), Sangwoo Han(Future Communication IC, Inc.)

Keywords: Direct Conversion, Receiver, CDMA, GPS, BiCMOS, LNA, Mixer, Channel selection filter,

VCO

Abstract: This paper describes a fully integrated zero-IF receiver for cellular CDMA and GPS applications. The single chip zero-IF receiver integrates the entire signal path for CDMA and GPS bands. The cellular-band LNA achieved a NF of 1.2dB, IIP3 of 11dBm, and a gain of 15.5dB. Cellular I/Q down-converter and baseband had a NF of 9dB, IIP3 of 9dBm, and IIP2 of 60dBm. The measured LO-to-RF is less than -110dBm at LNA input. Measured phase noise of cellular VCO was -134dBc/Hz at 900kHz offset at 1.76GHz. The receiver was fabricated in a 0.35um SiGe BiCMOS process.

10-4 16:10-16:22

A Single-Chip Direct-Sequence Spread-Spectrum CMOS Transceiver for High Performance, Low Cost 2.4-Ghz Cordless Applications

Ying-Hsi Lin(Realtek Semiconductor Corp.), Ren-Chieh Liu(Msquare Technologies Corp.), Ka-Un Chan(Realtek Semiconductor Corp.), Chia-Jun Chang(Realtek Semiconductor Corp.), Tsung-Ming Chen(Realtek Semiconductor Corp.), Ying-Yao Lin(Realtek Semiconductor Corp.), Han-Chang Kang(Realtek Semiconductor Corp.), Ning-You Yan(Msquare Technologies Corp.)

Keywords: RF transceiver, cordless phone

Abstract: A fully-integrated direct-sequence spread-spectrum (DSSS) CMOS transceiver for 2.4-GHz ISM band is presented. It integrates a RF transceiver, a frequency synthesizer, baseband filters, digital signal processing, an Adaptive differential pulse-code modulation (ADPCM) codec, and a programmable PA pre-driver. The transceiver chip achieves a measured sensitivity of -103 dBm and an output power of 3 dBm. The total chip area is 3.4 x 3.3 mm^2 in a standard RF 0.18-um CMOS technology.

10-5 16:23-16:35

A Complete Dual-band Chip-set with USB 2.0 Interface for IEEE 802.11 a/b/g WLAN applications

Keng Leong Fong(Ralink Technology), David Tung(Ralink Technology), Max Lee(Ralink Technology), Sheng Lee(Ralink Technology), Bart Wu(Ralink Technology), Paul Cheng(Ralink Technology), Tom Pare(Ralink Technology), Julia Feng(Ralink Technology), Julian Chang(Ralink Technology), Eli Simpson(Ralink Technology)

Keywords: wireless, wireless LAN, RF, radio transceiver, baseband processor, media access controller

Abstract: A dual-band (2.5 GHz and 5.5 GHz) wireless-LAN chip-set, consists of a RF IC and a BBP/MAC IC with integrated USB 2.0 interface, is presented. Together with external power amplifiers, this chip-set provides the complete solution and meets the IEEE 802.11a/b/g standard specifications. Without using external SAW filters, the system achieves receive sensitivity (54Mbps) of -70 dBm at antenna port, and transmit OFDM error-vector-magnitude better than -28 dB. The active die area of the RF IC and the BBP/MAC IC is 5.4 mm^2 and 17 mm^2 respectively. The complete solution uses few external components and occupies active board area of less than 1100 mm^2.

10-6 16:35-17:00

A Single-Chip Dual-Band 0.25um CMOS Transceiver for 802.11a/b/g Wireless LAN

Ming-Ching Kuo(Industrial Technology Research Institute), Yi-Bin Lee(Industrial Technology Research Institute), Shiau-Wen Kao(Industrial Technology Research Institute), Chih-Hung Chen(Industrial Technology Research Institute), Chun-Lin Ko(Industrial Technology Research Institute), Tzu-Yi Yang(Industrial Technology Research Institute)

Keywords: WLAN, 802.11a/b/g, transceiver
Abstract: This paper presents a dual-band, 5.15GHz-5.35GHz, 2.4GHz-2.5GHz, transceiver for IEEE 802.11a/b/g standards in a 0.25μm CMOS process. With a novel architecture and frequency planning, only one voltage-controlled oscillator and frequency synthesizer is required to perform frequency transferring for dual-band operation, and the building blocks of both receiver and transmitter could be shared as many as possible. The fully integrated VCO and frequency synthesizer centered at 3.8GHz achieves an integrated phase noise of 1.35° rms. The transmitter achieves -33dB EVM at -3dBm output power, and -29dB EVM at -7dBm output power from the integrated preamplifier for 2.4GHz and 5GHz bands respectively. The receiver also exhibits a noise figure of 3dB at 2.4GHz band and 3.8dB at 5GHz band. The transceiver occupies an area of 25mm².

Session 11 VCOs and PLLs

Nov. 2 14:55-17:00

Session Co-Chairs: *Shen-Iuan Liu(National Taiwan University) and Seung-Jun Lee(EWHA Womans University)*

11-1 14:55-15:20

A 1.3-2.8GHz Wide Range CMOS LC-VCO Using Variable Inductor

Yusaku Ito(Tokyo Institute of Technology), Yoshiaki Yoshihara(Tokyo Institute of Technology), Hirotaka Sugawara(Tokyo Institute of Technology), Kenichi Okada(Tokyo Institute of Technology), Kazuya Masu(Tokyo Institute of Technology)

Keywords: VCO, Variable inductor, Switched capacitor
Abstract: This paper proposes a novel wide-range tunable CMOS voltage controlled oscillator (VCO). VCO uses an on-chip variable inductor and switched capacitors as variable elements. The VCO was fabricated using a standard 0.18um CMOS process with five metal layers. The oscillation frequency can be tuned from 1.28GHz to 2.75GHz with tuning range of 72%. The proposed VCO operates with low phase noise, and it achieves high FOMt -205.9dBc/Hz.

11-2 15:20-15:45

Low-phase noise LC-tank Quadrature Voltage Controlled Oscillator

Chan-Young Jeong(Hanyang University), Mi-Young Lee(Hanyang University), Changsik Yoo(Hanyang University)

Keywords: QVCO, phase noise
Abstract: A low phase noise LC-tank quadrature voltage controlled oscillator (QVCO) is described. Two differential pairs (one for negative gm generation and the other one for the coupling input) of each resonator have separate bias current sources which are switched on and off by the coupling input of each resonator. The measured results of 5GHz quadrature VCOs implemented in a 0.13um CMOS process shows the proposed biasing scheme can improve the phase noise by 17dB from the conventional QVCO with constant tail current sources while the two QVCOs consume the same power (4.4mA from a 1.2V supply). The smaller 1/f noise of the switched current source improves the phase noise by 7dB. The additional 10dB improvement of the phase noise is obtained by employing the coupling input as the switching signal and separating the tail current sources for the two differential pairs of each resonator.

11-3 15:45-15:57

A 1V Dual-Band VCO Using an Integrated Variable Inductor

Lincoln Lai Kan Leung(Hong Kong University of Science & Technology), Kay W.C. Chui(Hong Kong University of Science & Technology), Howard Cam Luong(Hong Kong University of Science & Technology)

Keywords: Oscillator, VCO, wide-band

Abstract: An integrated variable inductor is proposed. Employing such a variable inductor in a 0.18um CMOS process at a 1-V supply, a VCO is demonstrated to oscillate in 2 distinct frequency bands from 2.2 GHz to 3.6 GHz and from 10.7 GHz to 11.3 GHz. The VCO measures phase noise of around -135.5 dBc/Hz for the lower band and -126.5dBc/Hz for the upper band at 10-MHz offset while consuming 5mW and occupying an area of 0.4x0.8mm^2.

11-4 15:58-16:10

A CMOS VCO with Optimized Tune Branches for Zero-IF CDMA Cellular Application in a 0.5um BiCMOS process

Jinhyuck Yu(Samsung Electronics), Sung-Gi Yang(Samsung Electronics), Sangsoo Ko(Samsung Electronics), Woonyun Kim(Samsung Electronics), Wooseung Choo(Samsung Electronics), Byeong-Ha Park(Samsung Electronics)

Keywords: Voltage controlled oscillator (VCO), CMOS, SiGe BiCMOS, accumulation-mode MOS (AMOS) varactors, phase noise, single-tone test, CDMA, cellular.

Abstract: A fully integrated, very-low phase-noise CMOS voltage controlled oscillator (VCO) has been implemented for zero-IF CDMA cellular receiver(Rx) using CMOS transistors in a 0.5μm SiGe BiCMOS process technology. To optimize the phase noise performance, the VCO used the proposed coarse and fine tune branch which employed high-Q accumulation-mode MOS(AMOS) varactors. The measured phase noise is below -133dBc/Hz at 900kHz offset frequency from a 1.762GHz carrier, which yields enough margin for the IS-98 single-tone test requirement. The integrated CDMA cellular Rx including this Rx VCO shows more than 2.5dB single-tone performance margin.

11-5 16:10-16:22

A Low-Phase-Noise Low-Phase-Error 2.4GHz CMOS Quadrature VCO

Jung-Yu Chang(National Taiwan University), Chia-Hsin Wu(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: quadrature voltage controlled oscillator (QVCO),phase noise

Abstract: A 2.4GHz low-phase-noise and low-phase-error LC tank quadrature voltage controlled oscillator (QVCO) using the parasitic vertical BJT coupling and RC phase shifters is presented. Based on the proposed techniques, the proposed QVCO can simultaneously have low phase noise and low phase error. This QVCO circuit has been realized in a 0.18μm triple-well CMOS process and exhibits below 0.2^o phase error with phase noise of -105dBc/Hz at 100kHz offset frequency . The tuning range is 380MHz from 2.27GHz to 2.65GHz with control voltage from 0.3V to 1.8V. It consumes 5.4mW at each tank. .

11-6 16:23-16:35

A Wide Lock-in Range PLL using Self-Calibrating Technique for Processors

Jingo Nakanishi(Renesas Technology Corp.), Hiromi Notani(Renesas Technology Corp.), Hiroshi Makino(Renesas Technology Corp.), Hirofumi Shinohara(Renesas Technology Corp.)

Keywords: PLL Lock-in Range Self-Calibrating

Abstract: We proposed a PLL using a self-calibrating technique. By estimating the margin for self-calibrating operation, the minimum number of digital calibration steps was determined. A PLL with a low test cost, a wide lock-in range and low jitter was designed and implemented using a 0.15μm 1.5 V CMOS process. The measured PLL lock-in range is 80 MHz - 630 MHz with four digital calibration steps.

11-7 16:35-16:47

All-Digital PLL with Ultra Fast Acquisition

Robert Bogdan Staszewski(Texas Instruments), Gabi Shriki(Texas Instruments), Poras Balsara(University of Texas, Dallas)

Keywords: RF, Bluetooth, PLL, all-digital, acquisition, deep-submicron CMOS

Abstract: A fully-digital frequency synthesizer for RF wireless applications has recently been proposed. When implemented in digital deep-submicron CMOS, the proposed architecture is more advantageous over conventional charge-pump-based PLL's since it exploits signal processing capabilities of digital circuits and avoids relying on the fine voltage resolution of analog circuits. In this paper, we present novel techniques used in the all-digital PLL to achieve an ultra fast frequency acquisition of

11-8 16:48-17:00

A Calibrated Pulse Generator for Impulse-Radio UWB Applications

Che-Fu Liang(National Taiwan University), Shih-Tsai Liu(National Taiwan University), Hsiang-Hui Chang(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: uwb, pulse generator

Abstract: A 100Mbps DLL-based pulse position modulation generator is presented for impulse-radio ultra-wideband applications. The pulse generator provides a data rate of 100Mbps and a pulse width of 1ns. To achieve an accurate pulse position and pulse width, a mixed-mode calibration circuit is used to calibrate the output buffer of the DLL. The chip is fabricated in a 0.35um CMOS process.

Session 12 High-performance Digital Circuits Design

Nov. 2 14:55-17:00

Session Co-Chairs: *Hideyuki Kabuo(Matushita) and Gin-Kou Ma(ITRI)*

12-1 14:55-15:20

A 1.2Mpixels/s/mW 3-D Rendering Processor For Portable Multimedia Application

Jeong-Ho Woo(Semiconductor System Laboratory), Min-Wuk Lee(KAIST), Hyejung Kim(KAIST), Ju-Ho Sohn(KAIST), Hoi-Jun Yoo(KAIST)

Keywords: Portable 3D Graphics, Low power, Texture Cache, RMW

Abstract: A 1.2Mpixles/s/mW 3-D rendering processor is designed and implemented for portable multimedia application. A sustained 20Mpixels/s pixel fill rate is obtained at 10MHz with the help of

embedded depth buffer and recursive sub- block mapped texture cache. In order to achieve low power rendering operation, SlimShader architecture with non-atomic read-modify-write scheme and logarithmic datapath is employed. The rendering processor consists of 281k logic gates and 164kB embedded SRAM in 25mm^2. It is fabricated in 0.18um 1-poly 6-metal CMOS logic process and real-time 3-D graphics images are successfully demonstrated on the system evaluation board. It consumes 17mW at 10MHz while drawing texture-mapped images.

12-2 15:20-15:45

An 865-μW H.264/AVC Video Decoder for Mobile Applications

Tsu-Ming Liu(National Chiao Tung University), Ting-An Lin(National Chiao Tung University), Sheng-Zen Wang(National Chiao Tung University), Wen-Ping Lee(National Chiao Tung University), Kang-Cheng Hou(National Chiao Tung University), Jiun-Yan Yang(National Chiao Tung University), Chen-Yi Lee(National Chiao Tung University)

Keywords: Video, VLSI

Abstract: A low power H.264/AVC video decoder LSI for mobile applications is presented. Video decoding of quarter-common intermediate format (QCIF) sequence at 30 frames per second is achieved at 1.2MHz clock frequency and requires about 865μW at 1.8-V supply voltage. Moreover, CIF, SD and HD sequence format are also supported. The decoder architecture is based on 4x4 sub-block level pipelining that achieves better buffer allocation and decoding throughput. In addition, several modules are designed with new features to improve overall system throughput (up to 260,000 Macro-Block/sec). The proposed solution integrates 456-k logic gates with 161Kb of embedded SRAM in 0.18μm single-poly six-metal CMOS process with area of 11.3mm^2.

12-3 15:45-15:57

A 231MHz, 2.18mW 32-bit Logarithmic Arithmetic Unit for Fixed-Point 3D Graphics System

Hyejung Kim(KAIST), Byeong-Gyu Nam(KAIST), Ju-Ho Sohn(KAIST), Hoi-Jun Yoo(KAIST)

Keywords: logarithmic, antilogarithmic, arithmetic, 3D graphics

Abstract: A 32-bit fixed-point logarithmic arithmetic unit is designed for mobile 3D graphics system. The proposed logarithmic arithmetic unit performs division, reciprocal, square-root, reciprocal-square-root and square operations in 2-cycle, and powering operation in 5-cycle. It uses programmable precision for accurate 3D pipeline computation and 8-region piecewise linear approximation model for logarithmic and exponential conversion to reduce the operation error under 0.2%. Its test chip is implemented by 1-poly 6-metal 0.18um CMOS technology with 9k gates. It operates at the maximum frequency of 231MHz and consumes 2.18mW.

12-4 15:58-16:10

Footless Dual-Rail Domino Circuit with Self-Timed Precharge Scheme

Kin Hooi Dia(University of Tokyo), Ruotong Zheng(University of Tokyo), Makoto Ikeda(University of Tokyo), Kunihiro Asada(University of Tokyo)

Keywords:

Abstract: This paper presents a new footless dual-rail domino circuit that efficiently combines a footless dynamic circuit technique with a robust self-timed precharge scheme for high performance VLSI design.

Along with these, the proposed circuit achieves a whole footless dual-rail domino circuit with the use of the proposed separator. A 20-stage NAND chain with fan-out 8 is implemented in 0.15μm SOI CMOS technology1 for performance evaluation. Measurement results reveal that the proposed circuit achieves 2.57, 1.72 and 1.12 times speed improvement over the circuit implemented with CPL, the conventional static CMOS and the conventional dynamic DCVSL, respectively.

12-5 16:10-16:35

An On-chip PVT Control System for Worst-caseless Lower Voltage SoC Design

Takayuki Gyohten(Renesas Technology Corp.), Fukashi Morishita(Renesas Technology Corp.), Mako Okamoto(Daioh Electric Corp.), Katsumi Dosaka(Renesas Technology Corp.), Kazutami Arimoto(Renesas Technology Corp.)

Keywords: Regulator, SRAM, operation margin, PVT control

Abstract: In this paper, we propose on-chip PVT (power, voltage, and temperature) control system for worst-caseless lower voltage SoC design that consist of the adaptive voltage management (AVM). The proposed AVM accurately controls to set the most suitable voltage level with table look-up method. This PVT control system realizes wide operating margin, DFM function for low voltage SoC. The experimental chip is fabricated on 90nm CMOS process and confirmed the proposed architecture accurately controls the voltage level and the operation margin securing at the lower voltage.

12-6 16:35-17:00

Mismatch Modeling and Simulation Methodology for Predicting the Output Voltage Variation of an LCD Driver

Kozo Hoshino(Sharp Corporation), Narakazu Shimomura(Sharp Corporation)

Keywords: Mismatch, Statistical Simulation Methodology, LCD Driver

Abstract: This paper presents a new mismatch modeling and simulation methodology for predicting the output voltage variation of an LCD (liquid crystal display) driver. The new model is especially effective for MV (medium voltage) MOSFETs. The new model takes into account the effect of source/drain drift resistance on the mismatch properties of the threshold voltage and the current gain. As a result, the model shows high precision over a wide range of transistor sizes and bias conditions. Circuit level SPICE simulation results show a better prediction for the output voltage variation than previous approaches.

Session P1 Poster I

Nov. 1 10:35-17:50

Session Chair: *Jerry Jou(National Chiao Tung University)*

P1-1 10:35-17:50

A 5.25 GHz Even Harmonic Mixer for Low Voltage Direct Conversion Receivers

Ming-Feng Huang(National Chung-Cheng University), Shuenn-Yuh Lee(National Chung Cheng University), Chung J. Kuo(National Chung-Cheng University)

Keywords: Low Power, Even Harmonic Mixer, Current Reuse, Folded-cascode

Abstract: This paper proposes a 5.25 GHz folded-cascode even harmonic mixer (FEHM) for low voltage applications. This FEHM adopts the folded technique to reduce the headroom voltage, employs current

reuse circuit to improve linearity, and uses double frequency technique to overcome the DC offset problem for direct conversion receivers. At an IF frequency of 500 kHz, the measurement reveals that the proposed FEHM possesses conversion gain of 8.89 dB, IIP3 of -11.555 dBm, and IIP2 of 17.32 dBm under supply voltage of 0.9 V with power consumption about 6.57 mW.

P1-2 10:35-17:50

A Wide-band Low Noise Quadrature CMOS VCO

Yi-Hsien Cho(National Taiwan University), Ming-Da Tsi(National Taiwan University), Ying-Tang Chang(Sunplus Tech. Corp.), Huei Wang(National Taiwan University)

Keywords: Quadrature VCO, phase noise

Abstract: A wide tuning range and low noise CMOS quadrature voltage-controlled oscillator (QVCO) using 0.18μm 1P6M standard CMOS process is proposed in this paper. The VCO is realized employing switchable capacitors, so as to work in dual band and increase operation frequency. Moreover, the dual band operation could decrease the tuning sensitivity in each band and hence lower the phase noise. The VCO operates from 5.14 to 6.3 GHz with more than 20% tuning range. The measured phase noise at 1-MHz offset is -120.2 dBc/Hz at 5.5 GHz with VCO cores drawing total current of 8 mA at 1.8 V supply and the output power is about 1.5 dBm.

P1-3 10:35-17:50

A Personal-Use Single-Chip Emulator Using Dynamically Reconfigurable Logic Array

Koji Kotani(Tohoku University), Soichiro Kita(Tohoku University), Naoto Miyamoto(Tohoku University), Takeshi Ohkawa(Tohoku University), Amir Jamak(Tohoku University), Tadahiro Ohmi(Tohoku University)

Keywords: reconfigurable logic, hardware emulator, temporal partitioning

Abstract: A personal-use single-chip emulation system using a dynamically reconfigurable logic array named Flexible Processor II (FP2) has been developed. It can emulate large target circuit by sequential execution of sub-circuits divided from the target circuit. The size of the target circuit for emulation is theoretically unlimited. In order to realize such features, FP2 is equipped with Temporal Communication Module (TCM) and Flexible Logic Element (FLE), which are essential for handling temporal data communication between divided sub-circuits and for reducing the amount of configuration data, respectively. A place-and-route tool for FP2 named PELOC, which takes care of sequential execution of divided sub-circuits and carries out the temporal partitioning, spatial partitioning, placement, routing and configuration data generation has also been developed. We have developed a single-chip emulation system on a printed circuit board and confirmed that its emulation speed is several hundred times faster than that of verilog simulator and in some cases also faster than a conventional emulator using lots of parallel-connected FPGAs.

P1-4 10:35-17:50

Segment Weighted Random BIST (SWR-BIST): A Low Power BIST Technique

Chun-Yi Lee(National Taiwan University), Chien-Mo Li(National Taiwan University)

Keywords: Low Power Testing, BIST

Abstract: This paper presents a segment weighted random built-in self test (SWR-BIST) technique for

low power testing. This technique divides the scan chain into segments of different weights. Heavily weighted segments have more biased probability than lightly weighted segments. Heavily weighted segments are placed closer to the end of scan chain than the lightly weighted segments so the scan-in transitions are minimized. In addition, scan cells in segments of the same weight are reordered to further reduce the scan-out transitions. Experiments on ISCAS circuits show that, compared with the pseudo random BIST, SWR-BIST effectively reduces the test power by 74%. The SWR-BIST circuitry is very small and it grows slowly with the CUT size. The penalty of this technique is area and routing overhead for scan chain reordering.

P1-5 10:35-17:50

A Single-Chip Low-Power Tunable CMOS Low-IF Single-Conversion ISM Receiver

Chia-Pei Chen(National Chiao-Tung University), Simon C. Li(National Yunlin University of Science and Technology), Hong-Sing Kao(National Chiao-Tung University), Chung-Chih Su(AlfaPlus Semiconductor Inc.), Kuei-Ann Wen(National Chiao-Tung University)

Keywords: single-chip, RF receiver, FM/FSK demodulator, IF section

Abstract: A single-chip tunable CMOS low-IF single-conversion receiver operated in the 915-MHz ISM band is proposed. A new 10.7-MHz IF section including a limiting amplifier and FM/FSK demodulator is employed. Near IF section sensitivity of -72 dBm, the demodulation constant of FM/FSK demodulator is 15 mV/kHz and the dynamic range of the limiting amplifier reaches 80dB. With on-chip tunable components in low power LNA and LC-tank VCO circuit, the receiver measures a RF gain of 15dB at 915-MHz, sensitivity of -80dBm at 0.1% BER, IIP3 of -9dBm, and NF of 5dB with current consumption of 33mA and a chip area of 6 mm^2.

P1-6 10:35-17:50

Design Exploration of a Spurious Power Suppression Technique (SPST) and Its Applications

Kuanhung Chen(National Chung-Cheng University), Kuochuan Chao(National Chung Cheng University), Jiunin Guo(National Chung Cheng University), Jinn-Shyan Wang(National Chung Cheng University), Yuansun Chu(National Chung Cheng University)

Keywords: H.264, power optimization, transform coding

Abstract: This paper presents the design exploration and application of a technique to suppress the spurious power dissipation existed in the data-paths for multimedia VLSI designs. The proposed technique adopts the design concept of separating the arithmetic units into Most Significant Part (MSP) and Least Significant Part (LSP), and then freezing the MSP whenever this part of circuits does no affect the computation result. This paper first explores three implementation approaches of realizing the SPST-based design concept to decide the most efficient one, and then uses this approach to reduce the spurious power of the multi-transform coding design in H.264 systems. The post-layout simulations show that the proposed SPST can save average 27.38% of power dissipation of the multi-transform design.

P1-7 10:35-17:50

A 0.9mW 0.01-1.4GHz Wideband CMOS Low Noise Amplifier for Low-Band Ultra Wideband Applications

Tsung-Te Liu(National Taiwan University), Chorng-Kuang Wang(National Taiwan University)

Keywords:
Abstract: This paper presents a low-power wideband CMOS LNA for low-band UWB application. An NMOS common-gate shunted by a PMOS common-source input stage achieves a wideband impedance matching -7dB from 10MHz to 1.4GHz. RF cascaded by an NMOS common-source output stage sharing the identical input stage bias current 500μA, the 0.18μm LNA provides a gain 22dB and is insensitive to process variations. The LNA consumes 0.9mW from a 1.8-V supply and occupies an area of 0.03mm^2.

P1-8 10:35-17:50

A 900 MHz CMOS RF Direct Conversion Receiver Front-end with 3-dB NF and 30-KHz 1/f Noise Corner

Sang-Gug Lee(Information and Communications University), Dong-Kyun Kang(MobilePro. Corporation), Trung-Kien Nguyen(Information and Communications University)

Keywords: 1/f Noise, CMOS, Direct Conversion, Noise Optimization, IEEE 802.15.4 ZigBee
Abstract: A low-power, low 1/f noise RF receiver front-end for 900 MHz IEEE 802.15.4 ZigBee standard in 0.18 um CMOS technology is implemented. In combination with LNA, a passive mixer showing excellent 1/f noise is adopted. The measured results show the conversion gain of 30 dB, NF of 3 dB with 1/f noise corner frequency of 30 KHz. Two-tone test measurements indicate -5 dBm IIP3, +45 dBm IIP2. The RF receiver front-end dissipates 2 mA from 1.8 V supply

P1-9 10:35-17:50

Single Polysilicon Gate High-Density Logic Using Independently-Controlled Double-Gate Devices

Meng-Hsueh Chiang(National Ilan University), Keunwoo Kim(IBM Corp.), Ching-Te Chuang(IBM Corp.), Christophe Tretz(IBM Corp.)

Keywords: Double-Gate MOSFET, Single Polysilicon Gate
Abstract: Novel double-gate (DG) CMOS logic with a single polysilicon gate process is proposed using independently biased gates. The unique gate-to-gate coupling of DG devices is exploited to improve circuit density, capacitance, performance, and power in 25 nm logic circuits by halving the number of stacked transistors as well as parallel transistors for implementing logic functions. The performance, power, and design trade-offs as well as layouts for logic gates are analyzed via mixed-mode two-dimensional numerical simulations.

P1-10 10:35-17:50

A 900 MHz Low-Voltage Low-Power Variable Gain CMOS Transmitter Front-end

Sang-Gug Lee(Information and Communications University), Won-Seok Oh(Korean Electronics Technology Institute), Trung-Kien Nguyen(Information and Communications University)

Keywords: CMOS, IEEE 802.15.4 ZigBee, Gain Variable, Low-Power,Transmitter
Abstract: This paper presents a low-voltage, low-power, variable gain transmitter front-end for 900 MHz ZigBee applications, in a 0.25 um CMOS technology. The up-mixer achieves a wide range-gain variation by adopting a novel transconductance stage. The measurements show the overall transmitter front-end conversion gain of 16 dB, dB-linear gain variation of over 46 dB with the linearity error less than „b 0.5 dB, output P-1dB of 2 dBm, while dissipating 3 mA from 1.25 V supply.

P1-11 10:35-17:50

A High Efficiency ALL-PMOS Charge Pump for Low-Voltage Operations

Na Yan(Fudan University), Hao Min(Fudan University)

Keywords: Charge pump, standard CMOS process, power efficiency, boosted transistor, number of stage, low voltage

Abstract: This paper presents a high performance ALL-PMOS charge pump suitable for implementation in standard CMOS processes. And only low voltage PMOS transistors are used. With the switching substrate technique and boosted transistor, the influence of body effect is eliminated and output voltage is greatly increased. A twelve-stage charge pump circuit is fabricated in a 0.35-um double-poly CMOS technology. Measurements at 3MHz have shown that for power supply voltages of 2V, 1.5V and 1V an output voltage of 15.5V, 10.4V and 3.6V can be generated respectively.

P1-12 10:35-17:50

A Digitally Controlled Oscillator for Low Jitter All Digital Phase Locked Loops

Kwang-Jin Lee(Korea University), Seung-Hun Jung(Korea University), Yun-Jeong Kim(Korea University), Chul Kim(Korea University), Suki Kim(Korea University), Uk-Rae Cho(Samsung Electronics), Choong-Guen Kwak(Samsung Electronics), Hyun-Geun Byun(Samsung Electronics)

Keywords: DCO, ADPLL, Oscillator

Abstract: This paper presents a Digitally Controlled Oscillator (DCO) for high speed ADPLLs. The proposed DCO circuit has control codes of thermometer type, which can reduce jitters. Performance of the DCO is verified through a novel ADPLL. The ADPLL chip with the DCO was fabricated using SEC 0.18um CMOS technology. The ADPLL has operation range between 520MHz and 1.5GHz and has 76ps peak-to-peak jitter at 668MHz.

Session P2 Poster II

Nov. 2 9:45-17:30

Session Chair: *Makoto Ikeda(University of Tokyo)*

P2-1 9:45-17:30

A Fast Offset-cancellation Single-to-differential Stage for Burst-mode Receiver Design

Chun-Chi Chen(SoC Technology Center)

Keywords: Optical Receiver, Passive Optical Network

Abstract: A fast single-to-differential stage is proposed to convert single-ended signal from a conventional TIA to fully differential output for burst-mode receiver design. The receiver realized with 0.35u SiGe BiCMOS process shows a dynamic range of -28dBm to -5.25dBm and settling time less than 20ns at 1.25Gbps.

P2-2 9:45-17:30

A 0.5 V 3.1 mW Fully Monolithic OOK Receiver for Wireless Local Area Sensor Network

Yu-Tso Lin(National Taiwan University), Tao Wang(National Taiwan University), Shey-Shi Lu(National Taiwan University), Guo-Wei Huang(National Nano Device Laboratories)

Keywords: low voltage, low power, receiver, monolithic, wireless sensor network,
Abstract: A low voltage (0.5 V) low power (3.1 mW) on-off keying (OOK) miniaturized (380 um x 220 um) monolithic receiver implemented in 0.18 um CMOS technology for wireless local area sensor network is demonstrated. This chip can receive small radio signal well with a sensitivity of -50 dBm (-62 dBm) and a maximum data rate of 2 Mbps at 433 MHz (150 MHz). When operated at 0.45 V, this receiver consumes less power (1.36 mW) with the same maximum data rate but a degraded sensitivity (-35 dBm) at 433 MHz.

P2-3 9:45-17:30

Digitally Controlled Phase Locked Loop with Tracking Analog-To-Digital Converter

Sooho Cha(Hanyang University), Chunseok Jeong(Hynix Semiconductor Inc.), Changsik Yoo(Hanyang University), Joongsik Kih(Hynix Semiconductor Inc.)

Keywords: Phase-locked loop
Abstract: A digitally controlled phase-locked loop (DCPLL) is described. The DCPLL has basically the same structure as a conventional analog PLL except for a tracking analog-to-digital converter (ADC). The tracking ADC generates the control signal for voltage controlled oscillator. Since the DCPLL employs neither digitally controlled oscillator nor time-to-digital converter - the key building blocks of digital PLL (DPLL), there is no need for the trade-off between jitter, power consumption and silicon area. The DCPLL was implemented in a 0.18um CMOS process and the active area is 0.35 mm2. While consuming 59mW from a 1.8V supply, the DCPLL shows 16.8 rms jitter.

P2-4 9:45-17:30

A 1.8-V 40-mW Wide-Band CMOS Synthesizer for Cable Tuner Applications

Ming Cheung Lau(Hong Kong University of Science & Technology), Howard Cam Luong(Hong Kong University of Science & Technology)

Keywords: Wide Band Frequency Synthesizer
Abstract: A 1.8-V wide-band CMOS synthesizer for cable tuner applications is designed in a 0.18-um CMOS process. A ring oscillator with switched-capacitor arrays is employed to achieve a wide operating frequency range from 160 MHz to 648 MHz. The measured phase noise is -104.16 dBc/Hz and -110 dBc/Hz at frequency offsets of 10 kHz and 1 MHz respectively. The spur performance is less than -64 dBc at 4-MHz offset. The measured IQ phase mismatch is less than 0.1 degree, and the image rejection measured with on-chip mixers is more than 61dB. The synthesizer dissipates 40mW from a single 1.8-V supply. The core chip area is 2 mm^2.

P2-5 9:45-17:30

Dual-Bias Power Amplifier Designs for WLAN Applications

Chien-Chang Huang(Yuan Ze University), Wei-Ting Chen(Yuan Ze University)

Keywords: Microwave Power Amplifier, InGaP/GaAs HBT, Nonlinear Distortion, WLAN, OFDM
Abstract: This paper presents the power amplifier (PA) design for IEEE 802.11g WLAN applications by using InGaP/GaAs hetrojunction bipolar transistors (HBT) with the dual bias network as the linearizer to improve the output power capability and linearity. The final designed PA utilizes 3.3 V supply

voltage with the measured data on the output power of 25.5 dBm, 22.8 dB in gain, and 42.8% power aided efficiency (PAE) for a 2.4 GHz single-tone stimulus. The measured performances under WLAN modulation signal excitation are 24 dBm output power and 31.5% of PAE with the adjacent-power-ratio (ACPR) less then -20 dBc, satisfying the specifications of the standard.

P2-6 9:45-17:30

A 1.25 to 5Gbps LVDS Transmitter with a Novel Multi-Phase Tree-Type Multiplexer

Chau Chin Su(National Chiao Tung University), Hung Wen Lu(National Central University)

Keywords: LVDS, high speed serial link, mux, serializer, PLL

Abstract: In this paper, we proposed a novel multi-phase multiplexer (MUX). Conventional multi-phase MUX max operate frequency is limited by the self parasitic capacitance at output node. We propose a novel MUX which overcome the disadvantage. The proposed MUX can operate at higher frequency than conventional multi-phase MUX. We use the proposed MUX to implement a 1.25Gbps to 5Gbps LVDS transmitter in 0.18 CMOS technology. The transmitter output data jitter is 61ps at 5Gbps and the total power consumption is about 100 mW.

P2-7 9:45-17:30

Global High-Speed Signaling in Nanometer CMOS

Joshua Jaeyoung Kang(University of Michigan), Jun Young Park(University of Michigan), Michael P Flynn(University of Michigan)

Keywords:

Abstract: A practical transmission line scheme, for long-range (~10 mm) on-chip, digital signaling in a conventional digital CMOS process is presented. Unlike other schemes, there is no requirement for up-conversion, equalization, or special metal processing. The new scheme eliminates the dispersion associated with long lossy lines, allowing very high rates (>40 Gb/s) to be achieved. Eye diagrams, based on line characteristics derived from EM simulation, indicate minimal inter-symbol interference at 40 Gb/s. For a 40 Gb/s link, in 130 nm CMOS, power consumption is shown to be less than a quarter that of a conventional parallel bus with optimally placed repeaters. The performance of a 0.72 cm link implemented in standard digital 180nm CMOS is verified with measurements.

P2-8 9:45-17:30

A Low-Power Dual-Band WLAN CMOS Receiver

Shiau-Wen Kao(Industrial Technology Research Institute), Ming-Ching Kuo(Industrial Technology Research Institute), Chao-Shiun Wang(National Taiwan University), Yi-Bin Lee(Industrial Technology Research Institute), Chih-Hung Chen(Industrial Technology Research Institute), Peng-Un Su(Industrial Technology Research Institute), Tzu-Yi Yang(Industrial Technology Research Institute)

Keywords: WLAN, 802.11a/b/g, receiver

Abstract: A dual-band, dual-conversion receiver integrated from LNA to analog baseband circuitry is presented. The low-pass filters integrate a cutoff frequency auto calibration scheme and can be automatically tuned from 6-MHz to 17-MHz with +/- 3% accuracy. This design is suitable for multi-standard, multi-bandwidth applications, such as 802.11a/b/g and the incoming 802.11n, while the

RF front-end is shared. The chip was fabricated in TSMC 0.25um CMOS process with 2.5V power supply. The noise figure is 2.8dB/3.9-dB for 2.4/5-GHz bands at the maximum gain setting, and the IIP3 of 10/-3-dBm is achieved for 2.4/5-GHz bands at the minimum gain. The receiver provides a programmable gain of 88/78-dB in 2dB steps and consumes 51/54-mA current for 2.4/5-GHz bands, respectively.

P2-9 9:45-17:30

A Low Power High Performance Register-Controlled Digital DLL for 2Gbps x32 GDDR SDRAM

Hyunwoo Lee(Hynix Semiconductor Inc.), Won-Joo Yun(Hynix Semiconductor Inc.), Sin-Deok Kang(Hynix Semiconductor Inc.), Hyung-Wook Moon(Hynix Semiconductor Inc.), Seung-Wook Kwack(Hynix Semiconductor Inc.), Dong-Uk Lee(Hynix Semiconductor Inc.), Ki-Chang Kwean(Hynix Semiconductor Inc.), Kwan-Weon Kim(Hynix Semiconductor Inc.), Young-Jung Choi(Hynix Semiconductor Inc.), Jin-Hong Ahn(Hynix Semiconductor Inc.)

Keywords: DLL Digital Power

Abstract: A new low power high performance RCDLL is presented. The circuit hs fine delay compensation ability,fast delay compensation according to external voltage variation, and inherent dury correction. The digital DLL used for 2Gbps 8Mx32 GDDR3 SDRAM is fabricated using for a 0.10um technplogy. Experimental results show less then +/- 1% duty correction from external duty error of +/- 5%, less than 400 cycle locking time, 1GHz operation frequency at 1.5V, 38mW at 1.5V/1Ghz, and a wide locking range fraom 250Mhz to 1Ghz

P2-10 9:45-17:30

DSP Architecture with Jumping-Floating-Point Number System

Yung Chun Lei(MediaTek Inc.), Chien Hung Lin(MediaTek Inc.)

Keywords: DSP, fixed-point, floating-point

Abstract: We introduce a number system called Jumping-Floating-Point(JFP), which has both the characteristics of the fixed-point and the floating-point number systems. We also introduce a DSP architecture with JFP processing capability. This DSP architecture is feasible and can be applied to traditional fixed-point DSP architecture without too much cost. According to our experiments, the JFP number system has better SNR than the fixed-point number system.

P2-11 9:45-17:30

A Low-phase-noise 1-GHz LC VCO Differentially Tuned by Switched Step Capacitors

Zhangwen Tang(Fudan University), Jie He(Fudan University), Hao Min(Fudan University)

Keywords: LC-VCO,Differentially Tuned Oscillator,Period Calculation Technique,Switched Step Capacitor

Abstract: This paper proposes a novel 1-GHz LC oscillator differentially tuned by switched step capacitors, which is implemented in a 0.25μm 1P5M CMOS process. A period calculation technique (PCT) is adopted to analyze the differential tuning characteristic of switched step capacitors. Due to the symmetric oscillation waveforms, the differentially tuned LC VCO has 7dB phase noise reduction in the 1/f3 region compared to the single-ended tuned topology, and 23.6dB CMRR. It achieves phase noise -83 dBc/Hz, -107 dBc/Hz and -130 dBc/Hz respectively at 10-kHz, 100-kHz and 1-MHz offsets, while dissipating 3.3mA current at 2.6V power supply. Chip size is 0.82mm x 0.84mm.

P2-12 9:45-17:30

Novel Test Structure to emulate Capacitance Variations of a Rate-Grade MEMS Gyroscope

Rajesh Sangati(Texas Instruments(India)), Sowjanya Syamala(National Semiconductor (India)), Navakanta Bhat(Indian Institute of Science,Bangalore)

Keywords: MEMS,Gyroscope,Test Structure,Charge Splitting

Abstract: In this paper a novel test structure, which emulates the capacitance variation of a MEMS gyroscope is presented. The rotational rate of the gyroscope is taken as an electrical signal which is converted into capacitance variations, that can be sensed by the sensor electronics. The continuous angular variations are converted into sampled capacitance changes proportional to the rotational rate. This obviates the need for multi-domain simulations and subsequently the multiple domain testing to validate the design of sensor electronics of the gyroscope. This will help in reducing the time to market and long product development cycles. The test structures are prototyped using 1.5um technology and are validated using a novel charge/discharge technique which measures a minimum capacitance change of 5fF.

P2-13 9:45-17:30

4 Gbps On-Chip Interconnection using Differential Transmission Line

Hiroyuki Ito(Tokyo Institute of Technology), Hideyuki Sugita(Tokyo Institute of Technology), Kenichi Okada(Tokyo Institute of Technology), Kazuya Masu(Tokyo Institute of Technology)

Keywords: Global Interconnect, Signal Integrity, Transmission Line, Delay, Power Consumption

Abstract: This paper demonstrates the differential transmission line interconnect for high-speed global interconnect IP. The interconnect is fabricated using a 180 nm CMOS technology. 4 Gbps signal transmission can be achieved in measurement results. The on-chip transmission line performs faster signal transmission than common RC interconnects.

P2-14 9:45-17:30

Design of a Multi-Context FPGA Using a Floating-Gate-MOS Functional Pass-Gate

Masanori Hariyama(Tohoku University), Sho Ogata(Tohoku University), Michitaka Kameyama(Tohoku University), Yasutoshi Morita(Nippon Precision Circuits Inc.)

Keywords: FPGA, DSP, Fine-Grained Architecture

Abstract: Multi-context FPGAs (MC-FPGAs) have multiple memory bits per configuration bit forming configuration planes for fast switching between contexts. The additional memory planes cause significant overhead in area and power consumption. To overcome the overhead, a fine-grained MC-FPGA architecture using a floating-gate-MOS functional pass gate(FGFP) is presented which merges threshold operation and storage function on a single floating-gate MOS transistor. The transistor count of the proposed multi-context switch(MC-switch) is reduced to 10% in comparison with SRAM-based one. The transistor count of the proposed MC-switch is also reduced to 20% in comparison with the MC-switch that uses floating-gate MOS transistors just as storage device. The test chip is designed using a 0.35um EPROM technology, and the area of the proposed MC-FPGA is reduced to about 50% of that of a conventional MC-FPGA.

P2-15 9:45-17:30

SiGe HBT based 24-GHz LNA and VCO for Short-Range Ultra-Wideband Radar Systems

Toru Masuda(Hitachi, Ltd., Central Research Laboratory), Takahiro Nakamura(Hitachi, Ltd., Central Research Laboratory), Masamichi Tanabe(Renesas Northern Japan Semiconductor), Nobuhiro Shiramizu(Hitachi, Ltd., Central Research Laboratory), Shin-Ichiro Wada(Hitachi, Micro Device Division), Takashi Hashimoto(Hitachi, Micro Device Division), Katsuyoshi Washio(Hitachi, Ltd., Central Research Laboratory)

Keywords: LNA, VCO, SiGe HBT, UWB, Short-range radar

Abstract: 24-GHz low noise amplifier (LNA) and voltage controlled oscillator (VCO) in 0.25μm SiGe BiCMOS technology were developed to create low-cost radio frequency (RF) modules for short-range ultra-wideband radar systems. A two-stage shunt-feedback LNA that used inductive biasing had a -3 dB bandwidth of 11.4 GHz, a noise figure of 3.8 dB at 24 GHz, and a group delay deviation within 21 ps (from 10 GHz to 30 GHz). The LC-tuned differential VCO, with a high quality-factor center-tapped inductor design, oscillated at 24 GHz with phase noise of -100 dBc/Hz at 1 MHz offset. The VCO core consumed only 2 mA of current.

P2-16 9:45-17:30

Audio-Specific Signal Processor (ASSP) for High-Quality Audio Codec

Suk Hyun Yoon(Ajou University), Myung Hoon Sunwoo(Ajou University), Jong Ha Moon(LG Electronics)

Keywords:

Abstract: This paper proposes an audio-specific signal processor for a high-quality audio codec. Filterbank calculation and Huffman decoding require massive computation in MPEG-2/4 AAC decoding. Therefore, the proposed architecture is specially designed for these tasks. The proposed architecture has two optimized units for the IMDCT (Inverse Modified Discrete Cosign Transform) and Huffman decoding. Performance comparisons show significant improvement compared with other commercial DSPs. The proposed ASSP has been synthesized using the Samsung SEC 0.18 um standard cell library. The proposed ASSP core consists of 120,283 gates and runs at 200 MHz.

P2-17 9:45-17:30

A CMOS Vision Sensor with on-the-fly Histogram Equalization Using TFS Encoding and AER Read-Out

Shoushun Chen(Hong Kong University of Science & Technology), Amine Bermak(Hong Kong University of Science & Technology), Dominique Martinez(LORIA-CNRS University)

Keywords: CMOS imager, On-chip Histogram equalization, AER, Time to First Spike vision sensor

Abstract: This paper presents a CMOS vision sensor performing image capture and on-chip histogram equalization. Both image capture and the processing are based on time-to-first spike encoding combined with Address Event Representation (AER) read-out scheme. The proposed approach not only provides a compact and efficient VLSI implementation but also eliminates voltage/current domain analog processing and hence provides immunity to dynamic range reduction caused by low voltage operation in advanced sub-micron technologies. The pixel values are read-out using an asynchronous handshaking type of read-out while the processing is carried out using simple and yet robust digital timer occupying a

very small silicon area 0.1 X 0.6 mm^2 in 0.35um CMOS). Low power operation (10nA per pixel) is achieved since the pixels are only allowed to switch once per frame and only active pixels are allowed to asynchronously access the bus. The prototype was implemented in 0.35um CMOS technology with a silicon area of 3.1 X 3.2 mm^2.

P2-18 9:45-17:30

A 1-V 27mW 10-GHz LC-NOR-Ring QVCO for UWB-OFDM Direct Frequency Synthesizer

Chien-Chih Lin(National Taiwan University), Chorng-Kuang Wang(National Taiwan University)

Keywords: QVCO, DFS

Abstract: This paper proposes an LC-NOR-ring quadrature voltage controlled oscillator(QVCO). Applied to the direct frequency synthesizer used in the frequency-hopped MB-OFDM UWB system, the ring is designed to enhance quadrature phase accuracy. To prevent from the inactive equilitrium state in an even-numbered delay-stage ring, the QVCO comprises four stages of NMOS-NOR gates that stimulate oscillation and equip with low-voltage operation capability. Inductor loads are used in accompany with the varactors to reduce the power consumption. Realized in a 0.18-um 1P6M CMOS process, the circuit draws 27-mA current from a 1-V supply. The core circuit occupies an area of 1.012mm x 0.35mm. The measured oscillation frequency shows the QVCO has the range of 9.7GHz to 10.GHz. The phase noise performance is above -90dBc/Hz from 10-kHz offset in the wideband sense.

P2-19 9:45-17:30

Quadrature Oscillator with Negative-Resistance Compensated Transformer Couple

Baoyong Chi(Tsinghua University), Xiaolei Zhu(Tsinghua University), Ziqiang Wang(Tsinghua University), Zhihua Wang(Tsinghua University)

Keywords: Oscillator, RF, CMOS

Abstract: A quadrature oscillator with the negative-resistance compensated transformer couple is presented. Two identical LC sub-harmonic oscillators are cross-coupled by the transformer to generate the quadrature outputs. The transformer also serves as the tail current source filtering network for the sub-harmonic oscillators to improve the phase noise performance. The loss of the transformer is partially compensated by the cross-coupled PMOS pair to overcome the possible undesired harmonic couple and to further improve the phase noise performance. The phase noise performance of the quadrature oscillator is 7dB better than the sub-harmonic oscillator itself by the simulation. The quadrature oscillator has been implemented in 0.25um CMOS process and the measurements how the proposed oscillator could achieve a phase noise of -130dBc/Hz at 1MHz offset from 1.13GHz carrier while it only draws an 8.0mA current from the 2.5V power supply.

P2-20 9:45-17:30

A 35MS/s and 2V/2.5V Current-mode Sample-and-Hold Circuit with an Input Current Linearization Technique

Yasuhiro Sugimoto(Chuo University), Yuji Gohda(Chuo University), Shigeto Tanaka(Chuo University)

Keywords: Analog Signals, Sample and Hold, Current-mode circuits

Abstract: This paper introduces a high-speed and high-accuracy current-mode sample-and-hold (S/H)

circuit that adopts the new linearization technique to the resistor-based voltage-to-current converted input current. The pseudo differential configuration is used to form the whole S/H circuit in order to cancel the clock feedthrough from the S/H switch.

The circuit is designed and fabricated by using the 0.35um CMOS process. The power supplies are 2 V for the analog part and 2.5 V for the logic part. The 1.34 MHz input signal with a -5 dB of full-scale current was applied to the S/H IC, and the measured distortion was -68 dB. The S/H IC operated with a signal-to-noise ratio (S/N) of 57 dB up to 10 MHz input signal when the clock frequency was 20 MHz, and with a S/N of 50 dB at 17.5 MHz input signal when the clock frequency was 35 MHz.

P2-21 9:45-17:30

A Direct Conversion CMOS Front-End for 2.4 GHz Band of IEEE 802.15.4 Standard

Vladimir Krizhanovskii(Information and Communications University), Trung Kien Nguyen(Information and Communications University), Sang-Gug Lee(Information and Communications University), Jong-Chan Choi(Korea Electronics Technology Institute)

Keywords: passive mixer, direct conversion, 1/f noise

Abstract: Design description and measurement results of 0.18μm CMOS direct conversion receiver front-end intended for use in a transceiver for 2.4 GHz band of 802.15.4 standard are presented. Front-end consists of LNA and two current-mode passive mixers. Single-ended RF drive of double-balanced I/Q mixers was used as a means of power dissipation reduction. The measurement showed the following performance: noise figure 7.3 dB, 1/f-noise corner 70 kHz, power gain 10 dB, input IP3 -8 dBm with DC current dissipation of 3.5 mA while operating from voltage supply of 1.8 V.

P2-22 9:45-17:30

Input Capacitance Modeling of Logic Gates for Accurate Static Timing Analysis

Takeshi Kouno(Kyoto University), Masanori Hashimoto(Osaka University), Hidetoshi Onodera(Kyoto University)

Keywords:

Abstract: This paper discusses how to improve input capacitance modeling of logic gates for accurate STA(static timing analysis). The input capacitance exhibits non-linear behavior and its value varies depending on the driving and loading condition of the gate. For the non-linearity issue, we propose to use an equivalent capacitance value derived by the integration of input current during partial transition. For the second issue, we suggest to consider the minimum apacitance as well as the maximum.

P2-23 9:45-17:30

A 2.5Gbps Burst-Mode Clock and Data Recovery Circuit

Che-Fu Liang(National Taiwan University), Sy-Chyuan Hwu(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: burst-mode, CDR

Abstract: A 2.5Gbps burst-mode CDR circuit is fabricated in 0.18um CMOS process. The data generator for this CDR circuit is presented with reduced hardware and low power dissipation. The tight timing budget of the clock generator is also relaxed. The bit error rate less than 10-12 is achieved for a PRBS of 231-1 with 500ppm frequency deviation. The area of the digital core is 0.36mm^2 and the power of

33mW/port is achieved for a 1.8V supply.

P2-24 9:45-17:30

A CMOS Image Rejection Mixer for DAB/DMB Low-IF Tuner IC Exhibiting 41dB Adjacent Channel Rejection Ratio

Youngho Cho(Integrant technologies, Inc.), Bonkee Kim(Integrant technologies, Inc.), Tae Wook Kim(Integrant technologies, Inc.), Min-Su Jeong(Integrant technologies, Inc.), Jung-Hwan Lee(Integrant technologies, Inc.), Seyeob Kim(Integrant Technologies, Inc.), Bo-Eun Kim(Integrant technologies, Inc.)

Keywords: Mixer, Image Rejection Mixer, Low-IF, DAB, DMB

Abstract: The image rejection mixer for Digital Audio Broadcasting and Digital Multimedia Broadcasting (DAB/DMB) is described. The mixer is implemented in a 0.18¥ìm six-layer metal CMOS process and occupies a 2.25mm^2. To obtain the ultimate level of image rejection without additional tuning, the double quadrature architecture is used and to linearize the RF buffer, differential transconductance linearization technique is used. The fabricated mixer exhibits 65 dB image rejection ratio, 41dB adjacent channel rejection ratio, 100 kHz ~ 1.65MHz image rejection bandwidth, 16dB gain, 35dBmV input-referred third order intercept point (IIP3), and 15mA current consumption from 1.8V supply.

P2-25 9:45-17:30

A 40~900MHz Broadband CMOS Differential LNA with Gain-Control for DTV RF Tuner

D.-R. Huang(National Cheng Kung University), Y.-K. Chu(Himax Technologies), H.-R. Chuang(National Cheng Kung University)

Keywords: 40~900MHz 0.18μm, CMOS, broadband LNA, dual-feedback, DTV tuner.

Abstract: This paper presents a 40~900 MHz broadband CMOS differential LNA with gain control for DTV RF tuner application. The LNA is fabricated in a TSMC 0.18μm CMOS process. The broadband differential LNA uses dual-feedback and shunt-shunt feedback topologies to achieve high and flat broadband response. The LNA is designed with 75Ω/75Ω differential input/output impedance for 75Ω TV system application. The circuit measurement is performed using an FR-4 PCB test fixture. In the frequency range of 40~900MHz, the LNA exhibits a gain of 20.26 +/- 0.41dB, noise figure less than 5dB, and input P1dB between -19.5 ~ -20.3dBm. The gain tuning range is from 20 to -42.8 +/- 4.9dB over 40~900MHz range. The power consumption is 43mW at VDD = 1.8 V.

P2-26 9:45-17:30

A 2.4~6GHz CMOS Broadband High-Gain Differential LNA for UWB and WLAN Receiver

Chung-Ping Chang(National Cheng Kung University), Cheng-Chi Yen(National Cheng Kung University), H.-R. Chuang(National Cheng Kung University)

Keywords: 0.18-um, CMOS, Broadband LNA, Differential, UWB, WLAN

Abstract: A 2.4-6 GHz broadband CMOS differential LNA for WLAN and UWB receiver is presented. The LNA is fabricated with the 0.18 μm 1P6M standard CMOS process. Measurement of the chip is performed on a FR-4 PCB test fixture. In the UWB low-band (3 to 5.15GHz), the broadband LNA exhibit a gain of 17.5-18.2 dB, noise figure of 3.4-5dB, input/output return loss better than 10 dB, and

input P1dB of ?7 dBm, respectively. In the band from 2.4 to 3GHz (covering a 802.11b/g band), the LNA exhibit a gain of 17.5-18dB and noise figure less than 3.5dB. From 5.2 to 6GHz, the noise figure of the LNA becomes higher than 5 dB. The gain also decrease to about 15 dB. The DC supply is 1.8V.

P2-27 9:45-17:30

A Low-Power and Compact Analog CMOS Processing Chip for Portable ECG Recorders

Maryam Shojaei-Baghini(Indian Institute of Technology Bombay), Rakesh K. Lal(IIT Bombay), Dinesh K. Sharma(IIT Bombay)

Keywords: Biopotential Signals, Analog Signals, Portable ECG Monitoring Devices, Low-Power

Abstract: This paper presents a three-channel low- power and compact analog processor including a test chip, fabricated in TSMC 0.35u mixed-mode CMOS process, for portable Electrocardiogram (ECG) monitoring devices. The chip integrates instrumentation amplifiers based on current balancing technique to implement more analog signal conditioning functions at instrumentation amplifiers. First order low-pass filtering as well as programmable high-pass filtering has been included in each instrumentation amplifier. Experimental results show that each channel draws 22 uA from a 3.3V lithium-ion battery. Measurement results satisfy recommended specifications for portable ECG recorders. The programmable test board, designed using the chip, records three-leads ECG with frontal plane and precordial leads selectivity. Analog signal conditioning circuit, experimental results and recorded ECGs are given in this paper.

P2-28 9:45-17:30

On-demand Pipelining for Improving Energy-Awareness

Chin-Hung Liu(National Chiao Tung University), Tay-Jyi Lin(National Chiao Tung University), Chie-Wei Liu(National Chiao Tung University), Chein-Wei Jen(National Chiao Tung University)

Keywords:

Abstract: Clock gating is a well-known technique to reduce the clock pulses when a pipelined datapath does not reach its peak throughput. This paper presents an on-demand pipelining scheme to further eliminate all redundant clock transitions, where the synchronization elements (i.e. registers or latches) are activated only when necessary. In our experiments with the UMC 0.18μm CMOS technology, the proposed approach saves up to 61% energy dissipation on conventional pipelines and 13% of those with gating clocks only. In contrast with the constant energy dissipation of conventional clock gating approaches, our on-demand pipelining consumes less and less energy as the allowed computation cycles increase for a given task. In other words, the proposed scheme has better energy awareness over varying throughput requirements.

P2-29 9:45-17:30

Design of a High-Performance Switch for Circuit-Switched On-Chip Networks

Chia-Ming Wu(National Dong Hwa University), Hsin-Chou Chi(National Dong Hwa University)

Keywords: Network-on-Chip, System-on-Chip, Switches, Interconnection Networks

Abstract: System-on-a-chip (SoC) designs provide designers to integrate dozens of heterogeneous IP blocks together by a dedicated interconnect network. The major problems in the ultra deep sub-micron technology SoC design arise from the interconnection networks, such as non-scalable global wire delay,

failure to achieve global synchronization, and errors due to signal integrity issues. These problems might be mitigated by the network-on-chip (NoC) approach based on regular on-chip communication networks. In this paper, we propose the pre-scheduled circuit-switched network for NoC architectures. We have designed the switch supporting the network. Such architectures based on circuit switching with efficient buffer management can achieve guaranteed transmission latencies.

Session DC Desgin Contest

Nov. 1 10:35-17:50

Session Chair: *Jerry Jou(National Chiao Tung University)*

DC-1 10:35-17:50

Networks-on-chip and Networks-in-Package for High-Performance SoC Platforms

Kangmin Lee(KAIST), Se-Joong Lee(KAIST), Donghyun Kim(KAIST), Kwanho Kim(KAIST), Gawon Kim(KAIST), Joungho Kim(KAIST), Hoi-Jun Yoo(KAIST)

Keywords: Networks-on-chip, Networks-in-Package, on-chip network, system-on-chip, low-power design, interconnection, serial communications, bus coding

Abstract: A structured packet-switched Networks-on-Chip (NoC) is designed and implemented for high-performance heterogeneous SoC design platform. The chip integrates multiprocessors, multiple memories, and other heterogeneous Intellectual Properties and interconnection with 51mW and 1.6GHz on-chip networks. The NoC adopts a partial activated crossbar, low-energy coding, and low-swing signaling for the power consumption optimization. A Network-in-Package integrating four NoCs is fabricated in a 676-BGA-type package for larger and scalable systems and demonstrates 2D-image-processing and 3D-graphics applications.

DC-2 10:35-17:50

A 1.1-V 9.9-mW MC-CDMA Downlink Baseband Receiver IC for Next-Generation Cellular Communication Systems

Pei-Yun Tsai(National Taiwan University), Tzi-Dar Chiueh(National Taiwan University)

Keywords: multi-carrier modulation, code-division multiple access, baseband receiver

Abstract: A baseband receiver IC for a downlink multicarrier code-division multiple access (MC-CDMA) system suitable for the next generation cellular communication in urban areas is designed and implemented. A robust tracking mechanism for synchronization errors and an accurate channel estimation strategy to overcome the challenge of outdoor fast-fading channels are provided in the proposed chip. Besides, low-power and low-complexity architecture design techniques are adopted to satisfy mobile receiver needs. Experimental results of the IC demonstrate its superior system performance and great reduction in power consumption. The chip was fabricated in a 0.18-um CMOS technology with a core area of 2.6 mm x 2.6 mm. It can support up to 21.7 Mbps uncoded data rate in a 5-MHz bandwidth. When running at 5.76 MHz, its power consumption is as low as 9.9 mW from a supply voltage of 1.1V.

DC-3 10:35-17:50

A 2.4GHz CMOS Quadrature VCO for 2.4GHz WLAN/Bluetooth Applications

Jung-Yu Chang(National Taiwan University), Chia-Hsin Wu(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords:

Abstract: A 2.4GHz low-phase-noise and low-phase-error LC tank quadrature voltage controlled oscillator (QVCO) using the parasitic vertical BJT coupling and RC phase shifters is presented. Based on the proposed techniques, the proposed QVCO can simultaneously have low phase noise and low phase error. This QVCO circuit has been realized in a 0.18μm triple-well CMOS process and exhibits below 0.2o phase error with phase noise of -105dBc/Hz at 100kHz offset frequency . The tuning range is 380MHz from 2.27GHz to 2.65GHz with control voltage from 0.3V to 1.8V. It consumes 5.4mW at each tank. .

DC-4 10:35-17:50

A Fast-Recovery Low Dropout Linear Regulator for Any-Type Output Capacitors

Sao-Hung Lu(National Taiwan University), Wei-Jen Huang(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords:

Abstract: A 1.8-V, 150-mA fast settling low dropout linear regulator (LDO) with single Miller compensation capacitor is presented. By utilizing the digital-controlled dynamic bias circuit to track the output current, the proposed LDO provides fast settling time, 4us with 0.5% error, for the output capacitors with low and high equivalent series resistance (ESR). The proposed LDO has been fabricated in a 0.35-um 2P4M CMOS technology, and the active chip area is 480um x 675 um. Furthermore, the line and load regulations are 0.127%/V and 40ppm/mA, respectively. The measured quiescent current is 45uA in 5V supply voltage

DC-5 10:35-17:50

A 1.8-V 531-mW Single-Chip Single-Conversion CMOS Cable TV Tuner

Wang Dan(Hong Kong University of Science & Technology), S.Z. Lou(Hong Kong University of Science & Technology), D. Lau(Hong Kong University of Science & Technology), E. Wang(Hong Kong University of Science & Technology), G. Wong(Hong Kong University of Science & Technology), Howard Cam Luong(Hong Kong University of Science & Technology)

Keywords: CMOS,cable TV tuner

Abstract: An integrated analog tuner for Open-Cable applications is designed in a standard 0.18μm CMOS process using single-conversion architecture. The tuner integrates a whole signal path including a wide-band low-noise amplifier, a novel image-rejection mixer, and a fully-integrated integer-N frequency synthesizer with a wide-band ring VCO. At 1.8-V supply and over the whole input frequency range from 54 MHz to 864 MHz, the tuner measures image rejection of 61dB, maximum noise figure of 8.5-dB, IIP2 of 74 dBmV and IIP3 of 46.75 dBmV corresponding to CTB of -53 dBc and CSO of -54.3 dBc. The tuner dissipates a total of 531 mW while occupying a chip area of 5.4 mm^2.

DC-6 10:35-17:50

10GBase-LX CMOS Automatic Gain Control Amplifier Design

I-Hsin Wang(National Taiwan University), Wei-Sheng Chen(National Taiwan University), Shen-Iuan Liu(National Taiwan University)

Keywords: 10GBase-LX, CMOS, AGC, Optical communication, VGA
Abstract: A 5Gbps automatic gain control amplifier is presented with 27.8dB input dynamic range for 10GBase-LX4 Ethernet in 0.18um CMOS technology. Five push-pull inverters use self-bias resistors and inductive-series peaking technique to realize a variable gain amplifier (VGA). This VGA achieves 4GHz bandwidth and 20dB linear-in-dB gain tuning range. The proposed 5Gbps AGC amplifier yields constant output amplitude 100mV for an input 27.8dB dynamic range.

DC-7 10:35-17:50

FPGA Prototype for WLAN OFDM Baseband with STPE of I/Q Mismatch Self Calibration Algorithm

Chia-Hung Hsu(National Taiwan University), Chih-Feng Wu(National Taiwan University), Chrong-Kuang Wang(National Taiwan University)

Keywords: IQ mismatch, compensation, FPGA, calibration, OFDM
Abstract: Based on the single tone power evaluation (STPE), a self-calibration algorithm of I/Q mismatch is proposed for the IEEE 802.11a WLAN systems. The self-calibration algorithm is performed by the digital baseband at transceiver start-up to measure the signal power of the single tone signal, which is located at the double frequency band at the receiver. Furthermore, the residual I/Q mismatch is tracked during the physical data transmission. Therefore, the design requirements of the RF front-end for the WLAN OFDM transceiver are alleviated. According to the proposed algorithm, the residual signal-to-noise ratio (SNR) degradation is totally less than 0.5dB with +/-5% gain mismatch (ΔG) and +/-5^{o} phase mismatch ($\Delta\theta$) in the transmitter and receiver respectively, and carrier frequency offset (CFO =+/- 232kHz). Finally, the prototype of the IEEE 802.11a WLAN baseband is realized by the Altera Stratix EP1S80 DSP development board with about 32000 logic elements at 40MHz.

DC-8 10:35-17:50

Scalable Security Processor Design and Its Implementation

Chen-Hsing Wang(National Tsing Hua University), Jen-Chieh Yeh(National Tsing Hua University), Chih-Tsun Huang(National Tsing Hua University), Cheng-Wen Wu(National Tsing Hua University)

Keywords:
Abstract: This paper presents a security processor to accelerate cryptographic processing in modern security applications. Our security processor is capable of popular cryptographic functions such as RSA, AES, hashing and random number generation, etc. With proposed Crypto-DMA controller, data gathering and scattering become flexible for security processing, using a simple descriptor-based programming model. The architecture of the security processor with its core-based platform is scalable and configurable for security variations in performance, cost and power consumption. Different number of data channels and cryptoengines can be used to meet the specifications. In addition, a DFT (design for test) platform is also implemented for the design-test integration. The security processor has been fabricated (using UMC 0.18um CMOS technology) and measured. The core area is 3.899mm x 2.296mm (525K gates approximately) and the operating clock rate is 66MHz.

DC-9 10:35-17:50

Area Efficient Architecture for the Embedded Block Coding in JPEG 2000

Yu-Wei Chang(National Taiwan University), Hung-Chi Fang(National Taiwan University),

Chun-Chia Chen(National Taiwan University), Liang-Gee Chen(National Taiwan University)

Keywords: JPEG 2000, Embedded Block Coding, Arithmetic Encoder
Abstract: An area efficient architecture for the embedded block coding in JPEG 2000 is implemented on a 1.23 mm^2 die using 0.18 um CMOS technology. This chip can support 16.7 MS/s lossless encoding. The area of the proposed architecture is only 1/6 of the conventional architectures while the throughput is the same as others. The proposed architecture has the highest performance comparing with other existing architectures according to the experimental results.

DC-10 10:35-17:50

A Wideband Programmable Spread-Spectrum Clock Generator

Sheng Feng Ho(Fu-Jen Catholic University)

Keywords: Spread-spectrum clock generator (SSCG), triangular modulation, harmonic, microprocessor, spread-spectrum, spread modulation, phase-locked loop (PLL)
Abstract: In this work, a spread-spectrum clock generator (SSCG) with triangular modulation is presented. The SSCG can be applied to most of microprocessor system. It has the effect of spreading the energy of a frequency harmonics over a wider bandwidth, and hence reducing the amplitudes of the harmonics. The digitally programming schemes are implemented in the charge pump current, the voltage controlled oscillator gain, the low-pass filter and the divider, to realize reusable silicon IP. The proposed SSCG can generate clocks of 64-MHz-1920-MHz with center spread modulation from +/- 1MHz to +/- 50MHz and the spread ratios equal to spread modulation divides output frequency. A test fabricated in a 0.18μm CMOS single-poly six-metal process is fabricated. The area 1.01um x 1.14um including the loop filter. It consumes 100mW of power at 266-MHz. Attenuation as high as 17dB is presented.

DC-11 10:35-17:50

The Split-Path AND-type Match-line Scheme for Very High-Speed Content Addressable Memories

Chia-Cheng Chen(Faraday Corp.), Hung-Yu Li(National Chung Cheng University), Jinn-Shyan Wang(National Chung Cheng University)

Keywords: high speed, content addressable memory, CAM
Abstract: The proposed split-path AND-type non-pipelined match-line scheme achieves over 50% search speed improvement compared to the pipelined NOR-type current-saving controlled match-line scheme. The highest world record of 1.6 ns search speed can also be traded for power saving by adopting voltage scaling. When the supply voltage is reduced to a level so that the energy efficiency of both kinds of design is almost equal, the new scheme still has 18% speed improvement.

DC-12 10:35-17:50

A Low-Power Tunable Single-Chip CMOS Low-IF Single-Conversion ISM Receiver

Chia-Pei Chen(National Chiao-Tung University), Simon C. Li(National Yunlin University of Science and Technology), Hong-Sing Kao(National Chiao-Tung University), Chung-Chih Su(AlfaPlus Semiconductor Inc.), Kuei-Ann Wen(National Chiao-Tung University)

Keywords: single-chip, RF receiver, FM/FSK demodulator, IF section

Abstract: A single-chip tunable CMOS low-IF single-conversion receiver operated in the 915-MHz ISM band is proposed. A new 10.7-MHz IF section including a limiting amplifier and FM/FSK demodulator is employed. Near IF section sensitivity of -72 dBm, the demodulation constant of FM/FSK demodulator is 15 mV/kHz and the dynamic range of the limiting amplifier reaches 80dB. With on-chip tunable components in low power LNA and LC-tank VCO circuit, the receiver measures a RF gain of 15dB at 915-MHz, sensitivity of -80dBm at 0.1% BER, IIP3 of -9dBm, and NF of 5dB with current consumption of 33mA and a chip area of 6 mm^2.

DC-13 10:35-17:50

720 x 480 30fps Efficient Prediction Core Chip for Stereo Video Hybrid Coding System

Li-Fu Ding(National Taiwan University), Shao-Yi Chien(National Taiwan University), Liang-Gee Chen(National Taiwan University)

Keywords:

Abstract: The chip design of prediction core in the stereo video hybrid coding system is implemented with 0.18μm 1P6M technology by TSMC. The die size is 4.53 mm2. This IC can can achieve real-time requirement under the operating frequency of 81 MHz for 30 D1 frames per second (fps) in the left and the right channel simultaneously, with ME/DE search range of [-64, +63] in horizontal direction and [-32, +31]/[-16, +15] in vertical direction. Compared with the hardware requirement for implementation of full search block matching algorithm (FSBMA), only 11.5% on-chip SRAM and 1/30 amount of PEs are needed. It shows that the hardware cost is quite small.

DC-14 10:35-17:50

A 10BIT 30MSPS IF Sampling CMOS A/D Converter

Jian Li(Fudan University), Xiaoyang Zeng(Fudan University), Bo Shen(Fudan University)

Keywords: Analog-to-Digital Converters, bootstrapping, wide-swing bias, pipeline, IF sampling

Abstract: This paper describes a 10bit 30MSPS CMOS analog-to-digital converter (ADC) for IF sampling applications, for example digital video broadcasting over cable (DVB-C), terrestrial (DVB-T) and handheld (DVB-H) systems. The proposed pipelined ADC adopts a power efficient amplifier sharing technique, a symmetrical gate-bootstrapping technique for a wideband SHA, a proposed stable high-swing bias circuit for a wide-swing gain-boosting telescopic amplifier. The measured differential and integral nonlinearities of the prototype in a 0.25-mm CMOS technology show less than 0.4 least significant bit (LSB) and 0.85LSB respectively at full sampling rate. The ADC exhibits higher than 9 effective number of bits (ENOB) for input frequencies up to 60MHz, which is the fourfold Nyquist rate (fs/2), at 30 MS/s. The ADC consumes 60 mW from a 3-V supply and occupies 1.36 mm2.

DC-15 10:35-17:50

Ultra Low-Cost 3.2Gb/s Optical-Rate Reed Solomon Decoder IC Design

An-Yeu Wu(National Taiwan University), Huai-Yi Hsu(National Taiwan University), Jih-Chiang Yeo(National Taiwan University)

Keywords: Forward Error Correction, Reed-Solomon, Just-in-Time Folding Modified Euclidean Algorithm

Abstract: Reed-Solomon (RS) code is a widely used Forward Error Correction (FEC) technology to

improve the channel impairments in the fiber communication systems. The typical parallel FEC architecture requires huge hardware cost to achieve very-high-speed transmission data rate for the optical systems. This paper presents an ultra low-cost VLSI architecture of RS decoder by using a novel Just-in-Time Folding Modified Euclidean Algorithm (JIT-FMEA). The JIT-FMEA VLSI architecture can greatly reduce the hardware complexity by about 50% from the fully expanded parallel architecture, while it can achieve very high throughput rate for the 10Gbase-LX4 optical communication system. The proposed RS decoder architecture has been designed and implemented by using 0.18-um CMOS standard cell technology at the supply voltage of 1.8V. Our design only requires about 21K gates and can achieve the data throughput rate of 3.2Gbit/s at clock frequency of 400MHz.

DC-16 10:35-17:50

A 124.8Msps, 15.6mW Field-Programmable Variable-Length Codec for Multimedia Applications

Chao-Ching Wang(National Chung Cheng University), Chingwei Yeh(National Chung Cheng University), Lin-Chi Lee(Winbond Corp.), Jinn-Shyan Wang(National Chung Cheng University)

Keywords: VLC/VLD, VLC codec, Group based, DIRAM and CAM

Abstract: A 124.8Msps, 15.6mW field-programmable VLC codec is proposed for multimedia applications. The design has 33% less transistors than its field-programmable predecessor. When measured by μW/Msym, the realized MPEG4 VLC/D chip is even 5% better than the state-of-the-art low-power non-programmable MPEG2 VLD which hardwires the entire design into random logic.

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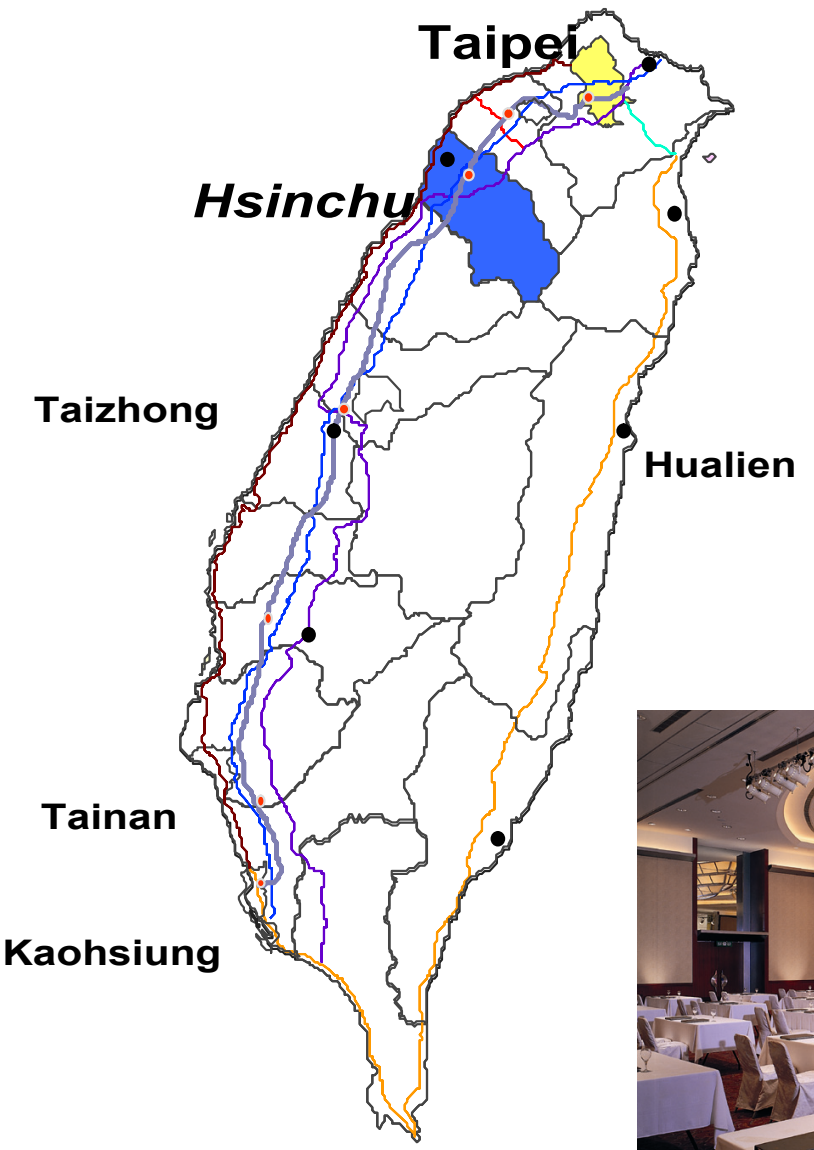

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