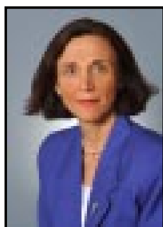
WELCOME FROM THE GENERAL CHAIR

On behalf of the IEDM Committee, I would like to welcome you to the 2002 IEEE International Electron Devices Meeting. This year the conference returns to San Francisco and continues a long tradition as the leading forum for the presentation of research and development in the area of electron devices and their applications. The strong international nature of our industry and the broad range of topics are evident, with invited speakers and contributed papers from around the world. A total of 598 abstracts were submitted from 30 different countries, with 534 of these abstracts submitted electronically via the World Wide Web. The total number of accepted abstracts was 212. We continue to focus on accessibility to the information in the IEDM abstracts. Short summaries of each abstract are included on the IEDM home page, and we encourage everyone to visit the site at http://www.ieee.org/conference/iedm. This year, we will once again feature the IEDM digital projection of presentation materials at the conference.

Shuji Ikeda
General Chair



Leda Lunardi
Technical Program Chair

Two short courses are scheduled for Sunday. These are designed for broad appeal to IEDM participants with material suitable for both newcomers as well as experts in the field. The courses are entitled "The Future of Semiconductor Manufacturing" and "RF Device Technologies for Communication Systems". These courses have been organized by internationally known researchers and will be presented by people active in the respective topics.

Jeff Welser
Technical Program Vice Chair

The plenary talks on Monday will feature presentations on "Lithography for Sub-100nm Applications", "Chip Technologies for Entertainment Robots: Present and Future", and "Photonic Bandgap Based Designs for Photonic Integrated Circuits". Speakers from Europe, Asia and North America will be featured.

The IEDM Luncheon speaker this year will be Andrew S. Grove of Intel. He will be speaking on "Changing Vectors of Moore's Law". Dr. Grove is Chairman of the Board of Intel Corp.

WELCOME FROM THE GENERAL CHAIR

The Emerging Technologies session this year is entitled "Bio-Electronic Devices," and consists of invited talks from experts in the field. The talks will cover electronic sensors for biological pharmaceutical and medical applications.

On Tuesday night, a panel session is planned on two important and potentially controversial topics: "Will SOI Ever Become a Mainstream Technology?" and "Embedded Memories, What Makes Sense, Cents?".

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Leda Lunardi, Technical Program Chair and Jeff Welser, Technical Program Vice Chair, I wish to express my sincere appreciation and congratulations to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 2002 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM.

It is with great pleasure that I extend a warm welcome to everyone attending the 2002 IEEE International Electron Devices Meeting.

Shuji Ikeda
General Chair

HIGHLIGHTS

SHORT COURSES

Sunday, December 8, 9:00 a.m. - 5:30 p.m.
Continental Ballrooms 1-4
Continental Ballrooms 6-9

PLENARY SESSION

Monday, December 9, 9:00 a.m. - 12:00 p.m.
Grand Ballroom B

PLENARY SESSION AWARD PRESENTATIONS

2001 Roger A. Haken Best Student Paper Award

To: Hideaki Majima, University of Tokyo
For the paper entitled: "Impact of Quantum Mechanical Effects on Design of Nanoscale Narrow Channel n- and p-type MOSFETs"

Paul Rappaport Award

To: Ioannis Kymissis, Massachusetts Institute of Technology,
Christos D. Dimitrakopoulos and Sampath Purushothaman, IBM T.J. Watson Reseach Center
For the paper entitled: "High-Performance Bottom Electrode Organic Thin-Film Transistors"

To: Raymond M. Warner, Jr.
For the paper entitled: "Microelectronics: Its Unusual Origin and Personality"

EDS Chapter of the Year Award

To: To Be Announced
"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

EDS Graduate Fellowships

To: Yung Fu Chong, National University of Singapore
Jack Chen, University of Illinois
David Fried, Cornell University
Ofir Bochobza-Degani, Techmion-Israel Institute of Technology
"To promote, recognize, and support graduate level study and research within the Electron Devices Society's field of interest"

EDS Distinguished Service Award

To: Lucian A. Kasprzak
"To recognize and honor outstanding service to the Electron Devices Society"

HIGHLIGHTS

J.J. Ebers Award

To: Lester F. Eastman, Cornell University
"For sustained technical contributions and leadership in the development of high frequency heterostructure transistors"

RECEPTION

Monday, December 9, 6:00 p.m. - 7:30 p.m.
Grand Ballroom B

IEDM LUNCHEON

Tuesday, December 10
12:20 p.m. - 2:00 p.m.
Grand Ballroom B

2002 IEEE Cledo Brunetti Award

To: Mark Lundstrom and Supriyo Datta, Purdue University
"For significant contributions to the understanding and innovative simulation of nano-scale electronic devices."

2002 IEEE Andrew S. Grove Award

To: Dimitri A. Antoniadis, Massachusetts Institute of Technology
"For seminal contributions to field-effect devices and silicon process modeling."

2002 IEEE Daniel E. Noble Award

To: Masataka Nakazawa, Tohoku University
"For pioneering development of 1.48 µm InGaAsP laser-diode pumping of erbium-doped fiber amplifiers (EDFA)."

LUNCHEON PRESENTATION

Luncheon Presentation: "Changing Vectors of Moore's Law" by Andrew S. Grove

PANEL SESSIONS

Tuesday, December 10
8:00 p.m. - 10:00 p.m.
Grand Ballroom A
Grand Ballroom B

2002 iedm

international Electron Devices meeting

GENERAL INFORMATION

San Francisco Hilton and Towers
333 O'Farrell St.
San Francisco, CA 94102
415-771-1400
December 8-11, 2002

REGISTRATION INFORMATION

	Advance Postmarked by November 16th	After November 16th or at Conference
Technical Session		
IEEE Member	$365.00	$405.00
Non-member	$440.00	$480.00
Students:		
Member	$ 50.00	$ 50.00
Non-Member	$ 85.00	$ 85.00
Short Courses (You must register in advance.)		
Member/Non-member	$400.00	
Student	$100.00	

Payment of the Technical Session registration fee entitles the registrant to one copy of the Technical Digest, one copy of the CD-ROM, one ticket for the Monday evening Wine and Cheese Reception and entrance to all technical sessions. Technical Session registration does not include entrance to the Short Courses. TO QUALIFY FOR THE MEMBER REGISTRATION FEE, REGISTRANT MUST BE A MEMBER OF IEEE PRIOR TO THE CONFERENCE.

Payment of the Short Course registration fee entitles the registrant to entrance to one short course, one copy of the course workbook and one CD ROM. Short Course registration does not include entrance to the Technical Sessions.

For Advance Registration, complete the Advance Registration Card (see centerfold) and return with remittance of appropriate registration fee NO LATER THAN NOVEMBER 16, 2002 to qualify for the early registration price. You must register in advance to attend the Short Courses.

Confirmations will be sent out to all conference registrants.

GENERAL INFORMATION

REGISTRATION FORM AND PAYMENT SHOULD BE SENT TO:

2002 IEDM
16220 S. Frederick Avenue
Suite 312
Gaithersburg, MD 20877 USA
301-527-0900

Checks MUST BE MADE PAYABLE TO 2002 IEDM, IN U.S. DOLLARS AND DRAWN ON A U.S. BANK. International registrants should not send wire transfers. If International participants cannot send a check prior to the conference, mail the registration form without payment prior to the conference. Bring payment with you and pay the registration fee onsite.

Your registration materials will be held for you at the conference. Your cancelled check is your receipt.

or register online at http://www.ieee.org/conference/iedm

CANCELLATION POLICY: You are encouraged to register in advance for your own convenience. Due to printing and hotel commitments, refunds requested after November 20 cannot be guaranteed. A $30.00 processing fee will be withheld from ALL refunds.

REGISTRATION CENTER: The Conference Registration Center, located in the East Lounge of the San Francisco Hilton and Towers, will be open as follows:

SHORT COURSE REGISTRANTS ONLY

Saturday, December 7	5:00 p.m. - 7:00 p.m.
Sunday, December 8	8:00 a.m. - 11:00 a.m.

TECHNICAL SESSION REGISTRANTS

Sunday, December 8	2:00 p.m. - 5:00 p.m.
Monday, December 9	8:00 a.m. - 5:00 p.m.
Tuesday, December 10	8:30 a.m. - 5:00 p.m.
Wednesday, December 11	8:30 a.m. - 3:00 p.m.

HOTEL RESERVATIONS: A block of rooms at the San Francisco Hilton and Towers has been reserved for IEDM participants. Special IEDM room rates are as follows:

Single: $180.00
Double: $180.00

Plus a 14.05% city tax.

To make a reservation, please complete the Hotel Reservation Form (see centerfold) and return directly to the San Francisco Hilton NO LATER THAN NOVEMBER 4th to qualify for a room under our special rates. An advance deposit or credit card guarantee is necessary to hold your room, if arrival is scheduled after 6:00 p.m.

SHORT COURSES: The IEDM sponsors two short courses on Sunday, December 8, from 9 a.m. to 5:30 p.m. The courses are “RF

Device Technologies for Communication Systems" and "The Future of Semiconductor Manufacturing." These courses will be presented by experts in the fields. Lectures will start with introductory material for the general audience and progress towards description of the latest developments.

To register, complete the Advance Registration form, (see centerfold). The registration fee is $400 and includes a visuals booklet, CD ROM, refreshments and lunch. Attendance is limited, so advance registration is recommended.

SHORT COURSE TAPES: The 1995-2002 Short Courses are available on VHS tapes. The cost is $380 for IEEE members and $450 for non-members. To place an order, please complete the VideoTape Order Form (see back flap) and return with payment to: IEEE Customer Service, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. Please note: NTSC is the video standard used in the US, Canada, Mexico and Japan. If you are uncertain of the standard (NTSC or PAL) used in your country, please contact IEEE prior to ordering by calling 1-732-981-0060 or 1-800-678-4333 or email customer-service@ieee.org

AIRLINE DISCOUNT PROGRAM: Special discounted airfares for your meeting have been negotiated by IEEE Global Travel Services. Discounts are as high as 20% off the lowest published airfares with American, Continental and United airlines. If Saturday night stays or super-saver airfares are not applicable, zone fares are available. Special rates have also been negotiated with Avis Rental Car Company.

Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Global Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (800-879-4333; and outside of the US and Canada, call (732) 562-5387. Or, you may visit their on-line travel service web site at www.ieeetravelonline.org. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere.

You may also your fax requirements to the IEEE Global Travel Services at (732) 562-8815. When faxing, please be sure to include your travel dates, departure, and return times, and phone and fax numbers. Also give the name of your meeting and indicate that the Electron Devices Society is the sponsoring society. A Travel Counselor will contact you promptly.

EVENING PANEL DISCUSSIONS: On Tuesday evening, December 10, beginning at 8:00 p.m., the IEDM will offer two evening Panel Discussions on timely issues.

1. Embedded Memories for SoC - What Makes Sense?
2. Will SOI Ever Become a Mainstream Technology?

TO PERMIT SPONTANEOUS AND CANDID DISCUSSION, NO VERBATIM RECORDING BY TAPE OR CAMERA WILL BE PERMITTED IN ANY PANEL DISCUSSION.

GENERAL INFORMATION

IEDM LUNCHEON: The IEDM luncheon featuring an address by Andrew Grove of Intel Corporation, will be held on Tuesday, December 10, at 12:20 p.m. in Grand Ballroom B. Luncheon tickets are available through Advance Registration or on-site at a cost of $40.00 for conference attendees only.

SPEAKER PREPARATION ROOM: The IEDM will sponsor a Speaker Preparation Room in Union Square 13 for speakers to upload their presentations. Speakers must upload their presentations 1 day in advance. There will be no previewing of presentations the day of the presentation.

Union Square 13 will be open for speaker use:

Saturday, December 8	5:00 p.m. – 7:00 p.m.
Sunday, December 9	8:00 a.m. – 5:00 p.m.
Monday, December 10	8:00 a.m. – 5:00 p.m.
Tuesday, December 11	8:30 a.m. – 5:00 p.m.
Wednesday, December 12	8:30 a.m. – 3:00 p.m.

WINE AND CHEESE RECEPTION: A Wine and Cheese Reception for conference participants and their guests will be held on Monday, December 9 from 6:00 p.m. to 7:30 p.m. in Grand Ballroom B. ONE ADMISSION TO THE RECEPTION IS INCLUDED IN THE REGISTRATION FEE.

TECHNICAL DIGEST/CD-ROM: Extra copies of the Technical Digest/CD ROM can be purchased by conference registrants through Advance Registration. A LIMITED number of Digests will be for sale after 2:00 p.m. on Tuesday, December 10 at the On-Site Registration Desk of the Conference. The unit cost of the Digest, if ordered through Advance Registration or purchased on-site is $125.00. Digests will be available after the conference by mail from IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855. Customer Service Department 732-981-0060 or toll free: 800-678-4333, email is customer-service@ieee.org. ONE COPY OF THE TECHNICAL DIGEST/CD ROM IS INCLUDED IN THE REGISTRATION FEE.

MESSAGE CENTER: An IEDM Message Board will be in operation in the Registration Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator 415-771-1400 for the IEDM Conference Message Desk. Please check the message board periodically.

MEMBERSHIP PROMOTION FOR NON-IEEE MEMBERS: Conference registrants will be able to join IEEE, the Electron Devices Society (EDS) and the Solid-State Circuits Society (SSCS) during the conference at the IEEE Membership Desk located in the Registration Center. If you registered and paid for the conference as a non-member, you will be receiving a CREDIT voucher worth $25 towards an IEEE membership, and free EDS and SSCS memberships for one year (worth $20). STUDENTS registering at the student non-member rate will receive a credit voucher that will entitle them to one-year of FREE IEEE, EDS and SSCS memberships.

MEMBERSHIP PROMOTION FOR CURRENT IEEE MEMBERS: For the first time, FREE Electron Devices Society membership for one-year will be offered to any IEEE member attending the IEDM who is not currently a member of EDS. A FREE EDS Membership Credit

GENERAL INFORMATION

Voucher will be available at the IEEE Membership Desk. Just complete the voucher by providing your name, address and member number and submit it to the Membership Desk. If you are currently a member of EDS, you cannot use this voucher to renew your membership. Credit vouchers are only valid at the IEDM and must be redeemed at the IEEE Membership Desk. Copies of the 2003 EDS Membership Brochure are also available at the Membership Desk, which will be open the following hours:

Sunday, December 8	5:00 p.m. - 7:00 p.m.
Monday, December 9	9:00 a.m. - 5:00 p.m.
Tuesday, December 10	9:00 a.m. - 5:00 p.m.
Wednesday, December 11	9:00 a.m. - 3:00 p.m.

ROGER A. HAKEN BEST STUDENT PAPER: The 2001 Roger A. Haken Best Student Paper will be presented on Monday, December 9, at the Plenary Session to Hideaki Majima, University of Tokyo, for the paper entitled: "Impact of Quantum Mechanical Effects on Design of Nanoscale Narrow Channel n- and p-type MOSFETs". One paper presented by a student at the 2002 IEDM will be selected for the 2002 Best Student Paper Award. To be eligible, the paper must be based on the student's own work and have been identified as a student paper at the time of submission. Presentation of the award will be made at the 2003 IEDM.

BADGES: Badges are required for admittance to all sessions and the Wine and Cheese Reception. Please wear your badge at all times, while attending the conference, so that you will not be delayed entry to a session.

PRESS ROOM: Beginning on Monday, the Press Room, located in Union Square 9, will be in operation during registration hours.

AIRPORT TRANSPORTATION: The SFO Airporter and taxi service is available from the San Francisco International Airport to the San Francisco Hilton and Towers Hotel. The following estimated rates are subject to change:
SFO Airporter - $10 one way/$20 roundtrip
Taxi - $30 one way

RECRUITING: In keeping with the long standing tradition of fostering a low key, research oriented atmosphere for the IEDM, the Conference Committee and the Electron Devices Society of the IEEE discourage overt and highly visible recruiting activities in association with the IEDM. IEEE policy #9.18 prohibits recruiting at IEEE-sponsored conferences, consequently, recruiters and recruitment advertisements will not be permitted in IEDM hotel space or meeting facilities and all unauthorized material will be removed from the premises.

PLEASE DIRECT CONFERENCE INQUIRIES TO:

Phyllis Mahoney
2002 IEDM
16220 S. Frederick Road, Suite 312
Gaithersburg, MD 20877 USA
TEL: 301/527-0900 EXT. 103
FAX: 301/527-0994
EMAIL: phyllism@widerkehr.com

2002 IEDM Conference and Program Committee

Seated from left to right: Kaizad Mistry, Short Course Vice-Chair; Yoshihiro Hayashi, Short Course Chair; Jeff Welser, Technical Program Vice-Chair; Shuji Ikeda, General Chair; Leda Lunardi, Technical Program Chair; H.S. Philip Wong, Publicity Vice-Chair; Kinam Kim, Asian Arrangements Co-Chair

First row standing from left to right: Phyllis Mahoney, Conference Manager; Dieter Vook, Emerging Technologies Chair; John Faricelli, Modeling and Simulation Subcommittee Chair; Katsuyoshi Washio, Solid State Devices Subcommittee Chair; Chiara Corvasce, Integrated Circuits and Manufacturing Subcommittee Chair; Cliff King, Publications Chair; Masaaki Niwa, Asian Arrangements Co-Chair; Guido Groeseneken, European Arrangements Co-Chair; Melissa Widerkehr, Conference Manager

Second row standing from left to right: Bo Willen, Quantum Electronics and Compound Semiconductors Subcommittee Chair; Ralf Brederlow, CMOS Devices Subcommittee Chair; Hans-Joachim Barth, European Arrangements Co-Chair; Vivek Subramanian, Process Technology Subcommittee Chair; Tiemin Zhao, Detectors, Sensors and Displays Subcommittee Chair; Tony Oates, CMOS and Interconnect Reliability Subcommittee Chair

SHORT COURSE: RF Device Technologies for Communication Systems

Sunday, December 8, 9:00 a.m. – 5:30 p.m.
Continental Ballrooms 1-4

Course Organizer: *Bin Zhao,*
Skyworks Solutions, Newport Beach, CA

Empowered by advanced digital communication techniques and digital signal processing, RF communications have evolved from traditional radio and TV broadcasting to a broad spectrum of exciting applications in bi-directional and interactive wireless communications such as cellular systems, smart handheld devices, wireless LANs, Bluetooth, HomeRF, GPS and broadband satellite solutions. These applications to communicate voice, data, and image/video to anywhere at any time rely on advances in semiconductor IC technologies to provide integrated solutions at affordable cost. Under the two communication resource constraints, bandwidth and power, many wireless communication systems have to push the RF devices to operate at their performance limits. This requirement leads to significant engineering challenges and opportunities in system architectures, circuit design, and device technology development. This short course will review the requirements, current solutions, and future perspectives in system architectures, circuit implementation, and device technologies for modern RF communication systems.

The first lecture will describe modern RF communication systems and architectures with an emphasis on fundamental principles and wireless transceiver architectures suitable for high integration and low power. The second lecture will cover the basic RFIC circuit building blocks (LNA, mixer, VCO, PA, etc.) and their requirements for RF devices. The impact of device technologies on different RF circuit functions will be discussed. The third lecture will review the status and challenging issues in RF device technologies including RF-CMOS, SOI, SiGe Bipolar, III-V HBT, on-chip passives, and novel RF MEMS devices. The fourth lecture will address the RF device modeling issues. Understanding and accurate modeling various RF device phenomena are critical for RFIC design and future RF device technology development. The final lecture will present several design and implementation examples in RF frequency synthesizer, single chip radio/Bluetooth, and DCR (direct conversion receiver) for 3G and 802.11 standards. RFIC design insights and implementation considerations in RF device technologies will be highlighted.

Introduction and Overview

Instructor: *Bin Zhao*
Skyworks Solutions, Newport Beach, CA

Modern RF Communication Systems and Architectures

Instructor: *Asad Abidi*
University of California, Los Angeles, CA

Types of Wireless Communication Devices
- Cellular Communications
- WLAN
- Paging and Low Power Communicators

Fundamentals of Wireless Transceivers
- Dynamic Range
- Noise and Linearity
- Cascade Effects
- Receiver Power Consumption
- Efficiency of Power Amplification

Transceiver Architectures Suited to High Integration
- Zero and Low IF Receivers
- Modulation Loop-Based Transmitters
- Problems and Limitations

Case Studies of RF-CMOS Receivers and Transmitters

Future Perspectives

RFIC and Requirements for RF Devices

Instructor: *Larry Larson*
University of California, San Diego, CA

Introduction

Impact of Device Scaling on RF Performance
- Bipolar/HBT Scaling
- MOSFET Scaling

Device Impact on Low-Noise Amplifier Performance
- Considerations for Low Noise Figure
- LNA Linearity Performance

Mixers for RF Frequency Translation
- CMOS vs. Bipolar Mixers
- Noise Behavior

VCO Design Considerations
- Resonant Circuit Quality Factor
- Fundamental Limits on VCO Phase Noise

Device Impact on Power Amplifier Performance
- Breakdown Voltage Limitations
- Long Term Reliability Trends

RF Device Technologies for Low Power
- Leakage, Carrier Mobility, Flicker Noise, etc.

Summary

RF Device Technologies

Instructor: *David Harame*
IBM, Essex Junction, VT

Introduction

RF CMOS
- MOSFET Optimization for RF/Analog
- Bulk and SOI
- CMOS Scaling (High-k, L=65nm & Beyond, etc)

SiGe BiCMOS
- SiGe HBT Basics
- Bipolar Device Optimization for RF/Analog

III-V Devices
- GaAs and InP HBTs

Active Device Comparisons
- Performance Matrix
- Figures of Merit

Advance in On-Chip Passives
- Resistors, Capacitors, and Inductors

Other RF Device Characteristics
- Microstrip and Coplanar
- Parasitics
- Substrate Isolation

RF MEMS
- Filters and Switches

Summary and Conclusions

Compact Device Modeling for RF Circuit Design

Instructor: *Michael Schroter*
University of Technology, Dresden, Germany

Introduction
- Why Compact Modeling
- Requirements

Bipolar Transistors
- Important Physical Effects
- Physics-Based Equivalent Circuit
- Basic Concept of An Advanced Compact Model

MOS Transistors
- Analog vs. Digital Model
- Important High-Frequency Effects
- Equivalent Circuit Extensions For High-Frequency Operation

Parasitic Effects
- Substrate Coupling
- Electrothermal Effects
- Device Interconnect and Pads

RF Passive Devices Modeling
- Resistors
- Capacitors/Varactors
- Transmission Lines
- Inductors

RF Device Modeling Issues and Challenges

Summary and Conclusions

Circuits Design for RF Communication Systems

Instructor: Domine Leenaerts
Philips Research Labs, Eindhoven, The Netherlands

Introduction

RF Frequency Synthesizer
- Specification
- Design
- Layout Considerations
- Circuit Performance

Single Chip Radio
- Impedance Matching
- Packaging
- ESD for RF Circuits
- Baseband/Analog/RF Integration
- Bluetooth Example

Direct Conversion Transceivers
- Intermodulation Distortion
- DC Offset Cancellation
- I/Q Generation
- UMTS/WCDMA Example
- 802.11a/b Example

Summary

SHORT COURSE: The Future of Semiconductor Manufacturing

Sunday, December 8, 9:00 a.m. – 5:30 p.m.
Continental Ballrooms 6-9

Course Organizer: Jack Y.C. Sun
TSMC, Hsin-Chu, Taiwan

In the last decade the semiconductor industry pulled off an impressive acceleration of Moore's law from 0.7um to the 130nm generation, with wafer size transitioning to 300mm, gate length scaled to 70nm, and the introduction of new materials such as nitrided oxide, cobalt silicide, copper metallization, low-k dielectric, and SOI. The cost of a fab, measured once in the millions of dollars is now measured in the billions. Integrated device manufacturers continue to drive bit density and frequency at a rapid pace, while foundries – with the economies of scale – have become an important part of the semiconductor industry by providing advanced process technologies and manufacturing services to fabless design houses, system companies, and even some integrated manufacturers. The absorption of new technologies and materials continues apace, and is a significant challenge to semiconductor manufacturing in the coming decade. Now the industry must overcome the rapidly approaching "red brick wall" of conventional CMOS scaling by pushing the limits and inserting emerging device structures and materials into manufacturing wherever possible and required. The industry must also be prepared to yield multi-GHz, multi-Gbit, and complex SoC chips with billions of transistors, miles of multi-layer interconnect wires, and new packaging where ppb level of defects and escalating manufacturing costs must be dealt with. This short course will address the opportunities and challenges of the future of semiconductor manufacturing. The lecturers will share their experience, vision, and insight in process technology and manufacturing.

The first lecture provides an overview of the future of semiconductor manufacturing, including business and application trends,

technology trend, the challenges of new modules and emerging device architectures, and technology transfer and ramp. The second lecture covers the trend and challenges of front end manufacturing technology and process modules, in particular, device scaling, gate dielectric, and lithography. The third lecture addresses the trend, challenges, and potential solutions of backend technology, process modules, and packaging. The state of the art 300mm manufacturing and future directions will be covered in the fourth lecture, including product-driven requirements, equipment, facilities, CIM, safety, and cost. Last but not the least in the fifth lecture, both process and design aspects of yield and reliability improvement for future semiconductor manufacturing will be covered, including challenges, methodology, models, tools, vehicles, and potential solutions.

Introduction

Instructor: Jack Y.C. Sun
TSMC, Hsin-Chu, Taiwan

Overview of Semiconductor Manufacturing

Instructor: Bruce Sohn
Intel Corporation, Rio Rancho, New Mexico

Worldwide Semiconductor Business Trends
- Logic, Memory, Communications
- IDM and Foundry Trends
- Moore's Law and the ITRS

New Technology Challenges
- New Materials: Dielectrics, SOI
- New Device Architectures
- Lithography Roadmap
- Advanced Process Control

Manufacturing Expertise & Supply Chain Management
- Scale: Capacity, Transfer and Ramp
- Design and Development for Manufacturability
- Transfer and Copy Exactly!
- Agility: Customer and Market Responsiveness
- Shrink and Enhancement
- Equipment and Materials Supply Lines
- Operational Excellence: Safety, Quality, Speed, Cost

Conversion to 300mm
- Cost, Productivity and Environmental Improvements
- Integrated Fab Design
- Automation: Mechanization and E-Manufacturing

Summary

Front End Manufacturing Technology

Instructor: Allen Bowling
Texas Instruments, Dallas, Texas

Transistor Performance Trends
- Microprocessor
- DSP

Transistor Scaling Challenges
- Isolation: Minimum Pitch and SOI

Gate Stack: Gate Dielectric - Leakage vs. Speed
Gate Electrode: Mid Gap vs. Dual Work Function Electrode
Ultra-Shallow Junction: Low Resistance Highly Abrupt Extensions

New Device Architectures
Ultra Thin Body
Double Gate Structures: FinFET, Pi-gate, etc
Other Devices: Quantum, Strained Silicon

New Front End Materials & Modules
Substrates SOI (GOI, SGOI, etc.), Strained Si, 450 mm Wafers
Gate Dielectrics: Oxide, Nitrided Oxide, High-K
Gate Electrodes: SiGe, Metal (Mid-Gap, Dual Metal, Single Metal)
UTB (SOI, SiGe): SOI Layer Thickness Control
Ultra-Shallow Junctions: Raised S/D
Gate Stack Etch and Clean

Lithography Trends
Gate CD Control
Isolation Requirements

Die Size/Circuit Complexity
Economics of 450 mm Wafers

Summary

Back End Manufacturing Technology

Instructor: N. Kobayashi
SELETE, Tsukuba, Japan

Interconnect Scaling Trends
Effective K, Resistance, Number of Interconnect Layers
Technology Requirements to Meet ITRS Roadmap
Impact of Interconnect Delay on Chip Performance

Technology Challenges for 65nm Back End
Present Backend Cu/LowK Process
Advanced Cu Electroplating amd CVD Barrier Technology
Low k ILD, Optimization for Low Keff, Role of Diffusion Barrier

New ILD Materials
Porous Low k Materials
Organic Polymer Materials
Impact of Weak Mechanical Strength

Integration Challenges
Lithography, Etch and CMP
Effect on Front End
Packaging

Reliability and Cost
Cu Reliability
Process Cost of Increasing Number of Layers

Summary

300mm Manufacturing

Instructor: J.J. Lin
TSMC, Hsin-Chu, Taiwan

Overview of 300mm Logic and DRAM Equipment
MPU, DRAM, ASIC, xPU, etc.
300mm Equipment Differences and Challenges
Process Scaling/Uniformity,
Litho, Thermal, CVD, Wet/Dry Etch, Thin Film, Epi, ...
Metrology
Throughput
Tool Reliability
Wafer Handling
300mm Fab
Fab Design,
Facilities and Supplies,
Factory Automation and CIM
Environmental and Safety
Development/Manufacturing Cost Projections and Reduction
Wafer/Mask
COO
Cost Reduction and Cross-Over Point
State of the Art 300mm Manufacturing
Future Directions
Summary

Yield & Reliability

Instructor: *P.K. Mozumder*
PDF Solutions, Richardson, TX

Challenges in Yield and Reliability
Yield Challenges in Sub-130nm Technologies
Reliability Issues in the Nanometer Era
Yield Learning Trends
Yield Improvement Opportunities
Taxonomy of Yield Improvement
Examples/Case Study
Tool and Techniques for Yield Improvement
Short and Full-Flow Test Vehicles
Characterization of Yield Loss Mechanisms
Yield Analysis Tools and Methods
Yield Monitoring and Maintenance
Process Based Yield Improvement
Defectivity Reduction
Optimizing Process Modules for Yield
Consumable Optimization
Design for Manufacturability
Functional Yield Improvement
Parametric Yield Improvement for Digital and Mixed Signal
Reliability Improvement and DFR (Design for Reliability)
Front End-of-Line
Back End-of-Line
Summary

Plenary Session

Monday, December 9, 9:00 a.m.
Grand Ballroom B

Welcome and Awards Presentation

General Chair: Shuji Ikeda, Trecenti Technologies

Invited Papers

Technical Program Chair: Leda Lunardi, JDS Uniphase Corporation

1.1 Lithography for Sub-100nm Applications, L. Van den hove, IMEC, Leuven, Belgium

Since the '60's lithography has enabled the ever continuing scaling, which has been the most important success factor for the entire semiconductor sector. This trend in further scaling will continue for at least another decade.

The lithography community is currently not only faced with increasing research expenditures related to concurrent development of many new lithography techniques such as the introduction of 157nm wavelength and next generation lithography techniques (EPL, EUVL, …), but because of delays with the introduction of these new techniques, current wavelengths have to be extended to future technology nodes, requiring unprecedented tool and infrastructure specifications. In addition, the narrowing down of various NGL techniques has taken a very long time and has required a lot of research efforts to sustain the required decisions.

In this presentation, we will be reviewing various lithography options for sub-100nm imaging. The technological status of 157nm will be discussed. Important breakthroughs have been realized during the last year. However, serious challenges remain (CaF_2 and pellicle availability). It will be demonstrated that next generation techniques, such as EUVL, also impose important technological challenges and may not be as easy as many proponents tend to suggest.

Hence, we believe that history will repeat itself and that current technologies, such as 193 nm lithography, will be used for patterning much smaller features than originally expected. Techniques to extend the use of current technologies, such as resolution enhancement techniques (RET) (Phase shifting masks, optical proximity correction, double exposure techniques, customized illumination technologies, …) and immersion lithography will be discussed and critical comparisons will be presented on the usefulness of these technologies for certain applications.

1.2 Chip Technologies For Entertainment Robots: Present and Future, T. Makimoto and T.T. Doi, Sony Corporation

The historical background, current status and future prospect of the entertainment robots will be reviewed and the critical roles played by the chip technologies, including processor performance, sensing capability and actuator elements, will be discussed.

The entertainment robots were developed and introduced to the market in late 1990's. Sony's AIBO, a dog-like entertainment robot, was the first of this kind and was sold through internet channels in 1999. The biped humanoid robots have also been developed and will be introduced to the market in the not too distant future. Examples of the latest development in this field will be demonstrated including Sony's SDR-4X which was developed in 2002.

The entertainment robots will keep providing never ending challenges for the chip engineers and will become a new "technology driver" in the coming decades.

1.3 Photonic Bandgap Based Designs for Photonic Integrated Circuits, E. Yablonovitch, University of California, Los Angeles, Los Angeles, CA

Photonic Crystals, the electromagnetic analog of semiconductor crystals, have stirred the imagination toward photonic integrated circuits. At the same time, the build-out of the telecommunications infrastructure is creating a demand for large volumes of optical communications components and sub-systems. Integration at the tiniest scale of photonic crystals allows the largest number of components to be produced from a single wafer, reducing cost, and allowing considerable optical complexity.

There have been a series of practical difficulties standing in the way of building practical micro-photonic circuits, that are gradually being solved; including, the input/output coupling efficiency problem, the nano-fabrication accuracy problem, the active device issues, electrical modulation schemes, device design software and simulation. Some of these problems are already solved, and we can project solutions to the others over the next few years.

Session 2: CMOS Devices — Transport and Mobility Enhancements

Monday, December 9, 1:30 p.m.
Grand Ballroom A

Co-Chairs: Malgorzata Jurczak, IMEC
Jack Kavalieros, Intel Corporation

1:30 p.m.
Introduction

1:35 p.m.
2.1 Strained Silicon MOSFET Technology (Invited), J. Hoyt, G. Xia, S. Eguchi, T. Drake, H. Nayfeh, E. Fitzgerald, D. Antoniadis, Massachusetts Institute of Technology, Cambridge, MA

2:00 p.m.
2.2 Novel Locally Strained Channel Technique for High Performance 55nm CMOS, K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto and Y. Inoue, Mitsubishi Electric Corporation, Hyogo, Japan

2:25 p.m.
2.3 Design for Scaled Thin Film Strained-SOI CMOS Devices with Higher Carrier Mobility, T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, T. Maeda and S. Takagi, ASET, Kawasaki, Japan

2:50 p.m.
2.4 Low-Frequency Noise Characteristics in SiGe Channel Heterostructure Dynamic Threshold pMOSFET (HDTMOS), A. Asai, J. Sato-Iwanaga, A. Inoue, Y. Hara, Y. Kanzawa, H. Sorada, T. Kawashima, T. Ohnishi, T. Takagi and M. Kubo, Matsushita Electric Industrial Co., Ltd., Osaka, Japan

3:15 p.m.
2.5 Temperature Experiment for Extracting Channel Backscattering Coefficients in Nanoscale MOSFETs, M.-J. Chen and K.-C. Huang, National Chiao-Tung University, Hsin-Chu, Taiwan, ROC

3:40 p.m.
2.6 Low Field Mobility Characteristics of Sub-100nm Unstrained and Strained Si MOSFETs, K. Rim, S. Narasimha*, M. Longstreet*, A. Mocuta* and J. Cai, IBM T.J. Watson Research Center, Yorktown Heights, NY and *IBM Microelectronics, Hopewell Junction, NY

4:05 p.m.
2.7 Experimental Study on Carrier Transport Mechanism in Ultrathin-body SOI n- and p-MOSFETs with SOI Thickness less than 5 nm, K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata and S. Takagi, Toshiba Corporation, Yokohama, Japan

4:30 p.m.
2.8 Examination of Hole Mobility in Ultra-thin Body SOI MOSFETs, Z. Ren, P. Solomon*, T. Kanarsky, B. Doris, O. Dokumaci, P. Oldiges, R. Roy*, E. Jones*, M. Ieong, R. Miller*, W. Haensch*, and H.-S.P. Wong*, IBM Microelectronics, Hopewell Junction, NY and *IBM TJ Watson Research Center, Yorktown Heights, NY

Session 3: Integrated Circuits and Manufacturing — Sub-100nm Logic Technology

Monday, December 9, 1:30 p.m.
Grand Ballroom B

Co-Chairs: S.C. Sun, Chartered Semiconductor
Witek Maszara, AMD

1:30 p.m.
Introduction

1:35 p.m.
3.1 65nm CMOS Technology (CMOS5) with High Density Embedded Memories for Broadband Microprocessor Applications, N. Yanagiya, S. Matsuda, S. Inaba, M. Takayanagi, I. Mizushima, K. Ohuchi, K. Okano, K. Takahasi, E. Morifuji, M. Kanda, Y. Matsubara, M. Habu, M. Nishigori, K. Honda, H. Tsuno, K. Yasumoto, T. Yamamoto, K. Hiyama, K. Kokubun, T. Suzuki, J. Yoshikawa, T. Sakurai, T. Ishizuka, Y. Shoda, M. Moriuchi, S. Kishida, H. Harakawa, H. Oyamatsu, N. Nagashima*, S. Yamada, T. Noguchi, Y. Okamoto* and M. Kakumu, Toshiba Corporation, Yokohama, Japan and *Sony Corporation, Yokohama, Japan

2:00 p.m.
3.2 A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 layers of Cu Interconnects, Low k ILD, and 1 μm^2 6-T SRAM Cell, S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber and M. Bohr, Intel Corporation, Hillsboro, OR

2:25 p.m.
3.3 A 90-nm CMOS Device Technology with High-Speed, General-Purpose, and Low-Leakage Transistors for System on Chip Applications, C.C. Wu, C.S. Chang, Y.K. Leung, H.T. Huang, D.W. Lin, Y.M. Sheu, W.J. Liang, C.H. Hsieh, L.K. Han, S.Y. Wu, S.S. Lin, H.C. Lin, C.H. Wang, M.H. Tsai, T.L. Lee, C.Y. Fu, C.W. Chang, S.C. Chen, S.M. Jang, S.L. Shue, C.H. Diaz, M.S.Liang, Y.J. Mii and Y.C. Sun, TSMC, Taiwan, ROC

2:50 p.m.
3.4 50nm Gate Length Logic Technology with 9-Layer Cu Interconnects for 90nm Node SoC Applications, Y.W. Kim, C.B. Oh, Y.G. Ko, K.T. Lee, J.H. Ahn, T.S. Park, H.S. Kang, D.H. Lee, M.K. Jung, H.J. Yu, K.S. Jung, S.H. Liu, B.J. Oh, K.S. Kim, G.J. Bae, W.S. Song, C.H. Jeon and K.P. Suh, Samsung Electronics, Kyounggi-Do, Korea

3:15 p.m.
3.5 A 90 nm Communication Technology Featuring SiGe HBT Transistors, RF CMOS, Precision R-L-C RF Elements and 1 μm^2 6-T SRAM Cell, K. Kuhn, M. Agostinelli, S. Ahmed, S. Chambers, S. Cea, S. Christensen, P. Fischer, J. Gong, C. Kardas, T. Letson, L. Henning, A. Murthy, H. Muthali, B. Obradovic, P. Packan, S.W. Pae, I. Post, S. Putna, K. Raol, A. Roskowski, R. Soman, T. Thomas, P. Vandervoorn, M. Weiss and I. Young, Intel Corporation, Hillsboro, OR

3:40 p.m.
3.6 High Performance Copper and Low-k Interconnect Technology Fully Compatible to 90nm-node SOC Application (CMOS4), M. Inohara, I. Tamura, T. Yamaguchi, H. Koike, Y. Enomoto*, S. Arakawa, T. Watanabe, E. Ide, S. Kadomura* and K. Sunouchi, Toshiba Corporation, Kanagawa, Japan and *Sony Corporation, Kanagawa, Japan

Session 4: Quantum Electronics and Compound Semiconductors — High Speed, Quantum, and Opto-Electronics

Monday, December 9, 1:30 p.m.
Continental Ballrooms 1-3

Co-Chairs: *Barbara Landini, Kopin Corporation*
Michael Schlechtweg, Fraunhofer Institute IAF

1:30 p.m.
Introduction

1:35 p.m.
4.1 High Speed HBTs and OEICs (Invited), H. Jäckel, U. Hammer, J. Ruiz, I. Schnyder, V. Schwarz, M. Gaspar*, D. Huber*, M. Rohner** and A. Huber***, Swiss Federal Institute of Technology, Zurich, Switzerland, *Optospeed SA, Rüschlikon, Switzerland, **Leica Geosystems, Heerbrugg, Switzerland and ***Zentrum fur Mikroelektronik, Windisch, Switzerland

2:00 p.m.
4.2 Single Photons and Entangled Photons from a Quantum Dot (Invited), J. Vuckovic, C. Santori, D. Fattal, M. Pelton, G. Solomon, B. Zhang, J. Plant and Y. Yamamoto, Stanford University, Stanford, CA

2:25 p.m.
4.3 High Efficient 820 nm MOS Ge Quantum Dot Photodetectors for Short-Reach Integrated Optical Receivers with 1300 and 1550 nm Sensitivity, B.-C. Hsu, S.T. Chang, C.-R. Shie, C.-C. Lai, P.S. Chen* and C.W. Liu, National Taiwan University, Taiwan, R.O.C and *ERSO/ITRI, Taiwan, R.O.C.

2:50 p.m.
4.4 Experimental Demonstration of a QCA Shift Register and Analysis of Errors, R. Kummamuru, A. Orlov, R. Ramasubramaniam, C. Lent, G. Bernstein and G. Snider, University of Notre Dame, Notre Dame, IN

3:15 p.m.
4.5 Novel Light Emitting Device with Ultrafast Color Switching, R. Koudelka, J. Woodall and E. Harmon*, Yale University, New Haven, CT and *LightSpin Technologies, Inc., Norfolk, MA

3:40 p.m.
4.6 Degradation Mechanisms of GaN-Based LEDs After Accelerated DC Current Aging, G. Meneghesso, S. Levada, R. Pierobon, F. Rampazzo, E. Zanoni, A. Cavallini*, A. Castaldini*, G. Scamarcio**, S. Du*** and I. Eliashevich***, University of Padova, Padova, Italy, *University of Bologna, Bologna, Italy, **University of Bari, Bari, Italy and ***GELcore LLC, Valley View, OH

Session 5: Modeling and Simulation — Compact Modeling

Monday, December 9, 1:30 p.m.
Continental Ballroom 4

Co-Chairs: Ronald van Langevelde, Philips Research Laboratories
Rafael Rios, Intel Corporation

1:30 p.m.
Introduction

1:35 p.m.
5.1 HiSIM: A MOSFET Model for Circuit Simulation Connecting Circuit Performance with Technology (Invited), M. Miura-Mattausch, H. Ueno, M. Tanaka, H. J. Mattausch, S. Kumashiro*, T. Yamaguchi**, K. Yamashita* and N. Nakayama*, Hiroshima University, Higashi-Hiroshima, Japan and *Semiconductor Technology Academic Research Center, Kanagawa, Japan

2:00 p.m.
5.2 A Three-Transistor Threshold Voltage Model for Halo Processes, R. Rios, W.-K. Shih, A. Shah, S. Mudanai, P. Packan, T. Sandford and K. Mistry, Intel Corp., Hillsboro, OR

2:25 p.m.
5.3 Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance, R.A. Bianchi, G. Bouche and O. Roux-dit-Buisson, STMicroelectronics, Crolles, France

2:50 p.m.
5.4 The Effective Drive Current in CMOS Inverters, M.H. Na, E. Nowak, W. Haensch* and J. Cai*, IBM Corporation, Essex Junction, VT and *IBM T.J. Watson Research Center, Yorktown Heights, NY

3:15 p.m.
5.5 Scattering Matrix Based Compact MOSFET Model, H. Wang and G. Gildenblat, The Pennsylvania State University, University Park, PA

3:40 p.m.
5.6 Compact Modeling of Drain and Gate Current Noise for RF CMOS, A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, V. Venezia, A. Zegers-van Duijnhoven, B. Neinhüs*, C. Jungemann* and D. Klaassen, Philips Research Laboratories, Eindhoven, The Netherlands and *University of Bremen, Bremen, Germany

4:05 p.m.
5.7 Compact Modelling of Cyclostationary Noise in Semiconductor Devices: A Critical Discussion, F. Bonani, S. Donati Guerrieri and G. Ghione, Politecnico di Torino, Torino, Italy

4:30 p.m.
5.8 A New, Closed-form Compact Model for the Cyclostationary Noise and LS Conversion Behaviour of RF Junction Diodes, F. Bonani, S. Donati Guerrieri and G. Ghione, Politecnico di Torino, Torino, Italy

Session 6: CMOS and Interconnect Reliability — Dielectric Degradation and Breakdown

Monday, December 9, 1:30 p.m.
Continental Ballroom 5

Co-Chairs: Robin Degraeve, IMEC
Kenji Okada, Matsushita Electric Industrial Co., Ltd.

1:30 p.m.
Introduction

1:35 p.m.
6.1 Correlated Defect Generation in Thin Oxides and Its Impact on Flash Reliability, D. Ielmini, A. Spinelli*, A. Lacaita and M. van Duuren**, Politecnico di Milano, Milano, Italy and *Universita degli Studi dell'Insubria, Como, Italy and **Philips Research Leuven, Leuven, Belgium

2:00 p.m.
6.2 Statistics of Successive Breakdown Events for Ultra-thin Gate Oxides, J. Suñé and E. Wu*, Universitat Autonoma de Barcelona, Bellaterra, Spain and *IBM Microelectronics Division, Essex Junction, VT

2:25 p.m.
6.3 Statistically Independent Soft Breakdowns Redefine Oxide Reliability Specifications, M. Alam, R. Smith, B. Weir and P. Silverman, Agere Systems, Murray Hill, NJ

2:50 p.m.
6.4 A New Model of Time Evolution of Gate Leakage Current after Soft Breakdown in Ultra-Thin Gate Oxides, T. Hosoi, P.L. Ré, Y. Kamakura and K. Taniguchi, Osaka University, Osaka, Japan

3:15 p.m.
6.5 Spectroscopic Analysis of Trap Assisted Tunneling in Thin Oxides by Means of Substrate Hot Electron Injection Experiments, F. Driussi, R. Iob, D. Esseni, L. Selmi, R. van Schaijk* and F. Widdershoven*, DIEGM, Udine, Italy and *Philips Research Leuven, Leuven, Belgium

3:40 p.m.
6.6 Dielectric Breakdown Induced Epitaxy in Ultrathin Gate Oxide – A Reliability Concern, K. Pey, C.H. Tung*, M. Radhakrishnan*, L.J. Tang* and W.H Lin**, Nanyang Technological University, Singapore and *Institute of Microelectronics, Singapore and **Chartered Semiconductor Manufacturing Ltd., Singapore

4:05 p.m.
6.7 Drain-Accelerated Degradation of Tunnel Oxides in Flash Memories, A. Chimenton, A. Spinelli*, D. Ielmini**, A. Lacaita**, A. Visconti*** and P. Olivo, Universita degli Studi de Ferrara, Ferrara, Italy, *Universita degli Studi dell'Insubria, Como, Italy, **Politecnico di Milano, Milano, Italy and ***STMicroelectronics, Agrate Brianza, Italy

4:30 p.m.
6.8 Observation of Hot-Carrier-Induced nFET Gate-Oxide Breakdown in Dynamically Stressed CMOS Circuits, B. Kaczer, F. Crupi*, R. Degraeve, Ph. Roussel, C. Ciofi* and G. Groeseneken, IMEC, Leuven, Belgium and *Universita degli Studi di Messina, Messina, Italy

Session 7: Solid State Devices — Nanoelectronics and Novel Memories

Monday, December 9, 1:30 p.m.
Continental Ballroom 6

Co-Chairs: *Sandip Tiwari, Cornell University*
Junji Koga, Toshiba Corporation

1:30 p.m.
Introduction

1:35 p.m.
7.1 Single-Electron Random-Number Generator (RNG) for Highly Secure Ubiquitous Computing Applications, K. Uchida, T. Tanamoto, R. Ohba, S. Yasuda and S. Fujita, Toshiba Corporation, Yokohama, Japan

2:00 p.m.
7.2 Effects of Ultra-Narrow Channel on Characteristics of MOSFET Memory with Silicon Nanocrystals Floating Gates, M. Saitoh, E. Nagata and T. Hiramoto, University of Tokyo, Tokyo, Japan

2:25 p.m.
7.3 Quantum-Well Memory Device (QWMD) with Extremely Good Charge Retention, Z. Krivokapic, T. Krishnamohan*, A. Halliyal, A. Jafarpour, S. Cherian, A. Holbrook, W. Zheng and M. Randolph, AMD, Sunnyvale, CA and *Stanford University, Stanford, CA

2:50 p.m.
7.4 Silicon-Rich-Oxides as an Alternative Charge-Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells, M. Rosmeulen*, E. Sleeckx and K. De Meyer*, IMEC, Leuven, Belgium and *IMEC and KU Leuven, Leuven, Belgium

3:15 p.m.
7.5 Novell Colossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory (RRAM), W. W. Zhuang, W. Pan, B.D. Ulrich, J.J. Lee, L. Stecker, A. Burmaster, D.R. Evans, S.T. Hsu, M. Tajiri*, A. Shimaoka*, K. Inoue*, T. Naka*, N. Awaya*, K. Sakiyama*, Y. Wang**, S.Q. Liu**, N.J. Wu**, and A. Ignatiev**, Sharp Laboratories of America, Camas, WA and *Sharp Corporation, Nara, Japan and **University of Houston, Houston, TX

Session 8: Detectors, Sensors and Displays — Recent Advances in Inertial and Biological MEMs

Monday, December 9, 1:30 p.m.
Continental Ballrooms 7-9

Co-Chairs: Jack Judy, UCLA
Benedetto Vigna, STMicroelectronics

1:30 p.m.
Introduction

1:35 p.m.
8.1 Recent Progress in Modularly Integrated MEMS Technologies (Invited), T.-J. King, R. Howe and S. Sedky*, University of California, Berkeley, CA and *The American University in Cairo, Cairo, Egypt

2:00 p.m.
8.2 Integrated Surface-Micromachined Z-axis Frame Microgyroscope, M. Palaniapan, R. Howe and J. Yasaitis*, University of California, Berkeley, CA and *Analog Devices, Inc., Cambridge, MA

2:25 p.m.
8.3 A Self-Assembly Conductive Device for Direct DNA Identification in Integrated Microarray Based System, M. Xue, J. Li*, W. Xu, Z. Lu*, P.K. Ko and M. Chan, Hong Kong University of Science and Technology, Hong Kong and *Southeast University, Nanjing, China PR

2:50 p.m.
8.4 A DNA Prism: The Physical Principles for Optimizing a Microfabricated DNA Separation Device, L.R. Huang, J. Tegenfeldt, J. Sturm, R. Austin and E.C. Cox, Princeton University, Princeton, NJ

3:15 p.m.
8.5 **Amorphous Silicon Pixel Amplifier with ΔV_T Compensation for Low Noise Digital Fluoroscopy**, K.S. Karim, A. Nathan, J. Rowlands*, University of Waterloo, Ontario, Canada and *University of Toronto, Ont., Canada

Session 9: Process Technology — Memories and Passive Components

Monday, December 9, 1:30 p.m.
Imperial Room

Co-Chairs: *U-In Chung, Samsung Electronics Co. Ltd.*
Pierre Bouillon, STMicroelectronics

1:30 p.m.
Introduction

1:35 p.m.
9.1 **Mass Production Worthy HfO_2-Al_2O_3 Laminate Capacitor Technology using Hf Liquid Precursor for Sub-100nm DRAMs**, J.-H. Lee , J. P. Kim, Y.-S. Kim, H.-S. Jung, N.-I. Lee, H.-K. Kang, K.-P. Suh, M.-M. Jeong, K.-T. Hyun, H.-S. Baik, Y.-S. Chung, H.-Y. Kim*, N.K. Lee*, X. Liu*, J. Winkler*, A. Londergan*, S. Ramanathan* and T. Seidel*, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea and *Genus, Inc., Sunnyvale, CA

2:00 p.m.
9.2 **Niobia-Stabilized Tantalum Pentoxide (NST) - Novel High-k Dielectrics for Low-Temperature Process of MIM Capacitors**, Y. Matsui, M. Hiratani, I. Asano* and S. Kimura, Hitachi, Ltd., Tokyo, Japan and *Elpida Memory, Inc., Kanagawa, Japan

2:25 p.m.
9.3 **Mass-Productive Ultra-Low Temperature ALD SiO_2 Process Promising for Sub-90nm Memory and Logic Devices**, J.-E. Park, J.-W. Lee, J.-H. Yang, K.-S. Chu, S.-H. Lee, J.-H. Ku, M.-H. Park, H.-K. Kang and K.-P. Suh, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea

2:50 p.m.
9.4 **Novel Shallow Trench Isolation Process Using Flowable Oxide CVD for Sub-100nm DRAM**, S.-W. Chung, S.-T. Ahn, S.-D. Lee, J.-S. Rhee, J. Ku, S. Park, Y.-W. Song, H.-S. Park and H.-C. Sohn, Hynix Semiconductor Inc., Kyoungki-do, Korea

3:15 p.m.
9.5 **Highly Reliable MONOS Devices with Optimized Silicon Nitride Film Having Deuterium Terminated Charge Traps**, M. Tanaka, S. Saida, Y. Mitani, I. Mizushima and Y. Tsunashima, Toshiba Corporation, Kanagawa, Japan

3:40 p.m.
9.6 Characterization and Comparison of Two Metal-Insulator-Metal Capacitor Schemes in 0.13 µm Copper Dual Damascene Metallization Process for Mixed-Mode and RF Applications, C.H. Ng, K.W. Chew, J.X. Li, T.T. Tjoa, L.N. Goh and S-.F. Chu, Chartered Semiconductor Manufacturing Ltd., Singapore

Session 10: CMOS Devices — Advanced Ultrathin-Body Devices

Tuesday, December 10, 9:00 a.m.
Grand Ballroom A

Co-Chairs: *Jack Hergenrother, Agere Systems*
Yasuo Yamaguchi, Mitsubishi Electric Corporation

9:00 a.m.
Introduction

9:05 a.m.
10.1 Metal-Gate FinFET and Fully-Depleted SOI Devices Using Total Gate Silicidation, J. Kedzierski, E. Nowak*, T. Kanarsky**, Y. Zhang, D. Boyd**, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong**, D. Canaperi, M. Krishnan, K.-L. Lee, B.A. Rainey*, D. Fried*, P. Cottrell*, H.-S.P. Wong, M. Ieong** and W. Haensch, IBM SRDC, Yorktown Heights, NY, *IBM Microelectronics, Essex Junction, VT and ** IBM Microelectronics, Hopewell Junction, NY

9:30 a.m.
10.2 FinFET Scaling to 10nm Gate Length, B. Yu, L. Chang*, S. Ahmed, H. Wang, S. Bell, C-Y Yang, C. Tabery, C. Ho, Q. Xiang, T-J King*, J. Bokor*, C. Hu*, M-R. Lin and D. Kyser, AMD, Inc., Sunnyvale, CA and *University of California, Berkeley, CA

9:55 a.m.
10.3 25nm CMOS Omega FETs, F.-L. Yang, H.-Y. Chen, F.-C. Chen, K.-N. Yang, Y.-L. Chan, M. Tang, C.-C. Huang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, M.-S. Liang and C. Hu, Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan, ROC

10:20 a.m.
10.4 FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering, Y.-K. Choi, L. Chang, P. Ranade, J. Lee, D. Ha, S. Balasubramanian, A. Agarwal*, T.-J. King and J. Bokor, University of California, Berkeley, CA and *Axcelis Technologies, Beverly, MA

10:45 a.m.
10.5 SON (Silicon-On-Nothing) P-MOSFETs with Totally Silicided ($CoSi_2$) Polysilicon on 5nm-Thick Si-Films: The Simplest Way to Integration of Metal Gates on Thin FD Channels, S. Monfray*, T. Skotnicki, B. Tavel*, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, C. Jenny, P. Mazoyer, R. Palla, F. Leverd, Y. Le Friec, R. Pantel, M. Haond, C. Charbuillet, C. Vizioz**, D. Louis** and N. Buffet**, STMicroelectronics, Crolles, France and *STMicroelectronics, Crolles, France and France Telecom, Meylan, France and **CEA LETI, Grenoble, France

11:10 a.m.
10.6 Extreme Scaling With Ultra-Thin Silicon Channel MOSFET's (XFET), B. Doris, M. Ieong, T. Kanarsky, Y. Zhang*, R.A. Roy*, O. Dokumaci, F.-F. Jamin, L. Shi*, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, M. Gribelyuk, E.C. Jones*, R. J. Miller*, H.-S.P. Wong* and W. Haensch*, IBM Microelectronics, Hopewell Junction, NY and *IBM T.J. Watson Research Center, Yorktown Heights, NY

11:35 a.m.
10.7 Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage, Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, E. Zhao, J. Zhang, J. Chan, A. Marathe and M.-R. Lin, AMD, Sunnyvale, CA

12:00 p.m.
10.8 Fully Depleted Surrounding Gate Transistor (SGT) for 70nm DRAM and Beyond, B. Goebel, J. Lützen, D. Manger, P. Moll, K. Mümmler, M. Popp, U. Scheler, T. Schlösser, H. Seidl, M. Sesterhenn, S. Slesazeck and S. Tegen, Infineon Technologies, Dresden, Germany

Session 11: Solid State Devices — Novel Devices

Tuesday, December 10, 9:00 a.m.
Continental Ballrooms 1-3

Co-Chairs: Thomas Skotnicki, STMicroelectronics
Andrea Lacaita, Politecnico di Milano

9:00 a.m.
Introduction

9:05 a.m.
11.1 Carbon Nanotube Electronics (Invited), P. Avouris, J. Appenzeller, V. Derycke, R. Martel and S. Wind, IBM T.J. Watson Research Center, Yorktown Heights, NY

9:30 a.m.
11.2 Short-Channel Like Effects in Schottky Barrier Carbon Nanotube Field-Effect Transistors, J. Appenzeller, J. Knoch*, R. Martel, V. Derycke, S. Wind and P. Avouris, IBM T.J. Watson Research Center, Yorktown Heights, NY and *Massachusetts Institute of Technology, Cambridge, MA

9:55 a.m.
11.3 I-MOS: A Novel Semiconductor Device with a Subthreshold Slope Lower than kT/q, K. Gopalakrishnan, P.B. Griffin and J. Plummer, Stanford University, Stanford, CA

10:20 a.m.
11.4 Polymeric Integrated Circuits: Fabrication and First Characterisation (Invited), D.M. de Leeuw, G. Gelinck, T. Geuns, E. van Veenendaal, E. Cantatore and B. Huisman, Philips Research Laboratories, Eindhoven, The Netherlands

10:45 a.m.
11.5 High Efficient 850nm and 1310nm Multiple Quantum Well SiGe/Si Heterojunction Phototransistors with 1.25 Plus GHz Bandwith, Z. Pei, C.S. Liang, L.S. Lai, Y.T. Tseng, Y.M. Hsu, P.S. Chen, S.C. Lu, C.M. Liu, M.-J. Tsai and C.W. Liu, Electronics Research and Service Organization, Hsinchu, Taiwan R.O.C

Session 12: Modeling and Simulation — Device Fluctuations and Interconnect Modeling

Tuesday, December 10, 9:00 a.m.
Continental Ballroom 4

Co-Chairs: *Kenji Nishi, Selete*
Christoph Wasshuber, Texas Instruments

9:00 a.m.
Introduction

9:05 a.m.
12.1 Determination of the Line Edge Roughness Specification for 34 nm Devices, T. Linton, M. Chandhok*, B.J. Rice* and G. Schrom*, Intel Corporation, Santa Clara, CA and *Hillsboro, OR

9:30 a.m.
12.2 Line Edge Roughness: Characterization, Modeling and Impact on Device Behavior, J.A. Croon, G. Storms, S. Winkelmeier*, I. Pollentier, M. Ercken, S. Decoutere, W. Sansen** and H.E. Maes, IMEC, Leuven, Belgium and * JSR Electronics, Leuven, Belgium and **K.U. Lueven, Leuven, Belgium

9:55 a.m.
12.3 Investigation of Realistic Dopant Fluctuation Induced Device Characteristics Variation for Sub-100nm CMOS by Using Atomistic 3D Process/Device Simulator, T. Ezaki, T. Ikezawa and M. Hane, NEC Corporation, Sagamihara, Japan

10:20 a.m.
12.4 An Effective Loop Inductance Model for General Non-orthogonal Interconnect with Random Capacitive Coupling, S.-P. Sim, C. Chao, S. Krishnan, D. Petranovic*, N. Arora**, K. Lee*** and C Y. Yang, Santa Clara University, Santa Clara, CA, *LSI Logic Corp., Milpitas, CA, **Simplex Solutions Inc., Sunnyvale, CA and ***KAIST, Taejon, Korea

10:45 a.m.
12.5 Optimal Global Interconnecting Devices for GSI, A. Naeemi and J.D. Meindl, Georgia Institute of Technology, Atlanta, GA

11:10 a.m.
12.6 Modelling and Analysis Of Power Dissipation in Single Electron Logic, S. Mahapatra, A.M. Ionescu, K. Banerjee* and M.J. Declercq, Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland and *University of California, Santa Barbara, CA

Session 13: CMOS and Interconnect Reliability — Soft Errors and ESD

Tuesday, December 10, 9:00 a.m.
Continental Ballroom 5

Co-Chairs: *Jose Maiz, Intel Corporation*
Charvaka Duvvury, Texas Instruments

9:00 a.m.
Introduction

9:05 a.m.
13.1 The Impact of Technology Scaling on Soft Error Rate Performance and Limits to the Efficacy of Error Correction (Invited), R. Baumann, Texas Instruments Inc., Dallas, TX

9:30 a.m.
13.2 Neutron-Induced Soft Errors, Latchup, and Comparison of SER Test Methods for SRAM Technologies, P. Dodd, M. Shaneyfelt, J. Schwank and G. Hash, Sandia National Laboratories, Albuquerque, NM

9:55 a.m.
13.3 Soft Errors in SRAM Devices Induced by High Energy Neutrons, Thermal Neutrons and Alpha Particles, H. Kobayashi, K. Shiraishi*, H. Tsuchiya*, H. Usuki**, Y. Nagai***, K. Takahisa***, T. Yoshiie#, Y. Sakurai# and T. Ishizaki#, Sony Corporation, Kanagawa, Japan, *Sony Corporation, Tokyo, Japan, **Sony Semiconductor Kyushu, Nagasaki, Japan, ***Osaka University, Osaka, Japan and #Kyoto University, Osaka, Japan

10:20 a.m.
13.4 Non-uniform Conduction Induced Reverse Channel Length Dependence of ESD Reliability for Silicided NMOS Transistors, K.-H. Oh, K. Banerjee*, C. Duvvury** and R.W. Dutton, Stanford University, Stanford, CA, *University of California, Santa Barbara, CA and **Texas Instruments, Dallas, TX

10:45 a.m.
13.5 Investigation of Thermal Distribution During Destructive Pulses in ESD Protection Devices Using a Single-Shot, Nanosecond Resolution, Two-Dimensional Interferometric Method, D. Pogany, S. Bychikhin, J. Kuzmik, V. Dubec, N. Jensen*, M. Denison*, G. Groos**, M. Stecher* and E. Gornik, Vienna University of Technology, Vienna, Austria, *Infineon Technologies, Munich, Germany and **University of the Federal Armed Forces Munich, Neubiberg, Germany

11:10 a.m.
13.6 A Fail-Safe ESD Protection Circuit with 230fF Linear Capacitance for High-Speed/High-Precision 0.18µm CMOS I/O Application, J. Lin, C. Duvvury, B. Haroun, I. Oguzman and A. Somayaji, Texas Instruments, Dallas, TX

Session 14: Process Technology — Metal Gate and FEOL Process Technology

Tuesday, December 10, 9:00 a.m.
Continental Ballroom 6

Co-Chairs: *Chris Auth, Intel Corporation*
Yoshitaka Tsunashima, Toshiba Corporation

9:00 a.m.
Introduction

9:05 a.m.
14.1 75nm Damascene Metal Gate and High-k Integration for Advanced CMOS Devices, B. Guillaumot, X. Garros, F. Lime**, K. Oshima*, B. Tavel***, J.A. Chroboczek***, P. Masson****, R. Truche*, A.M. Papon*, F. Martin*, J.F. Damlencourt*, S. Maitrejean*, M. Rivoire, C. Leroux*, S. Cristoloveanu**, G. Ghibaudo**, J.L. Autran****, T. Skotnicki and S. Deleonibus*, STMicroelectronics, Crolles, France and *CEA-Leti, Grenoble, France and **IMEP-ENSERG, Grenoble, France and ***Francetelecom RD Centre, Meylan, France and ****L2MP

9:30 a.m.
14.2 Tunable Work Function Dual Metal Gate Technology for Bulk and Non-Bulk CMOS, J.H. Lee, H. Zhong, Y.-S. Suh, G. Heuss, J. Gurganus, B. Chen and V. Misra, North Carolina State University, Raleigh, NC

9:55 a.m.
14.3 Tunable-Work-Function Molybdenum Gate Technology for FDSOI-CMOS, P. Ranade, Y.-K. Choi, D. Ha, A. Agarwal*, M. Ameen* and T.-J. King, University of California, Berkeley, CA and *Axcelis Technologies Inc., Beverly, MA

10:20 a.m.
14.4 Transistors with Dual Work Function Metal Gates by Single Full Silicidation (FUSI) of Polysilicon Gates, W. Maszara, Z. Krivokapic, P. King, J.-S. Goo and M.-R. Lin, AMD, Sunnyvale, CA

10:45 a.m.
14.5 A Novel Nickel SALICIDE Process Technology for CMOS Devices with Sub-40nm Physical Gate Length, J.P. Lu, D. Miles, J. Zhao, A. Gurba, Y. Xu, C. Lin, M. Hewson, J. Ruan, L. Tsung, R. Kuan, T. Grider, D. Mercer and C. Montgomery, Texas Instruments, Dallas, TX

11:10 a.m.
14.6 Advanced Source/Drain and Contact Technologies for Sub-70 nm CMOS (Invited), M. Öztürk, J. Liu, H. Mo and N. Pesovic, North Carolina State University, Raleigh, NC

11:35 a.m.
14.7 Sub-30 nm P^+ Abrupt Junction Formation in Strained Si/ $Si_{1-x}Ge_x$ MOS Device, K.L. Lee, J. Chu, J.Ott, H. Zhu*, P. Ronsheim*, P. Kozlowski, P. Saunders, F. Cardone, S. Koester and E.C. Jones, IBM T.J. Watson Research Center, Yorktown Heights, NY and *IBM Microelectronics Division, Hopewell Junction, NY

Session 15: Detectors, Sensors and Displays — Display and Field Emission Device

Tuesday, December 10, 9:00 a.m.
Continental Ballrooms 7-9

Co-Chairs: Shou-Gwo Wuu, TSMC
Man Wong, Hong Kong Univ. of Science & Technology

9:00 a.m.
Introduction

9:05 a.m.
15.1 Needs and Solutions of Future Flat Panel Display for IT Industry (Invited), K. Chung, C-W Kim and M.-P. Hong, Samsung Electronics Company, Suwon, Korea

9:30 a.m.
15.2 Ultra-Thin, High-Resolution, Flexible Electronic Ink Displays Addressed by a-Si Active-Matrix TFT Backplanes on Stainless Steel Foil, Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates and J. Goodman, E Ink Corporation, Cambridge, MA

9:55 a.m.
15.3 Temporal and Spatial Current Stability of the Integrated LD-MOSFET/ Field Emission Arrays, C.-Y. Hong and A. Akinwande, Massachusetts Institute of Technology, Cambridge, MA

10:20 a.m.
15.4 Organic Field Emission Device Integrated With Organic Transistor, I. Kymissis and A. Akinwande, Massachusetts Institute of Technology Microsystems Technology Laboratory, Cambridge, MA

10:45 a.m.
15.5 Field Electron Emission Device Using Silicon Nano-Wires, K. Sawada, M. Futagwa, Y. Arai, T. Kawano, H. Takao and M. Ishida, Toyohashi University of Technology, Toyohashi, Japan

Session 16: Integrated Circuits and Manufacturing — High Performance Embedded Technologies for SoC

Tuesday, December 10, 9:00 a.m.
Imperial Room

Co-Chairs: *Ranbir Singh, Agere Systems*
Coming Chen, UMC

9:00 a.m.
Introduction

9:05 a.m.
16.1 A High Performance 90nm SOI Technology with 0.992 μm^2 6T-SRAM Cell, M. Khare, S.K.H. Fung, R.A. Donaton, S. Greco, C. Brodsky, X. Chen, A. Chou, R. DellaGuardia, S. Deshpande, B. Doris, A. Gabor, M. Gribelyuk, S. Holmes, F. F. Jamin, S.H. Ku, W.L. Lai, W.H. Lee, Y. Li, P. McFarland, S. Mittl, R. Mo, W. Rausch, S. Sankaran, J. Snare, L. Tsou, A. Vayshenker, R. Viswanathan, D. Wehella-Gamag, S. Wu, T. Wagner, W. Yan, E. Barth, R. Ferguson, P. Gilbert, D. Schepis, A. Sekiguchi, R. Goldblatt, J. Welser, K.P. Muller and P. Agnello, IBM SRDC, Hopewell Junction, NY

9:30 a.m.
16.2 A Functional FinFET-DGCMOS SRAM Cell, E. Nowak, B. Rainey, D. Fried*, J. Kedzierski**, M. Ieong**, W. Leipold, J. Wright and M. Breitwisch, IBM Corporation, Essex Junction, VT, *Cornell University, Ithaca, NY and **IBM T.J. Watson Research Center, Yorktown Heights, NY

9:55 a.m.
16.3 A Highly Manufacturable High Density Embedded SRAM Technology for 90nm CMOS, Y. Fukaura, K. Kasai, Y. Okayama, H. Kawasaki, K. Isobe, M. Kanda, K. Ishimaru and H. Ishiuchi, Toshiba Corporation, Yokohama, Japan

10:20 a.m.
16.4 A Novel 0.79µm^2 SRAM Cell by KrF Lithography and High Performance 90nm CMOS Technology for Ultra High Speed SRAM, S.-M. Jung, H. Kwon, J. Jeong, W. Cho, S. Kim, H. Lim, K. Ko, Y. Rah, J. Park, H. Kang, G. Lyu, J. Park, C. Chang, Y. Jang, K. Kim and M.Y. Lee, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

10:45 a.m.
16.5 Manufacturable Embedded CMOS 6T-SRAM Technology with High-k Gate Dielectric Device for System-on-Chip Applications, H.S. Kang, C.B. Oh, H.J. Ryu, M.H. Oh, H.S. Jung, Y.S. Kim, J.H. Lee, N I. Lee, K.H. Cho, D.H. Lee, T.H. Yang, I.S. Cho, H.K. Kang, Y.W. Kim and K.P. Suh, Samsung Electronics, Kyoungi-Do, Korea

Luncheon Session

Tuesday, December 10, 12:20 p.m.
Grand Ballroom B

Luncheon Presentation: "Changing Vectors of Moore's Law,"
Andrew S. Grove

Andrew S. Grove was born in Budapest, Hungary in 1936. He graduated from the City College of New York in 1960 with a Bachelor of Chemical Engineering degree and received his Ph.D. from the University of California, Berkeley in 1963. Upon graduation, he joined the Research and Development Laboratory of Fairchild Semiconductor and became Assistant Director of Research and Development in 1967.

In July 1968, Dr. Grove participated in the founding of Intel Corporation. In 1979 he was named its President, and in 1987 he was named Chief Executive Officer. In May 1997 he was named Chairman and CEO, and in May 1998 he relinquished his CEO title and remains as Chairman of the Board.

Dr. Grove has written over 40 technical papers and holds several patents on semiconductor devices and technology. For six years he taught a graduate course in semiconductor device physics at the University of California, Berkeley. He currently is a lecturer at the Stanford University Graduate School of Business, teaching a course entitled "Strategy and Action in the Information Processing Industry".

Dr. Grove has received many honorary academic degrees, including an honorary Doctor of Science degree from the City College of New York (1985), an honorary Doctor of Engineering degree from Worcester Polytechnic Institute (1989) and an honorary Doctor of Laws degree from Harvard University (2000).

His first book, *Physics and Technology of Semiconductor Devices* (John Wiley and Sons, Inc., 1967) has been used at many leading universities in the United States. His book, *High Output Management* (Random House, 1983 and Vintage, 1985) has been translated into eleven languages, and has recently been updated and reissued by Vintage Books. His book titled, *One-on-One With Andy Grove*, was published by G.P. Putnam's Sons in June, 1987 and Penguin in 1989. His book, *Only the Paranoid Survive,* was published by Doubleday in September of 1996, and his latest

book, *Swimming Across*, was published in November, 2001 by Time Warner Books. An author of articles in *Fortune*, *The Wall Street Journal*, and the *New York Times*, he has written a weekly column on management which was carried by several newspapers, and a column on management for *Working Woman* magazine.

Awards Presentation
2002 IEEE Cledo Brunetti Award
2002 IEEE Andrew S. Grove Award
2002 IEEE Daniel E. Noble Award

Session 17: CMOS Devices — Alternative Gate and Channel MOSFETs

Tuesday, December 10, 2:15 p.m.
Grand Ballroom A

Co-Chairs: *Bin Yu, AMD*
Youri Ponomarev, Philips Research Leuven

2:15 p.m.
Introduction

2:20 p.m.
17.1 High Performance 40nm nMOSFETs With HfO_2 Gate Dielectric and Polysilicon Damascene Gate, B. Tavel, X. Garros*, T. Skotnicki*, F. Martin**, C. Leroux**, D. Bensahel*, M.N. Séméria**, Y. Morand*, J.F. Damlencourt**, S. Descombes*, F. Leverd*, Y. Le-Friec*, P. Leduc**, M. Rivoire*, S. Jullian*** and R.Pantel*, France Telecom R&D, Meylan, France, *STMicroelectronics, Crolles, France, **CEA-LETI, Grenoble, France and ***Philips Semiconductors, Crolles, France

2:45 p.m.
17.2 Dual-Metal Gate CMOS with HfO_2 Gate Dielectric, S. Samavedam, L.B. La, J. Smith, S. Dakshina-Murthy*, E. Luckowski, J. Schaeffer, M. Zavala, R. Martin, V. Dhandapani, D. Triyoso, H.H. Tseng, P.J. Tobin, D.C. Gilmer, C. Hobbs, W.J. Taylor, J.M. Grant, R.I. Hegde, J. Mogab, C. Thomas, P. Abramowitz, M. Moosa, J. Conner, J. Jiang, V. Arunachalam, M. Sadd, B.-Y. Nguyen and B. White, Motorola, Austin, TX and *AMD

3:10 p.m.
17.3 A Sub-400°C Germanium MOSFET Technology with High-k Dielectric and Metal Gate, C.O. Chui, H. Kim, D. Chi, B.B. Triplett, P.C. McIntyre and K.C. Saraswat, Stanford University, Stanford, CA

3:35 p.m.
17.4 High Mobility p-channel Germanium MOSFETs with a Thin Ge Oxynitride Gate Dielectric, H. Shang, H. Okorn-Schmidt, K.K. Chan, M. Copel, P. Kozlowski, S. Steen, S. Cordes, H.-S.P. Wong, E.C. Jones and W. Haensch, IBM T.J. Watson Research Center, Yorktown Heights, NY

4:00 p.m.
17.5 High Performance Damascene Gate CMOSFETs with Recessed Channel formed by Plasma Oxidation and Etching Method (RC-POEM), K. Matsuo, K. Sekine, T. Saito, K. Nakajima, K. Suguro and Y. Tsunashima, Toshiba Corporation, Yokohama, Japan

4:25 p.m.
17.6 Novel Low Offset Voltage Diode using Asymmetric Threshold Voltage MONOS-FET for Next Generation Devices Demanding Low Voltage Operation, S. Ueno, H. Furuta, Y. Okumura, T. Eimori and Y. Inoue, Mitsubishi Electric Corporation, Hyogo, Japan

Session 18: Solid State Devices — Integrated Power and Passive Components

Tuesday, December 10, 2:15 p.m.
Continental Ballrooms 1-3

Co-Chairs: *Satyen Mukherjee, Philips Research*
Michel Frei, Agere Systems

2:15 p.m.
Introduction

2:20 p.m.
18.1 A Low On-Resistance Trench Lateral Power MOSFET in a 0.6 μm Smart Power Technology for 20-30V Applications, N. Fujishima, M. Iwaya, M. Sawada, K. Tabuchi, S. Kajiwara and K. Mochizuki, Fuji Electric Corp. R&D, Nagano, Japan

2:45 p.m.
18.2 A 0.25μm CMOS Based 70V Smart Power Technology with Deep Trench for High-Voltage Isolation, V. Parthasarathy, R. Zhu, V. Khemka, T. Roggenbauer, A. Bose, P. Hui, P. Rodriquez, J. Nivison, D. Collins, Z. Wu and M. Butner, Motorola SPS, Tempe, AZ

3:10 p.m.
18.3 Technologies for RF Power LDMOSFETs Beyond 2 GHz: Metal/Poly-Si Damascene Gates and Low-Loss Substrates, J. Fiorenza, J. Scholvin and J. del Alamo, Massachusetts Institute of Technology, Cambridge, MA

3:35 p.m.
18.4 Saddle Add-On Metallisation (SAM) for RF Inductor Implementation in Standard IC Interconnects, B. Rejaei, J. Burghartz and H. Schellevis, TU Delft, Delft, The Netherlands

4:00 p.m.
18.5 A Broad-Band Scalable Lumped-Element Inductor Model Using Analytic Expressions to Incorporate Skin Effect, Substrate Loss, and Proximity Effect, F. Rotella, V. Blaschke* and D. Howard*, Skyworks Solutions Inc., Newport Beach, CA and *Jazz Semiconductor, Newport Beach, CA

4:25 p.m.
18.6 Ferromagnetic RF Inductors and Transformers for Standard CMOS/BiCMOS, Y. Zhuang, M. Vroubel, B. Rejaei, and J. Burghartz, TU Delft, Delft, The Netherlands

4:50 p.m.
18.7 Self-Assembled Out-of-Plane High-Q Integrated Inductors, K. van Schuylenbergh, C. Chua, D. Fork, J.-P. Lu and B. Griffiths*, Palo Alto Research Center, Palo Alto, CA and *Mixed Signal Systems Inc., Scotts Valley, CA

Session 19: Emerging Technologies — Bioelectronics Devices

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4

Co-Chair: *Dietrich Vook, Agilent Technologies*

2:15 p.m.
Introduction

2:20 p.m.
19.1 A VLSI Compatible Conducting Polymer Composite Based "Electronic Nose" Chip (Invited), N. Lewis, Noyes Laboratory, Pasadena, CA

2:45 p.m.
19.2 Fully Electronic DNA Detection on a CMOS Chip: Device and Process Issues (Invited), F. Hofmann, A. Frey, B. Holzapfl, M. Schienle, C. Paulus, P. Schindler-Bauer, D. Kuhlmeier*, J. Krause*, R. Hintsche**, E. Nebling**, J. Albers**, W. Gumbrecht***, K. Plehnert***, G. Eckstein*** and R. Thewes, Infineon Technologies, Munich, Germany, *november AG, Erlangen, Germany, **Fraunhofer Gesellschaft, Itzehoe, Germany and ***Siemens AG, Erlangen/Munich, Germany

3:10 p.m.
19.3 Retina Implant: Bridging Engineering and Medicine (Invited), W. Liu, North Carolina State University, Raleigh, NC

3:35 p.m.
19.4 Biomolecular Optoelectronic Devices and their Application to Artifical Vision (Invited), E. Greenbaum, M. Humayun**, T. Kuritz, J.W. Lee, C. Sanders, B. Bruce*, and I. Lee*, Oak Ridge National Laboratory, Oak Ridge, TN, *The University of Tennessee, Knoxville, TN and **University of Southern California, Los Angeles, CA

4:00 p.m.
19.5 Full-Implantable Auditory Prostheses: Restoring Hearing to the Profoundly Deaf (Invited), K.D. Wise and K. Najafi, University of Michigan, Ann Arbor, MI

Session 20: CMOS and Interconnect Reliability — NBTI, High-k and Process Impact on Reliability

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 5

Co-Chairs: *Luca Selmi, University of Udine*
Paolo Pavan, University of Modena and Reggio Emilia

2:15 p.m.
Introduction

2:20 p.m.
20.1 A Predictive Reliability Model for PMOS Bias Temperature Degradation, S. Mahapatra and M. Alam*, Indian Institute of Technology, Mumbai, India and *Agere Systems, Murray Hill, NJ

2:45 p.m.
20.2 NBTI Mechanism in Ultra-thin Gate Dielectrics -Nitrogen-Oriented Mechanism in SiON-, Y. Mitani, M. Nagamine, H. Satake and A. Toriumi*, Toshiba Corporation, Yokohama, Japan and *The University of Tokyo, Tokyo, Japan

3:10 p.m.
20.3 Localization of NBTI-Induced Oxide Damage in Direct Tunneling Regime Gate Oxide pMOSFET Using a Novel Low Gate-Leakage Gated-Diode (L^2-GD) Method, S.S. Chung, D.K. Lo, J.J. Yang* and T.C. Lin**, National Chiao Tung University, Taiwan, *Chang Gung University, Taiwan and **TSMC, Hsinchu, Taiwan

3:35 p.m.
20.4 Charge Trapping in High K Gate Dielectric Stacks, S. Zafar, A. Callegari, E. Gusev and M. Fischetti, IBM SRDC, Yorktown Heights, NY

4:00 p.m.
20.5 Towards Understanding Degradation and Breakdown of SiO_2 /High-k Stacks, T. Kauerauf, R. Degraeve, E. Cartier*, B. Govoreanu, P. Blomme, B. Kaczer, L. Pantisano, A. Kerber** and G. Groeseneken***, IMEC, Leuven, Belgium, *IBM affiliated to IMEC, Leuven, Belgium, **Infineon affiliated to IMEC, Leuven, Belgium and ***IMEC and KU, Leuven, Belgium

4:25 p.m.
20.6 Impact of Gate Area on Plasma Charging Damage: The "Reverse" Antenna Effect, A.T. Krishnan, S. Krishnan and P. Nicollian, Texas Instruments, Dallas, TX

4:50 p.m.
20.7 Variation in Natural Threshold Voltage of NVM Circuits Due to Dopant Fluctuations and its Impact on Reliability, D. Burnett, J. Higman, A. Hoefler, B. Li and P. Kuhn, Motorola, Austin, TX

Session 21: Integrated Circuits and Manufacturing — "Ultimate" Non Volatile Memories

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 6

Co-Chairs: *Olivier Faynot, LETI-CEA*
Sam Shichijo, Texas Instruments

2:15 p.m.
Introduction

2:20 p.m.
21.1 Demonstration of a 4Mb, High Density Ferroelectic Memory Embedded with a 130nm, 5LM Cu/FSG Logic Process, T. Moise, S. Summerfelt, H. McAdams, S. Aggarwal, K. Udayakumar, F. Celii, J. Martin, G. Xing, L. Hall, K. Taylor, T. Hurd, J. Rodriguez, K. Remack. M. Khan, K. Boku, G. Stacey, M. Yao, G. Albrecht, E. Zielinski, M. Thakre, S. Kuchimanchi, A. Thomas, B. McKee, J. Rickes*, A. Wang*, J. Grace*, J. Fong*, D. Lee*, C. Pietrzyk*, R. Lanham*, S. Gilbert*, D. Taylor*, J. Amano*, R. Bailey**, F. Chu**, G. Fox**, S. Sun** and T. Davenport**, Texas Instruments, Dallas, TX, *Agilent Technologies, Santa Clara, CA and **Ramtron International, Colorado Springs, CO

2:45 p.m.
21.2 4 Mbit Embedded FRAM for High Performance System on Chip (SoC) with Large Switching Charge, Reliable Retention and High Imprint Resistance, Y. Horii, Y. Hikosaka, A. Itoh*, K. Matsuura, M. Kurasawa*, G. Komuro, K. Maruyama*, T. Eshita and S. Kashiwagi, Fujitsu Limited, Atsugi, Japan and *Fujitsu Laboratories Ltd., Atsugi, Japan

3:10 p.m.
21.3 A Novel Stack Capacitor Cell for High Density FeRAM Compatible with CMOS Logic, T. Hayashi, Y. Igarashi, D. Inomata, T. Ichimori, T. Mitsuhashi, K. Ashikaga, T. Ito, M. Yoshimaru, M. Nagata*, S. Mitarai*, H. Godaiin*, T. Nagahama*, C. Isobe*, H. Moriya*, M. Shoji*, Y. Ito*, H. Kuroda*, M. Sasaki*, Oki Electric Industry Co., Tokyo, Japan and *Sony Corporation Semiconductor Network Company, Kanagawa, Japan

3:35 p.m.
21.4 Future 1T1C FRAM Technologies for Highly Reliable, High Density FRAM (Invited), S.Y. Lee and K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

4:00 p.m.
21.5 Fully Integrated 64Kb MRAM with Novel Reference Cell Scheme, H.S. Jeong, G.T. Jeong, G.H. Koh, I.H. Song*, W.J. Park*, T.W. Kim*, S.J. Chung*, Y.N. Hwang, S.J. Ahn, H.J. Kim, J.S. Hong, W.C. Jeong, S.H. Lee, J.H. Park, W.Y. Cho, K.H. Kwon, J.S. Kim, S. Song, H.J. Kim, J.H. Park, Y.K. Ha, J.H. Yi, Y. Ha, S.O. Park, U.I. Chung and K. Kim, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea and *Samsung Advanced Institute of Technology, Kyunggi-Do, Korea

Session 22: Detectors, Sensors and Displays — Thin Film Transistors

Tuesday, December 10, 2:15 p.m.
Continental Ballrooms 7-9

Co-Chairs: *Mike Hack, Universal Display Corporation*
Mutsumi Kimura, Seiko-Epson Corporation

2:15 p.m.
Introduction

2:20 p.m.
22.1 Polymer Gate Dielectric Pentacene TFTs and Circuits on Flexible Substrates, H. Klauk, M. Halik, U. Zschieschang, R. Brederlow*, W. Weber*, G. Schmid and W. Radlik, Infineon Technologies, Erlangen, Germany and *Infineon Technologies, Munich, Germany

2:45 p.m.
22.2 A New Multi-Channel Dual-Gate Poly-Si TFT Employing Excimer Laser Annealing Recrystallization on Pre-Patterned a-Si Thin Film, I.H. Song, S.H. Kang, W.J. Nam and M.K. Han, Seoul National University, Seoul, Korea

3:10 p.m.
22.3 High-Performance Single-Crystalline-Silicon TFTs on a Non-Alkali Glass Substrate, Y. Sano, M. Takei, A. Hara and N. Sasaki, Fujitsu Laboratories Ltd., Atsugi-shi, Japan

3:35 p.m.
22.4 Modeling of Metal-Induced-Lateral-Crystallization Mechanism for Optimization of High Performance Thin-Film-Transistor Fabrication, C.F. Cheng, M.C. Poon, M. Chan and C.W. Kok, Hong Kong University of Science and Technology, Hong Kong

4:00 p.m.
22.5 Junction Defects of Self-Aligned Excimer-Laser-Annealed Poly-Si TFT and a New Device Structure to Improve the Stability of Poly-Si TFT, K.-C. Park, S.-H. Jung, M.-C. Lee, J.-S. Kim and M.-K. Han, Seoul National University, Seoul, Korea

4:25 p.m.
22.6 Analysis of Reliability in Low-Temperature Poly-Si Thin Film Transistors Using Pico-Second Time-Resolved Emission Microscope, Y. Uraoka, N. Hirai*, H. Yano, T. Hatayama and T. Fuyuki, Nara Insitute of Science and Technology, Nara, Japan and *Hamamatsu Photonics, Nara, Japan

Session 23: Process Technology — Advanced Interconnect Processes

Tuesday, December 10, 2:15 p.m.
Imperial Room

Co-Chairs: *Thomas Bonifield, Texas Instruments Inc.*
Tatsuyuki Saito, Hitachi, Ltd.

2:15 p.m.
Introduction

2:20 p.m.
23.1 **90nm Generation Cu/CVD Low-k (k<2.5) Interconnect Technology**, T.I. Bao, C.C. Ko, J.Y. Song, L.P. Li, H.H. Lu, Y.C. Lu, Y.H. Chen, S.M. Jang, C.H. Yu and M.S. Liang, Taiwan Semiconductor Manufacturing Company, Taiwan, ROC

2:45 p.m.
23.2 **Via Design and Scaling Strategy for Nanometer Scale Interconnect Technologies**, S. Im, K. Banerjee* and K. Goodson, Stanford University, Stanford, CA and *University of California, Santa Barbara, CA

3:10 p.m.
23.3 **Cost-Effective "BARC/Resist-Via-Fill Free" Integration Technology for 0.13µm Cu/Low-k**, S.-G. Lee, K.-W. Lee, I.-G. Kim, W.-J. Park, Y.-J. Wee, W.-S. Song, J.-H. Kim, S.-J. Lee, J.-H. Lee, Y.-T. Lee, J.-H. Chung, H.-K. Kang and K.-P. Suh, Samsung Elecronics Co., Ltd., Kyunggi-Do, Korea

3:35 p.m.
23.4 **Advanced Metal Barrier Free Cu Damascene Interconnects with PECVD Silicon Carbide Barriers for 90/65-nm BEOL Technology**, Z.C. Wu, Y.C. Lu, C.C. Chiang*, M.C. Chen*, B.T. Chen, G.J. Wang, S.M. Jang, C.H. Yu and M.S. Liang, TSMC, Hsinchu, Taiwan and *National Chiao Tung University, Hsin-chu, Taiwan

4:00 p.m.
23.5 **Cu Dual Damascene Interconnects with In-Situ Fluorinated Carbon-Nitride (FCN: -C=N(F)-) Barrier Layers in Low-k Organic Film**, H. Ohtake, S. Saito, M. Tada, Y. Harada, T. Onodera and Y. Hayashi, NEC Corporation, Kanagawa, Japan

4:25 p.m.
23.6 **A 90nm Generation Copper Dual Damascene Technology with ALD TaN Barrier**, C.H. Peng, C.H. Hsieh, C.L. Huang, M.H. Tsai, M.W. Lin, J.L. Yang, J.B. Lai, S.L. Shue and M.S. Liang, Taiwan Semiconductor Manufacturing Company, Taiwan, ROC

Session 24: 2002 IEDM Evening Panel Discussion

Tuesday, December 10, 8:00 p.m.
Grand Ballroom A

"Embedded Memories for SoC — What Makes Sense?"

Silicon-on-a-Chip (SoC) has started driving VLSI technology more so than traditional Logic or Memory varieties. Meanwhile SIA projects memory content on SoC will be well over 50% by 2005. That means embedded memories will become the dominant factor in determining the success or failure of SoC products.

In this panel discussion, we will take a more tactical, and therefore practical, approach by focusing entirely on the evolutionary memory types to eliminate a lot of the speculations that has been stirred up recently by all the revolutionary or emerging memory types. The types of embedded memory that will be represented here by industry experts include 6T SRAM, 1T RAM, eDRAM, and Flash EEPROM. As many of the characteristics of these memories overlap, the task of choosing which memories to put on the SoC becomes more difficult. To make matters worse, the fact that it takes years and millions of dollars to make a particular type of memory available to put on SoC makes it harder to recover from a bad choice. So, what types of embedded memory should you develop or use - 6T SRAM, 1T RAM, eDRAM, or eFlash?

To balance out the views, we will also have an expert on Stacked Die or System-in-Package (SiP) to challenge the projected dominance of embedded memories.

Moderator: Ko-Min Chang, Motorola

Panelists:

Al Fazio
Intel Corporation

Eric Mazaleyrat
STMicroelectronics

Atsushi Nakamura
Hitachi

Bob Pitts
Texas Instruments

Chung Wang
TSMC

Session 25: 2002 IEDM Evening Panel Discussion

Tuesday, December 10, 8:00 p.m.
Grand Ballroom B

"*Will SOI Ever Become a Mainstream Technology?*"

The production of SOI chips has now been put into actual practice and a number of semiconductor companies have announced that they will pursue the production. The SOI is about to become a mainstream technology. However, there are still issues of controversy in regards to whether SOI devices are superior to bulk devices in a chip level, when the SOI technology should be introduced in production, and also what kind of SOI devices should be selected for each application. The technology choice largely depends on applications and the technology generation, and SOI will not necessarily be the best choice for all

of the products. At this panel session, it is our goal to focus our attention on the SOI technology, discussing the pros and cons on SOI and expanding the outlook of the future device technology.

- Bulk or SOI?
- Partially depleted or fully depleted?
- Body-tied or floating body?
- High-performance or low-power applications?
- Digital or RF/analog applications?
- Timing?

Moderator: Toshiro Hiramoto, University of Tokyo

Panelists:

Muhsin Celik
Motorola

Vivek De
Intel

Tsu-Jae King
University of California, Berkeley

Tadahiro Kuroda
Keio University

Shigenobu Maeda
Mitsubishi Electric

Hitoshi Wakabayashi
NEC

Isabel Y. Yang
IBM

Session 26: Process Technology — High-k Dielectrics: Performance and Reliability

Wednesday, December 11, 9:00 a.m.
Grand Ballroom A

Co-Chairs: *Veena Misra, North Carolina State University*
Helmut Tews, Infineon Technologies

9:00 a.m.
Introduction

9:05 a.m.
26.1 Fabrication of High Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs Using Deuterium Anneal, R. Choi, K. Onishi, C.S. Kang, S. Gopalan, R. Nieh, Y.H. Kim, J.H. Han, S. Krishnan, H. Cho, A. Shahriar and J.C. Lee, The University of Texas at Austin, Austin, TX

9:30 a.m.
26.2 Experimental Determination of Band Offset Energies Between Zr Silicate Alloy Dielectrics and Crystalline Si Substrates by XAS, XPS and AES and ab Initio Theory, G. Lucovsky, B. Rayner, Y. Zhang, and J. Whitten, North Carolina State University, Raleigh, NC

9:55 a.m.
26.3 Additional Scattering Mechanism for Mobility Degradation in Hf-silicate Gate MISFETs, T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake and N. Fukushima, Toshiba Corporation, Yokohama, Japan

10:20 a.m.
26.4 Advanced Gate Dielectric Materials for Sub-100 nm CMOS (Invited), H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama and Y. Yoshihara, Tokyo Institute of Technology, Yokohama, Japan

10:45 a.m.
26.5 Hard and Soft-Breakdown Characteristics of Ultra-Thin HfO_2 Under Dynamic and Constant Voltage Stress, Y.H. Kim, K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, R. Nieh, J. Han, S. Krishnan, and J. C. Lee, University of Texas, Austin, TX

11:10 a.m.
26.6 Proposed Universal Relationship Between Dielectric Breakdown and Dielectric Constant, J. McPherson, J. Kim, A. Shanware and H. Mogul, Texas Instruments, Dallas, TX

Session 27: CMOS Devices — Aggressively Scaled Planar MOSFET

Wednesday, December 11, 9:00 a.m.
Grand Ballroom B

Co-Chairs: *Meikei Ieong, IBM*
Greg Timp, University of Illinois

9:00 a.m.
Introduction

9:05 a.m.
27.1 14 nm Gate Length CMOSFETs Utilizing Low Thermal Process with Poly-SiGe and Ni Salicide, A. Hokazono, K. Ohuchi, M. Takayanagi, Y. Watanable, S. Magoshi, Y. Kato, T. Shimizu, S. Mori, H. Oguma, T. Sasaki, H. Yoshimura, K. Miyano, N. Yasutake, H. Suto, K. Adachi, H. Fukui, N. Tamaoki, T. Watanabe, Y. Toyoshima and H. Ishiuchi, Toshiba Corporation Semiconductor Company, Kanagawa, Japan

9:30 a.m.
27.2 Power-Constrained Device and Technology Design for the End of Scaling (Invited), D.J. Frank, IBM Semiconductor Research and Development Center, Yorktown Heights, NY

9:55 a.m.
27.3 Lateral Extension Engineering Using Nitrogen Implantation (N-tub) for High Performance 40 nm pMOSFET, Y. Momiyama, K. Okabe*, H. Nakao, M. Kase, M. Kojima and T. Sugii, Fujitsu Laboratories Ltd., Akiruno, Japan and *Fujitsu VLSI Process Technology Laboratory Ltd., Akiruno, Japan

10:20 a.m.
27.4 Device Performance of Sub-50 nm CMOS with Ultra-Thin Plasma Nitrided Gate Dielectrics, S. Inaba, T. Shimizu, S. Mori, K. Sekine, K. Saki, H. Suto, H. Fukui, M. Nagamine, M. Fujiwara, T. Yamamoto, M. Takayanagi, I. Mizushima, K. Okano, S. Matsuda, H. Oyamatsu, Y. Tsunashima, S. Yamada, Y. Toyoshima and H. Ishiuchi, Toshiba Corporation, Yokohoma, Japan

10:45 a.m.
27.5 High Performance 30nm Bulk CMOS for 65nm Technology Node (CMOS5), E. Morifuji, M. Kanda, N. Yanagiya, S. Matsuda, S. Inaba, K. Okano, K. Takahashi, M. Nishigori, H. Tsuno, T. Yamamoto, K. Hiyama, M. Takayanagi, H. Oyamatsu, S. Yamada, T. Noguchi and M. Kakumu, Toshiba Corporation, Yokohama, Japan

11:10 a.m.
27.6 Silicon on Depletion Layer FET (SODEL FET) for Sub-50 nm Node High Performance CMOS Applications: Novel Channel and S/D Profile Engineering Schemes by Selective Si Epitaxial Growth Technology, S. Inaba, K. Miyano, A. Hokazono, K. Ohuchi, I. Mizushima, H. Oyamatsu, Y. Tsunashima, Y. Toyoshima and H. Ishiuchi, Toshiba Corporation Semiconductor Co., Yokohama, Japan

11:35 a.m.
27.7 Novel SOI Wafer Engineering Using Low Stress and High Mobility CMOSFET with <100>-Channel for Embedded RF/Analog Applications, T. Matsumoto, S. Maeda, H. Dang, T. Uchida, K. Ota, Y. Hirano, H. Sayama, T. Iwamatsu, T. Ipposhi, H. Oda, S. Maegawa, Y. Inoue and T. Nishimura, Mitsubishi Electric Corporation, Hyogo, Japan

12:00 p.m.
27.8 0.1µm RFCMOS on High Resistivity Substrates for System on Chip (SOC) Applications, J.-Y. Yang, K. Benaissa, D. Crenshaw, B. Williams, S. Sridhar, J. Ai, G. Boselli, S. Zhao, S.-P. Tang, S. Ashburn, P. Madhani, T. Blythe, M. Nandakumar and H. Shichijo, Texas Instruments, Dallas, TX

Session 28: Quantum Electronics and Compound Semiconductors — Wide Bandgap RF Power Transistors

Wednesday, December 11, 9:00 a.m.
Continental Ballrooms 1-3

Co-Chairs: *Sandeep Bahl, Agilent Technologies Labs*
Greg DeSalvo, Northrop Grumman

9:00 a.m.
Introduction

9:05 a.m.
28.1 AlGaN/GaN HEMTs on SiC operating at 40 GHz, R. Quay, R. Kiefer, F. van Raay, H. Massler, S. Ramberger, S. Müller, M. Dammann, M. Mikulla, M. Schlechtweg and G. Weimann, Fraunhofer-Institute of Applied Solid-State Physics, Freiburg, Germany

9:30 a.m.
28.2 Ka-band 2.3W Power AlGaN/GaN Heterojunction FET, K. Kasahara, H. Miyamoto, Y. Ando, Y. Okamoto, T. Nakayama and M. Kuzuhara, NEC Corporation, Shiga, Japan

9:55 a.m.
28.3 10 W GaInP/GaAs Power HBTs for Base Station Applications, P. Kurpas, A. Maaßdorf, W. Doser*, P. Heymann, B. Janke, F. Schnieder, H. Blanck*, P. Auxemery**, D. Pons**, W. Heinrich and J. Würfl, Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany and *United Monolithic Semiconductors GmbH, Ulm, Germany and **United Monolithic Semiconductors SAS, Orsay, France

10:20 a.m.
28.4 Transistor Delay Analysis and Effective Channel Velocity Extraction in AlGaN/GaN HFETs, C. Bolognesi, A.C. Kwan and D. DiSanto, Simon Fraser University, Burnaby, Canada

10:45 a.m.
28.5 Experimental/Numerical Investigation on Current Collapse in AlGaN/GaN HEMT's, G. Verzellesi, R. Pierobon*, F. Rampazzo*, G. Meneghesso*, A. Chini**, D. Buttari**, U.K. Mishra**, C. Canali and E. Zanoni*, Università di Modena e Reggio Emilia, Modena, Italy and *Università di Padova, Padova, Italy and **University of California, Santa Barbara, CA

11:10 a.m.
28.6 Improved Intermodulation Distortion Profile of AlGaN/GaN HEMT at High Drain Bias Voltage, M. Nagahara, T. Kikkawa*, N. Adachi, Y. Tateno, S. Kato, M. Yokoyama, S. Yokogawa, T. Kimura*, Y. Yamaguchi, N. Hara* and K. Joshin*, Fujitsu Quantum Devices, Ltd., Yamanashi, Japan and *Fujitsu Laboratories Ltd., Kanagawa, Japan

11:35 a.m.
28.7 Linearity and Gain Characteristics of AlGaN/GaN HEMTs, Y.-F. Wu, P.M. Chavarkar, M. Moore, P. Parikh and U.K. Mishra, Cree Lighting Company, Goleta, CA

Session 29: Modeling and Simulation — Device Modeling

Wednesday, December 11, 9:00 a.m.
Continental Ballroom 4

Co-Chairs: *Antonio Abramo, University of Udine*
Christoph Jungemann, University of Bremen

9:00 a.m.
Introduction

9:05 a.m.
29.1 Nanoscale Device Modeling: The Green's Function Method (Invited), S. Datta, Purdue University, West Lafayette, IN

9:30 a.m.
29.2 Does Source-to-Drain Tunneling Limit the Ultimate Scaling of MOSFETs?, J. Wang and M. Lundstrom, Purdue University, West Lafayette, IN

9:55 a.m.
29.3 Assessment of Silicon MOS and Carbon Nanotube FET Performance Limits Using a General Theory of Ballistic Transistors, J. Guo, M. Lundstrom, S. Datta and P. McEuen*, Purdue University, West Lafayette, IN and *Cornell University, Ithaca, NY

10:20 a.m.
29.4 QDAME Simulation of 7.5 nm Double-Gate Si nFETs with Differing Access Geometries, S. Laux, A. Kumar and M. Fischetti, IBM SRDC, Yorktown Heights, NY

10:45 a.m.
29.5 Study of Low Field Electron Transport in Ultra-Thin Single and Double Gate SOI MOSFETs, D. Esseni, A. Abramo, L. Selmi and E. Sangiorgi, DIEGM, Udine, Italy

11:10 a.m.
29.6 Two-Dimensional Polysilicon Quantum-Mechanical Effects in Double-Gate SOI, C.-H. Choi, Z. Yu and R. Dutton, Stanford University, Stanford, CA

11:35 a.m.
29.7 A Study of Subband Structure and Transport of Two-Dimensional Holes in Strained Si p-MOSFETs Using Full-Band Modeling, H. Nakatsuji, Y. Kamakura and K. Taniguchi, Osaka University, Osaka, Japan

12:00 p.m.
29.8 Quantum Tunneling and Scalability of HfO_2 and HfAlO Gate Stacks, Y.T. Hou, M.F. Li, H.Y. Yu, Y.Jin* and D.L. Kwong**, National University of Singapore, Singapore, *Chartered Semiconductor Manufacturing Ltd, Singapore and **The University of Texas, Austin, TX

Session 30: CMOS and Interconnect Reliability — Cu Interconnect Reliability Issues

Wednesday, December 11, 9:00 a.m.
Continental Ballroom 5

Co-Chairs: *Hyeon-Deok Lee, Samsung Electronics Co., Ltd.*
Paul Besser, AMD

9:00 a.m.
Introduction

9:05 a.m.
30.1 True Influence of Wafer-Backside Copper Contamination During the Back-End Process on Device Characteristics, K. Hozawa, H. Miyazaki, S. Isomae and J. Yugami, Hitachi, Ltd., Tokyo, Japan

9:30 a.m.
30.2 Electromigration Reliability of Cu Interconnects and Effects of Low k Dielectrics (Invited), P.S. Ho, K.-D. Lee, E.T. Ogawa, X. Lu, H. Matsuhashi, V.A. Blaschke* and R. Augur*, The University of Texas at Austin, Austin, TX and *International SEMATECH, Austin, TX

9:55 a.m.
30.3 Mechanical Stress Measurements in Damascene Copper Interconnects and Influence on Electromigration Parameters, G. Reimbold, O. Sicardy*, L. Arnaud, F. Fillot and J. Torres**, CEA/LETI, Grenoble, France, *CEA, Grenoble, France and **ST Microelectronics, Crolles, France

10:20 a.m.
30.4 Suppression of Stress Induced Open Failures Between Via and Cu Wide Line by Inserting Ti Layer Under Ta/TaN Barrier, M. Ueki, M. Hiroi, N. Ikarashi, T. Onodera, N. Furutake, M. Yoshiki and Y. Hayashi, NEC Corporation, Kanagawa, Japan

10:45 a.m.
30.5 Stress-Induced Voiding Phenomena for an Actual CMOS LSI Interconnects, K. Yoshida, T. Fujimaki, K. Miyamoto, T. Honma, H. Kaneko, H. Nakazawa and M. Morita, Toshiba Corporation, Yokohama, Japan

11:10 a.m.
30.6 Suppression of Stress-Induced Voiding in Copper Interconnects, T. Oshima, K. Hinode, H. Yamaguchi, H. Aoki, K. Torii, T. Saito, K. Ishikawa, J. Noguchi, U. Tanaka, T. Nakamura, S. Uno, K. Tsugane, J. Murata, K. Kikushima, H. Sekisaka*, E. Murakami, K. Okuyama and T. Iwasaki**, Hitachi, Ltd., Tokyo, Japan, *Hitachi ULSI Systems Co., Ltd., Tokyo, Japan and **Hitachi, Ltd., Ibaraki, Japan

Session 31: Solid State Devices — High Performance SiGe Bipolar/BiCMOS Technology

Wednesday, December 11, 9:00 a.m.
Continental Ballroom 6

Co-Chairs: *Marco Racanelli, Jazz Semiconductor*
Joseph Boeck, Infineon Technologies

9:00 a.m.
Introduction

9:05 a.m.
31.1 Sub 5 ps SiGe Bipolar Technology, J. Böck, H. Schäfer, H. Knapp, D. Zöschg, K. Aufinger, M. Wurzer, S. Boguth, M. Rest, R. Schreiter, R. Stengl, T. Meister, Infineon Technologies, Munich, Germany

9:30 a.m.
31.2 Ultra-High-Speed Scaled-Down Self-Aligned SEG SiGe HBT Technology, K. Washio, E. Ohue, R. Hayami, A. Kodama*, H. Shimamoto*, M. Miura, K. Oda, I. Suzumura, T. Tominari and T. Hashimoto, Hitachi Ltd., Tokyo, Japan and *Hitachi Device Engineering, Co. Ltd., Tokyo, Japan

9:55 a.m.
31.3 SiGe HBTs with Cut-off Frequency Near 300GHz, J.-S. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S.-J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker*, K. Vaed, R. Volant, D. Ahlgren, G. Freeman, K. Stein and S. Subbanna, IBM Microelectronics, Hopewell Junction, NY and *IBM Microelectronics, Essex Junction, VT

10:20 a.m.
31.4 Novel Collector Design for High-Speed SiGe:C HBTs, B. Heinemann, H. Rücker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Höppner, D. Knoll, D. Krüger, B. Kuck, R. Kurps, M. Marschmeyer, H. H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, D. Wolansky, H.-E. Wulf, Y. Yamamoto and P. Zaumseil, IHP, Frankfurt, Germany

10:45 a.m.
31.5 Integration of a 0.13-µm CMOS and a High Performance Self-Aligned SiGe HBT Featuring Low Base Resistance, T. Hashimoto, Y. Nonaka, T. Saito, K. Sasahara, T. Tominari, K. Sakai, K. Tokunaga, T. Fujiwara, S. Wada, T. Udo*, T. Jinbo, K. Washio and H. Hosoe, Hitachi, Ltd., Tokyo, Japan and *Hitachi ULSI Systems Co. Ltd., Tokyo, Japan

11:10 a.m.
31.6 A Flexible, Low-Cost, High Performance SiGe:C BiCMOS Process with a One-Mask HBT Module, D. Knoll, K.E. Ehwald, B. Heinemann, A. Fox, K. Blum, H. Rücker, F. Fuernhammer, B. Senapati, R. Barth, U. Haak, W. Höppner, J. Drews, R. Kurps, S. Marschmeyer, H. Richter, T. Grabolla, B. Kuck, O. Fursenko, P. Schley, B. Tillack, Y. Yamamoto, K. Köpke, H. Wulf, D. Wolansky and W. Winkler, IHP, Frankfurt, Germany

11:35 a.m.
31.7 Noise Performance of a Low Base Resistance 200 GHz SiGe Technology, D. Greenberg, B. Jagannathan*, S. Sweeney**, G. Freeman* and D. Ahlgren*, IBM Research, Yorktown Heights, NY, *IBM Microelectronics, Hopewell Junction, NY and **IBM Microelectronics, Burlington, VT

Session 32: Detectors, Sensors and Displays — Photo Detectors and CMOS Imagers

Wednesday, December 11, 9:00 a.m.
Continental Ballrooms 7-9

Co-Chairs: *Jan Bosers, Dalsa B.V.*
Junichi Nakamura, Micron Japan, Ltd.

9:00 a.m.
Introduction

9:05 a.m.
32.1 Fabrication and Modeling of Gigahertz Photodetectors in Heteroepitaxial Ge-on-Si Using a Graded Buffer Layer Deposited by Low Energy Plasma Enhanced CVD, R.E. Jones, S.G. Thomas*, S. Bharatan*, R. Thoma*, C. Jasper*, T. Zirkle*, N.V. Edwards*, R. Liu*, X.D. Wang*, Q. Xie*, C. Rosenblad**, J. Ramm**, G. Isella***, H. von Känel***, J. Oh# and J.C. Campbel#, Motorola, Austin, TX and *Motorola, Tempe, AZ and **Unaxis Balzers Ltd, Balzers, Liechtenstein and ***ETH Zürich, Zürich, Switzerland and #University of Texas, Austin, TX

9:30 a.m.
32.2 A Novel Silicon Geiger-Mode Avalanche Photodiode, J.C. Jackson, A.P. Morrison*, D. Phelan** and A. Mathewson, NMRC, Cork, Ireland, *University College Cork, Ireland and **University College Galway, Ireland

9:55 a.m.
32.3 Integrated PIN Photodiodes in High-Performance BiCMOS Technology, M. Förtsch, H. Zimmerman, W. Einbrodt*, K. Bach* and H. Pless**, Vienna University of Technology, Vienna, Austria, *XFAB Semiconductor Foundries AG, Erfurt, Germany and **Melexis GmbH, Erfurt, Germany

10:20 a.m.
32.4 Trends in CMOS Image Sensor Technology and Design (Invited), A. Gamal, Stanford University, Stanford, CA

10:45 a.m.
32.5 Reset Noise Suppression in Two-Dimensional CMOS Photodiode Pixels Through Column-Based Feedback Reset, B. Pain, T. Cunningham, B. Hancock, G. Yang and M. Ortiz, California Institute of Technology, Pasadena, CA

11:10 a.m.
32.6 Active Pixel Image Sensor Scale Down in 0.18µm CMOS Technology, H.-C. Chien, S.-G. Wuu, D.-N. Yaung, C.-H. Tseng, J.-S. Lin, C.S. Wang, C.-K. Chang and Y.-K. Hsiao, Taiwan Semiconductor Manufacturing Co., Taiwan, ROC

Session 33: Integrated Circuits and Manufacturing — DRAM

Wednesday, December 11, 9:00 a.m.
Imperial Ballroom

Co-Chairs: *Carl Radens, IBM Microelectronics*
Donggun Park, Samsung Electronics

9:00 a.m.
Introduction

9:05 a.m.
33.1 Highly Manufacturable 90 nm DRAM Technology, Y.K. Park, C.H. Cho, K.H. Lee, B.H. Roh, Y.S. Ahn, S.H. Lee, J.H. Oh, J.G. Lee, D.H. Kwak, S.H. Shin, J.S. Bae, S.B. Kim, J.K. Lee, J.Y. Lee, M.S. Kim, J.W. Lee, D.J. Lee, S.H. Hong, D.I. Bae, Y.S. Chun, S.H. Park, C.J. Yun, T.Y. Chung and K. Kim, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea

9:30 a.m.
33.2 A Novel Robust TiN/AHO/TiN Capacitor and $CoSi_2$ Cell Pad Structure for 70nm Stand-Alone and Embedded DRAM Technology and Beyond, J.M. Park, Y.S. Hwang, D.S. Hwang, H.K. Hwang, S.H. Lee, G.Y. Kim, M.Y. Jeong, B.J. Park, S.E. Kim, M.H. Cho, D.I. Kim, J.-H. Chung, I.S. Park, C.-Y. Yoo, J.H. Lee, B.Y. Nam, Y.R. Park, C.-S. Kim, M.-C. Sun, J.-H. Ku, S. Choi, H.S. Kim, Y.G. Park and K. Kim, Samsung Electronics Co., Kyunggi-Do, Korea

9:55 a.m.
33.3 Interlayer Dielectric(ILD)-Related Edge Channel Effect in High Density DRAM Cell, I.-G. Kim, N.-S. Kim, S.-K. Choi, T.-U. Youn, H.-C. Jung, J.-S. Kweon, Y.-I. Chun, Y.-W. Kweon, W.-S. Kim, M.-J. Bong and J.-S. Park, Hynix Semiconductor Inc., Chungbuk, Korea

10:20 a.m.
33.4 Ultra-High-Performance 0.13-µm Embedded DRAM Technology Using TiN/HfO_2/TiN/W Capacitor and Body-Slightly-Tied SOI, Y. Aoki, T. Ueda, H. Shirai, T. Sakoh, T. Kitamura, S. Arai, M. Sakao, K. Inoue, M. Takeuchi, H. Sugimura, M. Hamada, T. Wake, I. Naritake, T. Iizuka, T. Yamamoto, K. Ando and K. Noda, NEC Corporation, Kanagawa, Japan

10:45 a.m.
33.5 High Performance Cell Technology Featuring Sub-100nm DRAM with Multi-Gigabit Density, B.-C. Lee, J.-R. Yoo, D.-H. Lee, C.-S. Kim, I.-S. Jung, S. Choi, U-I. Chung and J.-T. Moon, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

11:10 a.m.
33.6 A Fully Integrated Al_2O_3 Trench Capacitor DRAM for Sub-100nm Technology, H. Seidl, M. Gutsche, U. Schroeder*, T. Hecht*, S. Jakschik*, S. Kudelka*, T. Popp*, A. Orth*, H. Reisinger, A. Saenger*, B. Sell*, A. Birner*, K. Schupke* and J. Luetzen*, Infineon Technologies, Munich, Germany and *Dresden, Germany

11:35 a.m.
33.7 A Capacitorless Double-Gate DRAM Cell Design for High Density Applications, C. Kuo, T.J. King and C. Hu, University of California, Berkeley, CA

Session 34: Process Technology — High-k Dielectrics: Effect of Nitrogen

Wednesday, December 11, 1:30 p.m.
Grand Ballroom A

Co-Chairs: Bich-Yen Nguyen, Motorola
Toyoji Yamamoto, NEC Corporation

1:30 p.m.
Introduction

1:35 p.m.
34.1 Effects of Nitrogen in HfSiON Gate Dielectric on Its Excellent Electrical and Thermal Characteristics, M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama, Toshiba Corporation, Yokohama, Japan

2:00 p.m.
34.2 Improved Current Performance of CMOSFETs with Nitrogen Incorporated HfO_2-Al_2O_3 Laminate Gate Dielectric, H.-S. Jung, Y.-S. Kim, J.P. Kim, J.H. Lee, J.-H. Lee, N.-I. Lee, H.-K. Kang, K.-P. Suh, K.-H. Cho, H.-J. Ryu, C.-B. Oh, Y.W. Kim, Y.-S. Chung*, H.-S. Baik*, H.S. Chang** and D.W. Moon**, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea and *Samsung Advanced Institute of Technology, Kyunggi-Do, Korea and **Korea Research Institute of Standard and Science, Kyunggi-Do, Korea

2:25 p.m.
34.3 Thermally Stable CVD HfO_xN_y Advanced Gate Dielectrics with Poly-Si Gate Electrodes, C.H. Choi, S.J. Rhee, T.S. Jeon, N. Lu, J.H. Sim, R. Clark*, M. Niwa** and D.L. Kwong, The University of Texas, Austin, TX and *Schumacher, Carlsbad, CA and **Matsushita, Kyoto, Japan

2:50 p.m.
34.4 Ultra-Thin (T_{eff}^{inv}= 1.7 nm) Poly-Si-Gated SiN/HfO_2/SiON High-k Stack Dielectrics with High Thermal Stability (1050°C), Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii and T. Nakamura, Fujitsu Laboratories Ltd., Tokyo, Japan

3:15 p.m.
34.5 Nitrogen Concentration Effects and Performance Improvement of MOSFETs Using Thermally Stable HfO_xN_y Gate Dielectrics, C.S. Kang, H.-J. Cho, K. Onishi, R. Choi, Y. H. Kim, R. Nieh, J. Han, S. Krishnan and J.C. Lee, University of Texas at Austin, Austin, TX

3:40 p.m.
34.6 Nitride-Sandwiched-Oxide Gate Insulator for Low Power CMOS, D. Ishikawa, S. Sakai, K. Katsuyama and A. Hiraiwa, Hitachi, Ltd., Tokyo, Japan

Session 35: Modeling and Simulation — Process Modeling

Wednesday, December 11, 1:30 p.m.
Continental Ballroom 4

Co-Chairs: *Masami Hane, NEC Corporation*
Edwin Kan, Cornell University

1:30 p.m.
Introduction

1:35 p.m.
35.1 **Modeling of Ultrahighly Doped Shallow Junctions for Aggressively Scaled CMOS (Invited)**, H. Kennel, S. Cea, A. Lilak, P. Keys, M. Giles, J. Hwang, J. Sandford and S. Corcoran, Intel Corporation, Hillsboro, OR

2:00 p.m.
35.2 **A Physics Based Approach to Ultra-Shallow p^+-junction Formation at the 32nm Node**, A. Mokhberi, L. Pelaz*, M. Aboy*, L. Marques*, J. Barbolla*, P. Griffin, J.D. Plummer, E. Paton**, S. McCoy***, J. Ross***, K. Elliott*** and J. Gelpy***, Stanford University, Stanford, CA and *University of Valladolid, Valladolid, Spain, **Advanced Micro Devices, Sunnyvale, CA and ***Vortek Industries, Vancouver, Canada

2:25 p.m.
35.3 **Fluorine Diffusion: Models and Experiments**, R. Robison and M. Law, University of Florida, Gainesville, FL

2:50 p.m.
35.4 **Characterization of 2D Dopant Profile in L_{eff}~20 nm MOSFETs by Inverse Modeling with Precise $\partial C/\partial V$, $\partial V_{th}/\partial V$-L Measurement**, T. Tanaka, Y. Tagawa, S. Satoh and T. Sugii, Fujitsu Laboratories Ltd., Tokyo, Japan

3:15 p.m.
35.5 **A Feature Scale Model for Trench Capacitor Etch Rate and Profile**, W. Jacobs, A. Kersch, P. Moll*, W. Sabisch and G. Schulze Icking-Konert, Infineon Technologies, Munich, Germany and *Infineon Technologies, Dresden, Germany

Session 36: Detectors, Sensors and Displays — RF MEMs and Sensors

Wednesday, December 11, 1:30 p.m.
Continental Ballrooms 7-9

Co-Chairs: Christofer Hierold, ETH Zurich
Chris Nguyen, DARPA/MTO

1:30 p.m.
Introduction

1:35 p.m.
36.1 **Advancement of MEMS into RF-Filter Applications (Invited)**, R. Aigner, Infineon Technologies, Munich, Germany

2:00 p.m.
36.2 **Experimental Characterization of Stiction Due to Charging in RF MEMS**, W. M. van Spengen, R. Puers*, R. Mertens and I. De Wolf, IMEC, Leuven, Belgium and *K.U. Leuven, Leuven, Belgium

2:25 p.m.
36.3 Microfabricated Near-filed Scanning Microwave Probes, Y. Wang and M. Tabib-Azar, Case Western Reserve University, Cleveland, OH

2:50 p.m.
36.4 A CMOS Magnetic Latch with Extremely High Resolution, Z.Q. Li and X.W. Sun, Nanyang Technological University, Singapore

3:15 p.m.
36.5 An Organic Optical Bistable Switch, J. Xue and S.R. Forrest, Princeton University, Princeton, NJ

Session 37: Integrated Circuits and Manufacturing — Flash and Phase Change Memories

Wednesday, December 11, 1:30 p.m.
Imperial Room

Co-Chairs: *Emilio Camerlenghi, STMicroelectronics*
Kazunari Ishimaru, Toshiba Corporation

1:30 p.m.
Introduction

1:35 p.m.
37.1 A 2Gb NAND Flash Memory with 0.044µm² Cell Size using 90nm Flash Technology, D.-C. Kim, W.-C. Shin, J.-D. Lee, J.-H. Shin, S.-H. Hur, I.-G. Baik, Y.-C. Shin, C.-H. Lee, J.-S. Yoon, H.-G. Lee, K.-S. Jo, S.-W. Choi, B.-K. You, J.-H. Choi, D. Park and K. Kim, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

2:00 p.m.
37.2 Electronic Switching Effect in Phase-Change Memory Cells, A. Pirovano, A. Lacaita, D. Merlani, A. Benvenuti, F. Pellizzer and R. Bez, Politecnico di Milano, Milano, Italy and STMicroelectronics, Agrate Brianza, Italy

2:25 p.m.
37.3 An Embedded 90nm SONOS Nonvolatile Memory Utilizing Hot Electron Programming and Uniform Tunnel Erase, C. Swift, G. Chindalore, K. Harber, T. Harp, A. Hoefler, C. Hong, P. Ingersoll, C.B. Li, E. Prinz, and J. Yater, Motorola, Austin, TX

2:50 p.m.
37.4 PHINES: A Novel Low Power Program/Erase, Small Pitch, 2-Bit per Cell Flash Memory, C.C. Yeh, W.J. Tsai, M.I. Liu, T.C. Lu, S.K. Cho, C.J. Lin, T. Wang*, S. Pan and C.-Y. Lu, Macronix International Co., Ltd, Taiwan, ROC and *National Chiao-Tung University, Taiwan, ROC

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