international Electron Devices meeting

Hilton Washington
and Towers

Washington, DC

December 5-7, 2005

Sponsored by
Electron Devices Society of IEEE

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2005 Conference at a Glance

Date	Time	International Ballroom West	International Ballroom Center	International Ballroom East	Georgetown Room	Jefferson Room	Lincoln Room	Military Room	Thoroughbred Room
Sun.	9:00 a.m. -5:30 p.m.		**Short Course**	**Short Course**					
Mon.	9:00 a.m. -12:00 p.m.		**1** **PLENARY**						
	1:30 p.m. - 5:30 p.m.	**2** **Process Technology** High-k I Gate Stacks	**3** **Integrated Circuits and Manufacturing** Advanced CMOS and Platform Technology	**4** **Process Technology** Advanced Interconnect Technology	**5** **Displays, Sensors and MEMS** Organic and Flexible Electronics	**6** **CMOS Devices** Mobility Enhancement and Low Resistance Sources/Drain	**7** **Solid State and Nanoelectronic Devices** Non-Volatile Memory Technologies: MONOS and Nanocrystal Memories	**8** **CMOS and Interconnect Reliability** Interconnect, Plasma Damage, and ESD Reliability	**9** **Modeling and Simulation** Compact Models
	6:00 p.m. - 7:30 p.m.		**RECEPTION**						
Tues.	9:00 a.m. - 12:00 p.m.		**10** **CMOS Devices** High Performance CMOS	**11** **Solid State and Nanoelectronic Devices** Nanotubes and Nanowires for Thermal and Electrical Applications	**12** **Displays, Sensors and MEMS** MEMS Technologies and Applications	**13** **Integrated Circuits and Manufacturing** DRAM and NAND Flash	**14** **Process Technology** Advanced Integration Concepts	**15** **Quantum Power and Compound Semiconductor Devices** High Performance Si-RF Power and Power-Switching Devices	**16** **CMOS and Interconnect Reliability** Gate Dielectric Breakdown — Modeling and Mechanism
	12:20 p.m.	**LUNCHEON**							
	2:15 p.m. - 5:30 p.m.		**17** **Process Technology** High-k II Gate Dielectrics	**18** **Emerging Technologies** Flexible Electronics	**19** **Solid State and Nanoelectronic Devices** Novel Device Concepts	**20** **CMOS Devices** Strained-Silicon Technology	**21** **Modeling and Simulation** Nanowires and Nanotubes	**22** **CMOS and Interconnect Reliability** Process and Electrical Degradation in Flash Memories and Performance Boosted CMOS Devices	**23** **Quantum Power and Compound Semiconductor Devices** GaN High-Power Devices, Pushing the Limits
	8:00 p.m. - 10:00 p.m.	**24** **IEDM Evening Panel Session**	**25** **IEDM Evening Panel Session**						
Wed.	9:00 a.m. - 12:00 p.m.	**26** **Modeling and Simulation** Transport in Advanced Planar CMOS Devices	**27** **Process Technology** Fully Silicided Gates	**28** **Integrated Circuits and Manufacturing** Advanced SRAM and Novel Integration Technology	**29** **CMOS and Interconnect Reliability** Bias-Temperature Instability and Interface Traps	**30** **CMOS Devices** SOI and Multi-Gate Devices	**31** **Sold State and Nanoelectronic Devices** Resistive Switching Memories	**32** **Quantum Power and Compound Semiconductor Devices** High-Speed Compound Semiconductor Devices for Logic & Communications	**33** **Displays, Sensors and MEMS** Image Sensors and Photon Detectors
	1:30 p.m. - 5:30 p.m.	**34** **Process Technology** Advanced FEOL Technology	**35** **Integrated Circuits and Manufacturing** Non-Volatile Memories	**36** **CMOS Devices** Advanced Gate Stacks	**37** **Displays, Sensors, and MEMS** Thin Film Transistors for Displays and System on Panel	**38** **Solid State and Nanoelectronic Devices** Active and Passive Components in CMOS-Compatible Technlogies	**39** **Modeling and Simulation** Simulation of Doping and Stress Effects in Advanced CMOS	**40** **Quantum Power and Compound Semiconductor Devices** Silicon Challenges Conventional III-V Light Emitters	**41** **Modeling and Simulation** System Level Device Modeling

WELCOME FROM THE GENERAL CHAIR

On behalf of the entire IEDM Committee, I would like to welcome you to the 2005 IEEE International Electron Devices Meeting. We begin our second 50 years of existence honoring the past wealth of technical work presented here first as well as looking forward towards the future of this great conference. It continues to be the premier venue for presenting the latest, broadest and best technical information of critical importance to sustaining and expanding our world through exciting breakthroughs in electronic device technologies.

Jon Candelaria
General Chair

This great tradition continues to grow this year, with what we believe is the best collection of contributed and invited papers we've ever had. They will be presented by industrial and academic leaders and students from over sixteen countries around the world. Over 670 abstracts were submitted this year, a near record, of which more than 240 were accepted for presentation at this conference. Short summaries of each paper are included on the IEDM web site which we encourage everyone to visit – http://www.ieee.org/conference/iedm

Kaizad Mistry
Technical Program Chair

If you are not already an IEEE member, please consider joining this great institution which has played such an important role globally for over 120 years. More detailed information regarding IEEE is available at this conference and on their website – http://www.ieee.org

H.S. Philip Wong
Technical Program Vice Chair

In addition to the many regular paper sessions, we will again feature several very special sessions:

On Sunday, two short courses are scheduled entitled: "Next Generation Semiconductor Manufacturing" and "Low Power 'System-On-Chip' CMOS Technology Platforms". They have been designed for broad appeal to IEDM participants with material suitable for both newcomers as well as detailed

enough for experts in their fields. These courses have been organized and will be presented by internationally-known leading researchers active in their respective areas of technology.

The Plenary Session on Monday morning will feature the following invited talks – "More Than Moore: Micromachined Products Enable New Applications and Open New Markets", presented by Benedetto Vigna from ST Microelectronics; "Scaling, Power and the Future of CMOS", given by Mark Horowitz, Stanford University and Rambus, Inc.; and "Past and Future of Information Displays", by Kouji Suzuki, Toshiba Corp. and SED, Inc.

The Emerging Technology special session this year features breakthroughs in the area of Flexible Electronics, and will include five talks from leading experts in this exciting new area looking from a broad variety of perspectives including materials, processing and structures, as well as systems and applications.

On Tuesday night, we will again feature our popular and interactive Panel sessions. This year we will explore the questions "Will Non-Volatile Memory Technology Scale Past the End of the Decade?" and "Semiconductor Research and Development: Who Will Do It and Who Will Pay For It In 2010?" These discussions will be lead by two great sets of internationally-known panelists and moderators.

And last but certainly not least, on behalf of the IEEE Electron Device Society which sponsors IEDM, Kaizad Mistry, Technical Program Chair, and Philip Wong, Technical Program Vice-Chair, I want to express our sincere appreciation to each of the members of the IEDM committee for the outstanding job they have done in planning and organizing the 2005 conference. Likewise, all of the authors are to be commended for their tremendous efforts in preparing and sharing their latest work with us, covering so many fields of great importance and interest to our global technical audience.

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2005 IEEE International Electron Devices Meeting.

Jon Candelaria
General Chair

SHORT COURSES

Sunday, December 4, 9:00 a.m. - 5:30 p.m.
International Ballroom East, International Ballroom Center

PLENARY SESSION

Monday, December 5, 9:00 a.m. - 12:00 p.m.
International Ballroom Center

PLENARY SESSION AWARD PRESENTATIONS

2004 Roger A. Haken Best Student Paper Award:

To: Masumi Saitoh, University of Tokyo

For the paper entitled: "Room Temperature Demonstration of Integrated Silicon Single-electron Transistor Circuits for Current Switching and Analog Pattern Matching"

2005 EDS Chapter of the Year Award

To: To Be Announced

"To an EDS chapter, based on the quantity and quality of the activities and programs implemented by the chapter."

2005 EDS Graduate Student Fellowship Award

To: Christopher Morris, University of Washington; Elena Smotrova, National Academy of Sciences of Ukraine; Sun-Jung Kim, The National University of Singapore; and Tony Aik Seng Low, The National University of Singapore "

"To promote, recognize, and support graduate level study and research within the Electron Devices Society's field of interest."

2005 George E. Smith Award

To: Zhi-Yuan Charles Cheng, Arthur J. Pitera, Minjoo Larry Lee, Jongwan Jung, Judy L. Hoyt, Dimitri A. Antoniadis, and Eugene A. Fitzgerald

For the paper entitled: "Fully Depleted Strained-SOI n- and p-MOSFETs on Bonded SGOI Substrates and Study of the SiGe/BOX Interface"

2005 Paul Rappaport Award

To: Franco Stellari, Peilin Song, James C. Tsang, Moyra K. McManus and Mark B. Ketchen

For the paper entitled: "Testing and Diagnostics of CMOS Circuits Using Light Emission from Off-State Leakage Current"

2005 IEEE/EDS Fellows

(Only includes those who requested to be recognized at the IEDM)

Supriyo Bandyopadhyay, Virginia Commonwealth University, Richmond, VA, USA

"For contributions to device applications of nanostructures."

Duane S. Boning, Massachusetts Institute of Technology, Cambridge, MA, USA

"For contributions to modeling and control in semiconductor manufacturing."

Jeff D. Bude, Agere Systems, New Providence, NJ, USA

"For contributions to the deep submicron MOSFETs."

Robert S. Chau, Intel Corporation, Beaverton, OR, USA

"For contributions to gate dielectric and transistor technology for microprocessors."

Guido V. Groeseneken, IMEC, Leuven, Belgium

"For his contributions to the physical understanding and the modeling of reliability of metal oxide semiconductor field effect transistors."

James Albert Hutchby, Semiconductor Research Corp., Research Triangle Park, NC, USA

"For leadership in the development of high-efficiency solar cells and heterojunction bipolar transistors."

Masaaki Kuzuhara, University of Fukui, Japan
"For contributions to group III-V microwave devices."

John Melngailis, University of Maryland, College Park, MD, USA

"For contributions to focused ion beam applications."

Mehrdad J. Moslehi, Semizone Inc., Palo Alto, CA, USA

"For contributions to single wafer processing technologies."

Laurence W. Nagel, Omega Enterprises, Randolph, NJ, USA

"For contributions to the field of integrated circuit simulation."

Hidehito Obayashi, Hitachi High-Technologies Corporation, Hitachinaka, Ibaraki, Japan
"For contributions to critical dimension scanning electron microscopy."

Yutaka Ohmori, Osaka University, Suita, Osaka, Japan
"For contributions to the development of organic and semiconductor light emitting materials and devices."

Enrico Sangiorgi, University of Bologna, Cesna, FC, Italy
"For contributions to the modeling and characterization of hot carriers and non stationary transport effects in small silicon devices."

Tangali S. Sudarshan, University of South Carolina, Columbia, SC, USA
"For contributions to surface flashover of dielectric and semiconductor materials."

Juzer M. Vasi, Indian Institute of Technology (IIT), Bombay, Mumbai Maharashtra, India
"For leadership in microelectronics education."

Sophie V. Verdonckt-Vandebroek, Xerox Corporation, Webster, NY, USA
"For leadership in developing document systems."

Donald Coolidge Wunsch, University of Missouri - Rolla, Rolla, MO, USA
"For contributions to hardware implementations of reinforcement and unsupervised learning."

2005 EDS Distinguished Service Award

To: Cary Y. Yang

"To recognize and honor outstanding service to the Electron Devices Society."

2005 J.J. Ebers Award

To: To Be Announced

"To honor a single or a series of contributions of recognized scientific, economic, or social significance in the broad field of electron devices"

RECEPTION

Monday, December 5, 6:00 p.m. - 7:30 p.m.
International Ballroom Center

IEDM LUNCHEON

Tuesday, December 6
12:20 p.m. - 2:00 p.m.
International Ballroom West

2005 IEEE Cledo Brunetti Award

To: William Oldham, University of California, Berkeley

"For pioneering contributions to lithographic engineering and to high-density isolation technology"

2005 IEEE Andrew S. Grove Award

To: Tso-Ping Ma, Yale University

"For contributions to the development and understanding of CMOS gate dielectrics"

2005 IEEE David E. Noble Award

To: David L. Harame, IBM

"For the development of manufacturable Silicon Germanuim, HBT Bipolar and BiCMOS technologies"

LUNCHEON PRESENTATION

Luncheon Presentation: To Be Announced

PANEL SESSIONS

Tuesday, December 6
8:00 p.m. - 10:00 p.m.
International Ballroom East
International Ballroom Center

2005 iedm
international Electron Devices meeting

GENERAL INFORMATION

Hilton Washington
1919 Connecticut Avenue, NW
Washington, DC 20009
202-483-3000
December 5-7, 2005

REGISTRATION INFORMATION

	Advance (Postmarked by November 11th)	After November 11th or at Conference
Technical Session		
IEEE Member	$395.00	$435.00
Non-member	$485.00	$525.00
Students:		
Member	$ 50.00	$ 50.00
Non-Member	$ 85.00	$ 85.00
Short Courses		
Member	$400.00	
Non-member	$450.00	
Student	$100.00	

Short Courses (Due to limited space, it is recommended that you register in advance for the Short Courses)

Payment of the Technical Session registration fee entitles the registrant to one copy of the Technical Digest, one CD-ROM, one ticket for the Monday evening Wine and Cheese Reception and entrance to all technical sessions. Technical Session registration does not include entrance to the Short Courses. TO QUALIFY FOR THE MEMBER REGISTRATION FEE, REGISTRANT MUST BE A MEMBER OF IEEE PRIOR TO THE CONFERENCE.

Payment of the Short Course registration fee entitles the registrant to entrance to one short course, one copy of the course workbook and one copy of the CD-ROM of the short course workbook. Short Course registration does not include entrance to the Technical Sessions.

For Advance Registration, complete the Advance Registration Card (see centerfold) and return with remittance of appropriate registration fee NO LATER THAN NOVEMBER 11, 2005 to qualify for the early registration price. Due to limited space, it is recommended that you register in advance to attend the Short Courses.

Confirmations will be sent out to all conference registrants.

REGISTRATION FORM AND PAYMENT SHOULD BE SENT TO:

IEDM
16220 S. Frederick Avenue
Suite 312
Gaithersburg, MD 20877 USA
301-527-0900, ext 103

Checks MUST BE MADE PAYABLE TO IEDM, IN U.S. DOLLARS AND DRAWN ON A U.S. BANK. International registrants should not send wire transfers. If International participants cannot send a check prior to the conference, mail the registration form without payment prior to the conference. Bring payment with you and pay the registration fee onsite.

Your registration materials will be held for you at the conference. Your cancelled check is your receipt.

CANCELLATION POLICY: You are encouraged to register in advance for your own convenience. Due to printing and hotel commitments, refunds requested after November 11 cannot be guaranteed. A $30.00 processing fee will be withheld from ALL refunds.

REGISTRATION CENTER: The Conference Registration Center, located in the Lower Concourse of the Hilton Washington, will be open as follows:

SHORT COURSE REGISTRANTS ONLY

Saturday, December 3	5:00 p.m.- 7:00 p.m.
Sunday, December 4	8:00 a.m.- 12:00 p.m.

TECHNICAL SESSION REGISTRANTS

Sunday, December 4	2:00 p.m. - 5:00 p.m.
Monday, December 5	8:00 a.m. - 5:00 p.m.
Tuesday, December 6	8:30 a.m. - 5:00 p.m.
Wednesday, December 7	8:30 a.m. - 3:00 p.m.

HOTEL RESERVATIONS: A block of rooms at the Hilton Washington has been reserved for IEDM participants. Special IEDM room rates are as follows:

Single/Double: $186/$208
Plus a 14.05% city tax.

To make a reservation, please complete the Hotel Reservation Form (see centerfold) and return directly to the Hilton Washington NO LATER THAN NOVEMBER 10th to qualify for a room under our special rates. An advance deposit or credit card guarantee is necessary to hold your room, if arrival is scheduled after 6:00 p.m.

SHORT COURSES: The IEDM sponsors two short courses on Sunday, December 4, from 9 a.m. to 5:30 p.m. The courses are "Low Power 'System On Chip' CMOS Technology Platforms and "Next Generation Semiconductor Manufacturing" These courses will be presented by experts in the fields. Lectures will start with introductory material for the general audience and progress towards description of the latest developments.

To register, complete the Advance Registration form (see centerfold). The registration fee is $400 for members and $450 for non-members and includes a visuals booklet, CD-ROM, refreshments and lunch. Attendance is limited, so advanced registration is recommended.

EVENING PANEL DISCUSSIONS: On Tuesday evening, December 6, beginning at 8:00 p.m., the IEDM will offer two evening Panel Discussions on timely issues.

1. Will Non-Volatile Memory Technology Scale Past the End of the Decade?
2. Semiconductor Research and Development: Who Will Do It and Who Will Pay For It In 2010?

SPEAKER PREPARATION ROOM: The IEDM will sponsor a Speaker Preparation Room for speakers to preview their presentations. Speakers must preview their presentations 1 day in advance. There will be no previewing of presentations the day of the presentation.

The Speaker Ready Room will be open for speaker use:

Saturday, December 3	5:00 p.m. – 7:00 p.m.
Sunday, December 4	8:00 a.m. – 5:00 p.m.
Monday, December 5	8:00 a.m. – 5:00 p.m.
Tuesday, December 6	8:00 a.m. – 5:00 p.m.
Wednesday, December 7	8:00 a.m. – 12:00 p.m.

IEDM LUNCHEON: The IEDM luncheon will be held on Tuesday, December 6, at 12:20 p.m. in the International Ballroom West. Luncheon tickets are available through Advance Registration or on-site at a cost of $45.00 to conference attendees only.

WINE AND CHEESE RECEPTION: A Wine and Cheese Reception for conference participants and their guests will be held on Monday, December 5 from 6:00 p.m. to 7:30 p.m. in the International Ballroom. ONE ADMISSION TO THE RECEPTION IS INCLUDED IN THE REGISTRATION FEE.

TECHNICAL DIGEST and CD-ROM: Extra copies of the Technical Digest/CD-ROM can be purchased by conference registrants through Advance Registration. A LIMITED number of Digests will be for sale after 2:00 p.m. on Tuesday, December 6 at the On-Site Registration Desk of the Conference. The unit cost of the Digest, if ordered through Advance Registration or purchased on-site is $125.00. Digests will be available after the conference by mail from IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855. Customer Service Department 732-981-0060 or toll free: 800-678-4333, email is customer-service@ieee.org. ONE COPY OF THE TECHNICAL DIGEST/CD-ROM IS INCLUDED IN THE REGISTRATION FEE.

MEMBERSHIP PROMOTION FOR NON-IEEE MEMBERS: Conference registrants will be able to join IEEE, and the Electron Devices Society (EDS) during the conference at the IEEE Membership Desk located in the Registration Center. If you registered and paid for the conference as a non-member, you will be receiving a CREDIT voucher worth $25 towards an IEEE membership, and free EDS membership for one year (worth $11). STUDENTS registering at the student, non-member rate will receive a credit voucher that will entitle them to one-year of FREE IEEE and EDS memberships.

MEMBERSHIP PROMOTION FOR CURRENT IEEE MEMBERS: FREE Electron Devices Society membership for one-year will be offered to any IEEE member attending the IEDM who is not currently a member of EDS. A FREE EDS Membership Credit Voucher will be available at the IEEE Membership Desk. Just complete the voucher by providing your name, address and member number and submit it at the Membership Desk. If you are currently a member of EDS, you cannot use this voucher to renew your membership. Credit vouchers are only valid at the IEDM and must be redeemed at the IEEE Membership Desk. Copies of the 2006 EDS Membership Brochure are

also available at the Membership Desk, which will be open the following hours:

Monday, December 5	9:00 a.m. - 5:00 p.m.
Tuesday, December 6	9:00 a.m. - 5:00 p.m.
Wednesday, December 7	9:00 a.m. - 3:00 p.m.

MESSAGE CENTER: An IEDM Message Board will be in operation in the Registration Center during registration hours. Please advise callers who wish to reach you during the day to ask the hotel operator 202-483-3000 for the IEDM Conference Message Desk. Please check the message board periodically.

ROGER A. HAKEN BEST STUDENT PAPER: The 2004 Roger A. Haken Best Student Paper will be presented on Monday, December 5, at the Plenary Session to Masumi Saitoh, University of Tokyo for the paper entitled, "Room Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching."

One paper presented by a student at the 2005 IEDM will be selected for the 2005 Best Student Paper Award. To be eligible, the paper must be based on the student's own work and have been identified as a student paper at the time of submission. Presentation of the award will be made at the 2006 IEDM.

BADGES: Badges are required for admittance to all sessions and the Wine and Cheese Reception. Please wear your badge at all times while attending the conference, so that you will not be delayed entry to a session.

PRESS ROOM: Beginning on Monday, the Press Room, will be in operation during registration hours.

AIRPORT TRANSPORTATION: The Washington Flyer Shuttle Bus and taxi service is available from the Ronald Reagon National Airport and Dulles Int'l to the Hilton Washington. The following estimated rates are subject to change:
Washington Flyer Suttle Bus - $20 one way/ $30 round Trip
Taxi - $50 one way

RECRUITING: In keeping with the long standing tradition of fostering a low key, research oriented atmosphere for the IEDM, the Conference Committee and the Electron Devices Society of the IEEE discourage overt and highly visible recruiting activities in association with the IEDM. IEEE

policy #9.l8 prohibits recruiting at IEEE-sponsored conferences, consequently, recruiters and recruitment advertisements will not be permitted in IEDM hotel space or meeting facilities and all unauthorized material will be removed from the premises.

PLEASE DIRECT CONFERENCE INQUIRIES TO:

Phyllis Mahoney
2005 IEDM
16220 S. Frederick Road, Suite 312
Gaithersburg, MD 20877 USA
TEL: 301/527-0900 EXT. 103
FAX: 301/527-0994
EMAIL: phyllism@widerkehr.com

2005 IEDM Conference and Program Committee

Seated from left to right: Paolo Pavan, Europeon Arrangements Co-Chair, Ralf Brederlow, Short Course Chair, Vivek Subramanian, Publicity Vice Chair, Kaizad Mistry, Technical Program Chair, Jon Candelaria, General Chair, H.-S. Philip Wong, Technical Program Vice Chair, Thomas Bonifield, Publicity Chair, Thomas Skotnicki, European Arrangements Co-Chair

Standing from left to right: Phyllis Mahoney, Conference Planner, Akintunde Akinwande, Diplays, Sensors and MEMS Chair, Carlos Diaz, Asian Arrangements Co-Chair, Conor Rafferty, Modeling and Simulation Chair, Toshiro Hiramoto, CMOS Devices Chair, Chris Auth, Short Course Vice Chair, Ashraf Alam, CMOS and Interconnect Reliability Chair, Kazunari Ishimaru, Asian Arrangements Co-Chair, Glen Wilk, Process Technology Chair, Gaudenzio Meneghesso, Quantum Power and Compound Semiconductor Devices Chair, Bruce White, Solid State and Nanoelectronic Devices Chair, Meikei Ieong, Publications Chair, Luan Tran, Integrated Circuits and Manufacturing Chair, Melissa Widerkehr, Conference Planner

Missing: Veena Misra, Emerging Technologies Chair

SHORT COURSE: Low Power "System On Chip" CMOS Technology Platforms

Sunday, December 4, 9:00 a.m. – 5:30 p.m.
International Ballroom Center

Course Organizers: Margaret Huang, Freescale Semiconductor
Suresh Venkatesan, Freescale Semiconductor

Low Power technologies serve the rapidly growing portable electronics market including laptop computers, PDAs, cell phones, WLAN/WPAN connectivity devices, MP3 players, etc. A wide range of semiconductor technologies and design techniques serve this market. This short course will focus on CMOS SoC technology platform technologies and design techniques essential for enabling this market segment.

The short course is organized to focus on three areas: technology, design and modeling. The first lecture will discuss the requirements and transistor design issues in current and future low power technologies. The course will focus on issues and tradeoffs between low standby and low active power device design and will conclude with requirements for future innovations in low power process and transistor design. The second lecture will discuss embedded memory technologies critical for low power systems. Challenges and technology requirements as well as trends in embedded SRAM, DRAM, NV memory and emerging memory technologies will be discussed. The third and fourth lecture will cover digital and analog/RF circuit design aspects with special emphasis on technology and circuit co-optimization for low power systems using nanometer CMOS technologies. The digital design section will discuss general challenges for low power technology, discuss in detail circuits for leakage avoidance, control and tolerance, low power architectures and various system power management concern and conclude with discussion on technology, circuits, architecture and system co-optimization. The lecture on analog/RF designs will cover the impact of scaled CMOS on key design Figures-of-Merit, followed by discussion on specific analog/RF design blocks and the challenges for technology and design co-optimization for designs such as Op-Amps, converters, LNAs and VCOs. The final lecture will focus on modeling of scaled CMOS with emphasis on the modeling aspects critical for low power systems. Reduced supply voltages and the push to operate at low currents mean that the accuracy of near- and below-threshold modeling for MOSFETs is of prime importance, yet this is precisely where many existing models have the least physical accuracy. Modern surface-potential based models are recognized as the most physical and accurate near threshold, and will be reviewed in detail. Other critical near threshold modeling aspects including variability, noise and leakage current will also be discussed. Through this series of lectures, a comprehensive overview of state of the art Low Power SoC CMOS platforms will be provided.

Process Technology

Instructor: Scott Crowder, IBM

What is a Low Power Process?
- Low Standby vs. Low Active Power
- Low Cost vs. High Performance

Transistor Design for Low Standby Power
- Standby Power Components

Scaling Challenges
- Methods for Parasitic Leakage Reduction
- Materials/Innovations for Performance Scaling

Transistor Design for Low Operating Power
- Operating Power Components

Scaling Challenges
- Mobility Engineering
- Materials/Innovations for Performance Scaling

Additional Requirements for Low Power "System On Chip" Technology
- BEOL Scaling
- Passive Elements

Embedded Memory Technology for Low Power Systems

Instructor: Yasushi Yamagata, NEC Electronics

Importance of Embedded Memory
- Memory Content Trend
- Single-Core to Multi-Core

SRAM Challenges with Device Scaling
- Low Voltage Operation
- Device Variability
- Leakages
- SER
- Solution Candidate

Embedded DRAM
- Advantage/Requirement of Embedded DRAM
- Technology Trend
- Trench vs.Stack

Embedded DRAM Application

Embedded NV Memory
- Advantage/Requirement of Embedded NV
- Technology Trend
- Floating Gate vs. Charge Trap
- Embedded Flash for ROM Replacement

Emerging Memory Technology
- Overview of Various Technologies – Performance Trade-offs
- MRAM Technology - Issues and Future Prospects
- Nano-Bridges

Digital Design for Low Power Systems

Instructor: Shekhar Borkar, Intel

Active and Leakage Power Challenges
- Technology Outlook
- Active and Leakage Power Projections
- Cost

Circuits for Leakage Avoidance, Control, and Tolerance
- Dual Vt, Body Bias, Stack Effect, and Sleep Transistor Techniques
- Leakage Tolerant High Performance Circuits
- Leakage Control for Memory Circuits

Microarchitectures for Low Power
- Optimum Logic Pipelines
- Throughput Oriented Designs
- Multi-Everywhere: From Threads To Cores
- Technology and Design Co-Optimization Challenges

System Power Management
- Fine Grain Power Management
- Power Delivery
- Low Power Platform Design
- Power Management Software

Technology, Circuits, Microarchitecture, and System Co-Optimization

Analog/RF Design in Nanometer CMOS Technologies

Instructor: Willy Sansen, KU Leuven

Impact of Nanometer Channel Lengths on Transistor Performance
- Intrinsic Gain Reduction
- Speed Enhancement
- Noise - Thermal and 1/f Noise
- Offset
- Distortion Cancellation

Operational Amplifiers with Supply Voltage Below 1 V and with Minimum Power Consumption
- Gate-Driven, Bulk-Driven
- Single-Stage Amplifiers
- Two-Stage Miller Op-Amps
- Multi-Stage Amplifiers
- Technology and Design Co-Optimization Challenges

Low-Voltage Low-Power Delta-Sigma A-to-D Converters
- Switched Op-Amp Approach
- Full-Feedforward Approach
- Input-Series-Resistor Approach
- Technology and Design Co-Optimization Challenges

Communication Circuits
- VCO's with Low Phase Noise
- LNA's with Low Noise Figure
- Technology and Design Co-Optimization Challenges

Modeling for Digital and AMS/RF Design

Instructor: Colin McAndrew, Freescale Semiconductor

Overview
- Modeling Challenges and needs for Low-Power
- Additional Challenges from Technology Scaling
- Digital and Analog Needs
- Linkage to Circuit and System Level Design and Simulation

MOSFET Modeling
- Accurate Near-Threshold Modeling, State-of-the-Art Surface Potential Models
- Variability Exacerbation from Technology Scaling and Low Power Operation
- Noise
- Proximity Effects

Passive and Parasitic Modeling
- Shift in the Nature of Parasitic Capacitances, Dependence on Adjacent Structures
- Difficulties in Modeling of and Importance of Leakage for Static Power

System Level Modeling
- System and Architecture Level Modeling and Optimization for Low Power Design
- Dynamic and Static Power Dissipation

SHORT COURSE: Next Generation Semiconductor Manufacturing

Sunday, December 4, 9:00 a.m. - 5:30 p.m.
International Ballroom East

Course Organizer: *C. Rinn Cleavelin, Texas Instruments*

The last 2-3 generations of semiconductor manufacturing have presented some unique challenges. As the traditional scaling laws have started to slow, new materials have been increasingly added in order to continue the consistent gains in performance. These new materials have placed new requirements beyond just the typical scaling of feature sizes. Additionally the varieties of end-user requirements for ICs have led to a proliferation of processes tailored to the features of the application. These shifts have led to a need for substantial innovation in order to enable manufacturing of multi-core, multi-GHz microprocessors, multi-Gb memories, and low power SoCs. Frequently in the same factory! This short course will examine the requirements for the processes, from FEOL and BEOL to packaging to yield and reliability, that will be needed in order to produce these chips at high performance, high density and low cost. Through the five lectures, the speakers will detail the state of the art in process technology, the trends in development and provide insight into what the next generation of semiconductor manufacturing will look like.

The first lecture consists of an overview of the state of semiconductor manufacturing and what the future holds. This includes the global business trends, the impacts of introducing new materials and novel device architectures, and the outlook for 450mm wafers. The second lecture focuses on the front end manufacturing technology, delving into the problems confronting the development of new substrates, strain techniques, scaled junctions and the anticipated changes to the gate stack. In the third lecture, the speaker will detail the challenges in the back end manufacturing technology, including the material options for the interlayer dielectrics and interconnect metals, the integration issues with introducing these materials and examining the overall strategy for development. With the variety of chip packages and the tight coupling of the BEOL processing and the package, the fourth lecture will focus on packaging. The speaker will cover the state of lead-free, Cu, Low-k packaging and the obstacles in development of next generation packages including heat dissipation, SoC and interconnect options. The final lecture will focus on the impacts of these new materials/structures on the yield and reliability of the dies. The speaker will address the inevitable new fail modes that will require innovation in testing, models, tools and solutions to enable high yield and reliable chips.

Introduction

Organizer: C. Rinn Cleavelin, Texas Instruments

Overview of the Next Generation of Semiconductor Manufacturing

Instructor: Jai Hakhu, Intel

Worldwide Semiconductor Business Trends at the 45nm Node and Beyond
New Technology Challenges
Key Areas for Manufacturing Concern
Manufacturing Headlights – where are we headed?
Outlook for 450mm wafers
Summary

Front End of Line Manufacturing Technology

Instructor: Raj Jammy, IBM/SEMATECH

- Brief Review of current generation
- Scaling trends: factors driving change
  - Power and performance
- Substrates
  - Ultra Thin Body SOI
  - sSOI/SGOI
  - Hybrid Orientation Technology (HOT)
- Gate Dielectrics
  - Scaled SiON
  - High k dielectrics
- Gate Electrodes
  - Doped poly-Si
  - Metal gates
- Junctions
  - Scaling considerations and impact of series resistance
  - Rapid thermal anneals vs mSec anneal technologies
- Strain Engineering
  - Uniaxial vs biaxial
  - SiGe and stress liners
- Likely elements for next generation CMOS
- Next generation low power technologies
- Issues in implementation of key elements
  - Integration challenges
  - Process development and control
  - Contamination concerns
  - Reliability concerns
- Manufacturability concerns
  - Tool maturity/availability
  - Process control
  - CoO
  - Metrology
  - Operational flexibility and agility
- Summary and outlook for future scalability and manufacturability

Back End of Line Manufacturing Technology

Instructor: Hans-Joachim Barth, Infineon

Scope
Interconnect Scaling Directions
- Interconnect hierarchy

Materials and Processes
- overview established materials & processes (180nm-65nm node)
- Low k materials
- Thermo-mechanical properties & stress (oxide, dense & porous-low k)
- development of CVD low k precursors (3MS ‡ cyclic)
- Barriers & Cu seed
- ionized-PVD (pre-clean, re-sputtering approaches)
- ALD-barriers
- Cu – seed/plating/CMP

Integration Challenges
- Dual damascene integration
- Etch, ash & clean
- Barrier / low k interaction
- Adhesion & moisture control

Manufacturing and Tool Strategy
- Tool strategy & costs
- New metrology challenges
- Advanced process control strategy
- Frontside & backside cleans
- Wafer edge control

Future Interconnect Strategy
- limitations of material innovations
- design options
- evolutional approach (e.g. airgaps, 3D-IC stacking)
- future connectivity (e.g. RF & optical on chip, nanotubes)

Conclusions and future outlook

Packaging & the Integration with BEOL Manufacturing

Instructor: Charles Lee, Infineon Technologies Asia Pacific

Packaging trends and challenges
The impact of environmental friendly (Pb- and halogen-free) packaging
Cu/low-k packaging issues
System integration: SOC (System On Chip) vs SIP (System In Package) approach
Future outlook
Summary

Reliability & Yield

Instructor: Joe McPherson, Texas Instruments

Outline
General scaling trends impacting reliability & yield
New materials integration with conventional scaling
- Ultra-thin SiOxNy gate-dielectric scaling
- High-k gate dielectrics
- Metal gates
- Low-k interconnect dielectrics

Old materials integration with novel structures
- Strained Silicon
- Cladded Cu

Non-planar devices
Defect Detection
Wafer-level Monitoring —- diminishing returns
Physical Failure Analysis —- diminishing returns
Electrical Failure Analysis —- defect modeling required
Defect test structures —- physics-based defect structures required
Major reliability challenges for continued CMOS scaling
Stress migration
Electromigration
Interconnect Cracks and Delamination
Low-k TDDB
Ultra-thin SiOxNy TDDB
High-k TDDB
NBTI
Plasma Charging
Thermo-Mechanical Failures
Soft-Errors
ESD
Power Dissipation
Design-In Reliability
Build-in Reliability
SoC Challenges
Power density
Stacked Die
Beyond CMOS
Reinventing CMOS
"Nanoelectronics"
Molecular Electronics

Plenary Session

Monday, December 5, 9:00 a.m.
International Ballroom Center

Welcome and Awards

General Chair: Jon Candelaria, Motorola

Invited Papers

Technical Program Chair: Kaizad Mistry, Intel

1.1 More Than Moore: Micromachined Products Enable New Applications and Open New Markets, Benedetto Vigna, ST Microelectronics

Micro-Electromechanical Systems are not driven by the lithography scaling law, like memories and microprocessors. New manufacturing dimensions become relevant for the commercialization and the success of MEMS products and in the last years the rate of success of MEMS products increased tremendously. Bulk Acoustic Wave filters, 3-axis accelerometers for consumers markets, silicon Microphone and Micro-mirrors for projectors took off recently enabling new applications and enhancing the features of the current products. MEMS can substitute current products offering the advantage of lower size, greater reliability and lower power consumption, but can enable totally new applications like the data protection in Hard Disk Drive based devices. All the technical and business experts believe that after the "Nomadic Era" Wireless Sensor Networks and Domestic

Robots will represent the next big commercial wave for semiconductors. And MEMS will be one of the key enabler products for these new markets and applications. The talk will give a picture of the current and future prospects of MEMS technologies, products and applications.

1.2 **Scaling, Power and the Future of CMOS**, Mark Horowitz, Stanford University and Rambus, Inc.

In the mid 1980's the power growth that accompanied scaling forced the industry to focus on CMOS technology, and leave nMOS and bipolars for niche applications. Now 20 years later, CMOS technology is facing power issues of its own. After first reviewing the "cause" of the problem, it will become clear that there are not easy solutions this time — no new technology or simple system/circuit change will rescue us. Power, and not number of devices is now the primary limiter of chip performance, and the need to create power efficient designs is changing how we do design. This talk will review power optimized design methods and shows how power is strongly tied to performance and that variability aversely effects power efficiency. Projecting forward, it shows that unless die size shrinks, in future technologies most of the devices will need to be idle most of the time which has strong ramifications for the both the underlying device and system design.

1.3 **Past and Future of Information Displays**, Kouji Suzuki, Toshiba Corp. and SED, Inc.

A concise summary will be given of the history of display technology and new display devices coming in the near future. CRT (Cathode Ray Tube) display including CRT projection display was for a long time the only device capable of exhibiting moving picture images applicable to TV receivers. To improve bulky and heavy structure of CRT, FPDs (flat panel displays) have been developed and available in the market nowadays. Typical FPDs, namely LCD (Liquid Crystal Display) and PDP (Plasma Display Panel), have been applied to TV sets. Especially, LCD has many application fields, because of its size variation and high-resolution capability. However, picture quality of current FPD are still inferior to that of the CRT, and new types of flat panel display with high picture quality under development will come into the market in the near future. Some examples are OLED (Organic Light Emitting Diode) and FED (Field Emission Display). The presentation will also introduce key technologies which realize those displays.

Session 2: Process Technology – High-k I Metal Gate Stacks

Monday, December 5, 1:30 p.m.
International Ballroom West

Co-Chairs: Franck Arnaud, STMicroelectronics
Min Yang, IBM

1:35 p.m.
2.1 **A Thermally-Stable Sub-0.9nm EOT TaSix/HfSiON Gate Stack with High Electron Mobility Suitable for Gate-First Fabrication of hp45 LOP Devices**, S. Inumiya, Y. Akasaka, T. Matsuki, F. Ootsuka, K Torii and Y. Nara, Selete, Ibaraki, Japan

2:00 p.m.
2.2 **Advanced MOSFETs Using HfTaON/SiO_2 Gate Dielectric**

and TaN Metal Gate with Excellent Performances for Low Standby Power Application, X. Yu*, C. Zhu*, M. Yu^ M. F. Li*'^, A. Chin**, C. H. Tung^, D. Gui^^, D.-L. Kwong^, *National University of Singapore, Singapore, ^Institute of Microelectronics, Singapore, **National Chiao Tung University, Taiwan, ^^Chartered Semiconductor Manufacturing Ltd., Singapore

2:25 p.m.
2.3 **High Performance Tantalum Carbide Metal Gate Stack for nMOSFET Application**, Y.T. Hou, F.Y. Yen, P.F. Hsu, V.S. Chang, P.S. Lim, C.L. Hung, L.G. Yao, J.C. Jiang, H.J. Lin, Y. Jin, S.M. Jang, H.J. Tao, S.C. Chen, M.S. Liang, TSMC, Hsinchu, R.O.C.

2:50 p.m.
2.4 **Microstructure Modified HfO_2 Using Zr Addition with Ta_xC_y Gate for Improved Device Performance and Reliability**, R.I. Hegde, D.H. Triyoso, P.J. Tobin, S. Kalpat, M.E. Ramon, H.-H. Tseng, J.K. Schaeffer, E. Luckowski, W. J. Taylor, C. C. Capasso, D. C. Gilmer, M. Moosa, A. Haggag, M. Raymond, D. Roan, J. Nguyen, L.B. La, E. Hebert, R. Cotton, X-D. Wang, S. Zollner, R. Gregory, D. Werho, R.S. Rai, L. Fonseca, M. Stoker, C. Tracy, B.E. White Jr., Freescale Semiconductor Inc., Austin, TX

3:15 p.m.
2.5 **Universal Theory of Workfunctions at Metal/Hf-Based High-k Dielectrics Interfaces — Guiding Principles for Gate Metal Selection**, K. Shiraishi[1,2], Y. Akasaka[3], S. Miyazaki[4,2], T. Nakayama[5], T. Nakaoka[1], G. Nakamura[3], K. Torii[3], H. Furutou[4], A. Ohta[4], P. Ahmet[2], K. Ohmori[2], H. Watanabe[6], T. Chikyow[2], M. L. Green[7], Y. Nara[3], K. Yamada[8,2], [1]University of Tsukuba, Tsukuba, Japan, [2]NIMS, Tsukuba, Japan, [3]Selete, Tsukuba, Japan, [4]Hiroshima University, Hiroshima, Japan, [5]Chiba University, Chiba, Japan, [6]Osaka University, Osaka, Japan, [7]NIST, Gaithersburg, MD, [8]Waseda University, Tokyo, Japan

3:40 p.m.
2.6 **Dependence of PMOS Metal Work Functions on Surface Conditions of High-k Gate Dielectrics**, R. Jha, B. Lee, B. Chen, S. Novak, J. Lee, P. Majhi*, V. Misra, North Carolina State University, Raleigh, NC, *Intel Sematech Assignee, Austin, TX

Session 3: Integrated Circuits and Manufacturing – Advanced CMOS and Platform Technology

Monday, December 5, 1:30 p.m.
International Ballroom Center

Co-Chairs: Shih-Fen Huang, IBM
Yee-Chaung See, TSMC

1:35 p.m.
3.1 **Lithography for Manufacturing of Sub-65nm Nodes and Beyond (Invited)**, B. J. Lin, TSMC, Taiwan, R.O.C.

2:00 p.m.
3.2 **45-nm Node CMOS Integration with a Novel-STI Structure, and Full-NCS/Cu Interlayers for Low-Operation-Power (LOP) Applications**, M. Okuno, K. Okabe, T.

Sakuma, K. Suzuki, T. Miyashita, T. Yao, H. Morioka, M. Terahara, Y. Kojima*, H. Watatani, K. Sugimoto, T. Watanabe, Y. Hayami, T. Mori, T. Kubo, Y. Iba, I. Sugiura, H. Fukutome, Y. Morisaki, H. Minakata, K. Ikeda, S. Kishii, N. Shimizu, T. Tanaka, S. Asai, M. Nakaishi, S. Fukuyama, A. Tsukune, M. Yamabe, M. Miyajima, K. Kase*, K. Watanabe*, S. Sato, T. Sugii, Fujitsu Laboratories Ltd, Fujitsu Limited, Akiruno, Japan, *Mie, Japan

2:25 p.m.

3.3 **High Performance 65 nm SOI Technology with Enhanced Transistor Strain and Advanced-Low-K BEOL,** W-H. Lee, A.Waite*, H. Nii**, H. M. Nayfeh, V. McGahay, H. Nakayama^, D. Fried, H. Chen, L. Black*, R. Bolam, M. Cullinan-Scholl , C. Christiansen, D. Chidambarrao , D. R. Davies, A. Domenicucci, P. Fisher*, J. Fitzsimmons, J. Gill, M. Gribelyuk, D. Harmon, J. Holt, K. Ida^, M. Kiene*, J. Kluth*, C. Labelle*, D. Mocuta, S. Panda, M. Newport, A. Madan, K. Malone, P. V. McLaughlin, M. Minami^, R. Murphy, C. Muzzy, I. Peidous*, T. Sato**, A. Sakamoto^, G. Sudo**, T. Yamashita^, H. Zhu, P. Agnello, G. Bronner G. Freeman, S-F Huang, T. Ivers, S. Luning*, K. Miyamoto**, J. Pellerin*, K. Rim, D. Schepis, T. Spooner, H. Nye, X. Chen, M. Khare, M. Horstmann^^, A. Wei^^, T. Kammler^^, J. Höntschel^^, H. Bierstedt^^, H.-J. Engelmann^^, A. Hellmich^^, K. Hempel^^, G. Koerner^^, A. Neu^^, R. Otterbach^^, C. Reichel^^, M.Trentsch^^, P. Press^^, K. Frohberg^^, M. Schaller^^, H. Salz^^, J. Hohage^^, H. Ruelke^^, J. Klais^^, M. Raab^^, D. Greenlaw^^, N. Kepler^^, IBM Systems and Technology Group, *Advanced Micro Devices Inc. at IBM SRDC, **Toshiba America Electronic Components Inc., ^Sony Electronics Inc., Hopewell Junction, NY, ^^AMD Saxony LLC & Co. K.G., Dresden, Germany

2:50 p.m.

3.4 **A 65nm Ultra Low Power Logic Platform Technology Using Uni-axial Strained Silicon Transistors**, C.-H. Jan, P. Bai, S. Jacobs, K. Johnson, D. Jones, S. Klopcic, J. Lin, N. Lindert, A. Lio, S. Natarajan, J. Neirynck, P. Packan, I. Post, M. Patel, S. Ramey, P. Reese, A. Roskowski, Y. Wang, L. Wei, I. Young, K. Zhang, Y. Zhang, M. Bohr, B. Holt, Intel Corporation, Hillsboro, OR

3:15 p.m

3.5 **65nm CMOS Technology for Low Power Applications**, A. Steegen, R. Mo, R. Mann, M.-C. Sun^, M. Eller**, G. Leake, D. Vietzke**, A. Tilke**, F. Guarin, A. Fischer**, T. Pompl**, G. Massey, A. Vayshenker, W.-L. Tan*, A. Ebert, W. Lin*, W. Gao*, J. Lian**, J.-P. Kim^, P. Wrschka, J.-H. Yang^, A. Ajmera, R. Knoefler**, Y.-W. Teh*, F. Jamin, J.E. Park^, K. Hooper, C. Griffin, P. Nguyen, V. Klee**, V. Ku, C. Baiocco, G. Johnson, L. Tai, J. Benedict, S. Scheer, H. Zhuang**, V. Ramanchandran, G. Matusiewicz, Y.H. Lin, Y.K. Siew*, F. Zhang*, L.S. Leong*, S.L. Liew*, K.C. Park^, K.-W. Lee^, D.H. Hong^, S.-M. Choi^, E. Kaltalioglu**, S.O. Kim**, M. Naujok**, M. Sherony, A. Cowley, A. Thomas, J. Sudijono*, T. Schiml**, J.-H. Ku^, I. Yang, IBM SRDC, *Chartered Semiconductor Manufacturing, **Infineon Technologies AG, ^Samsung Electronics Co., Hopewell Junction, NY

3:40 p.m.

3.6 **System LSI Multi-Vth Transistors Design Methodology for Maximizing Efficiency of Body-Biasing Control to Reduce**

Vth Variation and Power Consumption, Y. Yasuda, N. Kimizuka, Y. Akiyama, Y. Yamagata, Y. Goto, K. Imai, NEC Electronics Corporation, Kanagawa, Japan

4:05 p.m.
3.7 Application of On-Chip MIM Decoupling Capacitor for 90nm SOI Microprocessor, D. Roberts, W. Johnstone, H. Sanchez, O. Mandhana, D. Spilo, J. Hayden, E. Travis, B. Melnick, M. Celik, B. W. Min, J. Edgerton, M. Raymond, E. Luckowski, C. Happ, A. Martinez, B. Wilson, P. Leung, T. Garnett, D. Goedeke, T. Remmel, K. Ramakrishna, B. White, Freescale Semiconductor Inc., Austin, TX

Session 4: Process Technology – Advanced Interconnect Technology

Monday, December 5, 1:30 p.m.
International Ballroom East

Co-Chairs: Victor Wang, Freescale Semiconductor
Gerald Beyer, IMEC

1:35 p.m.
4.1 A Robust 45 nm-node, Dual Damascene Interconnects with High Quality Cu/barrier Interface by a Novel Oxygen Absorption Process, M. Abe, M. Tada, H. Ohtake, N. Furutake, M. Narihiro, K. Arai, T. Takeuchi, S. Saito, T. Taiji*, K. Motoyama*, Y. Kasama*, K. Arita*, F. Ito, H. Yamamoto, M. Tagami, T. Tonegawa*, Y. Tsuchiya*, K. Fujii*, N. Oda*, M. Sekine*, Y. Hayashi, NEC Corporation, Kanagawa, Japan, *NEC Electronics, Kanagawa, Japan

2:00 p.m.
4.2 High Performance k=2.5 ULK Backend Solution Using an Improved TFHM Architecture, Extendible to the 45nm Technology Node, R. Fox, O. Hinsinger*, E. Richard**, E. Sabouret*, T. Berger*, C. Goldberg, A. Humbert**, G. Imbert*, P. Brun^, E. Ollier**, C. Maurice, M. Guillermet^, C. Monget*, V. Plantier**, H. Bono*, M. Zaleski, M. Mellier**, J.-P. Jacquemin**, J. Flake, B. G. Sharma, L. Broussous*, A. Farcy*, V. Arnal*, R. Gonella*, S. Maubert, V. Girault*, P. Vannier*, D. Reber, A. Schussler**, J. Mueller, W. Besling**, Freescale Semiconductor, *STMicroelectronics, **Philips Semiconductors, ^CEA-LETI, Crolles Cedex, France

2:25 p.m.
4.3 Integration of Cu and Extra Low-k Dielectric (k=2.5~2.2) for 65/45/32nm Generations, Y.N. Su, J.H. Shieh, J.S. Tsai, C.Y.Ting, C.H. Lin, C.L. Chou, J.W. Hsu, S.M. Jang, M.S. Liang, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan

2:50 p.m.
4.4 Interconnect Issues Post 45 nm (Invited), S.M. Rossnagel, R. Wisnieff, D. Edelstein, and T.S. Kuan*, IBM Research Div, Yorktown Heights, NY, * SUNY-Albany, NY

3:15 p.m.
4.5 Advanced Scalable Ultralow-k/Cu Interconnect Technology for 32- nm CMOS ULSI Using Self-Assembled Porous Silica and Self-aligned CoWP Barrier, T. Kikkawa*^, S. Chikaki**, R. Yagi**, M. Shimoyama**, Y. Shishida**, N. Fujii**, K. Kohmura**, H. Tanaka**, T. Nakayama**, S. Hishiya**, T. Ono**, T. Yamanishi**, A. Ishikawa**, H.

Matsuo**, Y. Seino*, N. Hata*, T. Yoshino*, S. Takada*, J. Kawahara**, K. Kinoshita**, *MIRAI-AIST, **MIRAI-ASET, Tsukuba, Japan, ^Hiroshima University, Hiroshima, Japan

Session 5: Displays, Sensors, and MEMS – Organic and Flexible Electronics

Monday, December 5, 1:30 p.m.
Georgetown Room

Co-Chairs: Arokia Nathan, Univerisity of Waterloo
William Milne, Univerisity of Cambridge

1:35 p.m.
5.1 A Flexible, Lightweight Braille Sheet Display with Plastic Actuators Driven by An Organic Field-Effect Transistor Active Matrix, Y. Kato, S. Iba, T.Sekitani, Y. Noguchi, K. Hizu, X. Wang, K. Takenoshita, Y. Takamatsu, S. Nakano, K. Fukuda, K. Nakamura, T. Yamaue, M. Doi, K. Asaka*, H. Kawaguchi, M. Takamiya, T. Sakurai, T. Someya, University of Tokyo, Tokyo, Japan, *National Institute of Advanced Industrial Science and Technology, Osaka, Japan

2:00 p.m.
5.2 Thin Film Transistor Circuits Integrated onto Elastomeric Substrates for Elastically Stretchable Electronics, S. P. Lacour, S. Wagner, Princeton University, Princeton, NJ

2:25 p.m.
5.3 High Mobility Solution-Processed OTFTs, S. K. Park, C.-C. Kuo, J. E. Anthony*, T. N. Jackson, Penn State University, University Park, PA, *University of Kentucky, Lexington, KY

2:50 p.m.
5.4 Low-Voltage Inkjetted Organic Transistors for Printed RFID and Display Applications, S. E. Molesa, A. de la Fuente Vornbrock, P. C. Chang, V. Subramanian, University of California Berkeley, Berkeley, CA

3:15 p.m
5.5 Realization of a 5-stage Divider Circuitry in p-type Polymer Transistor Technology, C. Lackner, H. Klauk*, W. Gut, M. Halik*, R. Spilka, U. Zschieschang*, A. Tanda, F. Eder*, D. Rohde*, T. Ostermann, G. Schmid*, Johannes Kepler University of Linz, Linz, Austria, *Infineon Technologies, Erlangen, Germany

3:40 p.m.
5.6 High Performance Nanocrystalline-Si TFT Fabricated at 150ºC Using ICP-CVD, S.-M. Han, J.-H. Park, H.-S. Shin, Y.-H. Choi, M.-K. Han, Seoul National University, Seoul, Korea

4:05 p.m.
5.7 An Integrated Position-Sensing System for a MEMS-Based Cochlear Implant, J. Wang, M. Gulari, K. D. Wise, University of Michigan, Ann Arbor, MI

Session 6: CMOS Devices – Mobility Enhancement and Low Resistance Source/Drain

Monday, December 5, 1:30 p.m.
Jefferson Room

Co-Chairs: Frederic Boeuf, STMicroelectronics
Huiling Shang, IBM T.J. Watson Research Center

1:35 p.m.
6.1 **Physical Mechanisms of Electron Mobility Enhancement in Uniaxial Stressed MOSFETs and Impact of Uniaxial Stress Engineering in Ballistic Regime,** K. Uchida, T. Krishnamohan, K. C. Saraswat, Y. Nishi, Stanford University, Stanford, CA

2:00 p.m.
6.2 **New Findings on Inversion-Layer Mobility in Highly Doped Channel Si MOSFETs,** Y. Nakabayashi, T. Ishihara, J. Koga, M. Takayanagi*, S. Takagi**, Toshiba Corporation, Yokohama, Japan, *Toshiba Corporation Semiconductor Company, Japan, **The University of Tokyo, Tokyo, Japan

2:25 p.m.
6.3 **Strained Si and Ge MOSFETs with High-K/Metal Gate Stack for High Mobility Dual Channel CMOS,** O. Weber[1,*], Y. Bogumilowicz1[1]**, T. Ernst[1], J.-M. Hartmann[1], F. Ducroquet[1]^, F. Andrieu[1], C. Dupré[1], L. Clavelier[1], C. Le Royer[1], N. Cherkashin[1]^^, M. Hytch[1]^^, H. Dansas[1], A.-M. Papon[1], V. Carron[1], C. Tabone[1], S. Deleonibus[11]. CEA-LETI, Grenoble Cedex, France, * LPM-INSA, Villeurbanne Cedex, France, **STMicroelectronics, Crolles Cedex, France, ^IMEP, Grenoble Cedex, France, ^^LAAS,CEMES/CNRS, Toulouse, France

2:50 p.m.
6.4 **Channel Backscattering Characteristics of Strained PMOSFETs with Embedded SiGe Source/Drain,** H.-N. Lin, H.-W. Chen*, C.-H. Ko*, C.-H. Ge*, H.-C. Lin, T.-Y. Huang, W.-C. Lee*, National Chiao-Tung University, Taiwan, R.O.C., *Taiwan Semiconductor Manufacturing Company, Taiwan, R.O.C.

3:15 p.m.
6.5 **Improved Sub-10-nm CMOS Devices with Elevated Source/Drain Extensions by Tunneling Si-Selective-Epitaxial-Growth,** H. Wakabayashi, T. Tatsumi, N. Ikarashi, M. Oshida, H. Kawamoto*, N. Ikezawa*, T. Ikezawa**, T. Yamamoto, M. Hane, Y. Mochizuki, T. Mogami, NEC Corporation, *NEC Electronics Corporation, **NEC Informatec Systems Ltd., Kanagawa, Japan

3:40 p.m.
6.6 **An Integrated Methodology for Accurate Extraction of S/D Series Resistance Components in Nanoscale MOSFETs,** S.-D. Kim, S. Narasimha*, K. Rim*, IBM SRDC, Essex Junction, VT, *Hopewell Junction, NY

Session 7: Solid-State and Nanoelectronic Devices – Non-Volatile Memory Technologies: MONOS and Nanocrystal Memories

Monday, December 5, 1:30 p.m.
Lincoln Room

Co-Chairs: Kanji Yoh, Hokkaido University
Ken Uchida, Toshiba Corporation

1:35 p.m.
7.1 **20nm-Gate Bulk-FinFET SONOS Flash**, J.-R. Hwang, T.-L. Lee, H.-C. Ma*, T.-C. Lee, T.-H. Chung, B.-C. Perng, J.-W. Hsu, M.-Y. Lee, C.-Y. Ting, C.-C. Huang, J.-H. Wang, J.-H. Shieh, F.-L. Yang, Taiwan Semiconductor Manufacturing Company, Taiwan, R.O.C., *National Chiao-Tung University, Taiwan, R.O.C.

2:00 p.m.
7.2 **Low Voltage High Speed SiO_2/AlGaN/$AlLaO_3$/TaN Memory with Good Retention**, A. Chin[1],*, C. C. Laio[1], K. C. Chiang[1], D. S. Yu[1], W. J. Yoo*, G. S. Samudra*, S. P. McAlister^, C. C. Chi^^, [1] National Chiao Tung University, Taiwan, R.O.C., *National University of Singapore, Singapore, ^National Research Council of Canada, Ottawa, Canada, ^^National Tsing Hua University, Taiwan, R.O.C.

2:25 p.m.
7.3 **Long Retention and Low Voltage Operation Using IrO_2/HfAlO/HfSiO/HfAlO Gate Stack for Memory Application**, Y.Q. Wang, P. K. Singh, W.J. Yoo, Y.C. Yeo, G. Samudra, A. Chin*, W.S. Hwang, J. H. Chen, S.J. Wang**, D-L. Kwong^, National University of Singapore, Singapore, *National Chiao Tung University, Taiwan, R.O.C., **Institute of Material Research and Engineering, Singapore, ^Institute of Microelectronics, Singapore and University of Texas, Austin, TX

2:50 p.m.
7.4 **High Density Silicon Nanocrystal Embedded in Silicon Nitride Prepared by Low Energy (<0.5keV) SiH_4 Plasma Immersion Ion Implantation for Non-volatile Memory Applications**, S. Choi, H. Choi, T.-W. Kim, H. Yang, T. Lee, S. Jeon*, C. Kim*, H. Hwang, Gwangju Institute of Science and Technology, Gwangju, Korea, *Samsung Advanced Institute of Technology, Suwon, Korea

3:15 p.m.
7.5 **Enhancement of Memory Window in Short Channel Non-Volatile Memory Devices using Double Layer Tungsten Nanocrystals**, S. K. Samanta, P. K. Singh, W.- J. Yoo, G. Samudra, Y.-C. Yeo, L. K. Bera*, N. Balasubramanian*, National University of Singapore, Singapore, *Institute of Microelectronics

3:40 p.m.
7.6 **Nanocrystal Flash Memory Fabricated with Protein-mediated Assembly**, S. Tang, C. Mao, Y. Liu, D. Q. Kelly, S. K. Banerjee, The University of Texas at Austin, Austin, TX

Session 8: CMOS and Interconnect Reliability – Interconnect, Plasma Damage, and ESD Reliability

Monday, December 5, 1:30 p.m.
Military Room

Co-Chairs: Seung Kang, Agere Systems
Takeshi Nogami, Sony Corporation

1:35 p.m.
8.1 Novel Dielectric Slots in Cu Interconnects for Suppressing Stress-induced Void Failure, Y.K. Lim[1],*, K.L. Pey*, J.B. Tan[1], T.J. Lee[1], D. Vigar[1], L.C. Hsia[1], Y.H. Lim[1], N.R. Kamat[1], [1]Chartered Semiconductor Manufacturing Ltd, Singapore,*Nanyang Technological University, Singapore

2:00 p.m.
8.2 Mechanism of Moisture Uptake Induced Via Failure and its Impact on 45nm Node Interconnect Design, T. Fujimaki, K. Higashi, N. Nakamura, N. Matsunaga, K. Yoshida^, N. Miyawaki*, M. Hatano, M. Hasunuma, J. Wada, T. Nishioka, K. Akiyama, H. Kawashima**, Y. Enomoto**, T. Hasegawa**, K. Honda, M. Iwai, S. Yamada, F. Matsuoka, Toshiba Corporation, Yokohama, Japan, ^Toshiba Microelectronics Corporation, Japan, *Toshiba Information Systems Corporation, Yokohama, Japan, **Sony Corporation, Japan

2:25 p.m.
8.3 Stress-Induced Voiding under Vias Connected to "Narrow" Copper Lines, T. Kouno, T. Suzuki*, S. Otsuka, T. Hosoda, T. Nakamura*, Y. Mizushima*, M. Shiozu, H. Matsuyama, K. Shono, H. Watatani, Y. Ohkura, M. Sato, S. Fukuyama, M. Miyajima, Fujitsu Limited, Tokyo, Japan, *Fujitsu Laboratories Limited, Tokyo, Japan

2:50 p.m.
8.4 Process Damages in HfO_2/TiN Stacks: The Key Role of H^0 and H_2 Anneals, X. Garros*, G. Reimbold*, O. Louveau^, P. Holliger*, C. Hobbs**, C. Leroux*, L. Pham Nguyen*,^, F Martin^, F. Boulanger*, *CEA-LETI, Grenoble Cedex, France, ^STMicroelectronics, Crolles Cedex, France, **Freescale, Crolles Cedex, France

3:15 p.m.
8.5 New Physical Insight and Modeling of Second Breakdown (It2) Phenomenon in Advanced ESD Protection Devices, A. Chatterjee, C. Duvvury*, K. Banerjee**, Vanderbilt University, Nashville, TN, *Texas Instruments, Dallas, TX, **University of Califoria, Santa Barba, CA

Session 9: Modeling and Simulation – Compact Models

Monday, December 5, 1:30 p.m.
Thoroughbred Room

Co-Chairs: Kuntal Joardar, Texas Instruments
Jeong-Taek Kong, Samsung Electronics Co. Ltd.

1:35 p.m.
9.1 **A New Compact Model for Junctions in Advanced CMOS Technologies**, A.J. Scholten, G.D.J. Smit, M. Durand, R. van Langevelde, C.J.J. Dachs, D.B.M. Klaassen, Philips Research Laboratories, Eindhoven, The Netherlands

2:00 p.m.
9.2 **High Performance, Sub-50nm MOSFETS for Mixed Signal Applications**, V. Dimitrov, J. Heng, K. Timp, O. Dimauro, R. Chan, J. Feng, W. Hafez, T. Sorsch*, W. Mansfield*, J. Miner*, A. Kornblit*, F. Klemens*, J. Bower*, R. Cirelli*, A. Taylor*, M. Feng, G. Timp, University of Illinois, Urbana, IL, *New Jersey Nanotechnology Consortium, Murray Hill, NJ

2:25 p.m.
9.3 **High-Voltage LDMOS Compact Model for RF Applications**, M.B. Willemsen, R. van Langevelde, Philips Research Laboratories, Eindhoven, The Netherlands

2:50 p.m.
9.4 **Physics-Based Noise Modelling of Semiconductor Devices in Large-Signal Operation Including Low -Frequency Noise Conversion Effects (Invited)**, G. Ghione, F. Bonani, S. Donati, F. Bertazzi, G. Conte, Politecnico di Torino, Torino, Italy

Session 10: CMOS Devices – High Performance CMOS

Tuesday, December 6, 9:00 a.m.
International Ballroom Center

Co-Chairs: David Burnett, Freescale Semiconductor
Tatsuya Ohguro, Toshiba Corporation

9:05 a.m.
10.1 **High Performance 35nm LGATE CMOS Transistors Featuring NiSi Metal Gate (FUSI), Uniaxial Strained Silicon Channels and 1.2nm Gate Oxide**, P. Ranade, T. Ghani, K. Kuhn , K. Mistry, S. Pae, L. Shifren, M. Stettler, K. Tone, S. Tyagi, M. Bohr, Intel Corporation, Hillsboro, OR

9:30 a.m.
10.2 **45-nm Node NiSi FUSI on Nitrided Oxide Bulk CMOS Fabricated by a Novel Integration Process**, S. Yu, J.-P. Lu, F. Mehrad, H. Bu, A. Shanware, M. Ramin, M. Pas, M.R. Visokay, S. Vitale, S.-H. Yang, P. Jiang, L. Hall, C. Montgomery, Y. Obeng, C. Bowen , H. Hong, J. Tran, R. Chapman, S. Bushman, C. Machala, J. Blatchford, R. Kraft, L. Colombo, S. Johnson, B. McKee, Texas Instruments Incorporated, Dallas, TX

9:55 a.m.
10.3 **High Performance CMOS Bulk Technology using Direct Silicon Bond (DSB) Mixed Crystal Orientation Substrates,** C.Y. Sung*, H. Yin, H. Ng, K. L. Saenger*, V. Chan, S.

Crowder, J. Li, J.A. Ott*, R. Bendernagel, J. Kempisty, V. Ku, H.K. Lee, Z.J. Luo, A. Madan, R.T. Mo, P. Nguyen, G. Pfeiffer, M. Raccioppo, N. Rovedo, D.K. Sadana*, J.P. de Souza*, R. Zhang, Z. Ren, C. Wann, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY

10:20 a.m.
10.4 High Performance CMOSFET Technology for 45nm Generation and Scalability of Stress-Induced Mobility Enhancement Technique, A. Oishi, O. Fujii, T. Yokoyama*, K. Ota*, T. Sanuki, H. Inokuma, K. Eda, T. Idaka, H. Miyajima, S. Iwasa, H. Yamasaki, K. Oouchi, K. Matsuo, H. Nagano, T. Komoda, Y. Okayama, T. Matsumoto*, K. Fukasaku*, T. Shimizu, K. Miyano, T. Suzuki, K. Yahashi, A. Horiuchi*, Y. Takegawa, K. Saki, S. Mori, K. Ohno*, I. Mizushima, M. Saito*, M. Iwai, S. Yamada, N. Nagashima*, F. Matsuoka, Toshiba Corporation, Yokohama, Japan, *Sony Corporation, Yokohama, Japan

10:45 a.m.
10.5 Integration and Optimization of Embedded-SiGe, Compressive and Tensile Stressed Liner Films, and Stress Memorization in Advanced SOI CMOS Technologies, M. Horstmann, A. Wei, T. Kammler, J. Höntschel, H. Bierstedt, H.-J. Engelmann, A. Hellmich, K. Hempel, G. Koerner, A. Neu, R. Otterbach, C. Reichel, M. Trentsch, P. Press, K. Frohberg, M. Schaller, H. Salz, J. Hohage, H. Ruelke, J. Klais, M. Raab , D. Greenlaw, N. Kepler, H. Chen*, D. Chidambarrao*, D. Fried*, J. Holt*, W. Lee*, H. Nii**, S. Panda*, T. Sato**, A. Waite^, S. Luning^, K. Rim*, D. Shepis*, M. Khare*, S.F. Huang*, J. Pellerin^, L.T. Su*, AMD Saxony LLC & Co., Dresden, Germany, *IBM Systems & Technology Group, Hopewell Junction, NY, **Toshiba America Electronic Components Inc., Hopewell Junction, NY, ^AMD Corporation, Hopewell Junction, NY

11:10 a.m.
10.6 High Performance 30 nm Gate Bulk CMOS for 45nm Node with Σ-shaped SiGe-SD, H. Ohta, Y. Kim, Y. Shimamune*, T. Sakuma, A. Hatada*, A. Katakami*, T. Soeda, K. Kawamura, H. Kokura, H. Morioka, T. Watanabe, J. Oh, Y. Hayami, J. Ogura, T. Mori, N. Tamura*, M. Kojima, T. Sugii*, K. Hashimoto, Fujitsu Limited, Tokyo, Japan, * Fujitsu Laboratories Ltd., Tokyo, Japan

11:35 a.m.
10.7 Record RF Performance of Sub-46nm Lgate NFETs in Microprocessor SOI CMOS Technologies, S. Lee*, L. Wagner, B. Jaganathan, S. Csutak, J. Pekarik*, N. Zamdmer, M. Breitwisch, R. Ramachandran, G. Freeman, IBM Systems and Technology Group, Hopewell Junction, NY, *IBM Systems and Technology Group, Essex Junction, VT

Session 11: Solid-State and Nanoelectronic Devices – Nanotubes and Nanowires for Thermal and Electrical Applications

Tuesday, December 6, 9:00 a.m.
International Ballroom East

Co-Chairs: Ali Javey, Stanford University
Ted Kamins, Hewlett Packard Labs

9:05 a.m.
11.1 Carbon Nanotube Interconnects: Implications for Performance, Power Dissipation and Thermal Management, N. Srivastava, R. V. Joshi*, K. Banerjee, University of California, Santa Barba, CA, *IBM T. J. Watson Research Center, Yorktown Heights, NY

9:30 a.m.
11.2 Electro-Thermal Transport in Metallic Single-Wall Carbon Nanotubes for Interconnect Applications, E. Pop, D. Mann, J. Reifenberg, K. Goodson, H. Dai, Stanford University, Stanford, CA

9:55 a.m.
11.3 Thermal and Source Bumps Utilizing Carbon Nanotubes for Flip-chip High Power Amplifiers, T. Iwai*,[1], H. Shioya*, D. Kondo*, S. Hirose*, A. Kawabata*, S. Sato*, M. Nihei*, T. Kikkawa[1], K. Joshin[1], Y. Awano*, N. Yokoyama*, *Fujitsu Laboratories, Atsugi, Japan, [1]Fujitsu Ltd., Atsugi, Japan

10:20 a.m.
11.4 Nanoelectromechanical DRAM for Ultra-Large-Scale Integration (ULSI), J.E. Jang, S.N. Cha, Y. Choi, D.J Kang, D.G. Hasko, J.E. Jung*, J.M. Kim*, G.A. J. Amaratunga, Cambridge University, Cambridge, U. K.,* Samsung Advanced Institute of Technology, Yongin, Korea

10:45 a.m.
11.5 Wrap-Gated InAs Nanowire Field Effect Transistor (Invited), L.-E. Wernersson*,^, T. Bryllert*,[#], E. Lind*, L. Samuelson*,^, *Lund University, Lund, Sweden, #Chalmers University of Technology, Göteborg, Sweden, ^QuMat Technologies AB, Lund, Sweden

11:10 a.m.
11.6 A New Logic Family Based on Hybrid MOSFET-Polysilicon Nano-Wires, S. Ecoffey, M. Mazza, V. Pott, D. Bouvet, A. Schmid, Y. Leblebici, M.J. Declercq, A.M. Ionescu, Swiss Federal Institute of Technology, Lausanne, Switzerland

Session 12: Displays, Sensors and MEMS – MEMS Technologies and Applications

Tuesday, December 6, 9:00 a.m.
Georgetown Room

Co-Chairs: Darrin Young, Case Western Reserve University
Juergen Brugger, EPFL

9:05 a.m.
12.1 CMOS-MEMS Resonant Mixer-Filters (Invited), G. Fedder, Carnegie Mellon University, Pittsburgh, PA

9:30 a.m.
12.2 Low Phase Noise Array-Composite Micromechanical Wine-Glass Disk Oscillator, Y.-W. Lin, S.-S. Li, Z. Ren, C.T.-C. Nguyen, University of Michigan, Ann Arbor, MI

9:55 a.m.
12.3 Frequency Tolerance of RF Micromechanical Disk Resonators in Nanocrystalline Diamond and Polysilicon Structural Materials, J. Wang, Y. Xie, C.T.-C. Nguyen, University of Michigan, Ann Arbor, MI

10:20 a.m.
12.4 Non-Linearity Cancellation in MEMS Resonators for Improved Power Handling, M. Agarwal, K.-K. Park, R. N. Candler, M. Hopcroft, C. M. Jha, R. Melamud, B. Kim, B. Murmann, T. W. Kenny, Stanford University, Stanford, CA

10:45 a.m.
12.5 Embedded MEMS Filter Chip and its Fabrication for VHF Applications, S. Mitarai, M. Tada, S. Yanagawa, T. Yamaguchi, T. Kinoshita, M. Tanaka, K. Ikeda, K. Yamashita, Sony Corporation, Kanagawa, Japan

11:10 a.m.
12p6 Piezoelectric RF MEMS Tunable Capacitor with 3V Operation Using CMOS Compatible Materials and Process, T. Kawakubo*, T. Nagano, M. Nishigaki, K. Abe, K. Itaya, Toshiba Corporation, Japan, *Toshiba Research Consulting Corporation, Japan

11:35 a.m.
12.7 GaN on Patterned Silicon (GPS) Technique for GaN-based Integrated Microsensors, Z. Yang, R. Wang, D. Wang, B. Zhang, K. J. Chen, K. M. Lau, Hong Kong University of Science and Technology, Hong Kong

12:00 p.m.
12.8 PECVD-Oxynitride Gas Chromatographic Columns, M. Agah, K.D. Wise, The University of Michigan, Ann Arbor, MI

Session 13: Integrated Circuits and Manufacturing – DRAM and NAND Flash

Tuesday, December 6, 9:00 a.m.
Jefferson Room

Co-Chairs: Carlos Mazure, SOITEC
Takashi Nakabayashi, Matsushita Electric Industrial Co. Ltd.

9:05 a.m.
13.1 A Floating Body Cell(FBC) Fully Compatible with 90nm CMOS Technology(CMOS4) for 128Mb SOI DRAM, Y. Minami, T. Shino, A. Sakamoto*, T. Higashi**, N. Kusunoki, K. Fujita, K. Hatsuda, T. Ohsawa, N. Aoki, H. Tanimoto, M. Morikado, H. Nakajima, K. Inoh, T. Hamamoto, A. Nitayama, Toshiba Corporation, Yokohama, Japan, *Toshiba Information Systems Corporation, Yokohama, Japan, **Toshiba Microelectronics Corporation, Yokohama, Japan

9:30 a.m.
13.2 A Novel Capacitor-Less DRAM Cell Using Thin Capacitively-Coupled Thyristor (TCCT), H.-J. Cho, F. Nemati, R. Roy, R. Gupta, K. Yang, M. Ershov, S. Banna, M. Tarabbia, C. Salling, D. Hayes, S. Robins, T-RAM Semiconductor, San Jose, CA

9:55 a.m.
13.3 Local-Damascene-FinFET DRAM Integration with p+ Doped Poly-Silicon Gate Technology for Sub-60nm Device Generations, Y.-S. Kim, S.-H. Lee, S.-H. Shin, S.-H. Han, J.-Y. Lee, J.-W. Lee, J. Han, S.-C. Yang, J.-H. Sung, E.-C. Lee, B.-Y. Song, D.-J. Lee, D.-I. Bae, W.-S. Yang, Y.-K. Park, K.-H. Lee, B.-H. Roh, T.-Y. Chung, K. Kim, W. Lee, Samsung Electronics Co. Ltd., Gyunggi-Do, Korea

10:20 a.m.
13.4 Overcoming of DRAM Scaling Limitation by Employing Straight Recessed Channel Array Transistor with <100> Uni-Axial and (100) Uni-Plane Channel, I.-G. Kim, S.-H. Park, J.-S. Yoon, D.-J. Kim, J.-Y. Noh, J.-H. Lee, Y.-S. Kim, M.-W. Hwang, K.-H. Yang, J.-S. Park, K. Oh, Samsung Electronics, Gyeonggi-Do, Korea

10:45 a.m.
13.5 Technology for Sub-50nm DRAM and NAND Flash Manufacturing (Invited), K. Kim, Samsung Electronics Co., Kyunggi-Do, Korea

11:10 a.m.
13.6 A Novel NAND-Type MONOS Memory using 63nm Process Technology for Multi-Gigabit Flash EEPROMs, Y. Shin, J. Choi, C. Kang, C. Lee, K.-T. Park, J.-S. Lee, J. Sel, V. Kim, B. Choi, J. Sim, D. Kim, H.-J. Cho, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

11:35 a.m.
13.7 A Novel P-Channel NAND-Type Flash Memory with 2-bit/cell Operation and High Programming Throughput (>20 MB/sec), H.-T. Lue, S.-Y. Wang, E.-K. Lai, M.-T. Wu, L.-W. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Hsinchu, Japan

Session 14: Process Technology – Advanced Integration Concepts

Tuesday, December 6, 9:00 a.m.
Lincoln Room

Co-Chairs: Simon Deleonibus, CEA/LETI
Sunit Tyagi, Intel Corporation

9:05 a.m.
14.1 Challenges for the DRAM Cell Scaling to 40nm (Invited), W. Mueller, W. Bergner, E. Erben, S. Jakschik, C. Kapteyn, A. Kersch, S. Kudelka, F. Lau, J. Luetzen, A. Orth, J. Nuetzel, J. Regul, T. Schloesser, A. Scholz, U. Schroeder, A. Sieck, A. Spitzer, M. Strasser, D. Temmler, P.F. Wang, S. Wege, R. Weis, Infineon Technologies, Dresden, Germany

9:30 a.m.
14.2 Fabrication of 3D Trench PZT Capacitors for 256Mbit FRAM Device Application, J.-M. Koo, B.-S. Seo, S. Kim, S. Shin, Jung-H. Lee, H. Baik, Jang-H. Lee, J.H. Lee, B.-J. Bae*, J.-E. Lim*, D.-C. Yoo*, S.-O. Park*, H.-S. Kim*, H. Han**, S. Baik**, J.-Y. Choi**, Y. J. Park**, Y. Park, Samsung Advanced Institute of Technology, Kyungki-Do, Korea, *Samsung Electronics Co. Ltd., Kyungki-Do, Korea, **Pohang University of Science and Technology, Pohang, Korea

9:55 a.m.
14.3 Highly Scalable Flash Memory with Novel Deep Trench Isolation Embedded into High-Performance CMOS for the 90nm Node & Beyond, D. Shum, A.T. Tilke, L. Pescini*, M. Stiftinger**, R. Kakoschke**, K.J. Han^, S.R. Kim^, V. Hecht^, N. Chan^, A. Yang^, R. Broze^, Infineon Technologies North America, Hopewell Junction, NY, *Infineon Technologies Dresden GmbH & Co. OHG, Dresden, Germany, **Infineon Technologies AG, Munich, Germany, ^Actel Corporation, Mountain View, CA

10:20 a.m.
14.4 New Three-Dimensional Integration Technology Using Self-Assembly Technique, T. Fukushima, Y. Yamada, H. Kikuchi, M. Koyanagi, Tohoku University, Miyagi, Japan

10:45 a.m.
14.5 Enabling SOI-Based Assembly Technology for Three-Dimensional (3D) Integrated Circuits (ICs), A.W. Topol, D.C. La Tulipe, L. Shi, S.M. Alam, D.J. Frank, S.E. Steen, J. Vichiconti, D. Posillico, M. Cobb, S. Medd, S. Goma, D. DiMilia, M. T. Robson, E. Duch, M. Farinelli, C. Wang, R. A. Conti, D.M. Canaperi, L. Deligianni, A. Kumar, K.T. Kwietniak, C. D'Emic, J. Ott, A.M. Young , K. W. Guarini, M. Ieong, IBM T.J. Watson Research Center, Yorktown Heights, NY

11:10 a.m.
14.6 Self-Assembling Resists for Nanolithography (Invited), P. F. Nealey, E. W. Edwards, M. Müller, M. P. Stoykovich, H.H. Solak*, J. J. de Pablo, University of Wisconsin-Madison, Madison, WI, *Paul Sherrer Institute, Villigen, Switzerland

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Session 15: Quantum, Power, and Compound Semiconductor Devices

Tuesday, December 6, 9:00 a.m.
Military Room

Co-Chairs: Helmut Brech, Freescale Semiconductor
Yutaka Hoshino, Renesas Technology Corporation

9:05 a.m.
15.1 High Frequency Power LDMOS Technologies for Base Station Applications Staus, Potential, and Benchmarking (Invited), G. Ma, Q. Chen**, O. Tornblad^, T. Wei^, C. Ahrens*, B. Goebel*, C. Kuehn*, U. Seidel*, Infineon Technologies, Tempe, AZ, *Infineon Technologies, Munich, Germany, **Infineon Technologies, Kista, Sweden, ^Infineon Technologies, Morgan Hill, CA

9:30 a.m.
15.2 High Performance RF Power LDMOSFETs for Cellular Handsets Formed in Thick-Strained-Si/Relaxed-SiGe Structure, M. Kondo, N. Sugii*, Y. Hoshino, W. Hirasawa**, Y. Kimura*, M. Miyamoto, T. Fujioka, S. Kamohara, Y. Kondo, S. Kimura*, I. Yoshida, Renesas Technology Corporation, Tokyo, Japan, *Hitachi Ltd., Japan, **Renesas Eastern Japan Semiconductor Inc., Japan

9:55 a.m.
15.3 Performance and Limitations of 65 nm CMOS for Integrated RF Power Applications, J. Scholvin, D.R. Greenberg*, J.A. del Alamo, MIT, Cambridge, MA, *IBM Research, Hopewell Junction, NY

10:20 a.m.
15.4 Dielectric Resurf: Breakdown Voltage Control by STI Layout in Standard CMOS, J. Sonsky, A. Heringa, Philips Research, Leuven, Belgium

10:45 a.m.
15.5 AlGaN/GaN Devices for Power Switching Systems (Invited), D. Ueda, T. Murata, M. Hikita, M. Yanagihara, S. Nakazawa, K. Inoue, H. Ishida, Y. Uemoto, T. Tanaka, T. Egawa*, Matsushita Electric Industrial Co. Ltd., Osaka, Japan, *Nagoya Institute of Technology, Osaka, Japan

11:10 a.m.
15.6 A Low On-Resistance High Voltage SOI LIGBT with Oxide Trench in Drift Region and Hole Bypass Gate Configuration, D. H. Lu, S. Jimbo, N. Fujishima, Fuji Electric Advanced Technology Co. Ltd., Nagano, Japan

Session 16: CMOS and Interconnect Reliability – Gate Dielectric Breakdown – Modeling and Mechanism

Tuesday, December 6, 9:00 a.m.
Thoroughbred Room

Co-Chairs: Paul Nicollian, Texas Instruments
Koji Eriguchi, Kyoto University

9:05 a.m.
16.1 Mechanisms of Hydrogen Release in the Breakdown of SiO_2-Based Gate Oxides, J. Suñé, E. Wu*, Universitat Autònoma de Barcelona, Bellaterra, Spain, *IBM Microelectronics Division, Essex Junction, VT

9:30 a.m.
16.2 The Roles of Hydrogen and Holes in Trap Generation and Breakdown in Ultra-thin SiON Dielectrics, P. E. Nicollian, A.T. Krishnan, C. Bowen, S. Chakravarthi, C. Chancellor, R. Khamankar, Texas Instruments Incorporated, Dallas, TX

9:55 a.m.
16.3 A Comprehensive Investigation of Gate Oxide Breakdown of P+Poly/PFETs Under Inversion Mode, E. Wu, J. Suñé*, W. Lai, A. Vayshenker, D. Harmon, IBM Microelectronics Division, Essex Junction, VT, *Universitat Autònoma de Barcelona, Bellaterra, Spain

10:20 a.m.
16.4 Theory of Hydrogen-Related Levels in Semiconductors and Oxides (Invited), C. G. Van de Walle, University of California, Santa Barba, CA

10:45 a.m.
16.5 Theory of "Current-Ratio" Method for Oxide Reliability: Proposal and Validation of a New Class of Two Dimensional Breakdown-Spot Characterization Techniques, M.A. Alam, D. Monroe*, B. Weir*, P. Silverman*, Purdue University, West Lafayette, IN, *Agere Systems, Allentown, PA

11:10 a.m.
16.6 Degradation and Breakdown of 0.9 nm EOT SiO_2/ALD HfO_2/Metal Gate Stacks Under Positive Constant Voltage Stress, R. Degraeve*, T. Kauerauf[*,1], M. Cho[*,^], M. Zahid^^, L.-Å Ragnarsson*, D.P. Brunco*, B. Kaczer*, P. Roussel*, S. De Gendt[*,1], G. Groeseneken[*,1], *IMEC, Leuven, Belgium, [1]Catholic University, Leuven, Belgium, ^Seoul National University, South Korea, ^^John Moores University, Liverpool, United Kingdom

Luncheon Session

Tuesday, December 6, 12:20 p.m.
International Ballroom West

Luncheon Presentation: *"Bits and Atoms"*
Prof. Neil Gershenfeld, Massachusetts Institute of Technology

Professor Gershenfeld will discuss emerging insights into the relationship between the digital world of bits and the physical world of atoms: "building with logic" (programmed assembly, to fabricate perfect macroscopic structures out of imperfect microscopic components) and "programming with math" (compiling mathematical programs into distributed physical dynamics, for engineering in a limit of thermodynamic complexity). Applications include analog logic, interdevice internetworking, paintable computing, and personal fabrication in developed and developing countries.

Prof. Neil Gershenfeld is the Director of MIT's Center for Bits and Atoms. His unique laboratory investigates the relationship between the content of information and its physical representation, from molecular quantum computers to virtuosic musical instruments. Technology from his lab has been seen and used in settings including New York's Museum of Modern Art and rural Indian villages, the White House/Smithsonian Millennium celebration and automobile safety systems, the World Economic Forum and inner-city community centers, Las Vegas shows and Sami herds. He is the author of numerous technical publications, patents, and books including "Fab," "When Things Start To Think," "The Nature of Mathematical Modeling," and "The Physics of Information Technology," and has been featured in media such as The New York Times, The Economist, CNN, and the McNeil/Lehrer News Hour. Dr. Gershenfeld has a BA in Physics with High Honors from Swarthmore College, a Ph.D. from Cornell University, was a Junior Fellow of the Harvard University Society of Fellows, and a member of the research staff at Bell Labs.

Awards Presentation

2005 IEEE Cledo Brunetti Award

2005 IEEE Andrew S. Grove Award

2005 IEEE Daniel E. Noble Award

Session 17: Process Technology – High-k II Gate Dielectrics

Tuesday, December 6, 2:15 p.m.
International Ballroom Center

Co-Chairs: Hirohito Watanabe, NEC Corporation
Gyo-Young Jin, Samsung Electronics

2:20 p.m.
17.1 Fluorine Incorporation into HfSiON Dielectric for V_{th} Control and Its Impact on Reliability for Poly-Si Gate pFET, M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura*, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, M. Yoneda, Renesas Technology Corporation, Hyogo, Japan, *Renesas Semiconductor Engineering Corporation, Hyogo, Japan

2:45 p.m.
17.2 Improvement in High-k (HfO_2/SiO_2) Reliability by Incorporation of Fluorine, K.-I. Seo, R. Sreenivasan, P. C. McIntyre, K. C. Saraswat, Stanford University, Stanford, CA

3:10 p.m.
17.3 Experimental Clarification of Mobility Determining Factors in HfSiON CMISFETs with Various Film Compositions, R. Iijima, M. Takayanagi*, T. Yamaguchi, M. Koyama, A. Nishiyama, Toshiba Corporation, Yokohama, Japan, *Toshiba Corporation Semiconductor Company, Yokohama, Japan

3:35 p.m.
17.4 High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements, M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, H. J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B .H. Lee, G. Pant*, B. E. Gnade*, M. J. Kim*, R. M. Wallace*, D. Guo**, H. Bu**, T.P. Ma**, SEMATECH, Austin, TX, *University of Texas at Dallas, Richardson, TX, **Yale University, New Haven, Connecticut

4:00 p.m.
17.5 Dramatic Improvement of Ge pMOSFET Characteristics Realized by Amorphous Zr-Silicate/Ge Gate Stack with Excellent Structural Stability through Process Temperatures, Y. Kamata, Y. Kamimuta, T. Ino, R. Iijima, M. Koyama, A. Nishiyama, Toshiba Corporation, Yokohama, Japan

4:25 p.m.
17.6 Ultra thin (EOT=3Å) and Low Leakage Dielectrics of La-Alminate Directly on Si Substrate Fabricated by High Temperature Deposition, M. Suzuki, M. Tomita, T. Yamaguchi, N. Fukushima, Toshiba Corporation, Kawasaki, Japan

Session 18: Emerging Technologies – Flexible Electronics

Tuesday, December 6, 2:15 p.m.
International Ballroom East

Chair: Veena Misra, North Carolina State University

2:20 p.m.
18.1 Organic Thin Electronics (Invited), T. Jackson, Penn State University, University Park, PA

2:45 p.m.
18.2 Flexible, Large-Area Sensors and Actuators with Organic Transistor Integrated Circuits (Invited), T. Someya*,^, T. Sakurai*, T. Sekitani*, *University of Tokyo, Tokyo, Japan, ^CREST/JST, Tokyo Japan

3:10 p.m.
18.3 Organic Circuits on Flexible Substrates (Invited), H. Klauk, Max Planck Institute for Solid State Research, Stuttgart, Germany

3:35 p.m.
18.4 Organic and Hybrid Organic/Inorganic Transistors for Chemical and Bio Sensing (Invited), A. Dodabalapur, D. Sharma, L. Wang, C. Burham, D. Fine, The University of Texas at Austin, Austin, TX

4:00 p.m.
18p5 Materials and Patterning Techniques for Macroelectronics (Invited), J. A. Rogers, University of Illinois, Urbana, IL

Session 19: Solid-State and Nanoelectronic Devices – Novel Device Concepts

Tuesday, December 6, 2:15 p.m.
Georgetown Room

Co-Chairs: Mark Reed, Yale University
Zoran Krivokapic, AMD

2:20 p.m.
19.1 A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM, M. Hosomi, H. Yamagishi, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada, M. Shoji, H. Kano, Sony Corporation, Kanagawa, Japan

2:45 p.m.
19.2 A New Nano-Electro-Mechanical Field Effect Transistor (NEMFET) Design for Low-Power Electronics, H. Kam, D. Lee, R. Howe, T.-J. King, University of California, Berkeley, CA

3:10 p.m.
19.3 Single Molecular Devices with Fullerenes and OligoPhenyleneVinylene (OPV) Derivatives (Invited), A. Danilov[1, *], S. Kafanov*, T. Bjørnholm[1], S. Kubatkin[*,] [1]University of Copenhagen, Denmark, *Chalmers University of Technology, Göteborg, Sweden

3:35 p.m.
19.4 The Micro to Nano Addressing Block (MNAB), K. Gopalakrishnan, R. S. Shenoy, C. Rettner, R. King, Y. Zhang*, B. Kurdi, L. D. Bozano, J. J. Welser, M. B.

Rothwell*, M. Jurich, M. I. Sanchez, M. Hernandez, P. M. Rice, W. P. Risk, H. K. Wickramasinghe, IBM Almaden Research Center, San Jose, CA, *IBM T.J. Watson Research Center, Yorktown Heights, NY

4:00 p.m.
19.5 Three Terminal Solid-Electrolyte Nanometer Switch, T. Sakamoto[*,1], N. Banno[*,1], N. Iguchi*, H. Kawaura*, S. Kaeriyama^, M. Mizuno^, K. Terabe[1,^^], T. Hasegawa[1,^^], M. Aono[1,^^], *NEC Corporation, Ibaraki, Japan, [1]ICORP-(JST), Kanagawa, Japan, ^NEC Corporation, Kanagawa, Japan, ^^National Institute of Material Science, Ibaraki, Japan

Session 20: CMOS Devices – Strained-Silicon Technology

Tuesday, December 6, 2:15 p.m.
Jefferson Room

Co-Chairs: Yee-Chia Yeo, National University of Singapore
Howard C.-H. Wang, TSMC

2:20 p.m.
20.1 Design of High Performance PFETs with Strained Si Channel and Laser Anneal, Z. Luo, Y. Chong*, J. Kim^, N. Rovedo, B. Greene, S. Panda, T. Sato^^, J. Holt, D. Chidambarrao, J. Li, R. Davis, A. Madan, A. Turansky, O. Gluschenkov, R. Lindsay**, A. Ajmera, J. Lee*, S. Mishra*, R. Amos, D. Schepis, H. Ng, K. Rim, IBM System & Technology Group, Hopewell Junction, NY, *Chartered Semiconductor Manufacturing Ltd., Hopewell Junction, NY, **Infineon Technologies AG, Hopewell Junction, NY, ^Samsung Electronics Co. Ltd., Hopewell Junction, NY, ^^Toshiba America Electronic Components Inc. at IBM SRDC, Hopewell Junction, NY

2:45 p.m.
20.2 Source/Drain Germanium Condensation for P-Channel Strained Ultra-Thin Body Transistors, K.-J. Chui, K.-W. Ang, A. Madan, G. H. Wang, C.-H. Tung*, L.-Y. Wong*, Y. Wang*, S.-F. Choy*, N. Balasubramanian*, M. F. Li , G. Samudra, Y.-C. Yeo, National Unversity of Singapore, Singapore, *Institute of Microelectronics, Singapore

3:10 p.m.
20.3 Thin Body Silicon-on-Insulator N-MOSFET with Silicon-Carbon Source/Drain Regions for Performance Enhancement, K.-W. Ang, K.-J. Chui, V. Bliznetsov*, Y. Wang*, L.-Y. Wong*, C.-H. Tung*, N. Balasubramanian*, M.-F. Li, G. Samudra, Y.-C. Yeo, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore

3:35 p.m.
20.4 New Stress Inducing Technique of Epitaxial Si on Recessed S/D Fabricated in Substrate Strained-Si of <100>-Channel on Rotated Wafers, T. Sanuki, H. Tanaka, K. Oota*, O. Fujii, R. Yamaguchi, K. Nakayama, Y. Morimasa, Y. Takasu, J. Idebuchi, N. Nishiyama, H. Fukui, H. Yoshimura, K. Matsuo, I. Mizushima, H. Ito, Y. Takegawa, M. Saito*, M. Iwai, N. Nagashima*, F. Matsuoka, Toshiba Corporation, Yokohama, Japan, *Sony Corporation, Yokohama, Japan

4:00 p.m.
20.5 Stress Memorization in High-Performance FDSOI Devices with Ultra Thin Silicon Channels and 25nm Gate Lengths, D. V. Singh, J. W. Sleight *, J. M. Hergenrother, Z. Ren* , K. A. Jenkins, O. Dokumaci* , L. Black**, J. B. Chang, H. Nakayama^, D. Chidambarrao* , R. Venigalla* , J. Pan**, W. Natzle, B. L. Tessier*, A. Nomura**, J. A. Ott, M. Ieong*, W. Haensch, IBM Semiconductor Research and Development Center, Yorktown Heights, NY, *IBM Systems and Technology Group, Hopewell Junction, NY, **Advanced Micro Devices Inc., Hopewell Junction, NY, ^Sony Electronics Inc., Hopewell Junction, NY

4:25 p.m.
20.6 Uniaxial-Biaxial Stress Hybridization For Super-Critical Strained-Si Directly On Insulator (SC-SSOI) PMOS With Different Channel Orientations, A.V-Y. Thean, L. Prabhu, V. Vartanian, M. Ramon, B-Y. Nguyen, T. White, H. Collard, Q-H Xie, S. Murphy, J. Cheek, S. Venkatesan, J. Mogab, C.H. Chang*, Y.H. Chiu*, H.C. Tuan*, Y.C. See*, M.S. Liang*, Y.C. Sun*, Freescale Semiconductor Inc., Austin, TX, *TSMC, Taiwan, R.O.C.

4:50 p.m.
20.7 Dislocation Engineering in Strained MOS Materials (Invited), E.A. Fitzgerald, M.L. Lee, D. Isaacson, D.A. Antoniadis, T.A. Langdo, MIT, Cambridge, MA

Session 21: Modeling and Simulation – Nanowires and Nanotubes

Tuesday, December 6, 2:15 p.m.
Lincoln Room

Co-Chairs: Gerhard Klimeck, Purdue University
Mark Stettler, Intel Corporation

2:20 p.m.
21.1 Computational Study of Carbon Nanotube p-i-n Tunnel FETs, S. O. Koswatta, D. E. Nikonov*, M. S. Lundstrom, Purdue University, West Lafayette, IN, *Intel Corporation, Santa Clara, CA

2:45 p.m.
21.2 Performance of Carbon Nanotube Field Effect Transistors with Doped Source and Drain Extensions and Arbitrary Geometry, G. Fiori, G.Iannaccone, G. Klimeck*, Universita degli Studi di Pisa, Pisa, Italy, *Purdue University, West Lafayette, IN

3:10 p.m.
21.3 Ballistic Transport in Si, Ge, and GaAs Nanowire MOSFETs, M. Bescond, N. Cavassilas*, K. Kalna, K. Nehari*, L. Raymond*, J. L. Autran*, M. Lannoo*, A. Asenov, University of Glasgow, Scotland, *Laboratoire Materiaux et Microelectronique de Provence, Marseille, France

3:35 p.m.
21.4 Bandstructure and Orientation Effects in Ballistic Si and Ge Nanowire FETs, J. Wang, A. Rahman, G. Klimeck, M. Lundstrom, Purdue University, West Lafayette, IN

4:00 p.m.
21.5 Performance Assessment of Sub-Percolating Nanobundle

Network Transistors by an Analytical Model, N. Pimparkar, J. Guo*, M. A. Alam, Purdue University, West Lafayette, IN, *University of Florida, Gainesville, FL

Session 22: CMOS and Interconnect Reliability – Process and Electrical Degradation in Flash Memories and Performance Boosted CMOS Devices

Tuesday, December 6, 2:15 p.m.
Military Room

Co-Chairs: Angelo Visconti, STMicroelectronics
William Tonti, IBM Microelectronics

2:20 p.m.
22.1 **4 Bit per Cell NROM Reliability (Invited)**, B. Eitan, G. Cohen, A. Shappir, E. Lusky, A. Givant, M. Janai, I. Bloom, Y. Polansky, O. Dadashev, A. Lavan, R. Sahar and E. Maayan, Saifun Semiconductors Ltd., Netanya, Israel

2:45 p.m.
22.2 **A New Charge-Trapping Technique to Extract SILC-trap Time Constants in SiO_2**, D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Chiavarone*, A. Visconti*, Politecnico di Milano, Milano, Italy, *STMicroelectronics, Agrate Brianza, Italy

3:10 p.m.
22.3 **BE-SONOS: A Bandgap Engineered SONOS with Excellent** Performance and Reliability, H.-T. Lue, S.-Y. Wang, E.-K. Lai, Y.-H. Shih, S.-C. Lai, L.-W. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Taiwan, R.O.C.

3:35 p.m.
22.4 **Highly Reliable 2-bit/cell Nitride Trapping Flash Memory Using a Novel Array-Nitride-Sealing (ANS) ONO Process**, Y.H. Shih, S.C. Lee, H.T. Lue, M.D. Wu, T.H. Hsu, E.K. Lai, J.Y. Hsieh, C.W. Wu, L.W. Yang, K. Y. Hsieh, K.C. Chen, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Taiwan, R.O.C.

4:00 p.m.
22.5 **BTI and Charge Trapping in Germanium p- and n-MOSFETs with CVD HfO_2 Gate Dielectric**, N. Wu, Q. Zhang, C. Zhu, C. Shen, M.F. Li, D.S.H. Chan, N. Balasubramanian*, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore

4:25 p.m.
22.6 **A New Insight into the Degradation Mechanisms of Various Mobility-Enhanced CMOS Devices with Different Substrate Engineering**, S. S. Chung, O. J. Liu, S. J. Wu*, C. S. Lai*, Y. C. Liu**, D. F. Chen**, H. S. Lin**, W. T. Shiau**, C. T. Tsai**, S. C. Chien**, S. W. Sun**, National Chiao Tung University, Taiwan, *Chang-Gung University, Taiwan, **United Microelectronics Corporation, Taiwan

4:50 p.m.
22.7 **Positive Bias and Temperature Stress Induced Two-Stage Drain Current Degradation in HfSiON nMOSFET's**, C. T. Chan, C. J. Tang, T. Wang, H. C.-H. Wang*, D. D. Tang*, National Chiao-Tung University, Taiwan, *Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan

Session 23: Quantum, Power, and Compound Semiconductor Devices

Tuesday, December 6, 2:15 p.m.
Thoroughbred Room

Co-Chairs: Ruediger Quay, Fraunhofer Institute of Applied Solid State Physics
Joachim Wuerfl, Ferdinand Braun Institute

2:20 p.m.
23.1 A 36mm GaN-on-Si HFET Producing 368W with 70% Drain Efficiency, R. Therrien, S. Singhal, J.W. Johnson, W. Nagy, R. Borges, A. Chaudhari, A.W. Hanson, A. Edwards, J. Marquart, P. Rajagopal, K.J. Linthicum, Nitronex Corporation, Raleigh, NC

2:45 p.m.
23.2 An Over 100 W n-GaN/n-AlGaN/GaN MIS-HEMT Power Amplifier for W-CDMA Base Station Applications, M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo, K. Joshin, Fujitsu Laboratories Ltd., Atsugi, Japan

3:10 p.m.

23.3 Novel AlGaN/GaN Dual-Field-Plate FET with High Gain, Increased Linearity and Stability, Y. Ando, A. Wakejima, Y. Okamoto, T. Nakayama , K. Ota, K. Yamanoguchi, Y. Murase, K. Kasahara, K. Matsunaga, T. Inoue, H. Miyamoto, R&D Association for Future Electron Devices, Otsu, Japan

3:35 p.m.
23.4 High Power, High Gain AlGaN/GaN HEMTs With Novel Powerbar Design, R. Lossy, A. Liero, J. Würfl. G. Tränkle, Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin, Germany

4:00 p.m.
23.5 8-Watt GaN HEMTs at Millimeter-Wave Frequencies, Y.-F. Wu, M. Moore, A. Saxler*, T. Wisleder, U. K. Mishra, P. Parikh, Cree Santa Barbara Technology Center, Goleta, CA, *Cree Inc., NC

4:25 p.m.
23.6 380V/1.9A GaN Power-HEMT: Current Collapse Phenomena Under High Applied Voltage and Demonstration of 27.1 MHz Class-E Amplifier, W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, T. Domon, I. Omura, M. Yamaguchi, Toshiba Corporation, Kawasaki, Japan

4:50 p.m.
23.7 Evidence of Traps Creation in GaN/AlGaN/GaN HEMTs After a 3000 Hour On-State and Off-State Hot Electron Stress, A.Sozza[1,2,3], C.Dua[1], E. Morvan[1], M.A. diForte-Poisson[1], S.L. Delage[1], F. Rampazzo[2], A. Tazzoli[2], F. Danesin[2], G. Meneghesso[2], E. Zanoni[2], A. Curutchet[3], N. Malbert[3], N. Labat[3], B. Grimber[4], J.C. De Jaeger[4], [1]Alcatel-THALES III-V Lab, Marcoussis, France, [2]Universita degli Studi di Padova Via Gradenigo, Padova, Italy, [3]Universite Bordeaux, Talence Cedex, France, [4]IEMN/Tiger, Villeneuve d'Ascq, France

Session 24: 2005 IEDM Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
International Ballroom Center

Semiconductor Research & Development: Who will do it and who will pay for it in 2010?

Moore's clock is still the major driver of our industry. But the growing technical requirements make manufacturing facilities increasingly expensive. This has caused a rising number of manufacturing joint ventures. But as R&D budgets are increasing faster than chip makers' revenues, and since we don't want to slow down Moore's clock, R&D is consolidating in major initiatives and institutes. As the industry is confronting the challenges of the coming 450mm wafer generation and of replacing the CMOS transistor by a "new switch", some questions seem legitimate: can we afford to slow down the clock? or will the consolidation continue? And if so, will this result in the ultimate global "public-private partnership", necessary to preserve the productivity gains that invigorate other sectors of the economy? What is the role of the equipment and material suppliers?

But there is another aspect that deserves attention. Everybody will agree that technological innovation is an important driver of economic growth. But to what extent are the dynamics of innovation determined by the relations between states and regions, and between governments and firms? Is a "techno-national" approach preferred, in which a nation or region invest heavily in order to exert control over the generation of semiconductor knowledge and attempts to acquire leadership or to avoid delocalization of its industry? Is a "techno-globalist" approach to be preferred, in which states will rather provide the necessary infrastructure for ambitious exploratory research while firms are responsible for technology development? And where does scientific excellence come into the picture? How long can companies do it on their own? What about industrial alliances? What about consortia and/or research institutes? What is the best way to share the future costs of semiconductor R&D?

To debate these topics we have invited a distinguished panel of leaders from industry and R&D organizations. Coming from Asia, Europe and the US they will be able to present a truly global perspective on these important issues.

Moderator: Gilbert Declerck, IMEC

Panel Members:

Chun-Yen Chang
National Chiao Tung University

Paolo Gargini
Intel

Giang Dao
Sematech

Hisatsune Watanabe
SELETE

Arthur Del Prado
ASMI

Joel Hartman
Crolles Alliance

Jack Sun
TSMC

Bernie Meyerson
IBM

Joo-Tae Moon
Samsung

Session 25: 2005 IEDM Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
International Ballroom East

Will Non-Volatile Memory Scale Past the End of the Decade?

Non-Volatile Memory, mainly Flash memory, has seen explosive growth over the past several years due to the emergence of portable consumer devices such as cell phones, cameras, and music players. This rapid growth is anticipated to continue as the reducing cost of NVM enables large amounts of rugged, low power, solid state storage in a very small space.

Flash memory has followed the scaling evolution of the semiconductor roadmap since its introduction in the late '80's, but further scaling is becoming increasingly complex as some of the fundamental physical charge storage limitations are being approached. While continued research on floating gate techniques should extend the current Flash technology capability through the end of this decade, there is increasing concern about scalability into the next decade. At the same time many new memory storage mechanisms and materials are showing promise as potential Flash replacement.

This panel will attempt to answer the question of Flash scalability by identifying the scaling issues and potential solutions as well as their timing for introduction into the Flash roadmap for the rest of this decade and well into next decade, including the impact of new memory materials or storage mechanisms.

Moderator: *Greg Atwood, Intel*

Panel Members:

Roberto Bez
ST Microelectronics

Shiuchi Tahara
NEC

Kinam Kim
Samsung

Toshitake Yaegashi
Toshiba

Giorgio Baccarani
University of Bologna

Albert Fazio
Intel

Rich Liu
Macronix

Session 26: Modeling and Simulation – Transport in Advanced Planar CMOS Devices

Wednesday, December 7, 9:00 a.m.
International Ballroom West

Co-Chairs: Enrico Sangiorgi, University of Bologna
Martin Stadele, Infineon Technologies

9:05 a.m.
26.1 **First-Principles Modeling of Double-Gate UTSOI MOSFETs,** M. H. Evans*, M. Caussanel*, R. D. Schrimpf*, S. T. Pantelides*,^, *Vanderbilt University, Nashville, TN, ^Oak Ridge National Laboratory, Oak Ridge, TN

9:30 a.m.
26.2 **Novel Channel Materials for Ballistic Nanoscale MOSFETs Band Structure Effects**, A. Rahman, G. Klimeck, M. Lundstrom, Purdue University, West Lafayette, IN

9:55 a.m.
26.3 **Investigation of Performance Limits of III-V Double-Gate NMOSFETs**, A. Pethe, T. Krishnamohan, D. Kim, S. Oh, H.-S. P. Wong, K. C. Saraswat, Stanford University, Stanford, CA

10:20 a.m.
26.4 **Scaling the High-Performance Double-Gate SOI MOSFET Down to the 32 nm Technology Node with SiO_2-Based Gate Stacks**, N. Barin, M. Braccioli, C. Fiegna*, E. Sangiorgi*, University of Ferrara, Italy, *University of Bologno, Italy

10:45 a.m.
26.5 **A Study of the Effect of the Interface Roughness on a DG-MOSFET Using a Full 2D NEGF Technique**, A. Martinez, A. Svizhenko*, M. P. Anantram*, J. R. Barker, A. R. Brown, A. Asenov, University of Glasgow, Glasgow, United Kingdom, *NASA Ames Research Center, Moffet Field, CA

11:10 a.m.
26.6 **Multi-Subband Monte Carlo Modeling of Nano-MOSFETs With Strong Vertical Quantization and Electron Gas Degeneration**, L. Lucci, P. Palestri, D. Esseni, L. Selmi, University of Udine, Udine, Italy

Session 27: Process Technology – Fully-Silicided Gates

Wednesday, December 7, 9:00 a.m.
International Ballroom Center

Co-Chairs: Sunit Tyagi, Intel Corporation
S.C. Chen, TSMC

9:05 a.m.

27.1 **Physical Mechanism of Work Function Modulation Due to Impurity Pileup at Ni-FUSI/SiO(N) Interface**, Y. Tsuchiya, M. Yoshiki, M. Koyama, A. Kinoshita, J. Koga, Toshiba Corporation, Yokohama, Japan

9:30 a.m.
27.2 **An Easily Integrable NiSi TOSI-Gate/SiON-Module for LP SRAM Applications Based on a Single Step Silicidation of Gate and Junction**, M. Müller, A. Mondot*, N. Gierczynski, D. Aimé*, B.Froment*, F. Leverd*, P. Gouraud*, A. Talbot*, S. Descombes**, Y. Morand*, G. Ribes*, J.-M. Roux*, S.

Pokrant, F. André*, T.Skotnicki*, Philips Semiconductor, Crolles Cedex, France, *STMicroelectronics, Crolles Cedex, France, **CEA-LETI, Grenoble, France

9:55 a.m.
27.3 Modulation of the Ni FUSI Workfunction of by Yb Doping: from Midgap to N-Type Band-Edge, H.Y. Yu, J.D. Chen*, M.F. Li*, S.J. Lee*, D.L. Kwong^, M. van Dal**, J.A. Kittl, A. Lauwers, E. Augendre, S. Kubicek, C. Zhao, H. Bender, B. Brijs, L. Geenen, P. Absil, M. Jurczak, S. Biesemans, IMEC, Leuven, Belgium, *SNDL, Singapore, **Philips Research, Leuven, Belgium, ^University of Texas, Austin, TX

10:20 a.m.
27.4 Lanthanide and Ir-based Dual Metal-Gate/HfAlON CMOS with Large Work-Function Difference, D. S. Yu*, A.Chin*,#, C. H. Wu^, M.-F. Li#, C. Zhu#, S. J. Wang^, W. J. Yoo#, B. F. Hung*, S. P. McAlister^^, *National Chiao-Tung University, Taiwan, R.O.C., #National University of Singapore, Singapore, ^National Cheng Kung University, Taiwan, R.O.C., ^^National Research Council of Canada, Ottawa, Cananda

10:45 a.m.
27.5 Demonstration of Ni Fully GermanoSilicide as a pFET Gate Electrode Candidate on HfSiON, H.Y. Yu, R. Singanamalla, K. Opsomer, E. Augendre, E. Simoen, J.A. Kittl, S. Kubicek, S. Severi, X.P. Shi, S. Brus, C. Zhao, J.F. de Marneffe, S. Locorotondo, D. Shamiryan, M. Van Dal*, A. Veloso, A. Lauwers, M. Niwa, K. Maex, K. D. Meyer, P. Absil, M. Jurczak, S. Biesemans, IMEC, Leuven, Belgium, *Philips Research, Leuven, Belgium

11:10 a.m.
27.6 Systematic Study of Workfunction Engineering and Scavenging Effect Using NiSi Alloy FUSI Metal Gates with Advanced Gate Stacks, Y.H. Kim, C. Cabral, Jr., E.P. Gousev, R. Carruthers, L. Gignac, M. Gribelyuk, E. Cartier, S. Zarfar, M. Copel, V. Narayanan, J. Newbury, B. Price, J. Accevedo, P. Jamison, B. Linder, W. Natzle, J. Cai, R. Jammy, M. Ieong, IBM SRDC, Yorktown Heights, NY

11:35 a.m.
27.7 CMOS Integration of Dual Work Function Phase Controlled Ni FUSI with Simultaneous Silicidation of NMOS (NiSi) and PMOS (Ni-rich silicide) Gates on HfSiON, A. Lauwers, A. Veloso, T. Hoffmann, M.J.H. van Dal, C. Vrancken, S. Brus, S. Locorotondo, J.-F. de Marneffe, B. Sijmus, S. Kubicek, T. Chiarella, M.A. Pawlak, K. Opsomer, M. Niwa, R. Mitsuhashi, K.G. Anil, H.Y. Yu, C. Demeurisse, R. Verbeeck, P. Absil, K. Maex, M. Jurczak, S. Biesemans, J. A. Kittl, IMEC, Leuven, Belgium

12:00 p.m.
27.8 NixTa1-xSi and NixPt1-xSi Ternary Alloys for Work Function Tuning on SiO2, HfSiOx and HfO2 Dielectrics, N. Biswas, S. Novak, M. Ozturk, V. Misra, North Carolina State Univerisity, Raleigh, NC

Session 28: Integrated Circuits and Manufacturing – Advanced SRAM and Novel Integration Technology

Wednesday, December 7, 9:00 a.m.
International Ballroom East

Co-Chairs: Tahir Ghani, Intel Corporation
Ted Houston, Texas Instruments, Inc.

9:05 a.m.
28.1 Erratic Fluctuations of SRAM Cache Vmin at the 90nm Process Technology Node, M. Agostinelli, J. Hicks, J. Xu, B. Woolery, K. Mistry, K. Zhang, S. Jacobs, J. Jopling, W. Yang, B. Lee, T. Raz, M. Mehalel, P. Kolar, Y. Wang, J. Sandford, D. Pivin, C. Peterson, M. DiBattista, S. Pae, M. Jones, S. Johnson, G. Subramanian, Intel Corporation, Hillsboro, OR

9:30 a.m.
28.2 Fluctuation Limits and Scaling Opportunities for CMOS SRAM Cells, A. Bhavnagarwala, S. Kosonocky, C. Radens*, K. Stawiasz, R. Mann*, Q. Ye*, K. Chin, IBM T.J. Watson Research Center, Yorktown Heights, NY, *IBM Systems & Technology Group, Hopewell Junction, NY

9:55 a.m.
28.3 High Density and High Speed SRAM Bit-Cells and Ring Oscillators due to Laser Annealing for 45nm Bulk CMOS, A. Pouydebasque, B. Dumont*, S. Denorme*, F. Wacquant*, M. Bidaud, C. Laviron^, A. Halimaoui*, C. Chaton^, J.D. Chapon*, P. Gouraud*, F. Leverd*, H. Bernard*, S. Warrick**, D. Delille, K. Romanjek, R. Gwoziecki^, N. Planes*, S. Vadot*, I. Pouilloux, F. Arnaud*, F. Boeuf*, T. Skotnicki*, Philips Semiconductors, Crolles, France, *STMicroelectronics, Crolles, France, **Freescale Semiconductor, Crolles, France, ^CEA-LETI, Grenoble, France

10:20 a.m.
28.4 Ultra-Fast Programming of Silicided Polysilicon Fuses Based on New Insights in the Programming Physics, T.S. Doorn, M. Altheimer*, Philips Research, Eindhoven The Netherlands, *Philips Semiconductors, Valbonne, France

10:45 a.m.
28.5 Wafer-Level Compliant Bump for Three-Dimensional LSI with High-Density Area Bump Connections, N. Watanabe, T. Kojima, T. Asano, Kyushu Institute of Technology, Fukuoka, Japan

11:10 a.m.
28.6 Successful Transferring of Active Transistors, RF-Passive Components and High Density Interconnect from Bulk Si to Organic Substrates, L. H. Guo, Q. X. Zhang, H. Y. Li, E. B. Liao, L. K. Bera, W. Y. Loh, C. C. Kuo, G. Q. Lo, N. Balasubramanian, D. L. Kwong, Institute of Microelectronics, Singapore

11:35 a.m.
28.7 Fabrication and Characterization of CMOSFETs on Porous Silicon for Novel Device Layer Transfer, H. Sanda, J. McVittie, M. Koto*, T. Yonehara*, Y. Nishi, Stanford University, Stanford, CA, *Canon Inc., Kanagawa, Japan

Session 29: CMOS and Interconnect Reliability – Bias-Temperature Instability and Inteface Traps

Wednesday, December 7, 9:00 a.m.
Georgetown Room

Co-Chairs: Ben Kaczer, IMEC
Ming-Fu Li, National University of Singapore and Institute of Microelectronics Singapore

9:05 a.m.
29.1 On the Dispersive Versus Arrhenius Temperature Activation of NBTI Time Evolution in Plasma Nitrided Gate Oxides: Measurements, Theory, and Implications, D. Varghese, D. Saha, S. Mahapatra, K. Ahmed*, F. Nouri*, M. Alam**, IIT Bombay, Mumbai, India, *Applied Materials, CA, **Purdue University, West Lafayette, IN

9:30 a.m.
29.2 Material Dependence of Hydrogen Diffusion and its Implications for NBTI Degradation, A. T. Krishnan, C. Chancellor, S. Chakravarthi, P. E. Nicollian, V. Reddy, A. Varghese, R. B. Khamankar, S. Krishnan, Texas Instruments, Dallas, TX

9:55 a.m.
29.3 Negative Bias Temperature Instability of Carrier-Transport Enhanced pMOSFET with Performance Boosters, H. S. Rhee, H. Lee, T. Ueno, D. S. Shin, S. H. Lee, M. Kim, H. S. Kim, N.-I. Lee, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea

10:20 a.m.
29.4 Defect Passivation with Fluorine in a Ta_xC_y/High-K Gate Stack for Enhanced Device Threshold Voltage Stability and Performance, H.-H. Tseng, P.J. Tobin, E. A. Hebert, S. Kalpat, M. E. Ramón, L. Fonseca, Z. X. Jiang, J. K. Schaeffer, R. I. Hegde, D. H. Triyoso, D. C. Gilmer, W. J. Taylor, C. C. Capasso, O. Adetutu, D. Sing, J. Conner, E. Luckowski, B. W. Chan, A. Haggag, S. Backer, R. Noble, M. Jahanbani, Y. H. Chiu, B. E. White, Freescale Semiconductor Inc., Austin, TX

10:45 a.m.
29.5 Accurate Circuit Performance Prediction Model and Lifetime Prediction Method of NBT Stressed Devices for Highly Reliable ULSI Circuits, R. Kuroda, K. Watanabe, A. Teramoto, M. Mifuji*, T. Yamaha*, S. Sugawa, T. Ohmi, Tohoku University, Sendai, Japan, *ROHM Co. Ltd., Shizuoka, Japan

11:10 a.m.
29.6 On-Chip Charge Pumping Method for Characterization of Interface States of Ultra Thin Gate Oxide in Nano CMOS Technology, H.-H. Ji, Y.-G. Kim, I.-S. Han, K.-M. Kim, J.-S. Wang, H.-D. Lee, S.-H. Park*, H.-S. Lee*,Y.-S. Kang*, D.-B. Kim*, C.-Y. Lee*, I.-H. Cho*, S.-Y. Kim*, S.-B. Hwang*, J.-G. Lee*, J.-W. Park*, Chungnam National University, Daejeon, Korea, *Magnachip Semiconductor Inc., Choongbuk, Korea

Session 30: CMOS Devices – SOI and Multi-Gate Devices

Wednesday, December 7, 9:00 a.m.
Jefferson Room

Co-Chairs: Hitoshi Wakabayashi, NEC Corporation
Serge Biesemans, IMEC

9:05 a.m.
30.1 High Performance Multi-Gate pMOSFETs using Uniaxially-Strained SGOI Channels, T. Irisawa, T. Numata, T. Tezuka, K. Usuda, S. Nakaharai, N. Hirashita, N. Sugiyama, E. Toyoda*, S.-I Takagi**, MIRAI-ASET, **MIRAI-AIST, *Toshiba Corporation, Kawasaki, Japan

9:30 a.m.
30.2 Inverted T Channel FET (ITFET) — Fabrication and Characteristics of Vertical-Horizontal, Thin Body, Multi-Gate, Multi-Orientation Devices, ITFET SRAM Bit-Cell Operation. A Novel Technology for 45nm and Beyond CMOS, L. Mathew, M. Sadd, S. Kalpat M. Zavala, T. Stephens, R. Mora, S. Bagchi, C. Parker, J. Vasek, D. Sing, R. Shimer, L. Prabhu, G.O. Workman, G. Ablen, Z.Shi, J. Saenz, B. Min, D. Burnett, B.-Y. Nguyen, J. Mogab, M.M. Chowdhury*, W. Zhang*, J.G. Fossum*, Freescale Semiconductor Inc., Austin, TX, *University of Florida, FL

9:55 a.m.
30.3 High Performance 5nm Radius Twin Silicon Nanowire MOSFET(TSNWFET) : Fabrication on Bulk Si Wafer, Characteristics, and Reliability, S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, J.-B. Park, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

10:20 a.m.
30.4 Process Integration Technology and Device Characteristics of CMOS FinFET on Bulk Silicon Substrate with Sub-10nm Fin Width and 20nm Gate Length, K. Okano, T. Izumida, H. Kawasaki, A. Kaneko, A. Yagishita, T. Kanemura, M. Kondo, S. Ito, N. Aoki, K. Miyano, T. Ono, K. Yahashi, K. Iwade, T. Kubota, T. Matsushita, I. Mizushima, S. Inaba, K. Ishimaru, K. Suguro, K. Eguchi, Y. Tsunashima, H. Ishiuchi, Toshiba Corporation Semiconductor Company, Yokohama, Japan

10:45 a.m.
30.5 GIDL (Gate-Induced Drain Leakage) and Parasitic Schottky Barrier Leakage Elimination in Aggressively Scaled HfO_2/TiN FinFET Devices, T. Hoffmann, G. Doornbos, I. Ferain, N. Collaert, P. Zimmerman, M. Goodwin, R. Rooyackers, K.G. Anil, Y. Yim, M. Jurczak, S. Biesemans, IMEC, Heverlee, Belgium

11:10 a.m.
30.6 Mobility Enhancement due to Volume Inversion in (110)-Oriented Ultra-thin Body Double-Gate nMOSFETs with Body Thickness Less Than 5 nm, G. Tsutsui, M. Saitoh, T. Saraya, T. Nagumo, T. Hiramoto, University of Tokyo, Tokyo, Japan

11:35 a.m.
30.7 Selective Epitaxial Channel Ground Plane Thin SOI CMOS Devices, Z. Ren, M. Ieong, J. Cai*, J. Holt, D. Boyd, R. Mo, H. Yin, O. Dokumaci, S. Kawanaka**, T. Sato**, P.

Ronsheim, J. Wang, C.Y. Sung, W. Haensch*, IBM SRDC, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY, **Toshiba America Electronic Components, Inc., Hopewell Junction, NY

Session 31: Solid-State and Nanoelectronic Devices – Resistive Switching Memories

Wednesday, December 7, 9:00 a.m.
Lincoln Room

Co-Chairs: Jean-Luc Autran, Universite Marsielle
Frans Widdershoven, Philips Research Leuven

9:05 a.m.
31.1 **Oxygen-Doped $Ge_2Sb_2Te_5$ Phase-Change Memory Cells Featuring 1.5-V/100-μA Standard 0.13μm CMOS Operations,** N. Matsuzaki, K. Kurotsuchi, Y. Matsui, O. Tonomura, N. Yamamoto, Y. Fujisaki, N. Kitai*, R. Takemura, K. Osada, S. Hanzawa, H. Moriya, T. Iwasaki, T. Kawahara, N. Takaura, M. Terao, M. Matsuoka^, M. Moniwa^, Hitachi Limited, Tokyo, Japan, *Hitachi ULSI Systems Co. Ltd., Tokyo, Japan, ^Renesas Technology Corp., Hyogo, Japan

9:30 a.m.
31.2 **Impact of Crystallization Statistics on Data Retention for Phase Change Memories,** A. Redaelli, D. Ielmini, A. L. Lacaita, F. Pellizzer*, A. Pirovano*, and R. Bez*, Politecnico di Milano, Milano, Italy, *STMicroelectronics, Agrate Brianza, Italy.

9:55 a.m.
31.3 **Non-Volatile Resistive Switching for Advanced Memory Applications,** A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, M. Taguchi, Spansion LLC, Sunnyvale, CA

10:20 a.m.
31.4 **Multi-Layer Cross-Point Binary Oxide Resistive Memory (OxRRAM) for Post-NAND Storage Application,** I. G. Baek, D. C. Kim*, M. J. Lee*, H. J. Kim, M. S. Lee, J. E. Lee, S. E. Ahn*, S. Seo*, J. H. Lee*, J. C. Park*, Y. K. Cha*, S. O. Park, H. S. Kim, I. K. Yoo*, U-I. Chung, J. T. Moon, B. I. Ryu, Samsung Electronics Co. Ltd., Kyeonggi-Do, Korea, *Samsung Advanced Institute of Technology, Kyeonggi-Do, Korea

10:45 a.m.
31.5 **Conductive Bridging RAM (CBRAM): An Emerging Non-Volatile Memory Technology Scalable to Sub 20nm,** M. Kund, G. Beitel, C.-U. Pinnow, T. Röhr, J. Schumann*, R. Symanczyk, K.-D. Ufert, G. Müller, Infineon Technologies AG, Munich, Germany, *Infineon Technologies, Dresden, Germany

11:10 a.m.
31.6 **Excellent Resistance Switching Characteristics of Pt/$SrTiO_3$ Schottky Junction for Multi-bit Nonvolatile Memory Application,** H. Sim, H. Choi, D. Lee, M. Chang, D. Choi, Y. Son, E.-H. Lee*, W. Kim*, Y. Park*, I.-K. Yoo*, H. Hwang, Gwangju Institute of Science and Technology, Gwangju, Korea, *Samsung Advanced Institute of Technology, Suwon, Korea

Session 32: Quantum, Power, and Semiconductors Devices

Wednesday, December 7, 9:00 a.m.
Military Room

Co-Chairs: Jesus del Alamo, Massachusetts Institute of Technology
Tetsuya Suemitsu, NTT Photonics Laboratories

9:05 a.m.
32.1 85nm Gate Length Enhancement and Depletion Mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications, S. Datta, T. Ashley*, R. Chau, K. Hilton*, R. Jefferies*, T. Martin*, T. Phillips*, Intel Corporation, Hillsboro, OR, *QinetiQ, Malvern, United Kingdom

9:30 a.m.
32.2 Performance Evaluation of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs For Beyond-CMOS Logic Applications, D. H. Kim, J. A. del Alamo, J. H. Lee*, K. S. Seo*, MIT, Cambridge, MA, *Seoul National University, Seoul, Korea

9:55 a.m.
32.3 Monolithic Integration of Enhancement- and Depletion-mode AlGaN/GaN HEMTs for GaN Digital Integrated Circuits, Y. Cai, Z. Cheng, W. C. W. Tang, K. J. Chen, K. M. Lau, Hong Kong University of Science and Technology, Hong Kong, R.O.C.

10:20 a.m.
32.4 Laterally Scaled-Down Tiered-Edge-Shaped Ohmic Structure of InP-based HEMTs for 2-S/mm gm and 500-GHz f_T, H. Matsuzaki, T. Maruyama*, M. Tokumitsu, T. Enoki, NTT Corporation, Kanagawa, Japan, *NTT Advanced Technology Corporation, Kanagawa, Japan

10:45 a.m.
32.5 The InP/GaAsSb Type-II Heterostructure System and its Application to High-Speed DHBTs and Photodetectors: Physics, Surprises, and Opportunities (Invited), C.R. Bolognesi, H.G. Liu, D.W. DiSanto, N.G. Tao, L. Zheng, X. Zhang, S.P. Watkins, Simon Fraser University, Burnaby BC, Canada

11:10 a.m.
32.6 Non-Uniform Degradation Behavior Across Device Width in RF Power GaAs PHEMTs, A. A. Villanueva, J. A. del Alamo, T. Hisaka*, K. Hayashi*, M. Somerville**, MIT, Cambridge, MA, *Mitsubishi Electric, Hyogo, Japan, **Olin College, Needham, MA

Session 33: Displays, Sensors and MEMS – Image Sensors and Photon Detectors

Wednesday, December 7, 9:00 a.m.
Thoroughbred Room

Co-Chairs: Keiji Mabuchi, Sony Corporation
Homayoon Haddad, Agilent Technologies

9:05 a.m.
33.1 A High-Performance and Low-Noise CMOS Image Sensor with an Expanding Photodiode Under the Isolation Oxide, K. Itonaga, H. Abe, I. Yoshihara, T. Hirayama, Sony Corporation, Kanagawa, Japan

9:30 a.m.
33.2 The Features and Characteristics of 1/3" 5M CMOS Image Sensor with 1.9x1.9µm^2 Pixels, C.-R. Moon, J. Jung, D. Kwon, S.-H. Lee, J.-S. Roh, K.-H. Paik, D.-C. Park, H. Kim, H. Jeong, J.-H. Sim, H. Noh, K. Lee, D. Lee, K. Kim, Samsung Electronics Co. Ltd., Gyeonggi-Do, Korea

9:55 a.m.
33.3 The Hole Role (Invited), A. Theuwissen, J. Bosiers, E. Roks, DALSA, Eindhoven, Netherlands

10:20 a.m.
33.4 High-Speed Blue-, Red-, and Infrared-Sensitive Photodiode Integrated in a 0.35µm SiGe:C-BiCMOS Process, G. Meinhardt, J. Kraft, B. Löffler, H. Enichlmair, G. Röhrer, E. Wachmann, M. Schrems, R. Swoboda*, C. Seidl*, H. Zimmermann*, Austriamicrosystems, Unterpremstätten, Austria, *Vienna University of Technology-EMST, Vienna, Austria

10:45 a.m.
33.5 A 28 Mega Pixel Large Area Full Frame CCD with 2x2 On-Chip RGB Charge Binning for Professional Digital Still Imaging, C. Draijer, F. Polderdijk, A. van der Heide, B. Dillen, W. Klaassens, J. Bosiers, DALSA Professional Imaging, Eindhoven, The Netherlands

11:10 a.m.
33.6 Influence of Terrestrial Cosmic Rays on the Reliability of CCD Image Sensors, A. Theuwissen, Bree, Belgium

11:35 a.m.
33.7 On-Chip Detection and Counting of Single-Photons, S. Tisa, F. Zappa, I. Labanca, Politecnico di Milano, Milano, Italy

12:00 p.m.
33.8 An Intra-Chip Electro-Optical Channel Based on CMOS Single Photon Detectors, M. Sergio, E. Charbon, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland

Session 34: Process Techology – Advanced FEOL Technology

Wednesday, December 7, 1:30 p.m.
International Ballroom West

Co-Chairs: Kyoichi Suguro, Toshiba Corporation
Mehmet Ozturk, North Carolina State University

1:35 p.m.
34.1 A Simple Approach to Optimizing Ultra-thin SiON Gate Dielectrics Independently for n- and p-MOSFETs, S. Tsujikawa, H. Umeda, T. Kawahara, Y. Kawasaki, K. Shiga, T. Yamashita, T. Hayashi, J. Yugami, Y. Ohno, M. Yoneda, Renesas Technology Corporation, Hyogo, Japan

2:00 p.m.
34.2 Dramatic Improvement of V_{fb} Shift and G_m^{max} with Ultra-Thin and Ultra-Low-Leakage SiN-Based SiON Gate Dielectrics, D. Matsushita, K. Muraoka, Y. Nakasaki, K. Kato, S. Kikuchi, K. Sakuma, Y. Mitani, K. Eguchi, M. Takayanagi, Toshiba Corporation, Yokohama, Japan

2:25 p.m.
34.3 Interface States as an Active Component for 20 nm Gate-Length Planar MOSFET with ElectroStatic Channel Extension (ESCE), G.H. Buh, T. Park, G.H. Yon, C.W. Ryoo, D.C. Kim, Y.G. Shin, U-I. Chung, J.T. Moon, Samsung Electronics Company, Kyunggi-Do, Korea

2:50 p.m.
34.4 Single Stress Liner for Both NMOS and PMOS Current Enhancement by a Novel Ultimate Spacer Process, Y. C. Liu, J.W. Pan, T.Y. Chang, P.W. Liu, B.C. Lan, C.H. Tung, C.H. Tsai, T.F. Chen, C.J. Lee, W.M. Wang, Y.A. Chen, H.L. Shih, L.Y. Tung, L.W. Cheng, T.M. Shen, S.C. Chiang, M.F. Lu, W.T. Chang, Y.H. L*, D. Nayak*, D. Gitlin*, H.L. Meng, C.T. Tsai, United Microelectronics Corporation, Hsin-Chu, Taiwan, *Xilinx, San Jose, CA

3:15 p.m.
34.5 Damage-Free Neutral Beam Etching Technology for High Mobility FinFETs, K. Endo, S. Noda*, M. Masahara, T. Kubota*, T. Ozaki*, S. Samukawa*, Y. Liu, K. Ishii, Y. Ishikawa, E. Sugimata, T. Matsukawa, H. Takashima, H. Yamauchi, E. Suzuki, National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan, *Tohoku University, Miyagi, Japan

3:40 p.m.
34.6 Sidewall Transfer Process and Selective Gate Sidewall Spacer Formation Technology for Sub-15nm FinFET with Elevated Source/Drain Extension, A. Kaneko, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, S. Inaba, T. Izumida, T. Kanemura, N. Aoki, K. Ishimaru, H. Ishiuchi, K. Suguro, K. Eguchi, Y. Tsunashima, Toshiba Corporation Semiconductor Company, Yokohama, Japan

Session 35: Integrated Circuits and Manufacturing – Non-Volatile Memories

Wednesday, December 7, 1:30 p.m.
International Ballroom Center

Co-Chairs: Roberto Bez, STMicroelectronics
Sang-Pil Sim, Samsung Electronics

1:35 p.m.
35.1 A 65nm NOR Flash Technology with 0.042µm^2 Cell size for High Performance Multilevel Application, G. Servalli, D. Brazzelli, E. Camerlenghi, G. Capetti, S. Costantini, C. Cupeta, D. De Simone, A. Ghetti, T. Ghilardi, P. Gulli, M. Mariani, A. Pavan, R. Somaschini, STMicroelectronics, Agrate Brianza, Italy

2:00 p.m.
35.2 35 nm Floating Gate Planar MOSFET Memory Using Double Junction Tunneling, R. Ohba, Y. Mitani, N. Sugiyama, S. Fujita, Toshiba Corporation, Yokohama, Japan

2:25 p.m.
35.3 Experimental and Theoretical Analysis of Scaling Issues in Dual-Bit Discrete Trap Non-Volatile Memories, L. Perniola[1,2,3], G. Iannaccone[1], B. De Salvo[2] G. Ghibaudo[3], G. Molas[2], C. Gerardi[4], S. Deleonibus[2], [1]Universita di Pisa, Pisa, Italy, [2]CEA-LETI, Grenoble, France, [3]IMEP-CNRS/INPG, Grenoble, France, [4]STMicroelectronics, Catane, Italy

2:50 p.m.
35.4 Robust Multi-bit Programmable Flash Memory Using a Resonant Tunnel Barrier, S. Kim, S. Jae Baik, Z. Huo, I.-S. Yeo, U. -I. Chung, J. T. Moon, B.-I. Ryu, Samsung Electronics Co. Ltd., Gyeonggi-Do, Korea

3:15 p.m.
35.5 Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E Speed., K.-H. Joo, X. Wang, S.-H. Lim, S.-J. Baik, Y.-W. Cha, I.-S. Yeo, U. -I. Chung, J. T. Moon, B.-I. Ryu, Samsung Electronics Co. Ltd., Gyeonggi-Do, Korea

3:40 p.m.
35.6 Quality Assured Mass Productive 1.6V Operational 0.18 µm 1T1C FRAM Embedded Smart Card with Advanced Integration Technologies against Defectives, J.-H. Kim, B.J. Koo, Y. M. Kang, J. H. Park, H. J. Joo, S. K. Kang, D. Y. Choi, H. S. Rhie, S. Y. Lee, H. S. Jeong, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

4:05 p.m.
35.7 High Speed Toggle MRAM with MgO-Based Tunnel Junctions, J.M. Slaughter, J. Calder, R. W. Dave, M. DeHerrera, M. Durlam, B. Garni, K. Smith, S. Tehrani, Freescale Semiconductor Inc., Chandler, AZ

4:30 p.m.
35.8 Assessment of Threshold Switching Dynamics in Phase-Change Chalcogenide Memories, D. Ielmini, A. L. Lacaita, D. Mantegazza, F. Pellizzer*, A. Pirovano*, Politecnico di Milano, Milano, Italy, *STMicroelectronics, Agrate Brianza, Italy

Session 36: CMOS Devices – Advanced Gate Stacks

Wednesday, December 7, 1:30 p.m.
International Ballroom East

Co-Chairs: Robert Lander, Philips Research Leuven
Kelin Kuhn, Intel Corporation

1:35 p.m.
36.1 HfSiON-CMOSFET Technology for Low Standby Power Applications (Invited), M. Takayanagi, T. Watanabe, R. Iijima*, M. Koyama*, T. Ino*, M. Koike*, K. Sekine, K. Eguchi, A. Nishiyama*, K. Ishimaru*, Toshiba Corporation Semiconductor Co., Yokohama, Japan, *Toshiba Corporation, Yokohama, Japan

2:00 p.m.
36.2 Demonstration of Recessed SiGe S/D and Inserted Metal Gate on HfO_2 for High Performance pFETs, P. Verheyen, G. Eneman, R. Rooyackers, R. Loo, L. Eeckhout, D. Rondas, F. Leys, J. Snow, D. Shamiryan, M. Demand, Th. Y. Hoffman, M. Goodwin, H. Fujimoto, C. Ravit, B-C. Lee, M. Caymax, K. De Meyer, P. Absil, M. Jurczak, S. Biesemans, IMEC, Heverlee, Belgium

2:25 p.m.
36.3 High Performance nMOSFET with $HfSi_x/HfO_2$ Gate Stack by Low Temperature Process, T. Hirano, T. Ando, K. Tai, S. Yamaguchi, T. Kato, S. Hiyama, Y. Hagimoto, S. Takesako, N. Yamagishi, K. Watanabe, R. Yamamoto, S. Kanda, S. Terauchi, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, S. Kadomura, N. Nagashima, Sony Corporation, Kanagawa, Japan

2:50 p.m.
36.4 Direct Measurement of Carrier Profiles in Operating Sub-30nm N-MOSFETs, H. Fukutome, Y. Momiyama*, E. Yoshida, M. Okuno, T. Itakura**, T. Aoyama, Fujitsu Laboratory Ltd., *Fujitsu Limited, **Fujitsu Analysis Lab, Tokyo, Japan

3:15 p.m.
36.5 Device and Circuit-Level Analog Performance Trade-Offs: A Comparative Study of Planar Bulk FETs Versus FinFETs, V. Subramanian[1,2], B. Parvais[1], J. Borremans[1,3], A. Mercha[1], D. Linten[1,3], P. Wambacq[1,3], J. Loo[1], M. Dehan[1], N. Collaert[1], S. Kubicek[1], R.J.P. Lander[4], J.C. Hooker[4], F.N. Cubaynes[4], S. Donnay[1], M. Jurczak[1], G. Groeseneken[1,2], W. Sansen[2], S. Decoutere[1], [1]IMEC, Leuven, Belgium, [2]K.U. Leuven, Leuven, Belgium, [3]V.U. Brussels, Brussels, Belgium, [4]Philips Research Leuven, Leuven, Belgium

3:40 p.m.
36.6 Drive Current Enhancement in High-k/Metal Gate Germanium-Carbide pMOSFETs Fabricated Directly on Si Substrates, D.Q. Kelly, J.P. Donnelly, S.V. Joshi, S. Dey, D.I. Garcia Gutierrez, M. Jose Yacamán, S.K. Banerjee, University of Texas at Austin, Austin, TX

4:05 p.m.
36.7 Vth Tunable CMIS Platform with High-k gate Dielectrics for 45-nm node, T. Hayashi, M. Mizutani, M. Inoue, J. Yugami, J. Tsuchimoto, M. Anma, S. Komori, K. Tsukamoto, Y. Tsukamoto, K. Nii, Y. Nishida, H. Sayama, T. Yamashita, H. Oda, T. Eimori, Y. Ohji, Renesas Technology Corporation, Hyogo, Japan

Session 37: Displays, Sensors and MEMS – Thin Film Transistors for Displays and System on Panel

Wednesday, December 7, 1:30 p.m.
Georgetown Room

Co-Chairs: Kyuha Chung, Samsung Electronics
Akintunde Akinwande, Massachusetts Institute of Technology

1:35 p.m.
37.1 0.1µm Poly-Si Thin Film Transistors for System-on-Panel (SoP) Applications, B.-Y. Tsui*,^, C.-P. Lin*, C.-F. Huang*, Y.-H. Xiao*, *National Chiao Tung University, Taiwan, R.O.C., ^National Nano Device Laboratories, Taiwan, R.O.C.

2:00 p.m.
37.2 High Mobility N-Channel and P-Channel Nanocrystalline Silicon Thin Film Transistors, C.-H. Lee, A. Sazonov, A. Nathan, University of Waterloo, Waterloo, Canada

2:25 p.m.
37.3 High Performance Single Grain Si TFTs Inside a Location-Controlled Grain by µ-Czochralski Process with Capping Layer, R. Vikas, R. Ishihara, Y. Hiroshima*, D. Abe*, S. Inoue*, T. Shimoda*, J.W. Metselaar, C.I.M. Beenakker, Delft University of Technology, Delft, The Netherlands, *Seiko-Epson Corporation, Nagano, Japan

2:50 p.m.
37.4 Low Temperature Single Grain Thin Film Transistor (LTSG-TFT) with SOI Performance Using CMP-Flattened Micro-Czochralski Process, H. Shimada, Y. Hiroshima, T. Shimoda, Seiko Epson Corporation, Nagano, Japan

3:15 p.m.
37.5 2-bit Poly-Si-TFT Nonvolatile Memory Using Hafnium Oxide, Hafnium Silicate and Zirconium Silicate, Y.-H. Lin, C.-H. Chien, T.-H. Chou, T.-S. Chao, C.-Y. Chang, T.-F. Lei, National Chiao-Tung University, Taiwan, R.O.C.

3:40 p.m.
37.6 Highly Efficient Current Scaling AMOLED Panel Employing a New Current Mirror Pixel Fabricated by Excimer Laser Annealed Poly-Si TFTs, J.-H. Lee, W.-J. Nam, M.-K. Han, Y.-M. Ha*, C.-H. Lee*, S.-K. Hong*, Seoul National University, Seoul, Korea, *LG Philips LCD Co. Ltd., Gyungbuk, Korea

4:05 p.m.

37.7 Novel Solid-State Spatial Light Modulator on Integrated Circuits for High-Speed Applications with Electro-Optic Thin Film, Y. Fujimori, T. Fujii, T. Suzuki, H. Kimura, T. Fuchikami, T. Nakamura, H. Takasu, ROHM Co. Ltd., Kyoto, Japan

Session 38: Solid-State and Nanoelectronic Devices – Active and Passive Components in CMOS-Compatible Technologies

Wednesday, December 7, 1:30 p.m.
Jefferson Room

Co-Chairs: Yukihiro Kiyota, Sony Corporation
Jamal Deen, McMaster University

1:35 p.m.
38.1 **Tunable On-Chip Inductors Up to 5 GHz Using Patterned Permalloy Laminations**, J. Salvia, J.A. Bain, C.P. Yue, Carnegie Mellon University, Pittsburgh, PA

2:00 p.m.
38.2 **Compact On-Chip Monopole Antennas on 20-Ω-cm Silicon Substrates for Operation in the 5.8-GHz ISM Band**, J.-J. Lin, H.-T. Wu, K.K. O, University of Florida, Gainesville, FL

2:25 p.m.
38.3 **A Novel CMOS-Compatible L-Shaped Impact-Ionization MOS (LI-MOS) Transistor**, E.-H. Toh, G.H. Wang, G.-Q. Lo*, N. Balasubramanian*, C.-H. Tung*, F. Benistant, L. Chan, G. Samudra, Y.-C. Yeo, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore

2:50 p.m.
38.4 **70nm Impact-Ionization Metal Oxide Semiconductor (I-MOS) Devices Integrated with Tunneling Field Effect Transistors (TFETs)**, W.Y. Choi, J.Y. Song, J.D. Lee, Y.J. Park, B.-G. Park, Seoul National University, Seoul, Korea

3:15 p.m.
38.5 **From DRAM to SRAM with a Novel SiGe-based Negative Differential Resistance (NDR) Device**, Y. Liang*, K. Gopalakrishnan*,^, P.B. Griffin*, J.D. Plummer*, *Stanford University, Stanford, CA, ^IBM Almaden Research Center, San Jose, CA

3:40 p.m.
38.6 **Low-Cost Self-Aligned SiGeC HBT Module for High-Performance Bulk and SOI RFCMOS Platforms**, P. Chevalier, D. Lagarde, G. Avenier, T. Schwartzmann, B. Barbalat, D. Lenoble, J. Bustos, F. Saguin, B. Vandelle, L. Rubaldo, A. Chantre, STMicroelectronics, Crolles, France

Session 39: Modeling and Simulation – Simulation of Doping and Stress Effects in Advanced CMOS

Wednesday, December 7, 1:30 p.m.
Lincoln Room

Co-Chairs: Conor Rafferty, Noble Device Technologies
Juergen Lorenz, Fraunhofer IISB

1:35 p.m.
39.1 **Understanding, Modeling and Optimizing Vacancy Engineering for Stable Highly Boron-Doped Ultrashallow Junctions**, N.E.B. Cowern, A.J. Smith, B. Colombeau, R. Gwilliam, B.J. Sealy, University of Surrey, Guildford, United Kingdom

2:00 p.m.
39.2 **Ultra-Thin-Body Fully-Depleted SOI Metal Source/Drain**

MOSFETs and ITRS Low-Standby-Power Targets Through 2018, D. Connelly, P. Clifton, C. Faulkner, D.E. Grupp, Acorn Technologies, Palo Alto, CA

2:25 p.m.
39.3 Moderately Doped Channel Multiple-FinFET for Logic Applications, Y. Shiho, Freescale Semiconductor Inc., Austin, TX

2:50 p.m.
39.4 Practical FinFET Design Considering GIDL for LSTP (Low Standby Power) Devices, K. Tanaka, K. Takeuchi, M. Hane, NEC Corporation, Sagamihara, Japan

3:15 p.m.
39.5 Thermal Phenomena in Deeply Scaled MOSFETs (Invited), J. A. Rowlette*, E. Pop*, S. Sinha*,^, M. Panzer*, K. E. Goodson*, *Stanford University, Stanford, CA, ^Intel Corporation, Hillsboro, OR

3:40 p.m.
39.6 Dual Stress Capping Layer Enhancement Study for Hybrid Orientation FinFET CMOS Technology, K. Shin, T.-J. King, University of California, Berkeley, CA

4:05 p.m.
39.7 A Full Self-Consistent Methodology for Strain-Induced Effects Characterization in Silicon Devices, P. Fantini, A. Ghetti, G.P. Carnevale, E. Bonera*, D. Rideau**, STMicroelectronics, Agrate Brianza, Italy, *Laboratorio Nazionale MDM-INFM, Agrate Brianza, Italy, **STMicroelectronics, Crolles Cedex, France

Session 40: Quantum, Power, and Compound Semiconductor Devices

Wednesday, December 7, 1:30 p.m.
Military Room

Co-Chairs: James Harris, Stanford University
Asif Khan, University of South Carolina

1:35 p.m.
40.1 Light Emitting Silicon Nanostructures (Invited), L. Dal Negro, M. Stolfi, J. H. Yi, J. Michel, J. LeBlanc*, J. Haavisto*, L.C. Kimerling, MIT, Cambridge, MA, *Charles Stark Draper Laboratory, Cambridge, MA

2:00 p.m.
40.2 Strain-Enhanced Si/Ge Heterojunction LED and GOI Detector, M.H. Liao, C.-Y. Yu, C.-F. Huang, C.-H. Lin, C.-J. Lee, M.-H. Yu, S.T. Chang*, C.-Y. Liang, C.-Y. Lee, T.-H. Guo, C.-C. Chang, C.W. Liu, National Taiwan University, Taiwan, R.O.C., *National Chung Hsing University, Taiwan, R.O.C.

2:25 p.m.
40.3 Dislocation Engineering for a Silicon-Based Light Emitter at 1.5 µm, M. Kittler*,#, M. Reiche^, T. Arguirov#, W. Seifert*,#, X. Yu*,#, *IHP GmbH, Frankfurt, Germany, #IHP/BTU Joint Lab, Cottbus, Germany, ^MPI für Mikrostrukturphysik, Halle, Germany

2:50 p.m.
40.4 Failure Mechanisms of Gallium Nitride LEDs Related with Passivation, M. Meneghini, L. Trevisanello, S. Levada, G.

Meneghesso, G. Tamiazzo, E. Zanoni T. Zahner*, U. Zehnder*, V. Härle*, University of Padova, Padova, Italy, *Osram Opto Semiconductors, Regensburg, Germany

3:15 p.m.
40.5 A Novel Silicon-Nitride Based Light-Emitting Transistor (SiNLET): Optical/Electrical Properties of a SONOS-Type Three-Terminal Electroluminescence Device for Optical Communication in ULSI, C.C. Yeh*, T. Wang*, Y.R. Chen*, F.M. Pan*, S.H. Gu*, W.J. Tsai, T.C. Lu, Y.Y. Liao, W.C. Ting, J. Ku, C-Y Lu, Macronix International Co. Ltd., Taiwan, R.O.C., *also with National Chiao-Tung University, Hsin-Chu, Taiwan

Session 41: Modeling and Simulation – System Level Device Modeling

Wednesday, December 7, 1:30 p.m.
Thoroughbred Room

Co-Chairs: Reinout Woltjer, Philips Research Laboratories Eindhoven
Tatsuya Kunikiyo, Renesas Technology Corporation

1:35 p.m.
41.1 Analysis and Implications of IC Cooling for Deep Nanometer Scale CMOS Technologies, S.-C. Lin, R. Mahajan*, V. De**, K. Banerjee, University of California, Santa Barbara, CA, *Intel Corporation, Chandler, AZ, **Intel Corporation, Hillsboro, OR

2:00 p.m.
41.2 Chip-Level Performance Maximization Using ASIS (Application-specific Interconnect Structure) Wiring Design Concept for 45 nm CMOS Devices, N. Oda, H. Imura, N. Kawahara, M. Tagami*, H. Kunishima, S. Sone, S. Ohnishi, Y. Kakuhara, M. Sekine, Y. Hayashi*, K. Ueno, NEC Electronics Corporation, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

2:25 p.m.
41.3 New Constraint for Vth Optimization for Sub 32nm Node CMOS Gates Scaling, E. Morifuji, P. Kapur, A.K.-A. Chao, Y. Nishi, Stanford University, Stanford, CA

2:50 p.m.
41.4 SOI 90-nm Ring Oscillator Sub-ps Model-Hardware Correlation and Parasitic-aware Optimization Leading to 1.94-ps Switching Delay, J.-O. Plouchart, J. Kim, B. J. Gross, K. Wu, R. Trzcinski, V. Karam*, T. Sandwick, P. Hyde, R. Williams, M.-H. Na, J. Mc Cullen, M. Bhushan, M. Ketchen, W. Clark, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, *Carleton University, Ontario, Canada

3:15 p.m.
41.5 The Origin of Variable Retention Time in DRAM, Y. Mori, K. Ohyu*, K. Okonogi*, R.-I. Yamada, Hitachi Ltd., Tokyo, Japan, *Elpida Memory Inc., Kanagawa, Japan

3:40 p.m.
41.6 Program and SILC Constraints on NC Memories Scaling: a Monte Carlo Approach, R. Gusmeroli, A.S. Spinelli, C. Monzio Compagnoni, D. Ielmini, F. Morelli, A.L. Lacaita, Politecnico di Milano, Milano, Italy

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