WELCOME FROM THE GENERAL CHAIR

On behalf of the entire IEDM Committee, I would like to welcome you to the 2007 IEEE International Electron Devices Meeting to be held December 10-12, 2007 in Washington, DC. The IEDM continues to be the world's premier venue for presenting the latest breakthroughs and the broadest and best technical information in electronic device technologies. This year we have a strong collection of both contributed and invited papers that will be presented by industrial and academic leaders and students from around the world. Short summaries of each paper are available on the IEDM web site which we encourage everyone to visit – http://www.ieee.org/conference/iedm. The full digest will be available on the IEEE Xplore website and the DVD package offered by the IEEE Electron Devices Society after the conference.

H.S. Philip Wong
General Chair

Ralf Brederlow
Technical Program Chair

Vivek Subramanian
Technical Program Vice Chair

In addition to the many regular paper sessions - and the always informative and entertaining IEDM Luncheon on Tuesday - we will again feature several special sessions:

On Sunday December 9, 2007, two short courses are offered: "Performance Boosters for Advanced CMOS Devices" and "Emerging Nanotechnology and Nanoelectronics." These courses have been organized and will be presented by internationally-known leading researchers active in their respective areas of technology. The topics have broad appeal to IEDM participants with material suitable for newcomers as well as experts in the field.

The Plenary Session on Monday morning will feature three invited talks: "Automotive Electronics – Enabling the Future of Individual Mobility", presented by Dr. Claus Schmidt of Robert Bosch GmbH; "Roles of Quantum Nanostructures on the Evolution and Future Advances of Electronic and Photonic Devices" , given by Prof. Hiroyuki Sakaki of Toyota Technological Institute; and "Combining Digital Optical MEMS, CMOS, and Algorithms for Unique Display Solutions, by Dr. Larry Hornbeck of Texas Instruments.

The Luncheon on Tuesday features internationally well-known leaders in the field as guest speaker. This year, the Luncheon talk will be given by Dr. Morris Chang of Taiwan Semiconductor Manufacturing Company (TSMC). On Tuesday night, we will again feature our popular and interactive Panel session. This year we will explore the question "Looking Beyond Silicon - A Pipe Dream or The Inevitable Next Step?". The discussions will be led by a set of internationally-known panelists and moderators. This year, we initiate a new special session on Tuesday evening to offer a forum for discussion on a topic of current interest in a different format. The special session will run in parallel with the Panel session and feature four invited speakers. Each speaker will present talks that include a tutorial of the subject followed by analysis of current trend and research directions. Through this special session, we aim at providing the IEDM attendees a window into new and relevant subjects that may be outside of their immediate responsibility. This year the special session will focus on "Device/Circuit Interactions in Highly-Scaled CMOS: Challenges and Potential Solutions", a subject that is gaining importance.

The Emerging Technology special session this year features breakthroughs in the area of energy generation and conversion, and will include five talks from leading experts in this exciting new area looking from a broad variety of perspectives including materials, processing, structures, and circuits.

On behalf of the IEDM, Ralf Brederlow the Technical Program Chair, and Vivek Subramanian the Technical Program Vice-Chair, I want to express our sincere appreciation to all of the IEDM authors and to each of the members of the IEDM committee. The authors really make the IEDM what it is; a forum for the presentation of the leading work in our field. The IEDM committee members did an outstanding job in planning and organizing the 2007 conference.

The IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE member, please consider joining this great institution which has played such an important role globally for over 120 years. More detailed information regarding the IEEE is available at this conference and on their website – http://www.ieee.org

It is again my great honor and pleasure to extend a warm welcome to everyone attending the 2007 IEEE International Electron Devices Meeting.

H.-S. Philip Wong
General Chair

SHORT COURSE: Performance Boosters for Advanced CMOS Devices

Sunday, December 9, 9:00am-5:30pm
International Ballroom Center

Course Organizer: Scott Thompson, University of Florida

The semiconductor industry is obtaining impressive increases in transistor performance with several recent papers reporting n and p-channel saturation currents at ~1.5 and 1.0 mA/mm, respectively. New material and process innovations are replacing conventional geometric scaling as the primary driver with ~1GPa of channel stress and high k metal gates now in production at the 45 nm technology node. The success of each new process generation now requires choosing the right set of performance enhancers for the targeted market. This short course will provide insight and in-depth tradeoffs for key process elements positioned to comprise the 32nm and beyond CMOS technologies.

The first lecture provides insight into the strained Si currently in production and targeted for future technologies. Other mobility enhancement techniques such as hybrid (110) wafer orientation will also be discussed. The second and third lectures cover high k metal gates which is the biggest and most challenging change to the transistor structure in the last 20 years. The lectures will provide both a tutorial on the physics of high k / metal gates along with integration and manufacturing tradeoffs facing the implementation at 45 and 32nm. High k / metal gates allow scaling of the planar structure to ~20nm which is near the limit for this planar architecture. The fourth lecture presenting on alternative device architecture and non si channel materials covers key issues with forming low resistive shallow junctions in Si versus other materials. Finally the last presenter will cover device and circuit metrics which help close and relate the transistor level gains to products, present device variability status and describe options for improving variability and highlight device architecture implications of power limitations.

Introduction

Instructor: Scott Thompson, University of Florida

Mobility Enhancements

Instructor: Ken Rim, IBM

Introduction
- Transport in nanoscale channels
- Concept of effective source velocity

Process Induced Strain
- Process Induced Strain Options
- Integration Challenges for various strain techniques
- Design Rule scalability of various techniques

Crystal Oreintations
- Transport on different crystal orientations
- Uniaxial and Biaxial Strain Reponse vs Orientaion
- Multi-Orientation Integration: HOT on SOI and bulk CMOS

Transport Enhanced Materials
- SSDOI, GOI
- Ge/SiGe Hetero III-V CMOS
- Heterogenous substrate integration

High K / Metal Gates: Physics

Instructor: Gerald Lucovsky, North Carolina State University

HiK Dielectrics:
- Physics of high-k dielectrics
- HiK material options: Pro/cons of different materials from fundamental standpoint

Physics of defects in high k films

Poly/HiK interaction
- Poly interaction with HiK
- Impact on mobility and Vt pinning. Device response

Physics of metal work functions
- Fundamental understanding of MG work function: electronic structure and interfaces
- EOT scaling expectations for HiK+MG stacks
- Mobility of Metal Gate / HiK stacks: fundamental understanding

High K / Metal Gates: Integration and Manufactorability

Instructor: Reza Arghavani, Applied Materials

HiK Depsoition:
- HiK deposition techniques
- Pro/cons of various techniques
- Importance of HiK/Si interface layer
- Surface preperation prior to HiK depsoition

Metal Gate Module and Integration :
- Metal gate work-function requirements.
- Metal gate material options
- Metal gate deposition techniques

HiK/MG Process Flows:
- CMOS Integration options with pro-cons
- Short channel transistor performance

HiK/MG Reliability
- Reliability requirements
- HiK+MG Stack: Bias Temp and TDDB reliability status (N & P)
  - Options for improving HiK+MG stack reliability

Aletrnative MOS Structures and Channel Materials

Instructor: Krishna Saraswat, Stanford University

Multi-gate structures: FinFET, TriGate, Double Gate
MuIti-gate structures: Integration flows and challenges
MuIti-gate structures: Metal gate selection issues unique to MultiGate
Alternate channel materials
- Steeper than 60mV/dec sub-threshold slope devices

Junction and Salicide engineering:
- Impact of paraitic resistance on the state-of-art transistors
- Dopant super-activation
- New salicides with improved transmission
- Metal S/D

Device / Circuit Interactions

Instructor: Paul Packan, Intel

Introduction:
- NMOS and PMOS Scaling trends
- Circuit performance benchmark metrics
- Circuit performance/power implications

Impact of Variability
- Sources of device variability- systematic and random
- Impact on circuit performance at scaled Vcc
- Mitigating variability at the circuit level
- Device Architecture Impact
- Planar devices
- Multi-gate devices
- Memory circuits (RF, SRAM)
- Performance at significantly scaled Vcc for various architectures

Circuit Architectures Impact
- Impact of different circuit classes vs Vcc
- Designing for power

Design for Manufacturability
- Lithography
- Layout
- Design rules and methodologies

SHORT COURSE: Emerging Nanotechnology and Nanoelectronics

Sunday, December 9, 9:00 a.m. - 5:30 p.m.

Course Organizer: Robert Chau, Intel Corporation

The semiconductor industry has entered the nanotechnology regime since the introduction of the 0.13um technology node in 2000, which had transistor physical gate length of about 70nm and physical SiO_2 thickness of less than 2.0nm. Since then, various silicon nanotechnologies have been introduced to continue the scaling and performance trends of the CMOS transistors. For example, strained silicon technology has been implemented in the 90nm and 65nm technology nodes to improve transistor electron and hole mobility. High-K gate dielectrics and metal gate electrodes have been successfully implemented in the 45nm technology node to improve transistor performance and reduce gate leakage current. Non-planar multi-gate transistors (e.g. Double-gate FINFET and Tri-gate transistors) are being developed to mitigate short-channel and random dopant fluctuation effects for future technology nodes beyond the 45nm node. Furthermore, intensive research is currently being carried out by both industry and academia on electronic materials other than silicon and their integration onto silicon wafers for future high-performance and energy-efficient VLSI nanoelectronics applications. For example, III-V quantum-well transistors and their integration on silicon are being researched for future high-speed, ultra-low-power CMOS applications. Bottom-up chemically synthesized electronic materials such as semiconductor nanowires and carbon nanotubes and their placement and assembly are being researched for future digital and data storage applications. Besides future computation and memory devices, these emerging nanotechnologies are finding potential applications in other important areas such as health and the environment, energy conversion and storage, consumer electronics, communications, sensors, etc. Nanotechnology-based solutions are being developed for a wide range of energy problems such as: solar electricity, hydrogen generation and storage, batteries, super-capacitors, fuel

cells, thermoelectrics, and energy scavenging. Recently, a new class of vibrating RF Nano-Electro-Mechanical (NEMS) resonators has emerged as a potential solution for next generation wireless communications. This short course will cover the research progress of various nanotechnologies that are of great interest and importance to the semiconductor industry. It will start with a session on III-V research for CMOS extension, followed by sessions on emerging nanotechnologies for digital and data storage applications, biotechnology and health applications, as well as for other branches of nanoelectronics applications. The short course will also include an important session on critical instrumentation and metrology for nanotechnology.

Introduction

Robert Chau, Intel Corporation
CMOS Extension via III-V Compound Semiconductors

Instructor: Jesus del Alamo, Massachusetts Institute of Technology

Introduction
- The Si CMOS revolution
- How does Si CMOS end?

What matters for logic in a transistor?
III-V CMOS
- Why III-V's?
- A vision for III-V CMOS

The "Grand Challenges" for III-V CMOS
- Heterogeneous substrate integration

Scalable self-aligned enhancement-mode III-V FETs
High-K gate insulator
III-V p-type devices
III-V 3D device architectures
What can we learn from III-V High Electron Mobility Transistors?
- Logic suitability of InGaAs HEMT

InGaAs HEMT scaling
The potential of InAs
Benchmarking against Si MOSFET

Nanowires, Nanotubes and Nanoribbons for Digital Computation and Data Storage Application

Instructor: Charles Lieber, Harvard University
Chemically-synthesized nanoscale building blocks

Size Resolution
Transport Studies
Dopant and Composition
Applications for logic and memory
Device structures
Performance
Sensing applications
Array Integration
Assembly Issues
Array architectures
Key technology challenges:
- device reproducibility
- large-scale assembly
- integration flows

Metrology, Nanocharacterization and Instrumentation for Emerging Nanotechnology and Nanoelectronics :

Instructors: David Seiler and Michael Postek, NIST

Frontiers of extending measurements to the nanoscale
- Characterization and Metrology at the nanoscale
- Challenges in nanometrology
- Requirements for new metrology tools

Workhorse tools and their impact
- Grand challenges
- Metrology drivers
- Applications and feasibility of existing tools

Electrical and optical examples
- Scanning probe microscopy
- Nanoelectronic test structures
- Scanning Hall probe microscopy
- Defect characterization by noise and RTS measurements
- Reliability characterization
- Fourier transform infrared spectroscopy
- Internal photoemission spectroscopy
- Ultraviolet spectroscopic ellipsometry
- Young's modulus determination for MEMS/NEMS structures
- Nanometrology via nanopores
- Single molecule mass spectrometry
- Scatterometry

SEM and TEM metrology
- Structure and interface properties
- Metrology of hard-soft materials
- Applications and examples

Concurrent characterization of electronic, chemical, physical and magnetic properties

Key challenges

Emerging Nanotechnology for Health and Environment

Instructor: Luke Lee, Swiss Federal Institute of Technology Zürich and University of California at Berkeley

Introduction
- Nanobiophotonics
- Optofluidic ICs
- Biological Application Specific Integrated Circuits (BASICs)

Bio-applications
- Quantitative Biology & Medicine
- Molecular Diagnostics on a Chip
- Systems Biology

Bio-electronic systems Integration
- Soft-state Biological Electronics
- Biologic CMOS ICs

Biologically-inspired Photonics & Optofluidic Electronics Technology and Science (BioPOETS)
- Innovative 3D Optical Systems on CMOS
- Biologically-inspired Optical Systems for Health and Environment Monitoring
- Quantum Nanoplasmonics
- Biomimetic Vision Computer: Artificial Retinal Computation

Key challenges
- Unconventional Fabrication Methods and Materials
- Biological Interface on CMOS: Soft-state Biological Interfaces
- New Vision Computer for Health and Environment Monitoring

Emerging Nanotechnology for Nanoelectronic Applications

Instructors: Valluri Rao, Intel Corporation, Pascal Ancey, ST Microelectronics, Thomas Skotnicki, ST Microelectronics

Nanotechnology for MEMS:
Introduction
- MEMS as it relates to end applications
- MEMS technology basics, Nano-Mechanics
- Fabrication, CMOS compatibility and integration with CMOS Scaling

Nanotechnology for Energy Generation and Storage
Nanocrystalline, layered-composite material for electrode of micro-battery
Nanocrystals to increase the catalytic activity per unit area in fuel cells
CNT enabling 3-dimensional, reducing the systems' size & weight
Nanotechnology for RF Communication
Silicon based mechanical micro-nanosystems (NEMS) for RF applications
CNT vibrating RF NEMS & hybrid CMOS –CNT RF integrated circuit
Single-walled CNTs (SWNTs) as nano-electromechanical transducers

Plenary Session

Monday, December 10, 9:00 a.m.
International Ballroom Center

Welcome and Awards

General Chair: H.S. Philip Wong, Stanford University

Invited Papers

Technical Program Chair: Ralf Brederlow, Texas Instruments Deutschland GmbH

1.1 Automotive Electronics - Enabling the Future of Individual Mobility, Claus Schmidt, Robert Bosch GmbH

Automotive electronics changed dramatically during the past 50 years due to increasing requirements by legislation, safety for passengers, emission and last but not least convenience and entertainment.

Starting from a few simple and isolated functions in corresponding electronic devices, automotive electronics developed into a completely networked architecture of many microprocessors. This network apart from other functions takes care of the management of vehicle dynamics, assists drivers in order to avoid collisions and other accidents, decreases pollution of the environment and reduces fuel consumption of the vehicles.

In order to handle the increasing complexity of these networks, specific domain oriented architectures of the electronics are necessary (some examples will be shown). Additionally the components of the electronics have to withstand high temperatures and strong vibrations and still provide a nearly zero-defect quality over the lifetime of a car. Specific mechatronic solutions for the

electronic control units in vehicles (e.g. utilization of ceramics as substrates for the components) are used therefore.

At the end all of these requirements from functionality, environment etc. strongly influence the design and technology for the semiconductors used in automotive electronics. Zero-defect quality, long-term reliability and supply, resistance to electric overstress, increasing functionality at decreasing cost are just a few examples of automotive specific requirements on semiconductors.

Nevertheless automotive semiconductors showed a healthy increase of revenues during the past 10 years and will continue to keep this pace in the foreseeable future.

1.2 Roles of Quantum Nanostructures on the Evolution and Future Advances of Electronic and Photonic Devices, Hiroyuki Sakaki, Toyota Technological Institute

In almost every branch of electronics, nanometer (nm) scale layered structures are routinely used as the core parts of key devices, such as Si MOS field-efffect transistors (FETs), heterostructure FETs, heterobipolar transistors, lasers, and LEDs. It is because electric conductivities and optical gains of semiconductors can be controlled very efficiently in such nanostructures simply by modulating the concentration of electrons and/or holes therein.

Moreover, these layered nanostructures have enabled the birth and development of such quantum devices as resonant tunneling diodes (RTDs), quantum well infrared photodetectors (QWIPs) and quantum cascade lasers (QCLs) that exploit the discrete energy levels or associated subbands of quasi-two dimensional (2D) electrons in such films. Note that these devices have allowed us to generate and utilize electromagnetic waves from 10GHz to 100THz. We examine the current state of layered nanostructure devices to discuss problems to be tackled.

The scaling or the lateral size reduction of FETs over the last several decades has led to amazing advances in FET-based electronics. As a result, 10nm-scale patterning technology, once regarded to be quite esoteric, has become the key technique for LSI and microwave electronics. In the mid-70's, long before the feature size of FETs reached the sub-100nm range, we started theoretical studies to control the in-plane motion of electrons quantum mechanically by using 10nm-scale box and wire structures. We intended to create new properties and functions of lower-dimensional electrons and to bring forth such new devices as quantum wire (QWR) FETs, quantum dot (QD) lasers and planar superlattice FETs.

Sparked by these proposals, numerous other proposals have been made and various processing methods have been developed to fabricate QD- and QWR-based materials and devices and to demonstrate their features. We examine the present state and future prospects of such research activities in expanding the forefront of IT technology. Specifically, we discuss first recent advances in such transport devices, as QWR FETs, QD-based charge storage devices, and also QD-based single-electron transistors and disclose possible roles they may play in the next-generation electronics.

We then examine also recent advances in QD-based photonic devices, such as QD lasers and amplifiers, QD-based single-photon emitters, and QD-based interband and intraband photodetectors.

Finally, we discuss a couple of exploratory attempts to look for new applications of QD and QWR structures in such areas as bio-

medical imaging, gas sensing, and quantum information processings.

1.3 Combining Digital Optical MEMS, CMOS, and Algorithms for Unique Display Solutions, Larry J. Hornbeck, Texas Instruments

The worldwide high-definition, large screen TV and front projection display markets are growing rapidly, fueled by a diversity of new applications, the availability of high-definition content, the replacement of legacy CRT technology, and the expectations of the consumer regarding styling, price and functionality. Manufacturers are scrambling to meet the needs of this diverse market with an array of technologies that include flat panel displays and microdisplay systems based on MEMS (microelectromechanical systems branded as DLP technology), HTPS (high-temperature polysilicon) LCD, and LCOS (liquid-crystal on silicon). This paper focuses on the integration of large pixel arrays of digital optical MEMS with CMOS (complementary metal-oxidesemiconductor) circuitry, combined with digital algorithms to achieve diverse display solutions ranging from pocket projectors and high-definition televisions to large-venue projectors and 3-D digital cinema. Topics include pixel design, operation, drive waveform optimization and scaling strategies; benefits and tradeoffs of 1-chip vs. 3-chip optical architectures, and solid-state vs. lamp-based illumination; subjective image quality and the role of algorithms; factors affecting image stability and reliability; and monolithic integration and packaging challenges.

Session 2: Integrated Circuits and Manufacturing - DRAM and Fuse Technology

Monday, December 10, 1:30 p.m.
International Ballroom West

Co-Chairs: Yuichi Matsui, Hitachi
Takeshi Hamamoto, Toshiba

1:30 p.m.
Introduction

1:35 p.m.
2.1 Memory Technologies for Sub-40nm Node (Invited), K. Kim, G. Jeong, Samsung Electronics Co.

2:00 p.m.
2.2 A Novel Cell Arrangement Enabling Trench DRAM Scaling to 40nm and Beyond, L. Heineck, W. Graf, M. Popp, D. Savignac*, H.-P. Moll, R. Tews, D. Temmler, G. Kar, J. Schmid, M. Rouhanian, I. Uhlig, M. Goldbach. E. Landgraf, M. Drubba, S. Lukas, D. Weinmann, W. Roesner*, W. Mueller, Qimonda Dresden GmbH & Co. OHG, *Qimonda AG

2:25 p.m.
2.3 High Performance Silicon-On-ONO (SOONO) Cell Array Transistors (SCATs) for 512Mb DRAM Cell Array Application, S.H. Kim, H.J. Bae, S.I. Hong, Y.L. Choi, E.J. Yoon, H.J. Song, C.W. Oh, Y.-S. Lee, H. Cho, D.-W. Kim, D. Park, and W.-S. Lee, Samsung Electronics Co.

2:50 p.m.
2.4 FBC's Potential of $6F^2$ Single Cell Operation in Multi-Gbit Memories Confirmed by a Newly Developed Method for Measuring Signal Sense Margin, F. Matsuoka, T. Ohsawa, T. Higashi*, H. Furuhashi, K. Hatsuda, K. Fujita, R. Fukuda,

N. Ikumi, T. Shino, Y. Minami, H. Nakajima, T. Hamamoto, A. Nitayama, and Y. Watanabe, Toshiba Corp., *Toshiba Microelectronics Corp.

3:15 p.m.
2.5 **A Novel Via-fuse Technology Featuring Highly Stable Blow Operation With Large On-Off Ratio For 32nm-Node And Beyond**, H. Takaoka, T. Ueda, H. Tsuda, and A. Ono, NEC Electronics Corporation

Session 3: CMOS Devices - Metal Gate & High-K Gate Dielectrics

Monday, December 10, 1:30 p.m.
International Ballroom Center

Co-Chairs: Jong Shik Yoon, Samsung Electronics
Aaron Thean, Freescale Semiconductor

1:30 p.m.
Introduction

1:35 p.m.
3.1 **Low V_T CMOS Using Doped Hf-Based Oxides, TaC-based Metals and Laser-only Anneal**, S. Kubicek, T. Schram, V. Paraschiv, R. Vos, M. Demand, C. Adelmann, T. Witters, L. Nyns, L. Ragnarsson, H. Yu, A.Veloso, R. Singanamalla, T. Kauerauf, E. Rohr, S. Brus, C. Vrancken, V.S.Chang, R. Mitsuhashi, A. Akheyar, H.-J. Cho, J.C. Hooker, B.J. O'Sullivan, T. Chiarella, C. Kerner, A. Delabie, S. Van Elshocht, K.De Meyer, S. De Gendt, P.P. Absil, T. Hoffmann and S. Biesemans, IMEC

2:00 p.m.
3.2 **Materials Science-based Device Performance Engineering for Metal Gate High-k CMOS** (Invited), A. Toriumi, K. Kita, K. Tomida, Y. Zhao, J. Widiez, T. Nabatame*, H. Ota**, and M. Hirose**, The University of Tokyo, *MIRAI-ASET, **MIRAI-AIST

2:25 p.m.
3.3 **Flexible, Simplified CMOS on Si(110) with Metal Gate / High k for HP and LSTP**, H.R. Harris, S.E. Thompson*, S. Krishnan, P. Kirsch, P. Majhi, C.E. Smith, M.M. Hussain, G. Sung*, S.C. Song, R. Choi, H. Adhikari, S. Suthram*, B.H. Lee, H.-H. Tseng, R. Jammy, Sematech, *The University of Florida

2:50 p.m.
3.4 **Strained FDSOI CMOS Technology Scalability Down to 2.5nm Film Thickness and 18nm Gate Length with a TiN/HfO_2 Gate Stack**, V. Barral, T. Poiroux, F. Andrieu, C. Buj-Dufournet, O. Faynot, T. Ernst, L. Brevard, C. Fenouillet-Beranger, D. Lafond, J.M. Hartmann, V. Vidal, F. Allain, N. Daval*, I. Cayrefourcq*, L. Tosti, D. Munteanu**, J.L. Autran** and S. Deleonibus, CEA-LETI MINATEC, **L2MP, *SOITEC

3:15 p.m.
3.5 **Intrinsic Origin of Electron Mobility Reduction in High-k MOSFETs - From Remote Phonon to Bottom Interface Dipole Scattering -**, H. Ota, A. Hirano*, Y. Watanabe*, N. Yasuda*, K. Iwamoto*, K. Akiyama*, K. Okada*, S. Migita, T. Nabatame*, A. Toriumi, MIRAI-ASRC AIST, *MIRAI-ASET

3:40 p.m.
3.6 **Integration Technology of PC-FUSI (Phase Controlled FUSI) / HfSiON Gate Stack for Embedded Memory Application**, M. Saitoh, T. Ogura*, K. Masuzaki, K. Takahashi, H. Sunamura, K. Manabe, H. Shirai*, T. Tatsumi, H. Watanabe, NEC Corporation and *NEC Electronics Corporation

Session 4: Solid State and Nanoelectronic Devices - SONOS and Charge Trapping Memory Devices

Monday, December 10, 1:30 p.m.
International Ballroom East

Co-Chairs: Alessandro Spinelli, Politecnico di Milano
Giorgio Baccarani, University of Bologna

1:30 p.m.
Introduction

1:35 p.m.
4.1 **15 nm Planar Bulk SONOS-type Memory with Double Junction Tunnel Layers using Sub-threshold Slope Control**, R. Ohba, Y. Mitani, N. Sugiyama and S. Fujita, Toshiba Corporation

2:00 p.m.
4.2 **Trap Layer Engineered Gate-All-Around Vertically Stacked Twin Si-Nanowire Nonvolatile Memory**, J. Fu, K. D. Buddharaju, S. H. G. Teo, Chunxiang Zhu, M. B. Yu, N. Singh, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, Institute of Microelectronics

2:25 p.m.
4.3 **Novel ZrO_2/Si_3N_4 Dual Charge Storage Layer to Form Step-Up Potential Wells for Highly Reliable Multi-Level Cell Application**, G. Zhang, W.S. Hwang*, S.M. Bobade, S.-H. Lee, B.-J. Cho*, W.J. Yoo, Sungkyunkwan University, *National University of Singapore

2:50 p.m.
4.4 **A NAND-type Flash Memory Using Impact Ionization Generated Substrate Hot Electron Programming (>20MB/sec) and Hot Hole Erasing**, J.-Y. Wu, M.-C. Kuo, T.-H. Hsu, K.F. Chen , Y.J. Chen, E.-K. Lai, M.-H. Lee, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, Macronix International Co.

3:15 p.m.
4.5 **A New Self-Aligned Nitride MTP Cell with 45nm CMOS Fully Compatible Process**, C.-E. Huang, H.-M. Chen*, H.-C. Lai, Y.-J. Chen, Y.-C. King, C.J. Lin, National Tsing-Hua University, *eMemory Technology Inc.

3:40 p.m.
4.6 **45nm Gateless Anti-Fuse Cell with CMOS Fully Compatible Process**, Y-H. Tsai, H-M. Chen*, H-Y. Chiu, H-S. Shih, Y-C. King, and C-J. Lin, National Tsing-Hua University, *eMemory Technology Inc.

Session 5: Modeling and Simulation - Performance Analysis and Transport Modeling

Monday, December 10, 1:30 p.m.
Georgetown Ballroom

Co-Chairs: Phil Oldiges, IBM
Tom Linton, Intel

1:30 p.m.
Introduction

1:35 p.m.
5.1 **Novel Carrier-Mobility Modeling with Interface States for MOSFETs with Highly Scaled Gate Oxide Based on First-principles Calculations**, T. Ishihara, D. Matsushita, K. Tatsumura, Y. Nakabayashi, J. Koga, K. Kato, Toshiba Corporation

2:00 p.m.
5.2 **On The Experimental Determination Of Channel Back-Scattering In NanoMOSFETs**, M. Zilli, P. Palestri, D. Esseni, L. Selmi, University of Udine

2:25 p.m.
5.3 **Simulation of Electron Transport in High-Mobility MOSFETs: Density of States Bottleneck and 'Source Starvation'**, M.V. Fischetti, L. Wang*, B. Yu*, C. Sachs, P.M. Asbeck*, Y. Taur*, M. Rodwell*, University of Massachusetts, *University of California

2:50 p.m.
5.4 **Performance Analysis of III-V Materials in a Double-Gate Nano-MOSFET**, K.D. Cantley, Y. Liu, H.S. Pal, T. Low, S.S. Ahmed, and M.S. Lundstrom, Purdue University

3:15 p.m.
5.5 **On the Performance Limit of Impact-Ionization Transistors**, C. Shen, J.-Q. Lin, E.-H. Toh, K.-F. Chang*, P. Bai*, C.-H. Heng, G. S. Samudra and Y.-C. Yeo, National University of Singapore, *Institute of High Performance Computing

3:40 p.m.
5.6 **Quantum Transport Simulation of Tunnel Based Spin Torque Transfer (STT) Devices: Design Trade offs and Torque Efficiency**, S. Salahuddin, D. Datta, P. Srivastava and S. Datta, Purdue University

Session 6: Process Technology - Advanced Junctions, Silicides and Novel Stress Engineering

Monday, December 10, 1:30 p.m.
Jefferson Room

Co-Chairs: Masataka Kase, Fujitsu Limited
Anand Murthy, Intel Corporation

1:30 p.m.
Introduction

1:35 p.m.
6.1 **A New Liner Stressor with Very High Intrinsic Stress (> 6 GPa) and Low Permittivity Comprising Diamond-Like Carbon (DLC) for Strained P-Channel Transistors**, K.-M. Tan, M. Zhu, W.-W. Fang, M. Yang*, T.-Y. Liow, R.T.P. Lee, K.M. Hoe**, C.-H. Tung**, N. Balasubramanian**, G.S.

Samudra, and Y.-C. Yeo, National University of Singapore, *Data Storage Institute, **Institute of Microelectronics

2:00 p.m.
6.2 Silicon-Germanium-Tin (SiGeSn) Source and Drain Stressors formed by Sn Implant and Laser Annealing for Strained Silicon-Germanium Channel P-MOSFETs, G.H. Wang, E.-H. Toh, X. Wang[1], D.H.L.Seng[2], S. Tripathy[2], T. Osipowicz, T.K. Chan, K.M. Hoe[3], C.H. Tung[3], S. Balakumar[3], G.-Q. Lo[3], G. Samudra, and Y.-C. Yeo, National University of Singapore, [1]Singapore Institute of Manufacturing Technology, [2]Institute of Materials Research and Engineering, [3]Institute of Microelectronics

2:25 p.m.
6.3 Interfacial Segregation of Metal at NiSi/Si Junction for Novel Dual Silicide Technology, Y. Nishi, Y. Tsuchiya, A. Kinoshita, T. Yamauchi, J. Koga, Toshiba Corporation

2:50 p.m.
6.4 A Novel Low Leakage-Current Ni Silicide Process in nMOSFETs on Si(110) Substrate, T. Yamaguchi, K. Kashihara, S. Kudo, K. Hayashi, N. Hashikawa, T. Okudaira, T. Tsutsumi, K. Maekawa, H. Oda, K. Asai, and M. Kojima, Renesas Technology Corp.

3:15 p.m.
6.5 Junction Profile Engineering with a Novel Multiple Laser Spike Annealing Scheme for 45-nm Node High Performance and Low Leakage CMOS Technology, T. Yamamoto, T. Kubo*, T. Sukegawa*, E. Takii*, Y. Shimamune, N. Tamura, T. Sakoda, M. Nakamura, H. Ohta, T. Miyashita, H. Kurata, S. Satoh, M. Kase* and T. Sugii, Fujitsu Laboratories Ltd., *Fujitsu Ltd.

3:40 p.m.
6.6 Low Temperature Implementation of Dopant-Segregated Band-edge Metallic S/D Junctions in Thin-Body SOI p-MOSFETs, G. Larrieu, E. Dubois, R. Valentin, N. Breil, F. Danneville, G. Dambrine, J.C. Pesant, IEMN-UMR CNRS

4:05 p.m.
6.7 Pushing Planar Bulk CMOSFET Scaling to its Limit by Ultimately Shallow Diffusion-Less Junction, K. Uejima, K. Yako, N. Ikarashi, M. Narihiro, M. Tanaka, T. Nagumo, A. Mineji*, S. Shishiguchi* and M. Hane, NEC Corporation, *NEC Electronics Corporation

Session 7: CMOS and Interconnect Reliability - Reliability Issues in Non-Volatile Memories and ESD

Monday, December 10, 1:30 p.m.
Lincoln Room

Co-Chairs: Gilles Reimbold, CEA/LETI
Harald Gossner, Infineon Technologies AG

1:30 p.m.
Introduction

1:35 p.m.
7.1 Reliability Issues and Scaling Projections for Phase Change Non Volatile Memories, A.L. Lacaita and D. Ielmini, Politecnico di Milano

2:00 p.m.
7.2 **Study of Local Trapping and STI Edge Effects on Charge-Trapping NAND Flash**, H.-T. Lue, T.-H. Hsu, S.-Y. Wang, Y.-H. Hsiao, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.Y. Lu, Macronix International Co. Ltd.

2:25 p.m.
7.3 **First Evidence for Injection Statistics Accuracy Limitations in NAND Flash Constant-Current Fowler-Nordheim Programming**, C. Monzio Compagnoni, A.S. Spinelli, R. Gusmeroli, A.L. Lacaita, S. Beltrami*, A. Ghetti*, A. Visconti*, Politecnico di Milano, *STMicroelectronics

2:50 p.m.
7.4 **Random Telegraph Noise in Flash Memories - Model and Technology Scaling**, K. Fukuda, Y. Shimizu, M. Kamoshida, C. Hu*, Toshiba Corporation, *University of California

3:15 p.m.
7.5 **Characterization and Monte Carlo Analysis of Secondary Electrons Induced Program Disturb in a Buried Diffusion Bit-line SONOS Flash Memory**, C.J. Tang*, C.W. Li, T. Wang, S.H. Gu, P.C. Chen, Y.W. Chang, T.C. Lu, W.P. Lu, K.C. Chen, and C.-Y. Lu, Macronix International Co. Ltd., *National Chiao-Tung University

3:40 p.m.
7.6 **Modeling and Analysis of Self-Heating in FinFET Devices for Improved Circuit and EOS/ESD Performance**, S. Kolluri, K. Endo*, E. Suzuki* and K. Banerjee, University of California, *AIST

4:05 p.m.
7.7 **A Microscopic Understanding of DENMOS Device Failure Mechanism Under ESD Conditions**, A. Chatterjee, S. Pendharkar*, Y.-Y. Lin*, C. Duvvury*, K. Banerjee, University of California, *Texas Instruments

Session 8: Solid State and Nanoelectronic Devices - Non-Classical Devices and Interconnects

Monday, December 10, 1:30 p.m.
Military Room

Co-Chairs: Jing Guo, University of Florida
Chi On Chui, University of California, Los Angeles

1:30 p.m.
Introduction

1:35 p.m.
8.1 **A Perpendicular Spin Torque Switching Based MRAM for the 28 nm Technology Node**, U.K. Klostermann, M. Angerbauer, U. Grüning, F. Kreupl, M. Röhrig*, F. Dahmani**, M. Kund, G. Mueller, Qimonda AG, *Siemens AG, ** Altis Semiconductor

2:00 p.m.
8.2 **WITHDRAWN**

2:25 p.m.
8.3 **Bended Gate-All-Around Nanowire MOSFET: A Device With Enhanced Carrier Mobility Due To Oxidation-Induced Tensile Stress**, K.E. Moselund, P. Dobrosz*, S. Olsen*, A. O'Neill*, L. De Michelis, V. Pott, D. Tsamados and A.M. Ionescu, Ecole Polytechnique Federale de Lausanne, *Newcastle University

2:50 p.m.
8.4 **Impact Ionization Nanowire Transistor with Multiple-Gates, Silicon-Germanium Impact Ionization Region, and Sub-5 mV/decade Subtheshold Swing**, E.-H. Toh, G.H. Wang, M. Zhu, C. Shen, L. Chan, G.-Q. Lo*, C.-H. Tung*, D. Sylvester**, C.-H. Heng, G. Samudra, and Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics, **University of Michigan

3:15 p.m.
8.5 **Pionics: the Emerging Science and Technology of Graphene-based Nanoelectronics**, W.A. de Heer, C. Berger, E. Conrad, P. First, R. Murali, J. Meindl, Georgia Institute of Technology

3:40 p.m.
8.6 **Fabrication and Characterization of Carbon Nanotube Interconnects**, G.F. Close and H.-S.P. Wong, Stanford University

4:05 p.m.
8.7 **Carbon Nanotube Vias: A Reality Check**, H. Li, N. Srivastava, J.-F. Mao*, W.-Y. Yin* and K. Banerjee, University of California, *Shanhai Jiao Tong University

Session 9: Displays, Sensors, and MEMS - Flexible and Organic Electronics

Monday, December 10, 1:30 p.m.
Thoroughbred Room

Co-Chairs: Hagen Klauk, Max Planck Institute for Solid State Research
Takao Someya, University of Tokyo

1:30 p.m.
Introduction

1:35 p.m.
9.1 **Matching Application-Specific Frontplanes to Generic Backplanes**, S. Wagner, Princeton University

2:00 p.m.
9.2 **An Approach to Cost-Effective, Robust, Large-Area Electronics using Monolithic Silicon**, K. Huang, R. Dinyari, G. Lanzara, J.Y. Kim, J. Feng, C. Vancura*, F.-K. Chang, and P. Peumans, Stanford University, *Robert Bosch LLC

2:25 p.m.
9.3 **Communication Sheets Using Printed Organic Nonvolatile Memories**, T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, Y. Kato, M. Takamiya, T. Sakurai, T. Someya, The University of Tokyo

2:50 p.m.
9.4 **F-TES ADT Organic Integrated Circuits on Glass and Plastic Substrates**, S.K. Park, D.A. Mouery, I. Kim, S. Subramanian*, D. Zhao, J.E. Anthony*, and T.N. Jackson, Pennsylvania State University, *University of Kentucky

3:15 p.m.
9.5 **Label-free Low-Cost Disposable DNA Hybridization Detection Systems Using Organic TFTs**, Q. Zhang, V. Subramanian, University of California

3:40 p.m.
9.6 **A 16-Byte Nonvolatile Bistable Polymer Memory Array on Plastic Substrates**, H.-T. Lin, Z. Pei*, J.-R. Chen, C.-P. Kung, Y.-C. Lin, C.-M. Tseng, and Y.-J. Chan, Industrial Technology Research Insitute, *National Chung Hsing University Institute

4:05 p.m.
9.7 **Stackable Resistive Memory Device Using Photo Cross-linkable Copolymer**, W.L. Kwan, R.J. Tseng, W. Wu, Q. Pei, Y. Yang, University of California, Los Angeles

Session 10: Integrated Circuits and Manufacturing - Advanced CMOS Logic and SoC Platforms

Tuesday, December 11, 9:00 a.m.
International Ballroom Center

Co-Chairs: Jon Cheek, Freescale Semiconductor
John Pellerin, Advanced Micro Devices

9:00 a.m.
Introduction

9:05 a.m.
10.1 **A Highly Scaled, High Performance 45nm Bulk Logic CMOS Technology with 0.242 mm^2 SRAM Cell**, K.L. Cheng, Y.P. Wang, D.W. Lin, C.M. Chu, Y.Y. Tarng, M.H. Hsieh, S.P. Fu, J.H. Chen, C.T. Lin, W.Y. Lien, H.Y. Huang, P.W. Wang, H.H. Lin, D.Y. Lee, M.J. Huang, C.F. Nieh, L.T. Lin, C.C. Chen, W. Chang, Y.H. Chiu, M.Y. Wang, C.H. Yeh, F.C. Chen, C.M. Wu, Y.H. Chang, S.C. Wang, H.C. Hsieh, M.D. Lei, K. Goto, C.C. Wu, H.J. Tao, M. Cao, H.C. Tuan, C.H. Diaz, Y.J. Mii, TSMC

9:30 a.m.
10.2 **A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging**, K. Mistry, C. Allen, C, Auth, B. Beattie, D. Bergstrom, M. Bost, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hatttendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, B. McIntyre, P. Moon, J. Neirynck, C. Parker, D. Parsons, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Schifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki, Intel Corp.

9:55 a.m.
10.3 **High Performance and Low Power Bulk Logic Platform Utilizing FET Specific Multiple-Stressors with Highly Enhanced Strain and Full-Porous Low-k Interconnects for 45nm CMOS Technology**, T. Miyashita, K. Ikeda, Y. S. Kim, T. Yamamoto, Y. Sambonsugi, H. Ochimizu, T. Sakoda, M. Okuno, H. Ohta, H. Fukutome, H. Minakata, Y. Hayami, K. Ookoshi*, Y. Shimamune, M. Fukuda*, A. Hatada*, K. Okabe*, T. Kubo*, M. Tajima*, T. Yamamoto*, E. Mutoh*, T. Owada*, M. Nakamura, H. Kudo, T. Mori*, A. Hasegawa*, N. Tamura, H. Kurata, K. Sukegawa, A. Tsukune, K. Ikeda, M. Kase*, S. Satoh and T. Sugii, Fujitsu Laboratories, Ltd., *Fujitsu Limited

10:20 a.m.
10.4 Record RF Performance of 45-nm SOI CMOS Technology, S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer and G. Freeman, IBM Systems and Technology Group

10:45 a.m.
10.5 Technology Elements for Common Platform Enablement (Invited), P. Gilbert, A. Steegen, D. Coolbaugh and V. Ramachandran, IBM SRDC

11:10 a.m.
10.6 A 32nm CMOS Low Power SoC Platform Technology for Foundry Applications with Functional High Density SRAM, S.-Y. Wu, J.J. Liaw, J.Y. Cheng, C.Y. Lin, M.C. Chiang, C.K. Yang, C.W. Chou, K.H. Pan, C.H. Yao, M.Y. Liu, L.C. Hu, C.H. Chang, S.Y. Chang, P.Y. Tong, Y.L. Hsieh, K.C. Ku, K.C. Lin, L.Y. Yeh, C.W. Chang, H.J. Lin, V. Chang, K.S. Chen, C.C Chen, S.M. Cheng, S.H. Yang, Y.M. Sheu, M.T. Yang, H.C. Tseng, K.T. Huang, T.L. Lee, S.C. Chen, S.M. Jang, Y.C. See, M.S. Liang, TSMC

11:35 a.m.
10.7 Fully-Depleted SOI Technology using High-K and Single-Metal Gate for 32nm Node LSTP Applications Featuring 0.179μm2 6T-SRAM Bitcell, C. Fenouillet-Beranger^, S.Denorme, B. Icard^, F. Boeuf, J. Coignus, O. Faynot^, L. Brevard^, C. Buj^, C. Soonekindt*, J. Todeschini*, J.C. Le-Denmat, N. Loubet, C. Gallon, P. Perreau^, S. Manakli, B. Minghetti, L. Pain^, V.Arnal, A. Vandooren**, D. Aime*, L.Tosti^ C. Savardi, M. Broekaart*, P. Gouraud, F. Leverd, V. Dejonghe*, P. Brun^, M. Guillermet^, M. Aminpur**, S. Barnola^, F. Rouppert^, F. Martin^, T. Salvetat^, S. Lhostis, C. Laviron^, N. Auriac**, T. Kormann*, G. Chabanne**, S. Gaillard, O. Belmont, E. Laffosse**, D. Barge*, A. Zauner*, A. Tarnowka*, K. Romanjec*, H. Brut, A. Lagha**, S. Bonnetier**, F. Joly, N. Mayet**, A. Cathignol*, D. Galpin, D. Pop, R. Delsol*, R. Pantel, F. Pionnier, G. Thomas, D. Bensahel, S. Deleonibus^, T. Skotnicki, H. Mingam, STMicroelectronics, *NXP Semiconducotr, **Freescale Semiconductor, ^CEA-LETI MINATEC

Session 11: CMOS Devices - High Performance Devices

Tuesday, December 11, 9:00 a.m.
International Ballroom East

Co-Chairs: Sanjay Natarajan, Intel Corporation
An Steegen, IBM Corporation

9:00 a.m.
Introduction

9:05 a.m.
11.1 Novel Diffusion Topography Engineering (DTE) for High Performance CMOS Applications, C.H. Ko, C.H. Ge, C.C. Chen, W.Y. Teo, H.N. Lin, H.W. Chen, C.W. Kuo, M.T. Yang, D.Y. Chen, C.Y. Fu, and W.C. Lee, TSMC

9:30 a.m.
11.2 Study on High Performance (110) PFETs with Embedded SiGe, S. Okamoto, K. Miyashita, N. Yasutake, T. Okada, H. Itokawa, I. Mizushima, A. Azuma, H. Yoshimura and T. Nakayama, Toshiba Corporation

9:55 a.m.
11.3 **High-Performance 45nm node CMOS Transistors Featuring Flash Lamp Annealing (FLA)**, T. Sanuki, T. Iwamoto*, K. Ota**, T. Komoda, H. Yamazaki**, A. Eiho, K. Miyagi, K. Nakayama, O. Fuji, M. Togo*, K. Ohno**, H. Yoshimura, K. Yoshida, T. Ito, A. Mineji*, K. Yoshino, T. Itani, K. Matsuo, K. Nakazawa**, M. Nakazawa**, T. Shinyama**, K. Suguro, I. Mizushima, S. Iwasa, S. Muramatsu*, K. Nagaoka**, M. Ikeda*, M. Saito**, H. Naruse, Y. Enomoto**, T. Kitano*, M. Iwai, K. Imai*, N. Nagashima**, T. Kuwata*, F. Matsuoka, Toshiba Corporation, *NEC Electronics Corporation, **Sony Corporation

10:20 a.m.
11.4 **45nm High-k/Metal-Gate CMOS Technology for GPU/NPU Applications with Highest PFET Performance**, C.H. Lee, Y.T. Hou, R. Chen , Y.S. Chao , Y.C. Liu, C.L. Chen, W.H. Guo, W.C. Yang, T.H. Perng, J.J. Shen, Y. Yasuda, H.T. Huang, K. Goto, K.T. Huang, H. Chuang, C.H. Diaz, and M.S. Liang, TSMC

10:45 a.m.
11.5 **High Performance Sub-40 nm Bulk CMOS with Dopant Confinement Layer (DCL) Technique as a Strain Booster**, H.Ohta, N.Tamura, H.Fukutome, M.Tajima*, K. Okabe*, A.Hatada*, K.Ikeda, K.Ohkoshi*,T.Mori*, K. Sukegawa, S.Satoh and T.Sugii, Fujitsu Laboratories, *Fujitsu Limited

11:10 a.m.
11.6 **Extreme High-Performance n- and p-MOSFETs Boosted by Dual-Metal/High-k Gate Damascene Process using Top-Cut Dual Stress Liners on (100) Substrates**, S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S.Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura and N. Nagashima, Sony Corp.

Session 12: Solid State and Nanoelectronic Devices - Phase Change Memory and New Approaches for Nanoelectronics

Tuesday, December 11, 9:00 a.m.
Georgetown Ballroom

Co-Chairs: Norikatsu Takaura, Hitachi, Ltd.
Dirk Wouters, IMEC

9:00 a.m.
Introduction

9:05 a.m.
12.1 **Design Considerations for Complementary Nanoelectromechanical Logic Gates**, K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J Provine, P. Peumans, R. T. Howe, H.-S.P. Wong, Stanford University

9:30 a.m.
12.2 **Isotopically Engineered Silicon Nanoelectronics**, K.M. Itoh, Keio University

9:55 a.m.
12.3 **Doped In-Ge-Te Phase Change Memory Featuring Stable Operation and Good Data Retention**, T. Morikawa, K. Kurotsuchi, M. Kinoshita, N. Matsuzaki, Y. Matsui, Y.

Fujisaki, S. Hanzawa, A. Kotabe, M. Terao, N. Takaura, H. Moriya, T. Iwasaki, M. Matsuoka*, F. Nitta*, M. Moniwa*, T. Koga*, Hitachi Ltd., *Renesas Technology Corp.

10:20 a.m.
12.4 Statistical Analysis and Modeling of Programming and Retention in PCM Arrays, D. Mantegazza, D. Ielmini, E. Varesi*, A. Pirovano*, A.L. Lacaita, Politecnico di Milano, *STMicroelectronics

10:45 a.m.
12.5 Evidence of the Thermo-Electric Thomson Effect and Influence on the Program Conditions and Cell Optimization in Phase-Change Memory Cells, D. Tio Castro, L. Goux*, G.A.M Hurkx, K. Attenborough, R. Delhougne, J. Lisoni*, F.J. Jedema, M.A.A. in't Zandt, R.A.M. Wolters, D.J. Gravesteijn, D.J. Wouters*, NXP Semiconductors, *IMEC

11:10 a.m.
12.6 A Novel Cross-Spacer Phase Change Memory with Ultra-Small Lithography Independent Contact Area, W.S. Chen, C.M. Lee, D.S. Chao, Y.C. Chen, F. Chen, C.W. Chen, P.H. Yen, M.J. Chen, W.H. Wang, T.C. Hsiao, M.Y. Liu*, T.C, Wang*, L.L Chein**, C.M. Huang**, L.S. Tu***, D. Huang^, T.H Yu^, M.J. Kao, and M.-J. Tsai, ITRI, *Powerchip Semiconductor Corp., **Promos Technologies ***Nanya Technology Corp., ^Winbond Electronics Corp.

11:35 a.m.
12.7 The Role of Interfaces in Damascene Phase-Change Memory, D.L. Kencke, I.V. Karpov, B.G. Johnson, S.J. Lee, D.C. Kau, S.J. Hudgens*, J.P. Reifenberg**, S.D. Savransky, J. Zhang, M.D. Giles, G. Spadini, Intel Corp., *Ovonyx Inc., **Stanford University

Session 13: Process Technology - Gate Stack Process I – Fundamental Aspects

Tuesday, December 11, 9:00 a.m.
Jefferson Room

Co-Chairs: Albert Chin, National Chiao Tung University
Stefan De Gendt, IMEC

9:00 a.m.
Introduction

9:05 a.m.
13.1 Tuning PMOS Mo(O,N) Metal Gates to NMOS by Addition of DyO Capping Layer, J. Petry, R. Singanamalla*, K. Xiong, C. Ravit, E. Simoens*, R. O'Connor*, A. Veloso*, C. Adelmann*, S. Van Elshocht*, V. Paraschiv*, S. Brus*, J.Van Berkum**, S. Kubicek*, K. De Meyer*, S.Biesmans*, J.C. Hooker, NXP Semiconductors, *IMEC, KU Leuven, **Philips Research

9:30 a.m.
13.2 Very Low V_t [Ir-Hf]/HfLaO CMOS Using Novel Self-Aligned Low Temperature Shallow Junctions, C. F. Cheng, C. H. Wu*, N. C. Su*, S. J. Wang*, S. P. McAlister** and A. Chin, National Chiao-Tung University, *National Cheng Kung University, **National Research Council of Canada

9:55 a.m.
13.3 Mechanism of V_{fb} roll-off with High Work function Metal Gate and Low Temperature Oxygen Incorporation to Achieve PMOS Band Edge Work function, S. C. Song, C. S. Park, J. Price*, C. Burham*, R. Choi, H. H. Tseng, B. H. Lee, and R. Jammy, SEMATECH, *University of Texas

10:20 a.m.
13.4 Comprehensive Study of V_{FB} Shift in High-k CMOS - Dipole Formation, Fermi-level Pinning and Oxygen Vacancy Effect -, Y. Kamimuta, K. Iwamoto, Y. Nunoshige*, A. Hirano, W. Mizubayashi*, Y. Watanabe, S. Migita*, A. Ogawa, H. Ota*, T. Nabatame, and A. Toriumi*, MIRAI-ASET, *MIRAI-AIST

10:45 a.m.
13.5 Wide Controllability in Flatband Voltage by Tuning Crystalline Microstructures in Metal Gate Electrodes, K. Ohmori, T. Chikyow*, T. Hosoi**, H. Watanabe**, K. Nakajima*, T. Adachi*, A. Ishikawa*, Y. Sugita^, Y. Nara^, Y. Ohji^, K. Shiraishi***, K. Yamabe***, K. Yamada, Waseda University, *National Institute for Materials Science, **Osaka University, ^SELETE, ***University of Tsukuba

11:10 a.m.
13.6 Clarification of Additional Mobility Components Associated with TaC and TiN Metal Gates in Scaled HfSiON MOSFETs Down to Sub-1.0nm EOT, K. Tatsumura, M. Goto, S. Kawanaka, K. Nakajima, T. Schimizu, T. Ishihara, M. Koyama, Toshiba Corporation

11:35 a.m.
13.7 Impact of Flash Annealing on Performance and Reliability of High-k/Metal-Gate MOSFETs for Sub-45nm CMOS, P. Kalra, P. Majhi[1], D. Heh[2], G. Bersuker[2], C. Young[2], N. Vora[3], R. Harris[4], P. Kirsch[5], R. Choi[2], M. Chang[6], J. Lee[6], H. Hwang[6], H-H Tseng[2], R. Jammy[5], and T-J King Liu, University of California, [1]Intel, [2]SEMATECH, [3]University of Texas at Austin, [4]AMD, [5]IBM, [6]GIST at Korea

Session 14: Emerging Technologies - Energy Harvesting Electron Devices

Tuesday, December 11, 9:00 a.m.
Lincoln Room

Chair: Bruce White, Binghamton University

9:00 a.m.
Introduction

9:05 a.m.
14.1 Future Developments in Silicon Solar Cells, R. Swanson, SunPower Corp.

9:30 a.m.
14.2 Energy Harvesting - A Systems Perspective, J. Rabaey, P. Wright, Berkeley Wireless Research Center

9:55 a.m.
14.3 Energy Harvesting for Electronics with Thermoelectric Devices Using Nanoscale Materials, R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, C. Caylor, RTI International

10:20 a.m.
14.4 From Nanogenerators to Nano-Piezotronics, Z.L. Wang

10:45 a.m.
14.5 **Micro-engineered Devices for Motion Energy Harvesting**, E. Yeatman, P. Mitcheson, A. Holmes, Imperial College London

Session 15: Quantum, Power, and Compound Semiconductor Devices - Reliability and Characterizations of Power HEMTs

Tuesday, December 11, 9:00 a.m.
Military Room

Co-Chairs: Isik Kizilyalli, Nitronex Corporation
Kevin Chen, Hong Kong University of Science and Technology

9:00 a.m.
Introduction

9:05 a.m.
15.1 **A Review of Failure Modes and Mechanisms of GaN-based HEMT's**, E. Zanoni, G. Meneghesso, G. Verzellesi*, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, Università di Padova, *Università di Modena e Reggion Emilia

9:30 a.m.
15.2 **Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors**, J. Joh, L. Xia, and J.A. del Alamo, Massachusetts Institute of Technology

9:55 a.m.
15.3 **Reliability of Enhancement-mode AlGaN/GaN HEMTs Fabricated by Fluorine Plasma Treatment**, C. Yi, R. Wang, W. Huang, W. C.-W. Tang, K.M. Lau, K.J. Chen, Hong Kong University of Science and Technology

10:20 a.m.
15.4 **Drain Corrosion in RF Power GaAs PHEMTs**, A. Villanueva, J. del Alamo, T. Hisaka*, T. Ishida*, Massachusetts Institute of Technology, *Mitsubishi Electric Corporation

10:45 a.m.
15.5 **Remarkable Breakdown Voltage Enhancement in AlGaN Channel HEMTs**, T. Nanjo, M. Takeuchi*, M. Suita, Y. Abe, T. Oishi, Y. Tokuda and Y. Aoyagi**, Mitsubishi Electric Corporation, *RIKEN, **Tokyo Institute of Technology

11:10 a.m.
15.6 **Characterisation of AlGaN/GaN HEMT Epitaxy and Devices on Composite Substrates**, G. Meneghesso, C. Ongaro, E. Zanoni, C. Brylinski*, M. A. Poisson*, V. Hoel**, J.C. de Jaeger**, P. Bove^, J. Thorpe#, Università di Padova, *ALCATEL-THALES, **IEMN/TIGER, ^PICOGIGA International, #United Monolithic Semiconductors GmbH

11:35 a.m.
15.7 **High-voltage Millimeter-Wave GaN HEMTs with 13.7 W/mm Power Density**, Y.-F. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, and A. Burk*, Cree Santa Barbara Technology, *Cree Inc.

Session 16: Displays, Sensors, and MEMS - RF MEMs

Tuesday, December 11, 9:00 a.m.
Thoroughbred Room

Co-Chairs: Werner Weber, Infineon Technologies AG
Thomas A. Friedmann, Sandia National Laboratories

9:00 a.m.
Introduction

9:05 a.m.
16.1 Scalable 1.1 GHz Fundamental Mode Piezo-Resistive Silicon MEMS Resonator, J.T.M. van Beek, G.J.A.M. Verheijden, G.E.J. Koops, K.L. Phan, C. van der Avoort, J. van Wingerden, D. Ernur Badaroglu, J.J.M. Bontemps*, NXP Semiconductors Research, *Technical University Eindhoven

9:30 a.m.
16.2 Internal Dielectric Transduction of a 4.5 GHz Silicon Bar Resonator, D. Weinstein, S.A. Bhave, Cornell University

9:55 a.m.
16.3 Single-Resonator Dual-Frequency Thin-Film Piezoelectric-on-Substrate Oscillator, R. Abdolvand, H. Mirilavasani, F. Ayazi, Georgia Institute of Technology

10:20 a.m.
16.4 Integrated MEMS LC Resonator with Sealed Air-Suspended Structure for Single-Chip RF LSIs, K. Kuwabara, N. Sato, H. Morimura, J. Kodate, M. Nakamura, M. Ugajin, T. Kamei*, K. Kudou*, K. Machida*, and H. Ishii, NTT Corporation, *NTT Advanced Technology Corporation

10:45 a.m.
16.5 Variable Capacitors and Tunable LC-Tanks Formed by CMOS-Compatible Metal MEMS for RF ICs, L. Gu, X. Li, Chinese Academy of Sciences

11:10 a.m.
16.6 MEMS Variable Capacitor Actuated with an Electrically Floating Plate, Y.J. Yoon, H.S. Lee, J-B Yoon, KAIST

11:35 a.m.
16.7 High Reproducibility and Reliability of Piezoelectric MEMS Tunable Capacitors for Reconfigurable RF Front-end, T. Kawakubo*, T. Nagano, N. Nishigaki, K. Itaya, Toshiba Corporation, *Toshiba Research Consulting Corporation

12:00 p.m.
16.8 Maneuvering Pull-in Voltage of an Electrostatic Micro-switch by Introducing a Pre-charged Electrode, H.-H. Yang, J.O. Lee, and J.-B. Yoon, Korea Advanced Institute of Science and Technology

Luncheon Session

Tuesday, December 11, 12:20 p.m.
International Ballroom West

Luncheon Presentation: "A Life in Semiconductors"
Morris Chang, Taiwan Semiconductor Manufacturing Company

In his fifty-third year in the semiconductor industry, the speaker notes four major technical, and one major business model innovations that were of "disruptive" significance. The four technical innovations were: the transistor, the integrated circuit, the MOS technology, and the microprocessor. The business model innovation was the foundry model and its twin, the fabless model.

As a result of the developments that emanated from those disruptive innovations, the value in the semiconductor industry has shifted from almost solely technology to partly technology and partly system architecture and chip design. The overall value can be further enhanced by partner-like collaboration among the technologists, system architects and chip designers. The current trend of commoditization of foundry service is not conducive to the enhancement of the overall value of the semiconductor industry.

Morris Chang is the founding Chairman of Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) since 1987. TSMC pioneered the "dedicated silicon foundry" industry and was a powerful force in building the "fabless" industry in the world.

Prior to his career in Taiwan, Dr. Chang's career was in the United States. He was the President and Chief Operating Officer of General Instrument Corporation in 1984-1985, and prior to that, he was at Texas Instruments for 25 years (1958-1983), where he was Group Vice President responsible for worldwide semiconductor business for six years.

Dr. Chang received his B.S. and M.S. degrees in Mechanical Engineering from Massachusetts Institute of Technology in 1952 and 1953, and his Ph.D. in Electrical Engineering from Stanford in 1964. He received honorary doctorates from seven universities.

Dr. Chang was the recipient of the IEEE Robert N. Noyce Award for Exceptional Contributions to Microelectronics Industry, and the "Exemplary Leadership Award" of the Fabless Semiconductor Association (FSA). He was selected by Business Week as one of the "Top 25 Managers of the Year" and "Stars of Asia" in 1998; and by BancAmerica Robertson Stephens as "One of The Most Significant Contributors in the 50 years of Semiconductor Industry" in 1998.

Dr. Chang is a life member emeritus of MIT Corporation, and a member of National Academy of Engineering (USA). He is also on the advisory boards of NYSE, Stanford University, and University of California at Berkeley.

Awards Presentation

2007 IEEE Cledo Brunetti Award

2007 IEEE Andrew S. Grove Award

2007 IEEE David Sarnoff Award

2007 IEEE Leon K. Kirchmayer Graduate Teaching Award

Session 17: Integrated Circuits and Manufacturing - Nonvolatile Memories

Tuesday, December 11, 2:15 p.m.
International Ballroom Center

Co-Chairs: Kirk Prall, Micron Technology
Michael Specht, Qimonda

2:15 p.m.
Introduction

2:20 p.m.
17.1 A High-Performance Multi-Level NAND Flash Memory with 43nm-Node Floating-Gate Technology, M. Noguchi, T. Yaegashi, H. Koyama, M. Morikado, Y. Ishibashi, S. Ishibashi, K. Ino, K. Sawamura, T. Aoi, T. Maruyama, A. Kajita, E. Ito, M. Kishida, K. Kanda, K. Hosono, S. Miyamoto, F. Ito*, Y. Hirata*, G. Hemink*,M. Higashitani*, A. Mak*, J. Chan*, M. Koyanagi, S. Ohshima, H. Shibata, H. Tsunoda and S. Tanaka, Toshiba Corp. and *Sandisk Corp.

2:45 p.m.
17.2 Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory, Y. Fukuzumi, R. Katsumata, M. Kito, M. Kido, M. Sato, H. Tanaka, Y. Nagata*, Y. Matsuoka, Y. Iwata, H. Aochi and A. Nitayama, Toshiba Corporation and *Toshiba Information Systems (Japan) Corporation

3:10 p.m.
17.3 Thorough Investigation of Si-Nanocrystal Memories with High-K Interpoly Dielectrics for Sub-45nm Node Flash NAND Applications, G. Molas, M. Bocquet, J. Buckley, J. P. Colonna, L. Masarotto, H. Grampeix, F. Martin, V. Vidal, A. Toffoli, P. Brianceau, P. Scheiblin, M. Gely, A. M. Papon, G. Auvert, L. Perniola, C. Licitra, T. Veyron, N. Rochat, C. Bongiorno*, S. Lombardo*, B. De Salvo, S. Deleonbus, CEA-LETI

3:35 p.m.
17.4 Novel Ultra-Low Voltage and High-Speed Programming/ Erasing Schemes for SONOS Flash Memory with Excellent Data Retention, S.S. Chung, Y.H. Tseng*, C.S. Lai*, Y.Y. Hsu**, E. Ho**, T. Chen**, L.C. Peng**, and C.H. Chu**, National Chiao Tung University, *Guang Gang University, **ProMOS Technology, Inc.

4:00 p.m.
17.5 Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory, T. Nirschl*, J. B. Philipp**, T. D. Happ**, G. W. Burr^, B. Rajendran^, M.-H. Lee#, A. Schrott^, M. Yang^, M. Breitwisch^, C.-F. Chen#, E. Joseph^, M. Lamorey^, R. Cheek^, S.-H. Chen#, S. Zaidi**, S. Raoux^, Y.C. Chen#, Y. Zhu^, R. Bergmann**, H.-L. Lung#, C. Lam^, *Infineon Technologies, ** Qimonda, ^IBM, #Macronix International Co. Ltd.

Session 18: CMOS Devices - Device/Design Interaction

Tuesday, December 11, 2:15 p.m.
International Ballroom East

Co-Chairs: Manfred Horstmann, AMD Dresden
Reinhard Mahnkopf, Infineon Technologies Munich

2:15 p.m.
Introduction

2:20 p.m.
18.1 Understanding Random Threshold Voltage Fluctuation by Comparing Multiple Fabs and Technologies, K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra**, A. Nishida, S. Kamohara, T. Hiramoto, MIRAI-Selete, **University of Tokyo

2:45 p.m.
18.2 Reducing Variation in Advanced Logic Technologies Approaches to Process and Design Manufacturibility of Nanoscale CMOS:, K.J. Kuhn, Intel Corporation

3:10 p.m.
18.3 Controllable Inverter Delay and Suppressing V_{th} Fluctuation Technology in Silicon on Thin BOX Featuring Dual Back-Gate Bias Architecture, R. Tsuchiya, T. Ishigaki*, Y. Morita*, Y. Yamaoka*, T. Iwamatsu, T. Ipposhi, H. Oda, N. Sugii*, S. Kimura*, K. Ito*, Y. Inoue, Renesas Technology Corp., *Hitachi, Ltd.

3:35 p.m.
18.4 Measurements of Inter-and-Intra Device Transient Thermal Transport on SOI FETs, P.M. Solomon, M. Shamsa*, K.A. Jenkins, C. P. D'Emic, A.A. Balandin* and W. Haensch, IBM *English University

4:00 p.m.
18.5 An Effective Switching Current Methodology to Predict the Performance of Complex Digital Circuits, K. von Arnim, C. Pacha, K. Hofmann, T. Schulz, K. Schrufer, J. Berthold, Infineon Technologies

4:25 p.m.
18.6 Direct Evaluation of DC Characteristic Variability in FinFET SRAM Cell for 32 nm Node and Beyond, S. Inaba, H. Kawasaki, K. Okano, T. Izumida, A. Yagishita, A. Kaneko, K. Ishimaru, N. Aoki, Y. Toyoshima, Toshiba Corporation Semiconductor Company

Session 19: CMOS and Interconnect Reliability - Advanced Dielectric Reliability

Tuesday, December 11, 2:15 p.m.
Georgetown Ballroom

Co-Chairs: Kin Leong Pey, Nanyang Technological University
Takeshi Furusawa, Renesas Technology Corp.

2:15 p.m.
Introduction

2:20 p.m.
19.1 On the Progressive Breakdown Statistical Distribution and its Voltage Acceleration, E.Y. Wu, S. Tous* and J. Sune*, IBM Microelectronics Division, *Universitat Autonoma de Barcelona

2:45 p.m.
19.2 Multiple Digital Breakdown and Its Consequence on Ultrathin Gate Dielectrics Reliability Prediction, V.L. Lo, K.L. Pey, C.H. Tung* and X. Li, Nanyang Technological University, *Institute of Microelectronics

3:10 p.m.
19.3 TDDB Reliability Prediction Based on the Statistical Analysis of Hard Break-Down Including Multiple Soft Breakdown and Wear Out, S. Sahhaf, R. Degraeve, Ph.J. Roussel, T. Kauerauf, B.Kaczer, G.Groeseneken, IMEC

3:35 p.m.
19.4 Multiprobe Two-Dimensional Mapping of Off-State Degradation in DeNMOS Transistors: How and Why Interface Damage Predicts Gate Dielectric Breakdown, D. Varghese, H. Kufluoglu, V. Reddy*, H. Shichijo*, D. Mosher*, S. Krishnan*, and M. A. Alam, Purdue University, *Texas Instruments

4:00 p.m.
19.5 Designing Reliable Systems with Unreliable Devices: Challenges and Opportunities, L. Benini, DEIS Università di Bologna

4:25 p.m.
19.6 Copper Wiring Encapsulation with Ultra-thin Barriers to Enhance Wiring and Dielectric Reliabilities for 32-nm Nodes and Beyond, H. Kudo, M. Haneda, H. Ochimizu, A. Tsukune, S. Okano, N. Ohtsuka, M. Sunayama, H. Sakai*, T. Suzuki, H. Kitada, S. Amari*, T. Tabira, H. Matsuyama*, N. Shimizu*, T. Futatsugi, and T. Sugii, Fujitsu Laboratories Ltd., *Fujitsu Limited

Session 20: Process Technology - Gate Stack Process II – Metal Gate/High K Integration

Tuesday, December 11, 2:15 p.m.
Jefferson Room

Co-Chairs: Kazuhiro Eguchi, Toshiba
Luigi Colombo, Texas Instruments

2:15 p.m.
Introduction

2:20 p.m.
20.1 Feasible Integration Scheme for Dual Work Function FUSI/HfSiON Gate Stacks with Selective Metal Pile-up to nMOSFET, Y. Tsuchiya, M. Yoshiki, A. Kaneko, S. Inumiya, T. Saito, K. Nakajima, T. Aoyama, J. Koga, A. Nishiyama, M. Koyama, Toshiba Corp.

2:45 p.m.
20.2 Gate-First Processed FUSI/HfO_2/$HfSiO_x$/Si MOSFETs with EOT=0.5 nm Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing, M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita*, N. Yasuda, H. Ota*, T. Nabatame and A. Toriumi*, MIRAI-ASET, *MIRAI-ASRC

3:10 p.m.
20.3 Single Metal/Dual High-k Gate Stack with Low V_{th} and Precise Gate Profile Control for Highly Manufacturable Aggressively Scaled CMISFETs, N. Mise, T. Morooka, S. Kamiyama, K. Murayama*, M. Sato, T. Ono, T. Eimori, Y. Nara, and Y. Ohji, Semiconductor Leading Edge

Technologies Inc., *Assoc. of Super-Advanced Electronics Technologies

3:35 p.m.
20.4 Practical Dual-Metal-Gate Dual-High-k CMOS Integration Technology for *hp* 32 nm LSTP Utilizing Process-Friendly TiAlN Metal Gate, M. Kadoshima, T. Matsuki, M. Sato, T. Aminaka, E. Kurosawa, A. Ohta*, H. Yoshinaga*, S. Miyazaki*, K. Shiraishi**, Y. Yamabe**, K. Yamada^, T. Aoyama, Y. Nara, Y. Ohji, Semiconductor Leading Edge Technologies Inc., *Hiroshima University, **University of Tsukuba, ^Waseda University

4:00 p.m.
20.5 A Dy_2O_3-capped HfO_2 Dielectric and TaC_x-based Metals Enabling Low-V_t Single-Metal-Single-Dielectric Gate Stack, V.S. Chang, L.-Ã. Ragnarsson, G. Pourtois, R. O'Connor, C. Adelmann, S. Van Elshocht, A. Delabie, J. Swerts, N. Van der Heyden, T. Conard, H.-J. Cho, A. Akheyar, R. Mitsuhashi, T. Witters, B.J. O'Sullivan, L. Pantisano, E. Rohr, P. Lehnen, S. Kubicek , T. Schram, S. De Gendt, P. P. Absil, and S. Biesemans, IMEC

4:25 p.m.
20.6 Band Edge Gate First HfSiON/Metal Gate n-MOSFETs using ALD-La_2O_3 Cap Layers Scalable to EOT=0.68 nm for hp 32nm Bulk Devices with High Performance and Reliability, S. Kamiyama, T. Miura, E. Kurosawa, M. Kitajima, M. Ootuka, T. Aoyama, and Y. Nara, SELETE

4:50 p.m.
20.7 Aggressively Scaled High-k Gate Dielectric with Excellent Performance and High Temperature Stability for 32nm and Beyond, P. Sivasubramani, P. D. Kirsch*, J. Huang, C. Park, Y. N. Tan, D.C. Gilmer, C. Young, R. Harris**, S.C. Song, D. Heh, R. Choi, P. Majhi^, G. Bersuker, B.H. Lee*, H.-H. Tseng, J.S. Jur#, D.J. Lichtenwalner#, A.I. Kingon#, and R. Jammy*, SEMATECH, *IBM, **AMD, ^Intel, #North Carolina State University

Session 21: Modeling and Simulation - Development and Applications of Compact Models for Advanced Circuits

Tuesday, December 11, 2:15 p.m.
Lincoln Room

Co-Chairs: Dirk Klaassen, NXP Semiconductors
Srinivas Jallepalli, Freescale Semiconductor

2:15 p.m.
Introduction

2:20 p.m.
21.1 A Unified Compact Model of the Gate Oxide Reliability for Complete Circuit Level Analysis, C-H Lee, G-Y Yang, J-K Park, Y-K Park, B-S Yoo, H-W Kim, D. Park, M-H Yoo, Samsung Electronics Co., Ltd.

2:45 p.m.
21.2 A Predictive Analytical Model of 3D MIM Capacitors for RC IC, N. Segura, S. Cremer, D. Gloria, L. Ciampolini, E. Picollet and M. Minondo, STMicroelectronics

3:10 p.m.
21.3 **Physically-Based Unified Compact Model for Low-Field Carrier Mobility in MOSFETs with Different Gate Stacks and Biaxial/Uniaxial Stress Conditions**, S. Reggiani, L. Silvestri, A. Cacciatori*, E. Gnani, A. Gnudi, G. Baccarani, University of Bologna, *University of Brescia

3:35 p.m.
21.4 **A New Model for 1/f Noise in High-k MOSFETs**, T. Morshed, S.P. Devireddy, M.S. Rahman, Z. Celik-Butler , H.-H. Tseng*, A. Zlotnicka**, A. Shanware^, K. Green^, J.J. Chambers^, M.R. Visokay^, M.A. Quevedo-Lopez^ and L. Colombo^, University of Texas, *Sematech, **Freescale Semiconductor, ^Texas Instruments

4:00 p.m.
21.5 **A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation**, D.D. Lu, M.V. Dunga, C.-H. Lin, A.M. Niknejad and C. Hu, University of California

4:25 p.m.
21.6 **High Performance CMOS Variability in the 65nm Regime and Beyond**, S. Nassif, K. Bernstein, D. Frank, A. Gattiker, W. Haensch, B. Ji, E. Nowak, D. Pearson, N. Rohrer, IBM

4:50 p.m.
21.7 **Rapid Circuit-based Optimization of Low Operational Power CMOS Devices**, P. Christie, A. Nackaerts, *T. Hoffmann*, A. Kumar, NXP Semiconductors, *IMEC

Session 22: Displays, Sensors, and MEMS - TFTs, Displays and Memories

Tuesday, December 11, 2:15 p.m.
Military Room

Co-Chairs: Mutsuko Hatano, Hitachi, Ltd.
William Milne, Cambridge University

2:15 p.m.
Introduction

2:20 p.m.
22.1 **ZnO Thin Film Transistor Ring Oscillators with Sub 75 ns Propagation Delay**, J. Sun, D. Mourey, D. Zhao, S. Park, S. Nelson*, D. Levy*, D. Freeman*, P. Cowdery-Corvan*, L. Tutt*, T. Jackson, Penn State University, *Eastman Kodak

2:45 p.m.
22.2 **New Approach for Passivation of Ga_2O_3-In_2O_3-ZnO Thin Film Transistors**, S.I. Kim, C.J. Kim, J.C. Park, I.Song, H. Lim, S.W. Kim, E. Lee, J.C. Lee and Y. Park, Samsung Advanced Institute of Technology

3:10 p.m.
22.3 **High Performance Transparent Thin Film Transistors Based on Indium Gallium Zinc Oxide as the Channel Material**, A. Suresh, P. Wellenius and J. Muth, North Carolina State University

3:35 p.m.
22.4 **Sub-Micron CMOS / MOS-Bipolar Hybrid TFTs for System Displays**, G. Kawachi, T. Okada, S. Tsuboi, M. Mitani, Advanced LCD Technologies Development Center Co., Ltd.

4:00 p.m.
22.5 **New In Situ Process of Top Gate Nanocrystalline Silicon Thin Film Transistors Fabricated at 180°C For The Suppression Of Leakage Current**, J-H Park, S-M Han, Y-H Choi and M-K Han, Seoul National University

4:25 p.m.
22.6 **Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually Controlled by Si Pillar Ungated FETs**, L. Velasquez-Garcia, B. Adeoti, Y. Niu, and A.I. Akinwande, MIT Microsystems Technology Laboratories

4:50 p.m.
22.7 **Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration**, W.Y. Choi, H. Kam, D. Lee, J. Lai and T-J King Liu, University of California

Session 23: Quantum, Power, and Compound Semiconductor Devices - III-V FETs for Microwave, Millimiter Wave and Digital Applications

Tuesday, December 11, 2:15 p.m.
Thoroughbred Room

Co-Chairs: Miroslav Micovic, HRL Laboratories, LLC
Patrick Fay, University of Notre Dame

2:15 p.m.
Introduction

2:20 p.m.
23.1 **Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz,** R. Lai, X.B. Mei, W.R. Deal, W. Yoshida, Y.M. Kim, P.H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier*, L. Samoska*, A. Fung*, Northrop Grumman Space Technology and *Jet Propulsion Laboratory

2:45 p.m.
23.2 **610GHz $In_{0.52}AlAs/In_{0.75}GaAs$ Metamorphic HEMTs with an Ultra-Short 15-nm-Gate**, S-J Yeon, M. Park and K. Seo, Seoul National University

3:10 p.m.
23.3 **0.1 mm $In_{0.2}Al_{0.8}Sb$-InAs HEMT Low Noise Amplifiers for Ultralow-Power Applications**, Y.C. Chou, M.D. Lange, J.B Boos*, B.R. Bennett*, J.M. Yang, C.H. Lin, J. Lee, P.S. Nam, A.L. Gutierrez, R.S. Tsai, M.E. Barsky, T.P. Chin, M. Wojtowicz, and A.K. Oki, Northrop Grumman Space Technology and *Naval Research Laboratory

3:35 p.m.
23.4 **High Mobility III-V MOSFETs for RF and Digital Applications**, M. Passlack, P. Zurcher, K. Rajaopalan, R. Droopad, J. Abrokwah, M. Tutt, J-B Park, E. Johnson, O. Hartin, A. Zlotnicka, P. Fejes, R. Hill*, D. Moran*, X. Li*, H. Zhou*, D. Macintyre*, S. Thoms*, A. Asenov*, K. Kalna* and I. Thayne*, Freescale Semiconductor, * University of Glasgow

4:00 p.m.
23.5 **Heterogeneous Integration of Enhancement Mode $In_{0.7}Ga_{0.3}As$ Quantum Well Transistor on Silicon Substrate using Thin (<2 um) Composite Buffer Architecture for High-Speed and Low-voltage (0.5V) Logic Applications**, M. K. Hudait, S. Datta, G. Dewey, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, M. Radosavljevic and R. Chau, Intel Corp.

4:25 p.m.
23.6 Logic Performance of 40 nm InAs HEMTs, D-H Kim and J. del Alamo, Massachusetts Institute of Technology

4:50 p.m.
23.7 90 nm Self-Aligned InGaAs HEMT for Logic Applications, N. Waldron, D-H Kim and J. A. del Alamo, Massachusetts Institute of Technology

5:15 p.m.
23.8 High Performance Submicron Inversion-Type Enhancement-Mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as Gate Dielectrics, Y. Xuan, Y.Q. Wu, T. Shen, T. Yang and P.D. Ye, Purdue University

Session 24 – 2007 IEDM Special Evening Session

Tuesday, December 11, 8:00 p.m.
International Ballroom Center

Session Chair: Ralf Brederlow, Texas Instruments
Device/Circuit Interactions in Highly-Scaled CMOS: Challenges and Potential Solutions

Pushing the limits of advanced CMOS technology has become increasingly challenging. The electrical behavior of advanced CMOS devices deviates strongly from ideal MOSFET behavior. As applications manufactured in those technologies demand for higher performance circuits and systems, co-optimization of technology, circuits and systems is becoming an industry trend. Specific tailoring of device parameters depending on the class of applications is widely seen. This is expected to continue or even to intensify in future technology nodes. Whereas this trend requires more technology specific knowledge for circuit designers, an understanding of basic circuit operation becomes more and more important for process platform development.

IEDM is addressing this trend in a special evening session. The invited talks in this session will address both the challenges and also the opportunities and potential solutions for circuit specific and application driven optimization of advanced CMOS technology. Circuit design problems and challenges with advanced CMOS technology, circuit/device co-optimization for different circuit and application needs, and multi-million gate circuit design challenges in advanced CMOS technology will be discussed by experts in their respective fields. A panel-like discussion with the audience is planned for the last part of the session.

8:00 – 8:05pm
Introduction

8:05 – 8:30pm
Technology/Circuit Co-Design for High Performance Logic
Kerry Bernstein, Norman Rohrer, IBM

8:30 – 8:55pm
Device/Circuit Variability Mechanisms and Mitigation in Highly-Scaled CMOS,, Andrew B. Kahng, UC San Diego

8:55 – 9:20pm
Leakage Reduction in Sub-100nm CMOS Technologies: Bridging the Gap Between Technology, Circuit Design and Low Power Product Requirements, Christian Pacha, Joerg Berthold, Infineon Technologies

9:20 – 9:45pm
Adaptive Design of SRAM Memory Cells, Koichiro Ishibashi, Renesas

9:45 – 10:00pm
Panel Discussion

Session 25 – 2007 IEDM Evening Panel Discussion

Tuesday, December 11, 2007
International Ballroom East

Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?

While the cadence of CMOS generations has continued nearly unabated, technology development has become an increasingly difficult and expensive proposition. Some well-established semiconductor companies are choosing to exit the technology race or at least to spread the risk of CMOS scaling by means of partnerships. Logic technology development is facing all kinds of trouble impeding the double-boon of Si FET scalability with commensurate performance improvement that has served the industry so well in the past. To mention a few, metal/high-k gate stack with suitable EOT is late, silicon strain engineering seems to be peaking at the 45 nm generation, non-planar channel FETs are still many years away.

With the end of Si FET scaling appearing increasingly near, searching for "beyond-Si" solutions has become imperative; from relatively "easy" transitions to high mobility semiconductors, like Ge and III-V's, to even higher mobility new materials such as carbon nanotubes, graphene, or other molecular structures. And even further, there are searches for new information representation and processing concepts beyond charge in FETs, as for example, spin-state devices. Of course, declaring silicon dead is premature at best, so the timing of such transitions will be dictated by the limits of our collective ingenuity in stretching the legs of the old warhorse.

This panel will address those limits and will assess the prospects of the various materials, structures and concepts that are being pursued as "beyond-Si" solutions. While in the end economic issues will play a crucial role in how technology will develop in the future the discussion will concentrate primarily on the technical aspects of the problems and solutions as the industry moves further away from the "scaling as we know it" era.

Moderator: Dimitri Antoniadis, Massachusetts Institute of Technology

Panel Members:

Wilfried Haensch, IBM
Suman Datta, Penn State University
Doggun Park, Samsung
Akira Toriumi, University of Tokyo
Yuh-Jier Mii, TSMC
Jean-Phippe Bourgoin, CEA LETI

Session 26: Quantum, Power, and Compound Semiconductor Devices - Ultra High Speed SiGe and InP-Based HBTs

Wednesday, December 12, 9:00 a.m.
International Ballroom West

Co-Chairs: Giovanni Ghione, Politecnico di Torino
Minoru Ida, NTT Photonics Laboratories

9:00 a.m.
Introduction

9:05 a.m.
26.1 130 nm SiGe BiCMOS Technology with 3.0 ps Gate Delay, H. Ruecker, B. Heinemann, R. Barth, J. Bauer, K. Blum, D. Bolze, J. Drews, A. Fox, O. Fursenko, T. Grabolla, U. Haak, W. Hoeppner, D. Knoll, K. Koepke, B. Kuck, A. Mai, S. Marschmeyer, T. Morgenstern, H. H. Richter, P. Schley, D. Schmidt, K. Schulz, B. Tillack, G. Weidner, W. Winkler D. Wolansky, H-E Wulf Y. Yamamoto, IHP

9:30 a.m.
26.2 A Novel Fully Self-Aligned SiGe:C HBT Architecture Featuring a Single Step Epitaxial Collector-Base Process, J.J.T.M. Donkers, M.C.J.C.M. Kramer, S. Van Huylenbroeck*, L.J. Choi*, P. Meunier-Beillard, G. Boccardi, W. van Noort, G.A.M. Hurkx, T. Vanhoucke, A. Sibaja-Hernandez*, F. Vleugels*, G. Winderickx*, E. Kunnen*, S. Peeters*, D. Baute*, B. De Vos*, T. Vandeweyer*, R. Loo*, R. Venegas*, R. Pijper, S. Decoutere*, E.A. Hijzen, NXP Semiconductors, *IMEC

9:55 a.m.
26.3 Electrically Pumped Ge Laser at Room Temperature, T-H. Cheng, C. T. Lee, M. H. Liao, P-S. Kuo, T. A. Hung, and C. W. Liu, National Taiwan University

10:20 a.m.
26.4 Type-II GaAsSb/InP DHBTs With Record f_T = 670 GHz and Simultaneous f_T, f_{MAX} > 400 GHz, W. Snodgrass, B-R Wu, K.Y. Cheng, and M. Feng, University of Illinois at Urbana-Champaign

10:45 a.m.
26.5 600 GHz InP/GaAsSb/InP DHBTs Grown by MOCVD with a Ga(As,Sb) Graded-Base and f_T X BV_{CEO} > 2.5 THz-V at Room Temperature, H.G. Liu, O. Ostinelli, Y. Zeng, C.R. Bolognesi, Swiss Federal Institute of Technology

11:10 a.m.
26.6 High-Speed InP HBT Technology for Advanced Mixed-Signal and Digital Applications, C. Monier, D. Scott, M. DAmore, B. Chan, L. Dang, A. Cavus, E. Kaneshiro, P. Nam, K. Sato, N. Cohen, S. Lin, K. Luo, J. Wang, B. Oyama, and A. G. Gutierrez, Northrop-Grumman Space Technology

Session 27: Process Technology - Advanced Process & Integration Technology

Wednesday, December 12, 9:00 a.m.
International Ballroom Center

Co-Chairs: Barbara De Salvo, CEA/LETI
Tze-Liang Lee, TSMC

9:00 a.m.
Introduction

9:05 a.m.
27.1 Embedded Flash on 90nm Logic Technology and Beyond for FPGAs, H. Kojima, T. Ema, T. Anezaki, J. Ariyoshi, H. Ogawa, K. Yoshizawa, S. Mehta*, S. Fong*, S. Logie*, R. Smoak*, D. Rutledge*, Fujitsu Ltd. And *Lattice Semiconductor Corp.

9:30 a.m.
27.2 Gatestacks for Scalable High-Performance FinFETs, G. Vellianitis, M.J.H. van Dal, L. Witters*, G. Curatola, G. Doornbos, N. Collaert*, C. Jonville, C. Torregiani*, L. S. Lai*, J. Petry, B.J. Pawlak, R. Duffy, M. Demand*, S. Beckx*, S. Mertens*, A. Delabie*, T. Vandeweyer*, C. Delvaux*, F. Leys*, A. Hikavy*, R. Rooyackers*, M. Kaiser, ** R.J.R. Weemaes**, F. Voogt, H. Roberts, D. Donnet, S. Biesemaris*, M Jurczaki*, R.J.P. Lander, NXP Semiconductors, *IMEC, **Philips

9:55 a.m.
27.3 Route to Low Parasitic Resistance in MuGFETs with Silicon-Carbon Source/Drain: Integration of Novel Low Barrier Ni(M)Si:C Metal Silicides and Pulsed Laser Annealing, R.T-P Lee, A.T-Y Koh, F-Y Liu, W-W Fang, T-Y. Liow. K-M. Tan, P-C. Lim*, A.E-J. Lim, M.Zhu, H-S. Wong, K-M. Hoe**, C-H. Tung**, G-Q. Lo**, X. Wang***, D.K-Y. Low***, G.S. Samudra, D-Z. Chi** and Y-C. Yeo, National University of Singapore, *Institute of Materials Research and Engineering, **Institute of Micro Electronics, ***Singapore Institute of Manufacturing Technology

10:20 a.m.
27.4 Si/SiGe Epitaxy: a Ubiquitous Process for Advanced Electronics, D. Dutartre, N. Loubet, F. Brossard, B. Vandelle, P. Chevalier, C. Fenouillet*, A. Pouydebasque**, STMicroelectronics, *CEA, **NXP

10:45 a.m.
27.5 Localized SOI Technology: An Innovative Low Cost Self-Aligned Process for Ultra Thin Si-Film on Thin BOX Integration for Low Power Applications, S. Monfray, MP. Samson, D. Dutartre, T. Ernst*, E. Rouchouze, D. Renaud*, B. Guillaumot, D. Chanemougame, G. Rabille, S. Borel*, JP. Colonna*, C. Arvet, N. Loubet, Y. Campidelli, JM. Hartmann*, L. Vandroux*, D. Bensahel, A. Toffoli*, F. Allain*, A. Margin, L. Clement**, A. Quiroga, S. Deleonibus*, T. Skotnicki, STMicroelectonics, *CEA/LETIMINATEC, ** NXP Semiconductor

11:10 a.m.
27.6 Proof of Ge-Interfacing Concepts for Metal/High-k/Ge CMOS -Ge-Intimate Material Selection and Interface Conscious Process Flow-, T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita and A. Toriumi, The University of Tokyo

Session 28: CMOS Devices - Physics and Technologies of Mobility Enhancement

Wednesday, December 12, 9:00 a.m.
International Ballroom East

Co-Chairs: Shinichi Takagi, University of Tokyo
Raphael Clerc, IMEP

9:00 a.m.
Introduction

9:05 a.m.
28.1 Extension of Universal Mobility Curve to Multi-Gate MOSFETs, H. Yoshimoto, N. Sugii, D. Hisamoto, S-I Saito, R. Tsuchiya and S. Kimura, Hitachi, Ltd.

9:30 a.m.
28.2 More-than-Universal Mobility in Double-Gate SOI p-FETs with Sub-10-nm Body Thickness -Role of Light-Hole Band and Compatibility with Uniaxial Stress Engineering-, Kobayashi, M. Saitoh, K. Uchida, Toshiba Corp.

9:55 a.m.
28.3 Physical Understanding of Fundamental Properties of Si (110) pMOSFETs - Inversion-Layer Capacitance, Mobility Universality, and Uniaxial Strain Effects -, M. Saitoh, S. Kobayashi, K. Uchida, Toshiba Corp.

10:20 a.m.
28.4 Mobility Enhancement in Uniaxially Strained (110) Oriented Ultra-Thin Body Single- and Double-Gate MOSFETs with SOI Thickness of less than 4 nm, K. Shimizu and T. Hiramoto, University of Tokyo

10:45 a.m.
28.5 Examination of Additive Mobility Enhancements for Uniaxial Stress Combined with Biaxially Strained Si, Biaxially Strained SiGe and Ge Channel MOSFETs, O. Weber, T. Irisawa*, T. Numata*, M. Harada*, N. Taoka**, Y. Yamashita*, T. Yamamoto*, N. Sugiyama*, M. Takenaka and S. Takagi, The University of Tokyo, *MIRAIASET, **MIRAI-AIST

11:10 a.m.
28.6 Interface-Engineered Ge (100) and (111), N- and P-FETs with High Mobility, D. Kuzum, A.J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, Stanford University

11:35 a.m.
28.7 Demonstration of High Performance PMOSFETs Using Si/Si_xGe_{1-x}/Si Quantum Wells with High-k/Metal Gate Stacks and Uniaxial Strain Additivity for 22 nm Technology and Beyond, S. Suthram, P. Majhi, G. Sun, P. Kalra*, R. Harris, K. J. Choi**, D. Heh, J. Oh, D. Kelly, R. Choi, B.J. Cho**, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, ***S.E. Thompson, H. H. Tseng, R. Jammy, SEMATECH, *University of California, **National University, ***University of Florida

Session 29: Modeling and Simulation - Nanotubes, Nanowires and Nanoribbons

Wednesday, December 12, 9:00 a.m.
Georgetown Ballroom

Co-Chairs: Giuseppe Iannaccone, University of Pisa
Nobuyuki Sano, University of Tsukuba

9:00 a.m.
Introduction

9:05 a.m.
29.1 Three-dimensional Modeling of Gate Leakage in Si Nanowire Transistors, M. Luisier, A. Schenk, W. Fichtner, ETHZ

9:30 a.m.
29.2 Band Structure Effects on the Current-Voltage Characteristics of SNW-FETs, E. Gnani, A. Gnudi, S. Reggiani, M. Rudan, G. Baccarani, University of Bologna

9:55 a.m.
29.3 1-D and 2-D Devices Performance Comparison including Parasitic Gate Capacitance and Screening Effect, L. Wei, J. Deng, H.-S. Philip Wong, Stanford University

10:20 a.m.
29.4 Exciton Generation in Suspended Carbon Nanotube FETs: A Computational Study, S.O. Koswatta, V. Perebeinos*, M.S. Lundstrom, Ph. Avouris*, Purdue University, *IBM Research Division

10:45 a.m.
29.5 A Comprehensive Atomic Study of Carbon Nanotube Schottky Diode Using First Principles Approach, P. Bai, K.T. Lam, E. Li, and K.K-F. Chang, Institute of High Performance Computing

11:10 a.m.
29.6 Analytical Model of Carbon Nanotube Electrostatics: Density of States, Effective Mass, Carrier Density, and Quantum Capacitance, D. Akinwande, Y. Lu, Hongjie Dai, Y. Nishi, H.-S. Philip Wong, Stanford University

11:35 a.m.
29.7 Performance Comparison of Graphene Nanoribbon Schottky Barrier and MOSFETs, G. Fiori, Y. Yoon*, S. Hong*, G. Iannaccone, J. Guo*, University de Pisa, *University of Florida

12:00 p.m.
29.8 Simulation Investigation of Double-Gate CNR-MOSFETs with a Fully Self-Consistent NEGF and TB Method, X. Guan, M. Zhang, Q. Liu, and Z. Yu, Tsinghua University

Session 30: Solid State and Nanoelectronic Devices - Emerging Resistive RAM and New Function on Silicon

Wednesday, December 12, 9:00 a.m.
Jefferson Room

Co-Chairs: Sunae Seo, Samsung
Jacques Gautier, CEA-LETI

9:00 a.m.
Introduction

9:05 a.m.
30.1 Low Power and High Speed Switching of Ti-doped NiO ReRAM Under the Unipolar Voltage Source of Less than 3V, K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, Fujitsu Laboratories

9:30 a.m.
30.2 2-Stack 1D-1R Cross-point Structure with Oxide Diodes as Switch Elements for High Density Resistance RAM Applications, M.J. Lee, Y. Park, B.S. Kang, S.E. Ahn, C.B. Lee, K.H. Kim, W. Xianyu, G. Stefanovich, J.H. Lee, S.J. Chung, Y.H. Kim, C.S. Lee, J.B. Park, I.G. Baek* and I.K. Yoo, Samsung Advanced Institute of Technology, *Samsung Electronics, Co., Ltd.

9:55 a.m.
30.3 Conductive-Filament Switching Analysis and Self-Accelerated Thermal Dissolution Model for Reset in NiO-based RRAM, U. Russo, D. Ielmini, C. Cagli, A. Lacaita, S. Spiga*, C. Wiemer*, M. Perego*, M. Fanciulli*, Politecnico di Milano, *CNR-INFM

10:20 a.m.
30.4 Fast Switching and Long Retention Fe-O ReRAM and its Switching Mechanism, S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K.Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa, T. Takagi, Matsushita Electric Industrial Co., Ltd.

10:45 a.m.
30.5 A Novel Resistance Memory with High Scalability and Nanosecond Switching, K. Aratani, K. Ohba, T. Mizuguchi, S. Yasuda, T. Shiimoto, T. Tsushima, T. Sone, K. Endo, A. Kouchiyama, S. Sasaki, A. Maesaka, N. Yamada, and H. Narisawa, Sony Corporation

11:10 a.m.
30.6 Silicon Photonics Approach for Nanotechnology Era, K. Ohashi, K. Nishi, J. Fujikata, M. Nakada, T. Ishi, T. Shimizu, K. Nose, A. Gomyo, T. Ishi, J. Ushida, M. Mizuno, M. Kinoshita, N. Suzuki, D. Okamoto, H. Yukawa, T. Tsuchizawa*, T. Watanabe*, K. Yamada*, S. Itabasi*, J. Akedo**, MIRAI-Selete, NEC, *NTT, **AIST

11:35 a.m.
30.7 Single-Electron Circuit for Stochastic Data Processing Using Nano-MOSFETs, K. Nishiguchi, A. Fujiwara, NTT Corporation

Session 31: CMOS and Interconnect Reliability - Negative Bias Temperature Instability

Wednesday, December 12, 9:00 a.m.
Lincoln Room

Co-Chairs: Gennadi Bersuker, SEMATECH
John Suehle, NIST

9:00 a.m.
Introduction

9:05 a.m.
31.1 New Characterization And Modeling Approach for NBTI Degradation from Transistor to Product Level, V. Huard, C. Parthasarathy, N. Rallet, M. Mammase, D. Barge, C. Ouvrard*, STMicroelectronics, *NXP Semiconductors

9:30 a.m.
31.2 Simultaneous Extraction of Recoverable and Permanent Components Contributing to Bias-Temperature Instability, T. Grasser, B. Kaczer*, P. Hehenberger, W. Goes, R. O'Connor*, H. Reisinger**, W. Gustin**, and C. Schluender**, TU Wien, *IMEC, **Infineon Technologies

9:55 a.m.
31.3 Theory and Practice of Ultra-fast Measurements for NBTI Degradation: Challenges and Opportunities, A.E. Islam, E. N. Kumar*, H. Das*, S. Purawat*, V. Maheta*, H. Aono**, E. Murakami**, S. Mahapatra*, and M.A. Alam, Purdue University, *IIT Bombay, **Renesas Technologies

10:20 a.m.
31.4 Material Dependence of NBTI Physical Mechanism in Silicon Oxynitride (SiON) p-MOSFETs: A Comprehensive Study by Ultra-Fast On-The-Fly (UF-OTF) I_{DLIN} Technique, E.N. Kumar, V.D. Maheta, S. Purawat, S. Rani, A. E. Islam*, K. Ahmed**, M. A. Alam* and S. Mahapatra, IIT Bombay, *Purdue University, **Applied Materials

10:45 a.m.
31.5 On-The-Fly Interface Trap Measurement and It's Impact on the Understanding of NBTI Mechanism for SiON p-MOSFETs, W.J. Liu, Z.Y. Liu, D. Huang, C.C. Liao*, L.F. Zhang*, Z.H. Gan*, W. Wong*, C. Shen**, and M-F. Li, Fudan University, *Semiconductor Manufacturing International Corp., National University of Singapore

11:10 a.m.
31.6 Real Vth Instability of pMOSFETs with SiON Under Practical Operation Conditions, J.F. Zhang, Z. Ji, M.H. Chang, B. Kaczer*, and G. Groeseneken*, Liverpool John Moores University, *IMEC

11:35 a.m.
31.7 New Observations on the Hot Carrier and NBTI Reliability of Silicon Nanowire Transistors, R. Wang, R. Huang, D-W Kim*, Y. He, Z. Wang, G. Jia, D. Park*, Y. Wang, Peking University, *Samsung Electronics Co.

12:00 p.m.
31.8 TiN Metal Gate Impact on NBTI Assessed by Interface States and Fast Transient Effects Characterization, M. Rafik, X. Garros*, G. Ribes, G. Ghibaudo*, C. Hobbs**, A. Zauner***, M. Muller***, V. Huard***, C.Ouvrard***, STMicroelectronics, *CEA-LETI, **IMEP ENSERG-23, ***Freescale, NXP

Session 32: Displays, Sensors, and MEMS - Chemical and Biological Sensors, and Microsystems

Wednesday, December 12, 9:00 a.m.
Thoroughbred Room

Co-Chairs: Julian Gardner, Warwick University
Joost van Beek, NXP Semiconductors

9:00 a.m.
Introduction

9:05 a.m.
32.1 Three Technologies for a Smart Miniaturized Gas-Sensor: SOI CMOS, Micromachining and CNTs - Challenges and Performance, F. Udrea, J.W. Gardner*, J. Park**, M.S. Haque, S.Z. Ali, P.K. Guha, S.M.C. Vieira, H.Y. Kim**, S.Y. Lee**, S. H. Kim**, Y. Choi**, K.C. Kim**, S.E. Moon**, W.I. Milne, and S. Maeng**, University of Cambridge, *University of Warwick, **Electronics and Telecommunication Research Institute

9:30 a.m.
32.2 AlGaN/GaN Heterojunction Field Effect Transistors for High Temperature Hydrogen Sensing with Enhanced Sensitivity, J. Song and W. Lu, The Ohio State University

9:55 a.m.
32.3 Improved Liquid Phase Chromatography Separation Using Sub-Micron Micromachining Technology, D. Sabuncuoglu Tezcan, A. Verbist, C. Van Hoof, W. De Malsche*, J. Vangelooven*, H. Eghbali*, D. Clicq*, G. Desmet* and P. De Moor, IMEC, *Vrije Universiteit Brussel

10:20 a.m.
32.4 A Micro Ionizer for Portable Mass Spectrometers using Double-gated Isolated Vertically Aligned Carbon Nanofiber Arrays, L.-Y. Chen, L.F. Velasquez-Garcia, X. Wang*, and K. Teo*, and A.I. Akinwande, Massachusetts Institute of Technology, *University of Cambridge

10:45 a.m.
32.5 Optoelectronic Tweezers for Manipulation of Cells and Nanowires, M.C. Wu, University of California

11:10 a.m.
32.6 Integrated ZnO Surface Acoustic Wave Microfluidic and Biosensor System, Y.Q. Fu, D.S. Lee*, X.Y. Du, S.C. Tan, J.K. Luo, A.J. Flewitt, S.H. Kim*, N. M. Park*, H. C. Yoon**, W.I. Milne, and S. Maeng*, University of Cambridge, *Electronics and Telecommunications Research Institute (ETRI), **Ajou University

11:35 a.m.
32.7 Electrical Measurement Of Adhesion and Viability of Living Cells with a Silicon Chip, L. Bandiera, M.Borgo, G. Cellere*, A.De Toni*, L. Santoni, M. Dal Maschio*, S. Girardi*, L. Lorenzelli**, and A. Paccagnella*, Biosilab, *Universita di Padova, **FBK-irst

Session 33: Quantum, Power, and Compound Semiconductor Devices - High Voltage Power Devices

Wednesday, December 12, 1:30 p.m.
International Ballroom West

Co-Chairs: Fred van Rijs, NXP Semiconductors
Vishnu Khemka, Freescale Semiconductor

1:30 p.m.
Introduction

1:35 p.m.
33.1 8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation, Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, T. Ueda, T. Tanaka, D. Ueda, Semiconductor Company, Matsushita Electric-Panasonic

2:00 p.m.
33.2 650V 3.1mΩcm^2 GaN-based Monolithic Bidirectional Switch Using Normally-off Gate Injection Transistor, T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, D. Ueda, Semiconductor Company, Matsushita Electric - Panasonic

2:25 p.m.
33.3 Current Collapseless High-Voltage GaN-HEMT and its 50-W Boost Converter Operation, W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, Y. Saito, I. Omura and M. Yamaguchi, Toshiba Corporation

2:50 p.m.
33.4 High-Performance P-Channel Diamond MISFETs with Alumina Gate Insulator, K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Kawarada, Waseda University

3:15 p.m.
33.5 Stress-Induced Mobility Enhancement for Integrated Power Transistors, P. Moens, J. Roig, F. Clemente*, I. De Wolf*, B. Desoete, F. Bauwens, M. Tack, AMI Semiconductor Belgium, *IMEC

3:40 p.m.
33.6 Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS, C.C. Cheng, J.F. Lin, T. Wang, T.H. Hsieh*, J.T. Tzeng*, Y.C. Jong*, R.S. Liou*, S.C. Pan*, and S.L. Hsu*, National Chiao-Tung University, *TSMC

Session 34: CMOS Devices - Advanced Device Structures

Wednesday, December 12, 1:30 p.m.
International Ballroom Center

Co-Chairs: Chih-Sheng Chang, TSMC
Akira Hokazono, Toshiba

1:30 p.m.
Introduction

1:35 p.m.
34.1 Observation of Mobility Enhancement In Strained Si And SiGe Tri-Gate MOSFETs with Multi-Nanowire Channels Trimmed by Hydrogen Thermal Etching, T. Tezuka, E. Toyoda*, S. Nakaharai, T.Irisawa, N. Hirashita, Y. Moriyama, N. Sugiyama, N. Taoka**, Y. Yamashita**, O. Kiso**, M. Harada, T. Yamamoto and S. Takagi**, MIRA-ASET, *Covalent Materials Corp., **MIRAI-AIST

2:00 p.m.
34.2 Investigation of Nanowire Size Dependency on TSNWFET, S.D. Suk, M. Li, Y-Y Yeoh, K. H. Yeo, K.H. Cho, I.K. Ku**, H. Cho*, WJ Jang *, D-W Kim, D. Park, and W-S Lee, Samsung Electronics

2:25 p.m.
34.3 New Self-Aligned Silicon Nanowire Transistors on Bulk Substrate Fabricated by Epi-Free Compatible CMOS Technology: Process Integration, Experimental Characterization of Carrier Transport and Low Frequency Noise, Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, Y. Wang, Peking University

2:50 p.m.
34.4 Experimental Investigation on Superior PMOS Performance of Uniaxial Strained <110> Silicon Nanowire Channel By Embedded SiGe(e-SG) Source/Drain, M. Li, K.H. Yeo, Y-Y Yeoh, S.D. Suk, K.H. Cho, D-W Kim, D Park, and W-S Lee, Samsung Electronics Co., Ltd.

3:15 p.m.
34.5 A Novel Body Effect Reduction Technique to Recessed Channel Transistor Featuring Partially Insulating Layer Under Source and Drain : Application to Sub-50nm DRAM Cell, J-M Park, S-O Sohn, J-S Park, J-B Lee, S. Yamada, W. Yang, D. Park, Samsung Electronics Co.

3:40 p.m.
34.6 Ultra-Low Leakage Silicon-on-Insulator Technology for 65 nm Node and Beyond, J. Cai, A. Majumdar, D. Dobuzinsky*, T.H. Ning, S. Koester, and W. Haensch, IBM Research, *IBM SRDC

Session 35: Solid State and Nanoelectronic Devices - Nanoscale Flash and DRAM Technologies

Wednesday, December 12, 1:30 p.m.
International Ballroom East

Co-Chairs: Tejas Krishnamohan, Intel
Samuel Fung, TSMC

1:30 p.m.
Introduction

1:35 p.m.
35.1 A High-Speed BE-SONOS NAND Flash Utilizing the Field-Enhancement Effect of FinFET, T-H Hsu, H-T Lue, E-K. Lai, .J-Y Hsieh, S-Y Wang, L-W Yang, T. Yang, Y-C King*, K-C Chen, K-Y Hsieh, R. Liu, and C-Y Lu, Macronix International Co., Ltd., *National Tsing-Hua University

2:00 p.m.
35.2 Highly Scalable Vertical Double Gate NOR Flash Memory, H. Cho, P. Kapur, P. Kalavade and K.C. Saraswat, Stanford University, *Intel

2:25 p.m.
35.3 Advantages of the FinFET Architecture in SONOS and Nanocrystal Memory Devices, S. Lombardo, C. Gerardi*, L. Breuil**, C. Jahan***, L. Perniola***, G. Cina*, D. Corso, E. Tripiciano*, V. Ancarani*, G. Iannaccone^, G. Iacono*, C. Bongiorno, C. Garozzo, P. Barbera, E. Nowak***, R. Puglisi, G. A. Costa*, C. Coccorese*, M. Vecchio*, E. Rimini, J. Van Houdt**, B. De Salvo***, M. Melanotte*, CNR-IMN, *STMicroelectronics, **IMEC, ***CEA-LETI, ^University of Pisa

2:50 p.m.
35.4 New Generation of Z-RAM, S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, Innovative Silicon

3:15 p.m.
35.5 A High Speed Unified-RAM (URAM) Cell Multi-Functioning Capacitorless DRAM and NVM, J-W Han, S-W Ryu, S-H Kim, C. Kim, M. Im, S-J Choi, J.S. Kim*, K.H. Kim*, J.S. Oh*, M.H. Song*, G.S. Lee*, Y.C. Park*, J.W. Kim*, and Y-K Choi, KAIST, *National Nanofab Center

3:40 p.m.
35.6 Extremely Low-voltage and High-speed Operation Bulk Thyristor-SRAM/DRAM (BT-RAM) Cell with Triple Selective Epitaxy Layers (TEL), T. Sugizaki, M. Nakamura, M. Yanagita, M. Shinohara, T. Ikuta, T. Ohchi, K. Kugimiya, S. Kanda, K. Yagami and T. Oda, Sony Corporation

Session 36: Modeling and Simulation - Simulation of Processes and Advanced Memories

Wednesday, December 12, 1:30 p.m.
Georgetown Ballroom

Co-Chairs: Masami Hane, NEC
Andrea Ghetti, STMicroelectronics

1:30 p.m.
Introduction

1:35 p.m.
36.1 Physical Interpretation, Modeling and Impact on Phase Change Memory (PCM) Reliability of Resistance Drift Due to Chalcogenide Structural Relaxation, D. Ielmini, S. Lavizzari, D. Sharma and A. L. Lacaita, Politecnico di Milano and IU.NET

2:00 p.m.
36.2 Physical Model for NAND Operation in SOI and Body-Tied Nanocrystal FinFLASH Memories, L. Perniola, E. Nowak, G. Iannaccone*, P. Scheiblin, C. Jahan, G. Pananakakis**, J. Razafindramora, B. De Salvo, S. Deleonibus, G. Reimbold, F. Boulanger, CEA-LETI, *Universita di Pisa, **IMEP/INPG

2:25 p.m.
36.3 Development of A 3D Simulator for Metal Nanocrystal (NC) Flash Memories Under NAND Operation, A. Nainani, S. Palit, P. K. Singh, N. Krishna*, J. Vasi and S. Mahapatra, IIT Bombay, *Applied Materials

2:50 p.m.
36.4 Recent Advances and Future Prospects of Atomistic Process Simulation, M. Jaraiz, P. Castrillo, R. Pinacho, and J.E. Rubio, University of Valladolid

3:15 p.m.
36.5 Analysis of As, P Diffusion and Defect Evolution During Sub-millisecond Non-melt Laser Annealing Based on an Atomistic Kinetic Monte Carlo Approach, T. Noda, W. Vandervorst*, S. Felch**, V. Parihar**, A, Cuperus**, R. Mcintosh**, C. Vrancken*, E. Rosseel*, H. Bender*, B. Van Daele*, M. Niwa, H. Umimoto, R. Schreutelkamp**, P.P. Absil*, M. Jurczak*, K. De Meyer*, S. Biesemans*, T. Y. Hoffmann*, Matsushita Electric Ind., *IMEC, **Applied Materials

3:40 p.m.
36.6 Experimental and Theoretical Analysis of Dopant Diffusion and C Evolution in High-C Si:C Epi Layers: Optimization of Si:C Source and Drain Formed by Post-Epi Implant and Activation Anneal, Y. Cho, N. Zographos*, S. Thirupapuliyur, and V. Moroz**, Applied Materials, *Synopsys Switzerland LLC, *Synopsys, Inc.

4:05 p.m.
36.7 Novel Doping Technology for a 1nm NiSi/Si Junction with Dipoles Comforting Schottky (DCS) Barrier, T. Yamauchi, Y. Nishi, Y. Tsuchiya, A. Kinoshita, J. Koga, K. Kato, Toshiba Corp.

Session 37: Process Technology - Interconnect and 3D-IC's

Wednesday, December 12, 1:30 p.m.
Jefferson Room

Co-Chairs: John Iacoponi, AMD
Toshiaki Hasegawa, Sony

1:30 p.m.
Introduction

1:35 p.m.
37.1 32 nm node Ultralow-k(k=2.1)/Cu Damascene Multilevel Interconnect using High-Porosity (50 %) High-Modulus (9 GPa) Self-Assembled Porous Silica, S. Chikaki, K. Kinoshita, T. Nakayama*, K. Kohmura**, H. Tanaka**, M. Hirakawa*, E. Soda, Y. Seino***, N. Hata***, T. Kikkawa***, and S. Saito, Selete, *ULVAC, Inc., **Mitsui Chemicals, Inc., ***AIST

2:00 p.m.
37.2 Cost-effective and High Performance Cu Interconnects (k_{eff}=2.75) with Continuous SiOCH Stack Incorporating a Low-k Barrier Cap (k=3.1), M. Ueki, H. Yamamoto, F. Ito, J. Kawahara, M. Tada, Y. Fukumoto, T. Takeuchi, S. Saito, N. Furutake, T. Onodera and Y. Hayashi, NEC Corporation

2:25 p.m.
37.3 Bulk and Interface Band Diagrams of Advanced Intermetal Dielectrics, C.Guedj, E. Martinez, C. Licitra, G.Imbert*, J.P. Barnes, D. Lafond, A. Toffoli, LETI-MINATEC, *STMicroelectronics

2:50 p.m.
37.4 FR-4 and CMOS: Enabling Technologies for Consumer Volume Millimeterwave Applications, J. Laskar, S.Pinel, D. Dawn, S. Sarkar, P. Sen B. Perunama and D. Yeh, Georgia Institute of Technology

3:15 p.m.
37.5 New Three-Dimensional Integration Technology Based on Reconfigured Wafer-on-Wafer Bonding Technique, T. Fukushima, Y. Yamada, H. Kikuchi, T. Konno, J. Liang, A. Mossad Ali, K. Sasaki, K. Inamura, T. Tanaka, and M. Koyanagi, Tohoku University

3:40 p.m.
37.6 Highly Reliable Thin MIM Capacitor on Metal (CoM) Structure with Vertical Scalability for Analog/RF Applications, N. Inoue, I. Kume, J. Kawahara, N. Furutake, T. Toda*, K. Matsui*, M. Furumiya*, T. Iwaki*, S. Shida*, Y. Hayashi, NEC Corp., *NEC Electronics Corp.

4:05 p.m.
37.7 Mass Productive Worthy MIM Capacitor On Gate poly silicon(MIM-COG) Structure Using $HfO_2/HfO_xC_yN_z/HfO_2$ Dielectric for Analog/RF/Mixed Signal Application, J-M Park, M-W Song W-H Kim, Y-K Jung, P-K Park, J-Y Kim, S-J Won, J-H Lee, N-I Lee and H-K Kang, Samsung Electronics Co., Ltd.

4:30 p.m.
37.8 Toward Next High Performances MIM Generation: Up To 30fF/µm² with 3D Architecture and High-k Materials, S. Jeannot, A. Bajolet, J.-P. Manceau, S. Cremer, E. Deloffre, J.P. Oddou, C. Perrot, D. Benoit, C. Richard, P. Bouillon, S. Bruyere, STMicroelectronics

Session 38: Displays, Sensors, and MEMS - Imagers and Optical Detectors

Wednesday, December 12, 1:30 p.m.
Lincoln Room

Co-Chairs: Bedabrata Pain, California Institute of Technology
Jan Bosiers, DALSA

1:30 p.m.
Introduction

1:35 p.m.
38.1 A 0.5mm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS, K. Fife, A. El Gamal, H.-S. Philip Wong, Stanford University

2:00 p.m.
38.2 Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels, T, Joy, S. Pyo, S. Park, C. Choi, C. Palsule, H. Han, C. Feng, S. Lee, J. McKee, P. Altice, C. Hong, C. Boemler, J. Hynecek, J. Lee, D. Kim, H. Haddad, and B. Pain*, Magnachip Corp. *Jet Propulsion Lab

2:25 p.m.
38.3 Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging, F. Taghibakhsh, K.S. Karim, Simon Fraser University

2:50 p.m.
38.4 Fully Implantable Retinal Prosthesis Chip with Photodetector and Stimulating Electrode Array, T. Tanaka, T. Kobayashi, K. Komiya, K. Sato, T. Watanabe, T. Fukushima, H. Tomita, H. Kurino, M. Tamai, and M. Koyanagi, Tohoku University

3:15 p.m.
38.5 3 D Real-time CCD Imager Based on Background-Level-Subtraction Scheme, Y. Hashimoto, F. Tsunesada, K. Imai, Y. Takada, K. Taniguchi*, Matsushita Electric Works, Ltd., *Osaka University

3:40 p.m.
38.6 Potentiality of Silicon Optical Modulator Based on Free-Carrier Absorption, T. Tabei, T. Hirata, K. Kajikawa, H. Sunami, Hiroshima University

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