5-DAY PROGRAM

SUNDAY ALL-DAY: 2 FORUMS:
9 TUTORIALS: nm Layout; SC Noise Analysis; Power-Delay Tradeoffs; Silicon-Body Interface; Digital - Ultra Low Voltage & Power; Embedded Memory; LC Oscillators; Rx Distortion; DPLL CDR
EVENING: 2 Special-Topic Sessions & Student Research Preview

THURSDAY ALL-DAY: 4 FORUMS:
Personalized Medical Care; Green Microprocessors; 3D Image Sensors; High-Speed Xcelvers
SHORT-COURSE: Cellular and Wireless LAN Transceivers

Transmitters for Wireless Infrastructure; ULV Circuits for Energy-Efficient Systems

IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2011 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 20, 21, 22, 23, 24

CONFERENCE THEME:

ELECTRONICS FOR HEALTHY LIVING

SAN FRANCISCO MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
Plenary Roundtable
(in addition to 3 Plenary talks)
Industrial Demo Session

ISSCC 2011 ADVANCE PROGRAM

Printed on Recycled Paper

ISSCC 2011
c/o S3 Digital Publishing Inc.
60A Capital Ave
Lisbon Falls, Maine 04252
USA

Next ISSCC Dates and Location: ISSCC 2012 will be held on February 19-23, 2012 at the San Francisco Marriott Marquis Hotel.

San Francisco Area Information: Make the most of your trip to San Francisco! Visit the San Francisco Convention & Visitors Bureau website at www.sfvisitor.org for ideas and information. For additional information on traveling throughout the city, visit BART's website at www.bart.gov.

Getting to the San Francisco Marriott Marquis Hotel: There are several transportation options to get from the San Francisco Airport (SFO) to the conference hotel. Visit the ISSCC website at www.isscc.org and select "Attendee/Travel from Airport" to download a Word document with directions and pictures. You can get a map and driving directions from the Marriott website at:
www.marriott.com/hotels/maps/travel/sfodt-san-francisco-marriott/

For Further Information:

Conference Information:	ISSCC@ieee.org
Hotel Information:	San Francisco Marriott Marquis 55 Fourth Street San Francisco, CA 94103 Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Phone: 416-418-3034 Fax: 416-971-2286 kfujino@cs.com
Registration Information:	YesEvents P.O. Box 32862 Baltimore, MD 21282 Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217 isscc.info@yesevents.com
Additional Information for Attendees, Authors and Press:	Please visit the ISSCC website at www.isscc.org.

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

CONFERENCE INFORMATION

HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the registration website.
FAX or mail: The Registration Form can be downloaded from the registration website. Please read the descriptions and instructions on the back of the form carefully.
Onsite: The Onsite Registration and Advance Registration Pickup Desks at ISSCC 2011 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis.
Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 14, 2011.** After January 14th, and on or before 11:59 pm Pacific Time Sunday January 30, 2011, registrations will be processed **at the Late Registration rates. After January 30th, you must register onsite at the onsite rates.**
IEEE members enjoy lower registration fees. Consider joining IEEE before registering.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Starting Sunday evening and continuing through Wednesday.
Technical Book Display: Several technical publishers will have professional books and textbooks for sale during the Conference.
Poster Session: ISSCC/DAC student contest winners will display their work in poster form.
Demo Session: Hardware demonstrations will support selected papers.
Author Interviews: Author Interviews will be held after each day's sessions.
Social Hours: Social Hour refreshments will be available Monday and Tuesday evenings.
University Events: Several universities are planning social events during the Conference.
ISSCC logo case: A convenient soft briefcase will be provided.
Digest of Technical Papers in both hard copy and on CD.
ISSCC 2011 Conference DVD that includes the Digest and Visuals Supplement (to be mailed in April). **Student registration does not include the ISSCC 2011 Conference DVD, however it is available for purchase at a reduced fee for students.**

OPTIONAL EVENTS

Educational Events: Many educational events are available on Sunday and Thursday for an additional fee. The all-day events include meals.
Women's Networking Reception: ISSCC will be sponsoring a networking event for women in solid-state circuits.

OPTIONAL PUBLICATIONS FOR SALE

ISSCC 2011 and Earlier Publications: There are several ways to purchase this material:
-Items listed on the registration form can be purchased with registration and picked up onsite at the conference or mailed to you when available.
-Visit the ISSCC Publications Desk located in the registration area where you can pick up (or order for future delivery) materials from ISSCC 2011 and earlier conferences.
-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail or fax.

HOW TO MAKE HOTEL RESERVATIONS

TO ALL ATTENDEES WHO NEED A HOTEL ROOM: We are offering this year a $100 MARRIOTT REBATE COUPON! If you register for ISSCC 2011 and spend at least three nights at the San Francisco Marriott Marquis, a credit of $100 will be applied to your hotel bill. Enjoy the convenience of staying at the Conference hotel AND save money too! See the hotel reservations site for details.

Online: Go to the conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott Marquis. **Conference room rates are $213 for a single/double, $233 for a triple and $253 for a quad.** We have negotiated that attendees staying at the Marriott Marquis receive **in-room Internet access for free**.
Telephone: Call 888-575-8934 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2011 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 30, 2011 to obtain the special ISSCC rates.

-Conference website: www.isscc.org
-Conference email: isscc@ieee.org
-Registration questions/adjustments: ISSCCinfo@yesevents.com

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 20th**, the day before the official opening of the Conference, ISSCC 2011 offers:

- A choice of up to 4 of a total of 9 Tutorials
- A choice of 1 of 2 Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are three events: Special-Topic Sessions entitled, "**Data-Converter Breakthroughs…** and **Wireless Sensor Systems…**" will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations by selected graduate-student researchers from around the world will begin at 7:45 pm. A distinguished circuit designer, Professor Paul Gray will provide introductory remarks at the Preview.

On **Monday, February 21st**, ISSCC 2011 offers three plenary papers on the theme: "Electronics for Healthy Living". This will be followed by a Technology Roundtable on challenges to be faced in the next 10x reduction in power, with six renowned panelists, a moderator, and three domain experts to pose questions. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees, and a Women's Networking Reception. The Social Hour held in conjunction with the Book Display will also feature posters from the winners of the joint ISSCC/DAC Student-Design Contest. Monday evening features a panel discussion on "**20 Years of Broadband Evolution…**", as well as two Special-Topic Sessions on "**Future System and Memory Architectures…**" **and** "**Body-Area Networks (BAN)…**".

On **Tuesday, February 22nd**, offers five parallel morning and afternoon technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will include Industrial Demo Sessions. Tuesday evening sessions include an evening panel on "**20/22nm Technology Options and Design Implications**", as well as two Special-Topic Sessions on "**Gb/s+ Portable Wireless Communications**" and "**Technologies for Smart Grid and Smart Meter**".

Wednesday, February 23rd, features five parallel sessions morning and afternoon.

On **Thursday, February 24th**, ISSCC offers a choice of five events:

- A Short Course on "**Cellular and Wireless LAN Transceivers: From Systems to Circuit Design**"
- Four Advanced-Circuit-Design Forums

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums and the Short Course.

Need Additional Information?
Go to: www.isscc.org

TUTORIALS — Sunday February 20, 2011

T1: Layout — The Other Half of Nanometer Analog Design
Jed Hurwitz, Gigle Networks

T2: Noise Analysis in Switched-Capacitor Circuits
Boris Murmann, Stanford Univ.

T3: Practical Power-Delay Design Trade-Offs
Tim Fischer, AMD

T4: Interfacing Silicon with the Human Body
Tim Denison, Medtronic

T5: Ultra-Low Power and Low Voltage in Digital Design
Jos Huisken, IMEC

T6: Embedded Memories for SoC
Harold Pilo, IBM

T7: Integrated LC Oscillators
Pietro Andreani, Lund Univ.

T8: Distortion in Cellular Receivers
Sven Mattisson, Ericsson

T9: DPLL-Based Clock and Data Recovery
John T. Stonick, Synopsys

2 FORUMS — Sunday February 20, 2011

Advanced Transmitters for Wireless Infrastructure
Ultra-Low Voltage VLSIs for Energy-Efficient Systems

4 FORUMS — Thursday February 24, 2011

Towards Personalized Medicine and Monitoring for Healthy Living
Design of "Green" High-Performance Processor Circuits
CMOS Image Sensors for 3D Capture
High-Speed Transceivers: Standards, Challenges, and Future

EVENING SESSIONS — February 20-22, 2011

Sunday: Student Research Preview
Data-Converter Breakthroughs in Retrospect
Wireless Sensor Systems: Solutions & Technology

Monday: Future System and Memory Architectures: Transformations by Technology and Applications
Body Area Networks (BAN): Technology, Solutions, and Standardization

Tuesday: Gb/s+ Portable Wireless Communications
Technologies for Smart Grid and Smart Meter

EVENING PANELS — February 21-22, 2011

Monday: 20 Years of Broadband Evolution: What's Next?

Tuesday: 20/22nm Technology Options and Design Implications

SHORT COURSE — Thursday February 24, 2011

Cellular and Wireless LAN Transceivers: From Systems to Circuit Design

Cellular and WLAN Systems and the SoC Transceiver
Instructor: Hooman Darabi

Front-end Circuit Design for RF Transceivers
Instructor: Behzad Razavi

Implementation of Direct-Conversion Transceivers
Instructor: Frank Op't Eynde

Recent Advances in RF Synthesis
Instructor: R. Bogdan Staszewski

ISSCC 2011 Papers at a Glance

Sessions 1-6, Monday February 21st • Sessions 7-17, Tuesday February 22nd • Sessions 18-28, Wednesday February 23rd

Session 1 - Plenary Session

1.1 **New Interfaces to the Body Through Implantable System Integration,** Stephen Oesterle, *Senior VP, Medtronic, Minneapolis, MN*

1.2 **Game-Changing Opportunities for Wireless Personal Healthcare and Lifestyle,** Jo De Boeck, *Senior VP, imec / Holst Centre, Leuven, Belgium*

1.3 **Eco-Friendly Semiconductor Technologies for Healthy Living,** Oh-Hyun Kwon, *President, Samsung Electronics, Giheung, Korea*

1.4 **Beyond the Horizon: The Next 10x Reduction in Power - Challenges and Solutions,** Moderator: Jan Rabaey, *University of California, Berkeley, Berkeley, CA*

Session 2 - Technologies For Health

2.1 **A 0.24nJ/b Wireless Body-Area-Network Transceiver with Scalable Double-FSK Modulation,** *KAIST*

2.2 **A 75μW Real-Time Scalable Network Controller and a 25μW ExG Sensor IC for Compact Sleep-Monitoring Applications,** *KAIST*

2.3 **A 3μW Wirelessly Powered CMOS Glucose Sensor for an Active Contact Lens,** *University of Washington*

2.4 **A 90nm CMOS SoC UWB Pulse Radar for Respiratory Rate Monitoring,** *University College Cork; Tyndall National Institute; University of Pisa; University of Reggio Calabria*

2.5 **A Broadband THz Imager in a Low-Cost CMOS Technology,** *CEA-LETI-MINATEC; Université Montpellier 2 -CNRS UMR*

2.6 **A Programmable Implantable Micro-Stimulator SoC with Wireless Telemetry: Application in Closed-Loop Endocardial Stimulation for Cardiac Pacemaker,** *National Chung Cheng University; National Yang-Ming University; National Chiao Tung University; National Taiwan University; RMIT University*

2.7 **A 660pW Multi-Stage Temperature-Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization,** *University of Michigan*

2.8 **A Low-Power Fully Integrated RF Locked Loop for Miniature Atomic Clock,** *CSEM*

Session 3 - RF Techniques

3.1 **Spur-Free All-Digital PLL in 65nm for Mobile Phones,** *Delft University of Technology; Texas Instruments*

3.2 **A 5.3GHz Digital-to-Time-Converter-Based Fractional-N All-Digital PLL,** *NXP Semiconductors*

3.3 **A 2.5GHz 32nm 0.35mm² 3.5dB NF -5dBm P_{1dB} Fully Differential CMOS Push-Pull LNA with Integrated 34dBm T/R Switch and ESD Protection,** *Intel*

3.4 **A 65nm CMOS Pulse-Width-Controlled Driver with $8V_{pp}$ Output Voltage for Switch-Mode RF PAs up to 3.6GHz,** *Delft University of Technology; NXP Semiconductors; NXP-TSMC Research Center*

3.5 **A Low-Power Process-Scalable Superheterodyne Receiver with Integrated High-Q Filters,** *Broadcom; University of California*

3.6 **A 40nm CMOS Highly Linear 0.4-to-6GHz Receiver Resilient to 0dBm Out-of-Band Blockers,** *imec; Renesas Electronics*

3.7 **A 1.0-to-4.0GHz 65nm CMOS Four-Element Beamforming Receiver Using a Switched-Capacitor Vector Modulator with Approximate Sine Weighting via Charge Redistribution,** *University of Twente; TNO Science and Industry*

3.8 **A Harmonic Rejection Mixer Robust to RF Device Mismatches,** *Silicon Laboratories*

Session 4 - Enterprise Processors & Components

4.1 **A 5.2GHz Microprocessor Chip for the IBM zEnterprise™ System,** *IBM Systems and Technology Group; IBM Research*

4.2 **Dynamic Hit Logic with Embedded 8Kb SRAM in 45nm SOI for the zEnterprise™ Processor,** *IBM Systems and Technology Group*

4.3 **A 32nm Westmere-EX Xeon® Enterprise Processor,** *Intel*

4.4 **Godson-3B: A 1GHz 40W 8-Core 128GFLOPS Processor in 65nm CMOS,** *Chinese Academy of Sciences; Loongson Technologies*

4.5 **Design Solutions for the Bulldozer 32nm SOI 2-Core Processor Module in an 8-Core CPU,** *AMD*

4.6 **40-Entry Unified Out-of-Order Scheduler and Integer Execution Unit for the AMD Bulldozer x86-64 Core,** *AMD*

4.7 **Clock Generation for a 32nm Server Processor with Scalable Cores,** *Intel*

4.8 **A 32nm 3.1 Billion Transistor 12-Wide-Issue Itanium® Processor for Mission-Critical Servers,** *Intel*

Session 5 - PLLs

5.1 **A 2.9-to-4.0GHz Fractional-N Digital PLL with Bang-Bang Phase Detector and 560fs_{rms} Integrated Jitter at 4.5mW Power,** *Politecnico di Milano*

5.2 **An Injection-Locked Ring PLL with Self-Aligned Injection Window,** *MediaTek*

5.3 **A 0.4-to-3GHz Digital PLL with Supply-Noise Cancellation Using Deterministic Background Calibration,** *Oregon State University*

5.4 **A 0.1-f_{ref} BW 1GHz Fractional-N PLL with FIR-Embedded Phase-Interpolator-Based Noise Filtering,** *Pohang University of Science and Technology*

5.5 **A Scalable sub-1.2mW 300MHz-to-1.5GHz Host-Clock PLL for System-on-Chip in 32nm CMOS,** *Intel*

5.6 **A 570fs_{rms} Integrated-Jitter Ring-VCO-Based 1.21GHz PLL with Hybrid Loop,** *Toshiba*

5.7 **A Rotary-Traveling-Wave-Oscillator-Based All-Digital PLL with a 32-Phase Embedded Phase-to-Digital Converter in 65nm CMOS,** *Panasonic*

Session 6 - Sensors & Energy Harvesting

6.1 **A Low-Power 3-Axis Digital-Output MEMS Gyroscope with Single Drive and Multiplexed Angular Rate Readout,** *STMicroelectronics; University of Padova*

6.2 **A 50mW CMOS Wind Sensor with ±4% Speed and ±2° Direction Error,** *Tsinghua University; Delft University of Technology*

6.3 **A Telemetric Stress-Mapping CMOS Chip with 24 FET-Based Stress Sensors for Smart Orthodontic Brackets,** *University of Freiburg - IMTEK; HSG-IMIT*

6.4 **A 21b ±40mV Range Read-Out IC for Bridge Transducers,** *Delft University of Technology*

6.5 **A ±1.5% Nonlinearity 0.1-to-100A Shunt Current Sensor Based on a 6kV Isolated Micro-Transformer for Electrical Vehicles and Home Automation,** *CEA-LETI-MINATEC; Schneider Electric*

6.6 **Indirect X-ray Photon-Counting Image Sensor with 27T Pixel and 15e^-_{rms} Accurate Threshold,** *Caeleste; Vrije Universiteit Brussel*

6.7 **A 1.32pW/frame•pixel 1.2V CMOS Energy-Harvesting and Imaging (EHI) APS Imager,** *University of Idaho*

6.8 **5μW-to-10mW Input Power Range Inductive Boost Converter for Indoor Photovoltaic Energy Harvesting with Integrated Maximum Power Point Tracking Algorithm,** *imec - Holst Centre; Philips Research Laboratories; imec; KU Leuven*

6.9 **A Self-Supplied Inertial Piezoelectric Energy Harvester with Power-Management IC,** *University of Michigan*

Session 7 - Multimedia & Mobile

7.1 **A 216fps 4096×2160p 3DTV Set-Top Box SoC for Free-Viewpoint 3DTV Applications,** *National Taiwan University*

7.2 **A Highly Parallel and Scalable CABAC for Next-Generation Video Coding,** *Massachusetts Institute of Technology*

7.3 **A 275mW Heterogeneous Multimedia Processor for IC-Stacking on Si-Interposer,** *KAIST*

7.4 **A 57mW Embedded Mixed-Mode Neuro-Fuzzy Accelerator for Intelligent Multi-core Processor,** *KAIST*

7.5 **A 28nm 0.6V Low-Power DSP for Mobile Applications,** *Texas Instruments; Massachusetts Institute of Technology; Texas Instruments (now with MaxLinear)*

7.6 **A MIMO WiMAX SoC in 90nm CMOS for 300km/h Mobility,** *ITRI; National Taiwan University*

7.7 **A 70Mb/s -100.5dB Sensitivity 65nm LP MIMO Chipset for WiMAX Portable Router,** *MediaTek*

7.8 **A Direct Digital Frequency Synthesizer with Minimized Tuning Latency of 12ns,** *University of California*

Session 8 - Architectures & Circuits for Next-Generation Wireline Transceivers

8.1 **11.3Gb/s CMOS SONET-Compliant Transceiver for Both RZ and NRZ Applications,** *Broadcom*

8.2 **A Full-Duplex 10GBase-T Transmitter Hybrid with SFDR >65dBc Over 1 to 400MHz in 40nm CMOS,** *Teranetics*

8.3 **A 40Gb/s TX and RX Chip Set in 65nm CMOS,** *National Taiwan University*

8.4 **10:4 MUX and 4:10 DEMUX Gearbox LSI for 100-Gigabit Ethernet Link,** *Hitachi*

8.5 **A 12.5+12.5Gb/s Full-Duplex Plastic Waveguide Interconnect,** *Sony; California Institute of Technology*

8.6 **A Highly Digital 0.5-to-4Gb/s 1.9mW/Gb/s Serial-Link Transceiver Using Current-Recycling in 90nm CMOS,** *Oregon State University; IBM Zurich Research Laboratory*

8.7 **A 1-to-6Gb/s Phase-Interpolator-Based Burst-Mode CDR in 65nm CMOS,** *University of Toronto; Fujitsu Laboratories*

8.8 **A 14Gb/s High-Swing Thin-Oxide Device SST TX in 45nm CMOS SOI,** *IBM Zurich Research Laboratory; Miromico*

Session 9 - Wireless & mm-Wave Connectivity

9.1 **A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE 802.15.3c,** *Tokyo Institute of Technology*

9.2 **A 65nm CMOS Fully Integrated Transceiver Module for 60GHz Wireless HD Applications,** *CEA-LETI-MINATEC; STMicroelectronics*

9.3 **A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications,** *SiBEAM*

9.4 **A 65nm CMOS 4-Element Sub-34mW/Element 60GHz Phased-Array Transceiver,** *University of California*

9.5 **An 87GHz QPSK Transceiver with Costas-Loop Carrier Recovery in 65nm CMOS,** *National Taiwan University*

9.6 **A 65nm Dual-Band 3-Stream 802.11n MIMO WLAN SoC,** *Atheros Communications*

9.7 **A 0.46mm² 4dB-NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS** *University of Macau; Instituto Superior Tecnico*

9.8 **An All-Digital 8-DPSK Polar Transmitter with Second-Order Approximation Scheme and Phase Rotation-Constant Digital PA for Bluetooth EDR in 65nm CMOS,** *Toshiba Semiconductor*

9.9 **A Digital-Intensive Receiver Front-End Using VCO-Based ADC with an Embedded 2nd-Order Anti-Aliasing Sinc Filter in 90nm CMOS,** *KAIST*

Session 10 - Nyquist Rate Converters

10.1 **A 480mW 2.6GS/s 10b 65nm CMOS Time-Interleaved ADC with 48.5dB SNDR up to Nyquist,** *NXP Semiconductors*

10.2 **A 12b 1GS/s SiGe BiCMOS Two-Way Time-Interleaved Pipeline ADC,** *Texas Instruments*

10.3 **An 800MS/s Dual-Residue Pipeline ADC in 40nm CMOS,** *Broadcom*

10.4 **A 16b 80MS/s 100mW 77.6dB SNR CMOS Pipeline ADC,** *Analog Devices*

10.5 **A 0.024mm² 8b 400MS/s SAR ADC with 2b/Cycle and Resistive DAC in 65nm CMOS,** *University of Macau; University of Pavia*

10.6 **A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC,** *Massachusetts Institute of Technology*

10.7 **A 12b 1.25GS/s DAC in 90nm CMOS with >70dB SFDR up to 500MHz,** *National Chiao Tung University*

10.8 **A 56GS/s 6b DAC in 65nm CMOS with 256×6b memory,** *Ciena*

Session 11 - Non-Volatile Memory Solutions

11.1 **A 151mm² 64Gb MLC NAND Flash Memory in 24nm CMOS Technology,** *Toshiba Semiconductor; Toshiba Memory Systems; Sandisk*

11.2 **A 4Mb Embedded SLC Resistive-RAM Macro with 7.2ns Read-Write Random-Access Time and 160ns MLC-Access Capability,** *ITRI; National Tsing Hua University; National Central University*

11.3 **A 32Gb MLC NAND Flash Memory with V_{th} Margin-Expanding Schemes in 26nm CMOS,** *Hynix Semiconductor*

11.4 **95%-Lower-BER 43%-Lower-Power Intelligent Solid-State Drive (SSD) with Asymmetric Coding and Stripe Pattern Elimination Algorithm,** *University of Tokyo; SIGLEAD*

11.5 **An Offset-Tolerant Current-Sampling-Based Sense Amplifier for Sub-100nA-Cell-Current Nonvolatile Memory,** *National Tsing Hua University; TSMC; Fukuoka Institute of Technology*

11.6 **A Low-Voltage 1Mb FeRAM in 0.13μm CMOS Featuring Time-to-Digital Sensing for Expanded Operating Margin in Scaled CMOS,** *Massachusetts Institute of Technology; Texas Instruments*

11.7 **A 4Mb Conductive-Bridge Resistive Memory with 2.3GB/s Read-Throughput and 216MB/s Program-Throughput,** *Sony; Sony LSI Design*

11.8 **A 7MB/s 64Gb 3-Bit/Cell DDR NAND Flash Memory in 20nm-Node Technology,** *Samsung Electronics*

Session 12 - Design in Emerging Technologies

12.1 **A 95mV-Startup Step-Up Converter with V_{TH}-Tuned Oscillator by Fixed-Charge Programming and Capacitor Pass-On Scheme,** *University of Tokyo; Semiconductor Technology Academic Research Center*

12.2 **100V AC Power Meter System-on-a-Film (SoF) Integrating 20V Organic CMOS Digital and Analog Circuits with Floating Gate for Process-Variation Compensation and 100V Organic PMOS Rectifier,** *University of Tokyo; Dai Nippon Printing*

12.3 **Real-Time Current-Waveform Sensor with Plugless Energy Harvesting from AC Power Lines for Home/Building Energy-Management Systems,** *NEC*

12.4 **A 3.9ns 8.9mW 4×4 Silicon Photonic Switch Hybrid Integrated with CMOS Driver,** *IBM T. J. Watson Reseach Center*

12.5 **A 820GHz SiGe Chipset for Terahertz Active Imaging Applications,** *University of Wuppertal; IHP*

12.6 **A 130μA Wake-Up Receiver SoC in 0.13μm CMOS for Reducing Standby Power of An Electric Appliance Controlled by An Infrared Remote Controller,** *Toshiba*

12.7 **Programmable Cell Array Using Rewritable Solid-Electrolyte Switch Integrated in 90nm CMOS,** *NEC*

12.8 **6W/25mm² Inductive Power Transfer for Non-Contact Wafer-Level Testing,** *Keio University*

12.9 **GHz-Range Continuous-Time Programmable Digital FIR with Power Dissipation that Automatically Adapts to Signal Activity,** *Columbia University; CEA-LETI-MINATEC*

Session 13 - Analog Techniques

13.1 **A Simple LED Lamp Driver IC with Intelligent Power-Factor Correction,** *Fairchild Semiconductor*

13.2 **A 1.2A Buck-Boost LED Driver with 13% Efficiency Improvement Using Error-Averaged SenseFET-Based Current Sensing,** *Oregon State University; National Semiconductor*

13.3 **Filterless Integrated Class-D Audio Amplifier Achieving 0.0012% THD+N and 96dB PSRR When Supplying 1.2W,** *Dialog Semiconductor*

13.4 **A 5.9nV/√Hz Chopper Operational Amplifier with 0.78μV Maximum Offset and 28.3nV/°C Offset Drift,** *Analog Devices*

13.5 **A Current-Feedback Instrumentation Amplifier with a Gain Error Reduction Loop and 0.06% Untrimmed Gain Error,** *Delft University of Technology*

13.6 **A 6.7nV/√Hz Sub-mHz-1/f-Corner 14b Analog-to-Digital Interface for Rail-to-Rail Precision Voltage Sensing,** *Robert Bosch*

13.7 **A 36V JFET-Input Bipolar Operational Amplifier with 1μV/°C Maximum Offset Drift and -126dB Total Harmonic Distortion,** *Texas Instruments*

13.8 **A 3.3V-Supply 120mW Differential ADC Driver Amplifier in 0.18μm SiGe BiCMOS with 108dBc IM3 at 100MHz,** *Intersil*

Session 14 - High-Performance Embedded Memory

14.1 **A 64Mb SRAM in 32nm High-k Metal-Gate SOI Technology with 0.7V Operation Enabled by Stability, Write-Ability and Read-Ability Enhancements,** *IBM Systems and Technology Group*

14.2 **A 4R2W Register File for a 2.3GHz Wire-Speed POWER™ Processor with Double-Pumped Write Operation,** *IBM T. J. Watson Reseach Center; IBM Systems and Technology Group; Hoerner & Sulger*

14.3 **An 8MB Level-3 Cache in 32nm SOI with Column-Select Aliasing,** *AMD*

14.4 **A 28nm High-Density 6T SRAM with Optimized Peripheral-Assist Circuits for Operation Down to 0.6V,** *Massachusetts Institute of Technology; Texas Instruments*

Session 15 - High-Performance SoCs & Components

15.1 **A Fully Integrated Multi-CPU, GPU and Memory Controller 32nm Processor,** *Intel*

15.2 **An 80Gb/s Dependable Communication SoC with PCI Express I/F and 8 CPUs,** *Renesas Electronics; University of Tsukuba*

15.3 **A Fully-Integrated 3-Level DC/DC Converter for Nanosecond-Scale DVS with Fast Shunt Regulation,** *Harvard University*

15.4 **A Low-Power Integrated x86-64 and Graphics Processor for Mobile Computing Devices,** *AMD*

15.5 **A Programmable Adaptive Phase-Shifting PLL for Clock Data Compensation Under Resonant Supply Noise,** *University of Minnesota*

15.6 **A Side-Channel and Fault-Attack Resistant AES Circuit Working on Duplicated Complemented Values,** *CEA-LETI-MINATEC; Ecole Nationale Supérieure des Mines de Saint-Etienne*

Session 16 - mm-Wave Design Techniques

16.1 **A 21.7-to-27.8GHz 2.6-Degrees-rms 40mW Frequency Synthesizer in 45nm CMOS for mm-Wave Communication Applications,** *NXP Semiconductors*

16.2 **A mm-Wave Quadrature VCO Based on Magnetically Coupled Resonators,** *University of Pavia; University of Modena e Reggio Emilia; Istituto Universitario di Studi Superiori di Pavia*

16.3 **A 6.5mW Inductorless CMOS Frequency Divider by 4 Operating up to 70GHz,** *University of Pavia; University of Modena e Reggio Emilia; Istituto Universitario di Studi Superiori di Pavia*

16.4 **A 60GHz Antenna-Referenced Frequency-Locked Loop in 0.13μm CMOS for Wireless Sensor Networks,** *University of Michigan*

16.5 **A 220-to-275GHz Traveling-Wave Frequency Doubler with -6.6dBm Power at 244GHz in 65nm CMOS,** *Cornell University*

16.6 **Distributed Active Radiation for THz Signal Generation,** *California Institute of Technology*

16.7 **A 120GHz 10Gb/s Phase-Modulating Transmitter in 65nm LP CMOS,** *KU Leuven*

16.8 **A 1.5GHz-Modulation-Range 10ms-Modulation-Period 180kHz_{rms}-Frequency-Error 26MHz-Reference Mixed-Mode FMCW Synthesizer for mm-Wave Radar Application,** *Toshiba*

16.9 **A Short-Range UWB Impulse-Radio CMOS Sensor for Human Feature Detection,** *University of Southern California; National Tsing Hua University*

16.10 **83GHz 13.5mW/Pixel CMOS Regenerative Receiver for mm-Wave Imaging Applications,** *University of California*

Session 17 - Biomedical & Displays

17.1 **A 160μW 8-Channel Active Electrode System for EEG Monitoring,** *imec - Holst Centre; Delft University of Technology; imec*

17.2 **A 0.013mm² 5μW DC-Coupled Neural Signal Acquisition IC with 0.5V Supply,** *University of California; Telegent Systems*

17.3 **An AC-Powered Optical Receiver Consuming 270μW for Transcutaneous 2Mb/s Data Transfer,** *Institute for Microelectronic and Mechatronics Systems; Ulm University; Intelligent Medical Implants*

17.4 **A Neural Stimulator Front-End with Arbitrary Pulse Shape, HV Compliance and Adaptive Supply Requiring 0.05mm² in 0.35μm HVCMOS,** *Ulm University*

17.5 **A Low Noise Current Readout Architecture for Fluorescence Detection in Living Subjects,** *Stanford University; National Semiconductor*

17.6 **A Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor,** *University of Michigan*

17.7 **A 160×128 Single-Photon Image Sensor with On-Pixel 55ps 10b Time-to-Digital Converter,** *Delft University of Technology; STMicroelectronics; University of Edinburgh; Fondazione Bruno Kessler - IRST; EPFL*

17.8 **Bidirectional OLED Microdisplay: Combining Display and Image Sensor Functionality into a Monolithic CMOS Chip,** *Fraunhofer Institute for Photonic Microsystems*

17.9 **A 0.014mm² 9b Switched-Current DAC for AMOLED Mobile Display Drivers,** *KAIST*

17.10 **A 10b Resistor-Resistor-String DAC with Current Compensation for Compact LCD Driver ICs,** *National Tsing Hua University; National Chi Nan University; University of California*

Session 18 - Organic Innovations

18.1 **An 8b Organic Microprocessor on Plastic Foil,** *imec; KU Leuven; Polymer Vision; TNO Science and Industry; KHLim*

18.2 **A 3.3V 6b 100kS/s Current-Steering D/A Converter Using Organic Thin-Film Transistors on Glass,** *Institute for Microelectronics Stuttgart (IMS CHIPS); University of Stuttgart; Max Planck Institute for Solid State Research*

18.3 **A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power,** *University of Minnesota; Optomec*

18.4 **Fully Printed Organic CMOS Technology on Plastic Substrates for Digital and Analog Applications,** *CEA-LITEN; STMicroelectronics*

Session 19 - Low-Power Digital Techniques

19.1 **A Voltage-Scalable Biomedical Signal Processor Running ECG Using 13pJ/cycle at 1MHz and 0.4V,** *imec; NXP Semiconductors*

19.2 **An 82μA/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications,** *Texas Instruments*

19.3 **Comparison of 65nm LP Bulk and LP PD-SOI with Adaptive Power Gate Body Bias for an LDPC Codec,** *STMicroelectronics; CEA-LETI-MINATEC*

19.4 **A 77% Energy-Saving 22-Transistor Single-Phase-Clocking D-Flip-Flop with Adaptive-Coupling Configuration in 40nm CMOS,** *Toshiba*

19.5 **A 62mV 0.13μm CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic,** *University of Freiburg - IMTEK; HSG-IMIT*

19.6 **A 0.27V 30MHz 17.7nJ/transform 1024-pt Complex FFT Core with Super-Pipelining,** *University of Michigan; Arizona State University*

Session 20 - High-Speed Transceivers & Building Blocks

20.1 **A 4-Channel 10.3Gb/s Transceiver with Adaptive Phase Equalizer for 4-to-41dB Loss PCB Channel,** *Fujitsu Laboratories of America; Fujitsu Laboratories*

20.2 **A 1.0625-to-14.025Gb/s Multimedia Transceiver with Full-rate Source-Series-Terminated Transmit Driver and Floating-Tap Decision-Feedback Equalizer in 40nm CMOS,** *LSI*

20.3 **Analog-DFE-Based 16Gb/s SerDes in 40nm CMOS That Operates Across 34dB Loss Channels at Nyquist with a Baud Rate CDR and 1.2V_{pp} Voltage-Mode Driver,** *Texas Instruments; Arda Technologies*

20.4 **An 8.4mW/Gb/s 4-Lane 48Gb/s Multi-Standard-Compliant Transceiver in 40nm Digital CMOS Technology,** *SnowBush-Gennum; formerly with SnowBush-Gennum*

20.5 **A Pattern-Guided Adaptive Equalizer in 65nm CMOS,** *University of Toronto; Fujitsu Laboratories*

20.6 **A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization,** *National Taiwan University*

20.7 **A 5.4Gb/s Adaptive Equalizer Using Asynchronous-Sampling Histograms,** *Yonsei University*

20.8 **A 0.076mm² 3.5GHz Spread-Spectrum Clock Generator with Memoryless Newton-Raphson Modulation Profile in 0.13μm CMOS,** *Korea University*

Session 21 - Cellular

21.1 **A SAW-less GSM/GPRS/EDGE Receiver Embedded in a 65nm CMOS SoC,** *MediaTek*

21.2 **A 9-Band WCDMA/EDGE Transceiver Supporting HSPA Evolution,** *ST-Ericsson; Ericsson; Formerly with ST-Ericsson; Lund University*

21.3 **A 65nm CMOS SoC with Embedded HSDPA/EDGE Transceiver, Digital Baseband and Multimedia Processor,** *Qualcomm*

21.4 **A Receiver for WCDMA/EDGE Mobile Phones with Inductorless Front-End in 65nm CMOS,** *MediaTek*

21.5 **A Compact SAW-less Multiband WCDMA/GPS Receiver Front-End with Translational Loop for Input Matching,** *NXP Semiconductors*

21.6 **A Multiband LTE SAW-less Modulator with -160dBc/Hz RX-Band Noise in 40nm LP CMOS,** *imec; Renesas Electronics*

21.7 **A Fully Digital Multimode Polar Transmitter Employing 17b RF DAC in 3G Mode,** *Infineon Technologies; DICE*

21.8 **A Low-Power Wideband Polar Transmitter for 3G Applications,** *Broadcom; University of California*

Session 22 - DC/DC Converters

22.1 **A Fully Integrated Power-Management Solution for a 65nm CMOS Cellular Handset Chip,** *ST Ericsson*

22.2 **A Digitally Controlled DC-DC Converter for SoC in 28nm CMOS,** *Infineon Technologies*

22.3 **20μA to 100mA DC-DC Converter with 2.8 to 4.2V Battery Supply for Portable Applications in 45nm CMOS,** *Massachusetts Institute of Technology; Texas Instruments*

22.4 **A Digitally Controlled DC-DC Buck Converter with Lossless Load-Current Sensing and BIST Functionality** *Arizona State University; Jet Propulsion Laboratory*

22.5 **Zero-Order Control of Boost DC-DC Converter with Transient Enhancement Using Residual Current,** *KAIST*

22.6 **Robust and Efficient Synchronous Buck Converter with Near-Optimal Dead-Time Control,** *KAIST*

22.7 **A 90% Peak Efficiency Single-Inductor Dual-Output Buck-Boost Converter with Extended-PWM Control,** *Fudan University; Brandenburg University of Technology*

22.8 **Spurious-Noise-Free Buck Regulator for Direct Powering of Analog/RF Loads Using PWM Control with Random Frequency Hopping and Random Phase Chopping,** *Iowa State University*

Session 23 - Image Sensors

23.1 **An 80μV_{rms}-Temporal-Noise 82dB-Dynamic-Range CMOS Image Sensor with a 13-to-19b Variable-Resolution Column-Parallel Folding-Integration/Cyclic ADC,** *Shizuoka University; Brookman Technology; Sanei Hytechs*

23.2 **A Sub-Electron Readout Noise CMOS Image Sensor with Pixel-Level Open-Loop Voltage Amplification,** *Heliotis; CSEM; EPFL*

23.3 **A 320×256 90dB SNR and 25μm-Pixel-Pitch Infrared Image Sensor,** *CEA-LETI-MINATEC; Sofradir*

23.4 **A 16 Mfps 165kpixel Backside-Illuminated CCD,** *Kinki University; DALSA PI; University of Arizona; NHK Science and Technical Laboratories*

23.5 **A 300mm Wafer-Size CMOS Image Sensor with In-Pixel Voltage-Gain Amplifier and Column-Level Differential Readout Circuitry,** *Canon*

23.6 **A 128×96 Pixel Event-Driven Phase-Domain ΔΣ-Based Fully Digital 3D Camera in 0.13μm CMOS Imaging Technology,** *University of Edinburgh; STMicroelectronics*

23.7 **An Angle-Sensitive CMOS Imager for Single-Sensor 3D Photography,** *Cornell University*

23.8 **A 1/13-inch 30fps VGA SoC CMOS Image Sensor with Shared Reset and Transfer-Gate Pixel Control,** *Aptina Imaging*

23.9 **A 1/2.33-inch 14.6M 1.4μm-Pixel Backside-Illuminated CMOS Image Sensor with Floating Diffusion Boosting,** *Samsung Electronics; Samsung Semiconductor*

23.10 **An APS-C Format 14b Digital CMOS Image Sensor with a Dynamic Response Pixel,** *Aptina Imaging*

23.11 **A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout,** *Sony; Sony LSI Design*

Session 24 - Transmitter Blocks

24.1 **A 40nm Wideband Direct-Conversion Transmitter with Sub-Sampling-Based Output Power, LO Feedthrough and I/Q Imbalance Calibration,** *Broadcom*

24.2 **A Flip-Chip-Packaged 1.8V 28dBm Class-AB Power Amplifier with Shielded Concentric Transformers in 32nm SoC CMOS,** *Intel*

24.3 **A Switched-Capacitor Power Amplifier for EER/Polar Transmitters,** *University of Washington*

24.4 **An EDGE/GSM Quad-Band CMOS Power Amplifier,** *Samsung Electro-Mechanics*

24.5 **A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS,** *University of California*

Session 25 - CDRs & Equalization Techniques

25.1 **A 5Gb/s Adaptive DFE for 2× Blind ADC-Based CDR in 65nm CMOS,** *University of Toronto; Fujitsu Laboratories*

25.2 **A 0.5-to-2.5Gb/s Reference-less Half-Rate Digital CDR with Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance,** *Oregon State University*

25.3 **A TDC-less 7mW 2.5Gb/s Digital CDR with Linear Loop Dynamics and Offset-Free Data Recovery,** *Oregon State University*

25.4 **A Digital Wideband CDR with ±15.6Kppm Frequency Tracking at 8Gb/s in 40nm CMOS,** *Broadcom*

25.5 **A 20Gb/s Digitally Adaptive Equalizer/DFE with Blind Sampling,** *National Taiwan University*

25.6 **A 15Gb/s 0.5mW/Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation,** *California Institute of Technology*

25.7 **A 10Gb/s Half-UI IIR-Tap Transmitter in 40nm CMOS,** *Netlogic Microsystems*

25.8 **A 13.8mW 3.0Gb/s Clock-Embedded Video Interface with DLL-Based Data-Recovery Circuit,** *Seoul National University*

Session 26 - Low-Power Wireless

26.1 **A 7.9μW Remotely Powered Addressed Sensor Node Using EPC HF and UHF RFID Technology with -10.3dBm Sensitivity,** *Graz University of Technology; Infineon Technologies*

26.2 **An Isolator-less CMOS RF Front-End for UHF Mobile RFID Reader,** *KAIST; PHYCHIPS*

26.3 **A 2.4GHz ULP OOK Single-Chip Transceiver for Healthcare Applications,** *Holst Centre / imec; Panasonic*

26.4 **A 120μW MICS/ISM-Band FSK Receiver with a 44μW Low-Power Mode Based on Injection-Locking and 9x Frequency Multiplication,** *University of Washington*

26.5 **A GPS/Galileo SoC with Adaptive In-Band Blocker Cancellation in 65nm CMOS,** *MediaTek*

26.6 **A 0.05-to-10GHz 19-to-22GHz and 38-to-44GHz SDR Frequency Synthesizer in 0.13μm CMOS,** *HKUST*

26.7 **A 4.6GHz MDLL with -46dBc Reference Spur and Aperture Position Tuning,** *University of California; Oracle*

Session 27 - Oversampling Converters

27.1 **A 4GHz CT ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW,** *NXP Semiconductors; Delft University of Technology*

27.2 **An 8mW 50MS/s CT ΔΣ Modulator with 81dB SFDR and Digital Background DAC Linearization,** *Ulm University*

27.3 **A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bidirectional Single-Slope Quantizer,** *Oregon State University*

27.4 **A 250mV 7.5μW 61dB SNDR CMOS SC ΔΣ Modulator Using a Near-Threshold-Voltage-Biased CMOS Inverter Technique,** *KU Leuven*

27.5 **A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-Amp Third-Order ΔΣ Modulator Consuming 140μW,** *University of Pavia*

27.6 **A 1.7mW 11b 1-1-1 MASH ΔΣ Time-to-Digital Converter,** *KU Leuven; SCK-CEN; KH Kempen*

27.7 **A 120dB-SNR 100dB-THD+N 21.5mW/Channel Multibit CT ΔΣ DAC,** *Analog Devices*

27.8 **A 108dB-DR 120dB-THD and 0.5V_{rms} Output Audio DAC with Inter-Symbol-Interference-Shaping Algorithm in 45nm CMOS,** *Texas Instruments*

Session 28 - DRAM & High-Speed I/O

28.1 **An 8.4Gb/s 2.5pJ/b Mobile Memory I/O Interface Using Bidirectional and Simultaneous Dual (Baseband and RF-Band) Signaling,** *University of California; Hongik University; TSMC*

28.2 **A 2.7Gb/s/mm² 0.9pJ/b/Chip 1Coil/Channel ThruChip Interface with Coupled-Resonator-Based CDR for NAND Flash Memory Stacking,** *Keio University*

28.3 **A 12Gb/s Non-Contact Interface with Coupled Transmission Lines,** *Keio University*

28.4 **A 4.8Gb/s Impedance-Matched Bidirectional Multi-Drop Transceiver for High-Capacity Memory Interface,** *Seoul National University; Sungkyunkwan University*

28.5 **A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-Based Stacking,** *Samsung Electronics*

28.6 **A 40nm 2Gb 7Gb/s/pin GDDR5 SDRAM with a Programmable DQ Ordering Crosstalk Equalizer and Adjustable Clock-Tracking BW,** *Samsung Electronics*

28.7 **A 58nm 1.8V 1Gb PRAM with 6.4MB/s Program BW,** *Samsung Electronics*

28.8 **A 1.6V 1.4Gb/s/pin Consumer DRAM with Self-Dynamic Voltage-Scaling Technique in 44nm CMOS Technology,** *Hynix Semiconductor; Korea University*

28.9 **An Embedded DRAM Technology for High-Performance NAND Flash Memories,** *Toshiba*

28.10 **A 700MHz 2T1C Embedded DRAM Macro in a Generic Logic Process with No Boosted Supplies,** *University of Minnesota*