2024 Taiwan and Japan Conference on Circuits and Systems

TJCAS 2024

Aug. 23-25, 2024, Kumamoto, Japan

https://yumilab.ei.st.gunma-u.ac.jp/~tjcas2024/

Organizers

IEEE CASS Japan Joint Chapter
IEEE CASS Fukuoka Chapter
IEEE CASS Kansai Chapter
IEEE CASS Shikoku Chapter
IEEE CASS Taipei Chapter
IEEE CASS Tainan Chapter

Sponsors

Kumamoto University
Kumamoto Int'l Convention & Tourism Bureau
IEEE SSCS Japan Chapter
IEEE SSCS Kansai Chapter
IEEE CEDA All Japan Joint Chapter

熊本大学 Kumamoto University

CAS

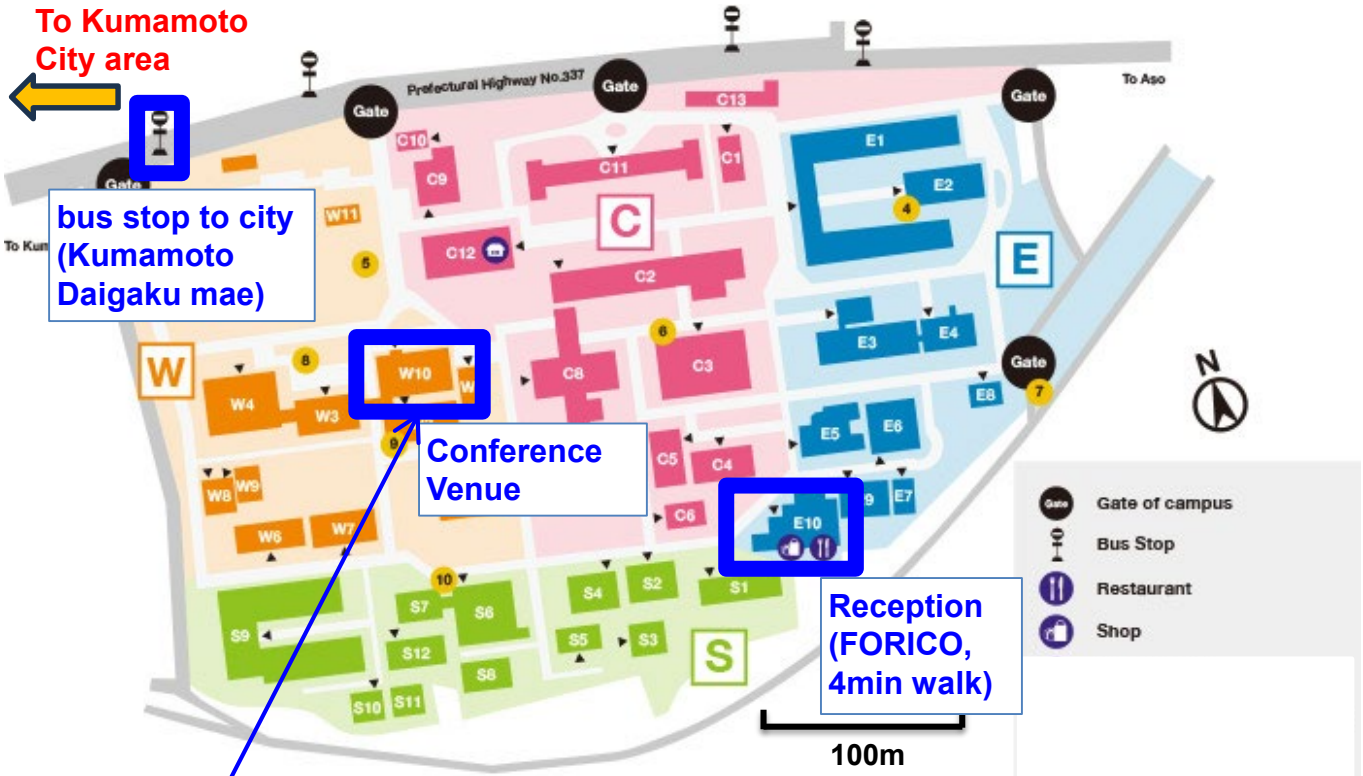
SSCS

CEDA® IEEE Council on Electronic Design Automation

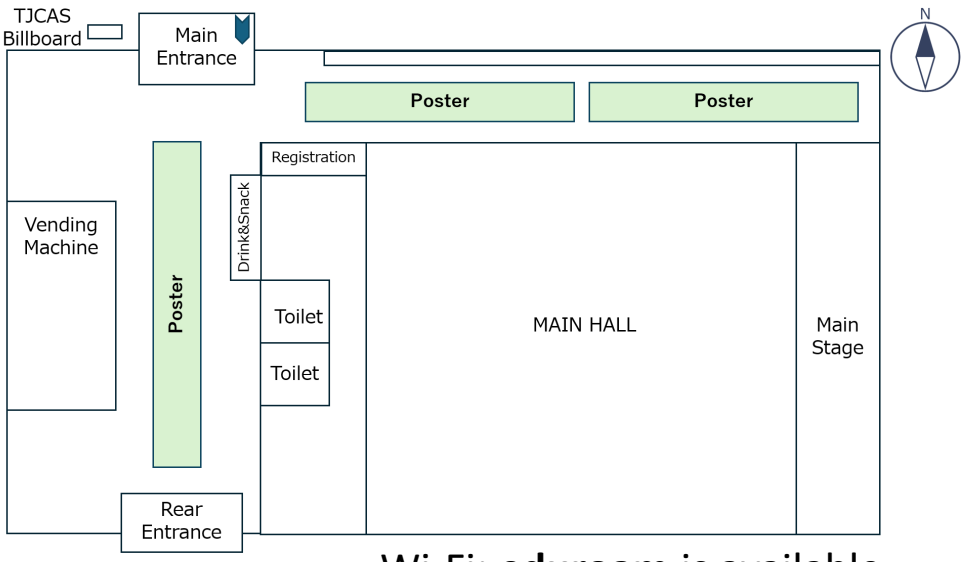
Conference Venue

100th Anniversary Hall

Kumamoto University　Kurokami South Campus

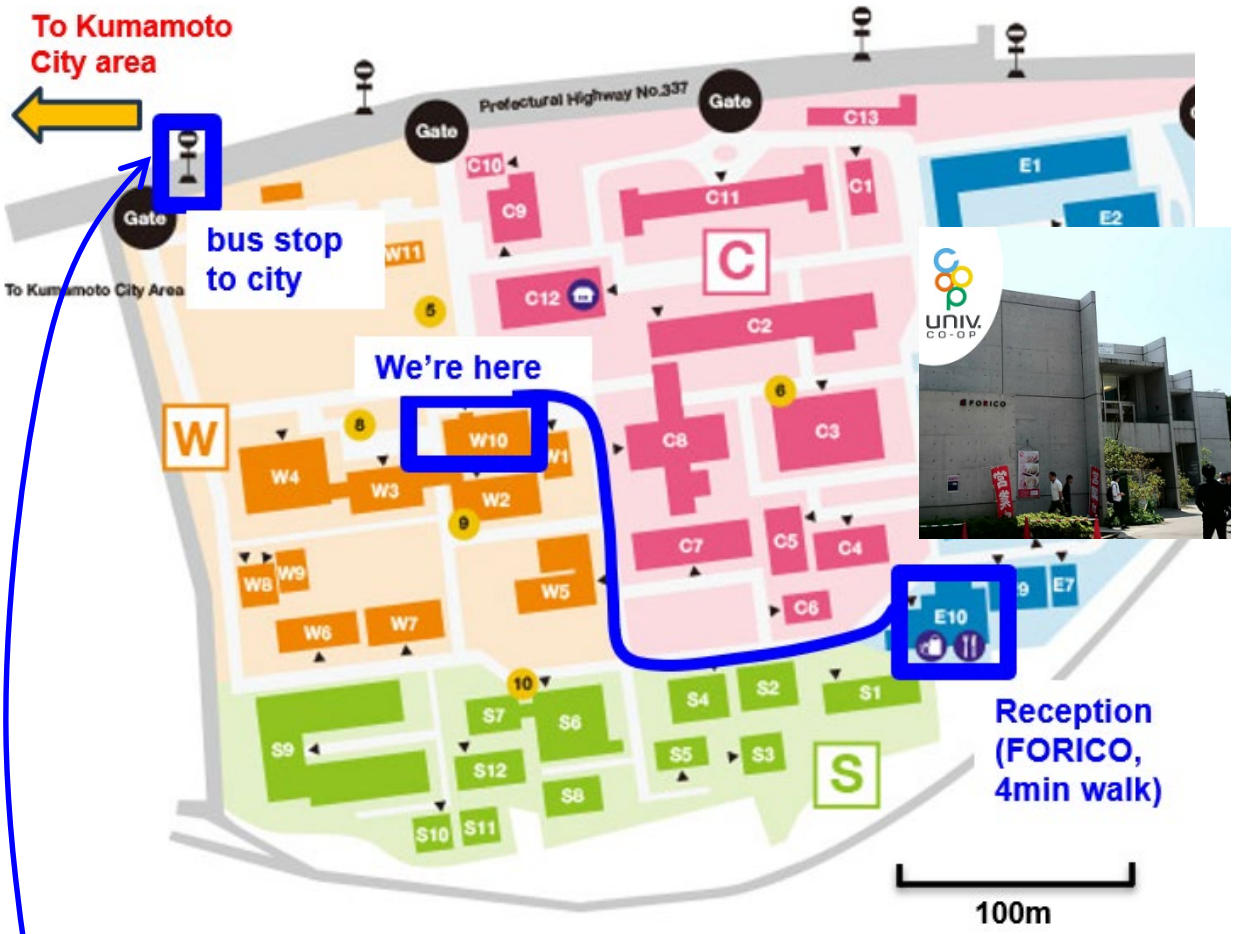


W10: **100th Anniversary Hall**



Wi-Fi: **eduroam** is available

Welcome Reception (Aug. 23rd, 17:30-)



2nd floor in FORICO cafeteria
Light meals and drinks provided.

Please use local bus or walk (if young ^^;) to city center.

Bus time schedule on weekdays
(To Kumamoto city area including Sakura machi bus terminal)

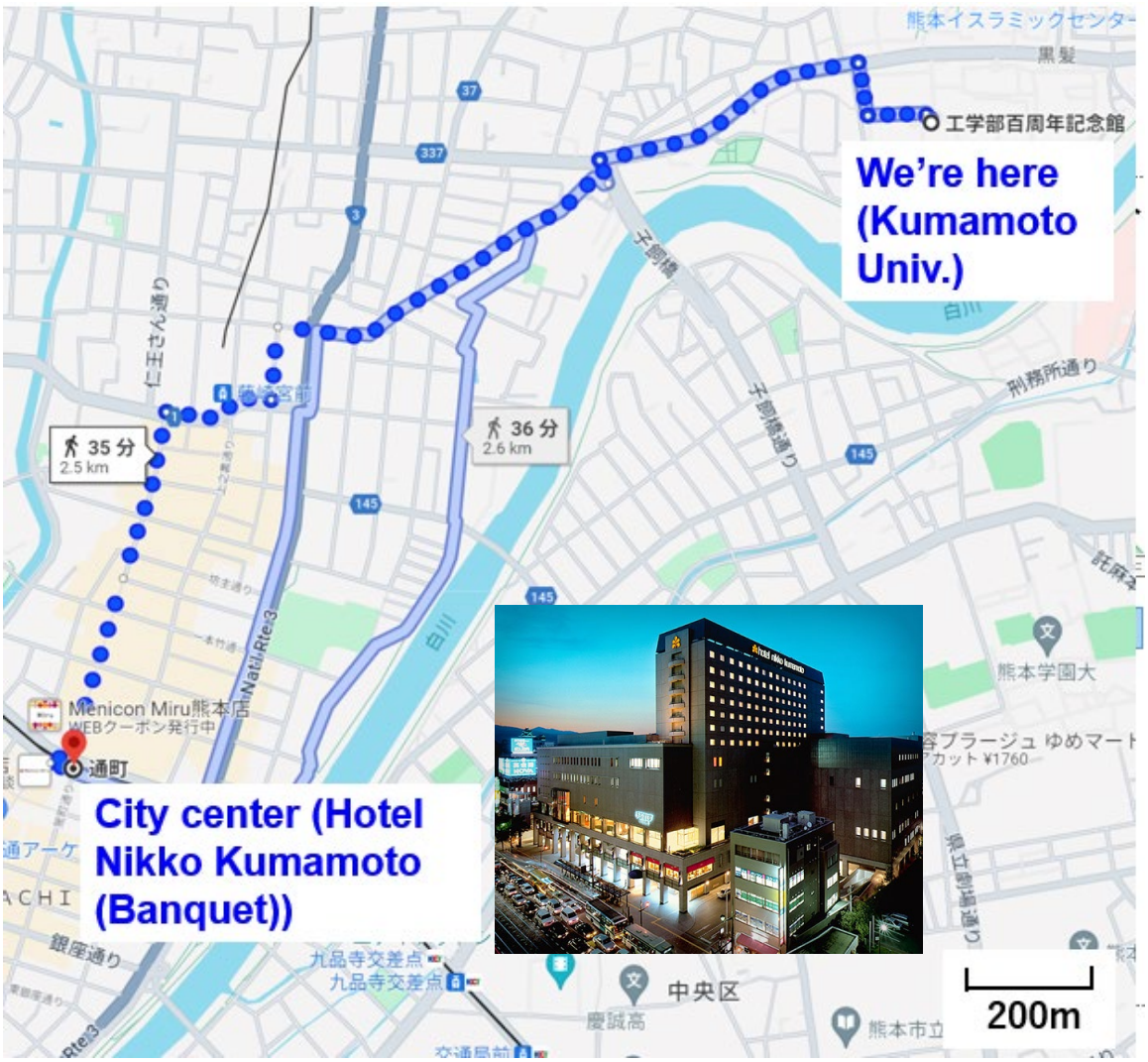
hour	minute						
18	03	10	19	27	34	45	54
19	14	24	29	54			
20	14	29	44	59			
21	14	29					
22	19						

Banquet (Aug. 24th, 18:30-20:30)

Held at **Hotel Nikko Kumamoto** (5th floor, Room **Amakusa**)
https://nikko-kumamoto.co.jp/en/

For those who have extra banquet tickets, or who go directly to the hotel, please come to the 5th floor of the hotel by **18:15**.
(Foyer is available on the 5th floor)

Conference attendees go to the hotel by **chartered buses** from 100th aniv. Hall at Kumamoto University.
The buses will depart around **17:00**.



Program at a Glance

Date	Time	Program
Aug. 23rd	15:00	Registration start
IEEE Circuits and Systems Society Outreach	16:00～16:30	**Invited Talk**
	16:30～17:00	Free Discussion
	17:30～	**Welcome Reception** (Cafeteria “Forico” at Kurokami south campus)
Aug. 24th	08:40	Registration start
	9:00- 9:10	Opening ceremony
	9:10-10:50	Plenary session **Keynote Speech I, II**
	10:50～11:10	Coffee break
	11:10～12:40	**Poster session I**
	12:40～13:30	Lunch
	13:30～14:15	Plenary session **Keynote Speech III**
	14:15～14:30	Coffee break
	14:30～16:00	**Poster session II**
	18:30～20:00	**Banquet** at Hotel Nikko Kumamoto
Aug. 25th	Buses depart at 9:30 from **Sakuramachi Bus Terminal**	**Social Program** Session (Bus trip to Aso Geopark)

Program

Friday, August 23, 2024

2024 IEEE Circuits and Systems Society Outreach

YP/Industry Meeting for Encouraging Students & Young Researchers between Taiwan and Japan through the semiconductor industry

Session I Invited talk

Time: 16:00 - 16:30, Friday, August 23, 2024
Chair: Hao SAN (Tokyo City Univ., Japan)

I-1 (Time: 16:00 - 16:15)

Title	(Invited Paper) High-level synthesys for accelerator synthesis
Author	*Kenshu Seto (Kumamoto Univ., Japan)

I-2 (Time: 16:15 - 16:30)

Title	(Invited Paper) The integrated circuit education and design environment in Taiwan
Author	Hsie-Chia Chang (National Yang Ming Chiao Tung Univ., Taiwan)

Session D Free Discussion

Time: 16:30 - 17:00, Friday, August 23, 2024
Chair: Hao SAN (Tokyo City Univ., Japan)

Saturday, August 24, 2024

Session K1 Plenary session I

Time: 9:10 - 10:50, Saturday, August 24, 2024
Chair: Yasushi YUMINAKA (Gunma Univ., Japan)

K1-1 (Time: 9:15 - 10:00)

Title	(Keynote Speech) Energy Harvesting Integrated Circuit for Battery-free IoT Devices
Author	*Po-Hung Chen (National Yang Ming Chiao Tung Univ., Taiwan)

K1-2 (Time: 10:00 - 10:45)

Title	(Keynote Speech) Circuits and Algorithms for Analog/Mixed-Signal IC Test in the Digital Exploding Society
Author	*Haruo Kobayashi (Gunma Univ., Japan)

Session P1 Poster session I

Time: 11:10 - 12:40, Saturday, August 24, 2024
Chairs: Shunsuke KOSHITA (Hachinohe Inst. of Tech., Japan), Kazushi KAWAMURA (Tokyo Inst. of Tech., Japan)

P1-1 (Analog Circuit)

Title	Ripple-based Implementation of Order-Power Distribution Control on a Single-Inductor Quad-Output Buck Converter
Author	Hong-Jhih Jhou, *Le-Ren Chang-Chien (National Cheng Kung Univ., Taiwan)

P1-2 (Analog Circuit)

Title	A Study on Cell Mismatch of a 4kb PMOS-Read-Port Low-Leakage 8T SRAM
Author	Chien-Hung Chen, Wu-Wun Chen, *Chao-Yu Chen, Yi Chiu, Hao-Chiao Hong (National Yang Ming Chiao Tung Univ., Taiwan)

P1-3 (Analog Circuit)

Title	A Fractional Frequency Divider Using Pipelined Phase Interpolation Compensation Technology
Author	*Ching-Yuan Yang, Chun-Hung Lin (National Chung Hsing Univ., Taiwan)

P1-4 (Analog Circuit)

Title	Analysis of Compensation in PAM4 Equalizer Using Stacked Partial Equalization Technique
Author	*Shogo Ishida, Junsei Ohshika, Daisuke Ito, Makoto Nakamura (Gifu Univ., Japan)

P1-5 (Analog Circuit)

Title	A Mm-Wave 5G Broadband Power Amplifier with Subthreshold Adaptive Biasing in 22 nm FD-SOI
Author	Liang-Wei Ouyang, Clint Sweeney (Texas Tech Univ., USA), Jill Mayeda (Texas Tech Univ./TokyoTech, USA), Jerry Lopez (Texas Tech Univ./NFR, USA), *Donald Y.C. Lie (Texas Tech Univ., USA)

P1-6 (Analog Circuit)

Title	A Design of Battery Charger Boost Converters Operating at Input Voltages Below 10 mV for Energy Harvesting
Author	*Wataru Saito (Shizuoka Univ., Japan), Toru Tanzawa (Waseda Univ., Japan)

P1-7 (Analog Circuit)

Title	Comparative Study on De-embedding Model of Coplanar-Probe-to-Microstrip-Line Pad Structure
Author	*Kan Ishiguro, Tsugumichi Shibata (Tokyo City Univ., Japan)

P1-8 (Analog Circuit)

Title	NN Model of the Equivalent Circuit Parameters for Microstrip Line Width Discontinuities
Author	*Keito Naitoh, Yuta Hukushi, Tsugumichi Shibata (Tokyo City Univ., Japan)

P1-9 (Digital Circuits)

Title	An Image assisted Visual Odometry Estimation Scheme and Its Hardware Implementation
Author	Yun-Chieh Lu, *Yin-Tsung Hwang (National Chung Hsing Univ., Taiwan)

P1-10 (Digital Circuits)

Title	FPGA Implementation of Spatial-Temporal-Majority Filter for Event-based Vision Sensor
Author	*Ryuta Toyoda, Ninnart Fuengfusin, Hakaru Tamukoh (Kyushu Inst. of Tech., Japan)

P1-11 (Digital Circuits)

Title	Complexity Reduction Techniques in Compositional Formal Verification for ISA Checking OoO CPU
Author	*Yean-Ru Chen, Yu-Ting Chou, Ji-Qing Yan (National Cheng Kung Univ., Taiwan)

P1-12 (Digital Circuits)

Title	MCUs Calculation Performance Evaluation for Universal Boards Embedded with AVR, ARM and ESP32
Author	*HAOHAO ZHANG, Yasushi Yuminaka (Gunma Univ., Japan)

P1-13 (Digital Circuits)

Title	Kernel-agnostic Dataflow for CNN and Transformer Accelerator
Author	*Chin-Cheng Wei, Bo-Wei Lin, Chung-Ho Chen (National Cheng Kung Univ., Taiwan)

P1-14 (VLSI Design)

Title	Squaremax: A Hardware-Friendly Alternative to Softmax Function
Author	*Juinn-Dar Huang, Meng-Hsun Hsieh, Xuan-Hong Li, Yu-Hsiang Huang, Pei-Hsuan Kuo (National Yang Ming Chiao Tung Univ., Taiwan)

P1-15 (VLSI Design)

Title	Base Conversion Accelerator for Homomorphic Encryption
Author	*Qi-Xian Wu, Ming-Der Shieh (National Cheng Kung Univ., Taiwan)

P1-16 (VLSI Design)

Title	Real-time PCA Face Recognition using SVD and Threshold Filter
Author	*Cheng Lun Chen, Lih Yih Chiou (National Cheng Kung Univ., Taiwan)

P1-17 (VLSI Design)

Title	Optimization Algorithms for Generalized Channel Routing Problem
Author	*Zezhong Wang, Masayuki Shimoda, Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

P1-18 (VLSI Design)

Title	An IR-Drop Model for RRAM Crossbar Array Considering Data Allocation
Author	Shih-Han Chang, Tung Lin, *Yun-Hsin Liu, Chien-Nan Jimmy Liu (National Yang Ming Chiao Tung Univ., Taiwan)

P1-19 (Neural Network)

Title	A Location Estimation System Based on the WiFi Beacon Signals Using Machine Learning
Author	*Hikaru Ihara, Hao San, Tsugumichi Shibata (Tokyo City Univ., Japan)

P1-20 (Neural Network)

Title	Method for Estimating Human Posture of Table Tennis Athletes
Author	*Hau-Ping Chen, Wen-Ho Juang (National Formosa Univ., Taiwan)

P1-21 (Neural Network)

Title	Voice Activation Prototype Design Applied to Robotic Arm
Author	*Ying-Hsiu Hung, Tsai-Yen Wei, Jeng-Dao Lee, Shin-Chi Lai (National Formosa Univ., Taiwan)

P1-22 (Other)

Title	A LoRaWAN-Based Sensor Network for Monitoring Rodent Activity
Author	*Szu-Ting Wang, Shang-Sian Wu, Kuo-Cheng Tseng, Li-Chuan Hsu, Song-Min Ke, Shin-Chi Lai (National Formosa Univ., Taiwan)

P1-23 (Other)

Title	The adaptive medical image compression based on JPEG-LS
Author	*Ya-Yun Huang, Wei-Chen Tu (National Cheng Kung Univ., Taiwan), Shih-Lun Chen (Chung Yuan Christian Univ., Taiwan)

P1-24 (Other)

Title	A Thin Coil for High-Efficiency Wireless Power Transfer
Author	*Tatsumu Mitsuhashi, Amane Yamamoto, Atsushi Kurokawa (Hirosaki Univ., Japan)

P1-25 (Other)

Title	Investigation of Lower Limit of Measurement Time for Noncontact Respiration Rate Measurement Using Millimeter-Wave Radar
Author	*Shota Ueda, Hiroto Fujii, Shintaro Arai, Kohei Saeki, Ryohei Yoshitake, Eri Iwata (Okayama Univ. of Science, Japan), Suguru Kameda (Hiroshima Univ., Japan), Ataru Yamaoka (S-Takaya Electronics Industry, Japan)

P1-26 (Other)

Title	A Study on Detection Accuracy Improvement of Transmitter in Visible Light Communication Using Propeller LED Transmitter and Camera
Author	*Wataru Tafusa (Okayama Univ. of Science, Japan), Daisuke Ito (Gifu Univ., Japan), Shintaro Arai (Okayama Univ. of Science, Japan)

P1-27 (Other)

Title	High-Performance and Lifetime-aware Write Scheduling for DDR-interfaced PCMs
Author	*Ya-Chi Chang, Chien-Hao Hao, Yi-Jung Chen (National Chi Nan Univ., Taiwan)

P1-28 (Other)

Title	Prototype Design of Real-time Remote Monitoring System Applied to Autonomous Vehicle in Campus Scenarios
Author	*Song-Min Ke, Li-Chuan Hsu, Shang-Sian Wu, Guan-Yu Lai, Szu-Ting Wang, Shin-Chi Lai (National Formosa Univ., Taiwan)

P1-29 (Other)

Title	Design of a Dual-Frequency Rectifier With Compensated Zero Impedance Angle
Author	*Yinchen Xie, Akihiro Konishi, Kien Nguyen, Hiroo Sekiya (Chiba Univ., Japan)

P1-30 (Other)

Title	Improving visibility under light from RGB color LED lighting
Author	*Taiga Ogiwara, Seigi Ryu, Yuji Sano (Toyo Univ., Japan), Kaho Morishita (Mitsubishi Electric Lighting, Japan)

P1-31 (Other)

Title	Sports Blood Oxygen and Heart Rate Sensing: CNN-based Denoising Autoencoder for Motion Artifact Reduction in Photoplethysmography
Author	*Li-Chuan Hsu, Yao-Feng Liang (National Formosa Univ., Taiwan), Wei-Da Chen (National Yunlin Univ. of Science and Tech., Taiwan), Shin-Chi Lai (National Formosa Univ., Taiwan)

P1-32 (Other)

Title	Multilingual Translation System Design with Personalized Voice Characteristics
Author	Guan-Yu Lai, *Chen-Hua Chen, Chuan Lee, Shin-Chi Lai (National Formosa Univ., Taiwan)

Session K2 Plenary session II

Time: 13:30 - 14:15, Saturday, August 24, 2024

K2-1 (Time: 13:30 - 14:15)

Title	(Keynote Speech) Leveraging Machine Learning for VLSI Physical Design
Author	*Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

Session P2 Poster session II

Time: 14:30 - 16:00, Saturday, August 24, 2024

Chairs: Kazushi KAWAMURA (Tokyo Inst. of Tech., Japan), Shunsuke KOSHITA (Hachinohe Inst. of Tech., Japan)

P2-1 (Analog Circuit)

Title	Yagi-Uda Type Microstrip Patch Antenna for Microwave Power Transfer
Author	*Wataru Takeshita, Tsugumichi Shibata (Tokyo City Univ., Japan)

P2-2 (Analog Circuit)

Title	Performance Feasibility of Multisection Line Impedance Transformers with Shorter Length
Author	*Kei Terui, Tsugumichi Shibata (Tokyo City Univ., Japan)

P2-3 (Analog Circuit)

Title	Optimal Micro-CMOS Technology for Bitrate and Power Efficiency in LD Driver
Author	*Junji Togashi, Ryuma Mochizuki, Daisuke Ito, Makoto Nakamura (Gifu Univ., Japan)

P2-4 (Analog Circuit)

Title	An 117-TOPS/W Fully Analog Computing-in-Memory Macro with Zero-Crossing-Based Amplification for Edge-AI Devices
Author	*Wei-Cheng Huang, Soon-Jyh Chang (National Cheng Kung Univ., Taiwan)

P2-5 (Analog Circuit)

Title	Design of Self-Oscillating Class-E Inverter
Author	*Yutaro Komiyama (Chiba Univ., Japan), Wenqi Zhu (Tokyo Univ. of Science, Japan), Akihiro Konishi, Kien Nguyen, Hiroo Sekiya (Chiba Univ., Japan)

P2-6 (Analog Circuit)

Title	The Study of ISDM Time-Domain Noise Slicing Optimization
Author	Hao-Hsuan Chang, *Ci-Ren Chen (National Taiwan Univ., Taiwan)

P2-7 (Analog Circuit)

Title	A Fast Transient Response Hybrid Single-Inductor Dual-Output Converter with < 1% Under/Overshoot at 570mA Load Change
Author	*Philex Fan, Ray Bo-Ray Chen (National Cheng Kung Univ., Taiwan)

P2-8 (Analog Circuit)

Title	Wireless Power Transfer System with Synchronous Class-E Rectifier
Author	*HANXIAO WANG, HIROO SEKIYA (Chiba Universiry, Japan)

P2-9 (Analog Circuit)

Title	A 340-GHz Mixer-First Receiver Front-End Design
Author	Wei-Che Sun, *Chien-Nan Kuo (National Yang Ming Chiao Tung Univ., Taiwan)

P2-10 (Digital Circuits)

Title	Improvement of Accuracy Based on Notch Filtering in Speech Recognition Systems
Author	*Takafumi Ibonai, Shunsuke Koshita (Hachinohe Inst. of Tech., Japan)

P2-11 (Digital Circuits)

Title	Development of pragma generator to improve estimating circuit performance
Author	*Kazuki Tokuishi, Masato Kiyama, Motoki Amagasaki, Kenshu Seto (Kumamoto Univ., Japan)

P2-12 (Digital Circuits)

Title	Effective Dual-mode Compute-in-Memory Macro for Incremental Learning
Author	Lih-Yih Chiou, Yun-Ru Chen, *I-Ting Chen, Zhi-Yu Chen (National Cheng Kung Univ., Taiwan)

P2-13 (Digital Circuits)

Title	A Stochastic Computation Approach to FIR Digital Filtering for Specch Signal Processing
Author	*Shunsuke Koshita, Asuma Onodera (Hachinohe Inst. of Tech., Japan)

P2-14 (Digital Circuits)

Title	A Cost-Efficient DFT Accelerator Design for EIS Multi-Frequency Analysis
Author	*Wen-Ho Juang, Hau-Ping Chen (National Formosa Univ., Taiwan)

P2-15 (VLSI Design)

Title	Low Performance Overhead and High-Secure Cache Design Against Conflict-based Cache Side-channel Attacks
Author	Chen-Che Lin, *Yong-Sheng Liu, Lih-Yih Chiou (National Cheng Kung Univ., Taiwan)

P2-16 (VLSI Design)

Title	Implementation of A2C Algorithm in Reinforcement Learning on CPU-FPGA Embedded System
Author	*Chavakorn SOMJAISUK, Yukio MITSUYAMA, Wang LIAO (Kochi Univ. of Tech., Japan)

P2-17 (VLSI Design)

Title	FPGA Acceleration for Image Classification in ROS2 System
Author	*Wayoon THONGCHAI, Chavakorn SOMJAISUK, Yukio MITSUYAMA, Wang LIAO (Kochi Univ. of Tech., Japan)

P2-18 (VLSI Design)

Title	Profiler for Rapid Analysis of Performance and Power for Single Core NVDLA Accelerator
Author	Wan-Yun Chang, *Pei-Yu Pan, Lih-Yih Chiou (National Cheng Kung Univ., Taiwan)

P2-19 (Neural Network)

Title	Sensor Information Reduction for Anomaly Detection in Predictive Maintenance System
Author	*Atsuhiro Tadenuma (Sanden, Japan), Haohao Zhang, Yasushi Yuminaka (Gunma Univ., Japan)

P2-20 (Neural Network)

Title	Implementing Embedded Keyword Recognition Systems Using AI-Generated Speech for Data Augmentation
Author	*Yi-Chang Zhu, Szu-Ting Wang, Shin-Chi Lai (National Formosa Univ., Taiwan)

P2-21 (Neural Network)

Title	Drunk Driving Detection Using Adjusting Mini-Batch at Run Time in Two-Stage Deep Neural Network
Author	*Chun-Hao Huang, Robert Chen-Hao Chang (National Chung Hsing Univ., Taiwan)

P2-22 (Other)

Title	Integrated System Design for Low-Latency Multilingual Translation and Smart Speech Synthesis Applied to Conference Scenarios
Author	Chen-Hua Chen, *Guan-Yu Lai, Chuan Lee, Shin-Chi Lai (National Formosa Univ., Taiwan)

P2-23 (Other)

Title	YOLO Based Pose Estimation with Keypoints Detection and Angle Relationship for Recognizing User's Interests on Interactive Advertising Displays
Author	Yu-En Lee, *Chih-Peng Fan (National Chung Hsing Univ., Taiwan)

P2-24 (Other)

Title	Low-Cost People Flow Monitoring System Based on LoRa
Author	*Shang-Sian Wu, Li-Chuan Hsu, Song-Min Ke, Guan-Yu Lai, Szu-Ting Wang, Shin-Chi Lai (National Formosa Univ., Taiwan)

P2-25 (Other)

Title	Implementing Secure Communication with AES Algorithm in ROS 2
Author	*Yuan-Ching Fang, Wei-Chieh Hsu, Yun-Shuai Yu (National Formosa Univ., Taiwan)

P2-26 (Other)

Title	Advanced Denoising Autoencoder with CNN Architecture for Enhancing the Quality of Photoplethysmography Signals
Author	*Yao-Feng Liang, Li-Chuan Hsu, Chen-Peng Wang (National Formosa Univ., Taiwan), Ying-Hsiu Hung, Yen-Ching Chang (National Yunlin Univ. of Science and Tech., Taiwan), Szu-Ting Wang (National Formosa Univ., Taiwan), Ming-Hwa Sheu (National Yunlin Univ. of Science and Tech., Taiwan), Shin-Chi Lai (National Formosa Univ., Taiwan)

P2-27 (Other)

Title	Characteristics of Circular Coupler Structures in Capacitive Power Transfer
Author	*Amane Yamamoto, Tatsumu Mitsuhashi, Atsushi Kurokawa (Hirosaki Univ., Japan)

P2-28 (Other)

Title	Position Recognition in Mobile Wireless Charging Using Coil Sensors
Author	*Shogo Omata, Kotaro Terada, Atsushi Kurokawa (Hirosaki Univ., Japan)

P2-29 (Other)

Title	Communication Performance Comparison of DCO-OFDM Transmission in High-Dynamic Range Camera-Based Visible Light Communication With Varying QAM Modulation Order and Number of Subcarriers
Author	*Noor Muhammad A Zeem Bin Noor Aznan, Maki Yasui, Shintarou Arai (Okayama Univ. of Science, Japan)

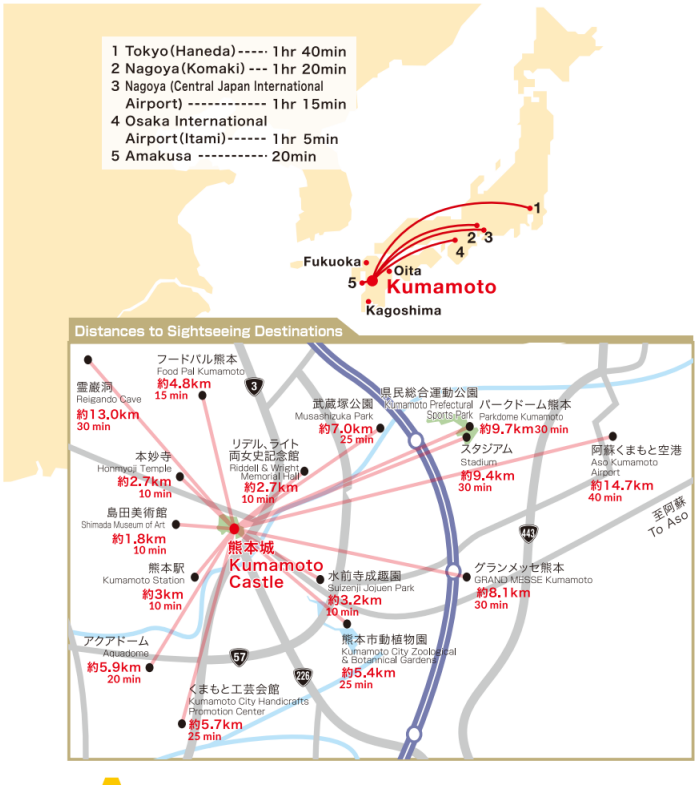
P2-30 (Other)

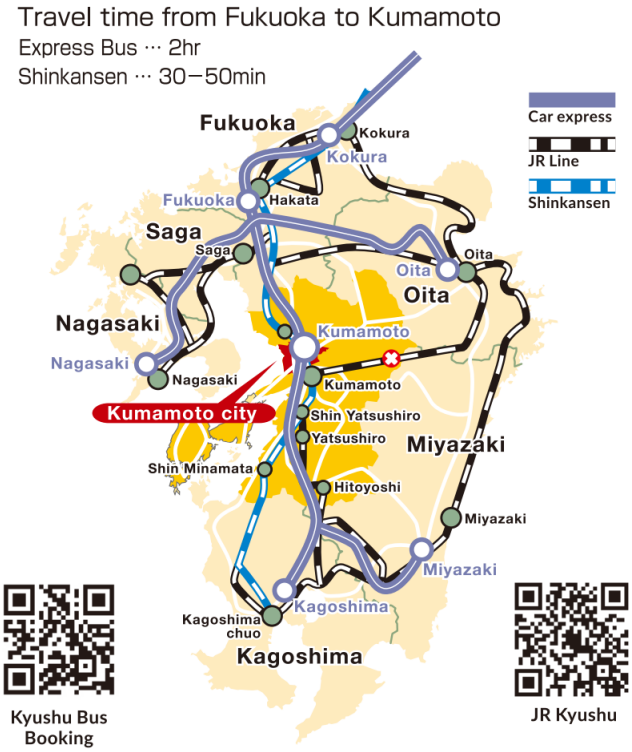
Title	A Study on Demodulation Performance for Blurred Received Images in Image Sensor Communication Using Light Trail Surface by Propeller LED Transmitter
Author	*Naoyuki Otsubo (Okayama Univ. of Science, Japan), Daisuke Ito (Gifu Univ., Japan), Shintaro Arai (Okayama Univ. of Science, Japan)

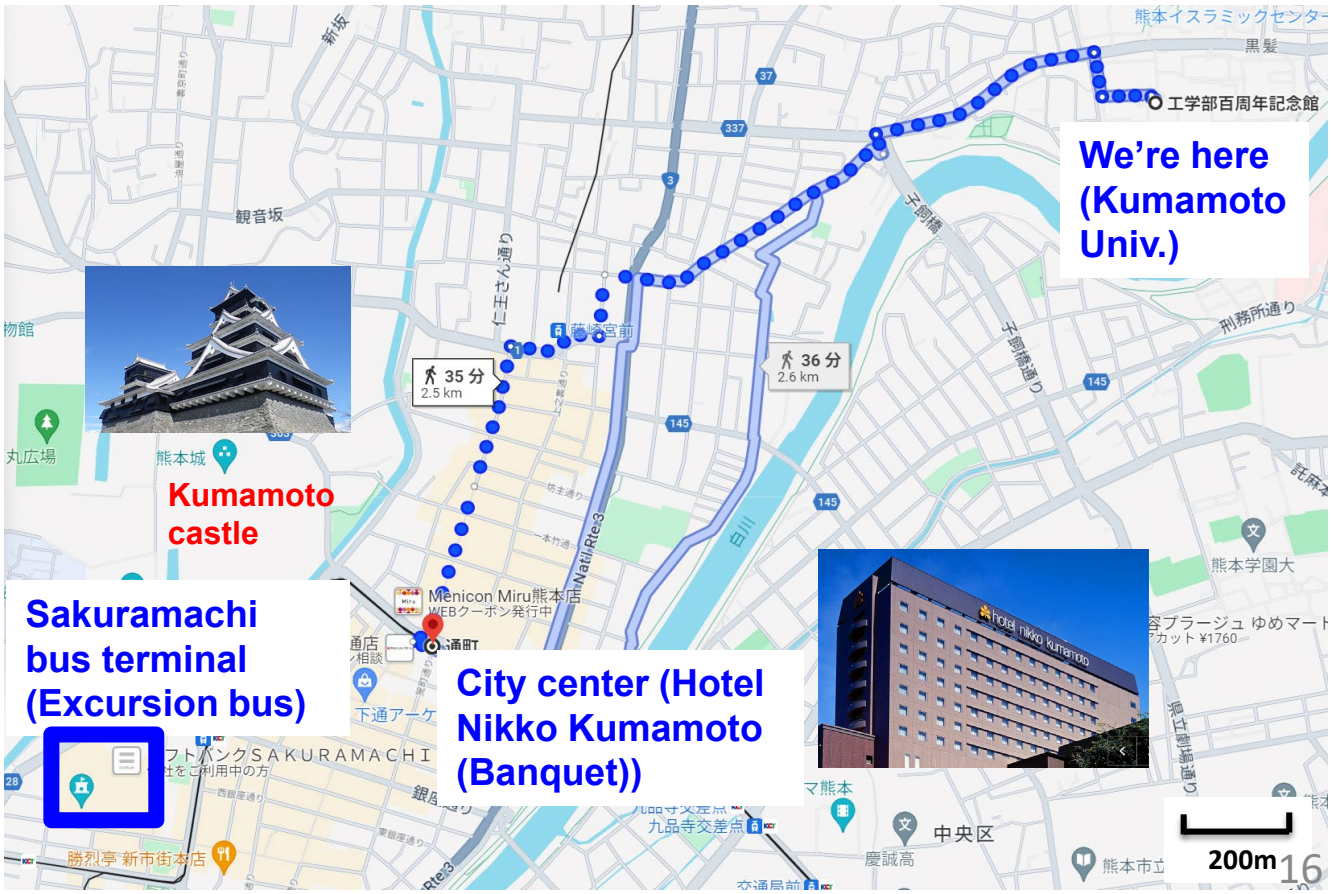
P2-31 (Other)

Title	3D-LSI Emulation Chips for BUS Behavioral and Thermal Modeling
Author	*Takeshi Ohkawa, Masaki Nakamura, Yuto Shiota, Takeshi Kuboki, Masahiro Aoyagi (Kumamoto Univ., Japan)

Map


1 Tokyo(Haneda)----- 1hr 40min
2 Nagoya(Komaki) --- 1hr 20min
3 Nagoya (Central Japan International Airport) ---------- 1hr 15min
4 Osaka International Airport(Itami)------ 1hr 5min
5 Amakusa ---------- 20min
Fukuoka
Oita
Kumamoto
Kagoshima
Distances to Sightseeing Destinations
熊本城
Kumamoto Castle
To Aso


Travel time from Fukuoka to Kumamoto
Express Bus ··· 2hr
Shinkansen ··· 30−50min
Car express
JR Line
Shinkansen
Fukuoka
Kokura
Hakata
Saga
Oita
Nagasaki
Kumamoto
Kumamoto city
Shin Yatsushiro
Yatsushiro
Miyazaki
Shin Minamata
Hitoyoshi
Kagoshima chuo
Kagoshima
Kyushu Bus Booking
JR Kyushu


We're here (Kumamoto Univ.)
工学部百周年記念館
Kumamoto castle
熊本城
Sakuramachi bus terminal (Excursion bus)
City center (Hotel Nikko Kumamoto (Banquet))
hotel nikko kumamoto
35 分
2.5 km
36 分
2.6 km
200m

Social program (Aug. 25th, 9:10-17:00)

Attendees who registered social program in the online registration, or those who have extra ticket can join.

Two charted buses come to Sakura machi bus terminal (“Chartered” bus stop next to **bus stop 24 (green platform)**) **at 9:10am.**

Buses leave at 9:30am on time, and the location of bus stop is confusing, so please don’t be late.

Both buses will arrive at **Kumamoto airport at around 16:00** and will be back to Sakuramachi at around **17:00**.

We will visit Aso (TSMC fab(just from bus window), Daikanbo and Kusasenri, etc).

How to go to Charted bus stop in Sakura-machi for social program?

It is in Sakura-machi bus terminal, but it's confusing.
https://sakuramachi-kumamoto.jp/bus

At first, please go to the 2nd Floor of Sakura machi and then go down to the 1st floor as follows.

Go to the 2nd floor of Sakuramachi.
Find green numbers **24-29**.

Please take the escalator down to the **1st floor**.

Please get on the busses at Charted bus stop which is next to **bus stop 24** (**buses arrive at 9:10am and depart at 9:30am**)

You'll be able to get on the buses around **9:10**.

Voting for Poster Presentations
(Accepted until Aug. 24th 16:30)

For each poster session (AM and PM), please select **one paper** that you consider the best based on the quality, uniqueness, and clarity of the presentation. Please use the QR code below to vote via Google Form, one vote in the morning and one in the afternoon.
If you cannot use the Google Form, please use the paper ballot provided. Please note that each person may only vote **once**, and votes for papers on which you are a co-author will be invalidated.

QR code will be informed at the conference site.

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